Power Efficiency Comparisons of Interchip Optical Interconnect Architectures

Arun Palaniappan and Samuel Palermo, *Member, IEEE*

***Abstract*—High-bandwidth interchip optical interconnect architectures have the potential to address increasing input–output bandwidth demands. This brief compares several optical interconnect architectures on the basis of power efficiency in 90- and 45-nm CMOS technologies. Under consideration are a near-term architecture consisting of discrete vertical-cavity surface-emitting lasers (VCSELs) with p-i-n photodetectors (PDs) and three long-term integrated photonic architectures that use waveguide metal–semiconductor–metal PDs and either electroabsorption modulator (EAM), ring resonator modulator (RRM), or Mach–Zehnder modulator (MZM) sources. An optimal current density methodology with normalized transistor parameters extracted from circuit simulations is applied to jointly optimize driver and receiver circuitry to minimize the total link power dissipation. The analysis results show that the VCSEL-based link is limited by VCSEL bandwidth and maximum power levels, rather than circuit bandwidth, and achieves a maximum of 24 Gb/s in both the 90- and 45-nm nodes. The EAM and the RRM are both attractive integrated photonic technologies capable of scaling data rates past 30 Gb/s at power efficiency levels near 0.5 mW/Gb/s in the 45-nm node and are primarily limited by coupling and device insertion losses. While the MZM offers robust operation due to its wide optical bandwidth, significant improvements in power efficiency must be achieved to become applicable for high-density applications.**

***Index Terms*—Electroabsorption modulators (EAMs), Mach–Zehnder modulators (MZMs), metal–semiconductor–metal (MSM) photodetector (PD), optical interconnects, ring resonator (RR), transimpedance amplifier (TIA), vertical-cavity surface-emitting laser (VCSEL).**

I. Introduction

INCREASING interchip communication bandwidth demand has motivated investigation into using optical interconnect architectures over channel limited electrical counterparts. Optical interconnects with negligible frequency-dependent loss and high bandwidth [1] provide a viable alternative to achieve dramatic power efficiency improvements at per-channel data rates exceeding 10 Gb/s. This has motivated extensive research into optical interconnect technologies suitable for high-density integration with CMOS chips.

Directly modulated lasers and optical modulators, both electroabsorption and refractive, have been proposed as high-bandwidth optical sources, with these different sources displaying tradeoffs in both device and circuit driver efficiency. Vertical-cavity surface-emitting lasers (VCSELs) [2] are an attractive candidate due to their ability to directly emit light with low threshold currents and reasonable slope efficiency values; however, their speed is limited by both electrical parasitics and carrier–photon interactions. A device that does not display this carrier speed limitation is the electroabsorption modulator (EAM), based on either the quantum-confined Stark effect (QCSE) [3] or the Franz–Keldysh effect [4], which is capable of achieving acceptable contrast ratios (CRs) at low drive voltages over tens of nanometers of optical bandwidth. Ring resonator modulators (RRMs) [5], [6] are refractive devices that display very high resonant quality factors and can achieve high CRs with small dimensions and low capacitance; however, their optical bandwidth is typically less than 1 nm. Another refractive device capable of wide optical bandwidth (> 100 nm) is the Mach–Zehnder modulator (MZM) [7]; however, this comes at the cost of a large device and high voltage swings. All of the optical modulators also require an external source laser and incur additional coupling losses relative to a VCSEL-based link.

Photodetector (PD) efficiency plays a key role in setting the maximum data rate and tolerable channel loss. High-speed p-i-n photodiodes [8] are commonly used in optical receivers due to their high responsivity and low capacitance, whereas emerging ultralow capacitance waveguide PDs [9] integrated with CMOS receivers have the potential to dramatically improve optical receiver efficiency.

The objective of this brief is to compare in nanometer CMOS technologies the power efficiency of optical interconnect architectures based on the aforementioned optical devices. This brief uses current state-of-the-art and reasonable projected optical device parameters and leverages previous optimization methods for optical receiver design [10] and overall link design [11]–[13]. In addition, an optimal current density methodology with normalized transistor parameters extracted from circuit simulations is applied to jointly optimize driver and receiver circuitry to minimize the total link power dissipation.

The optical interconnect architectures under consideration are outlined in Section II, including a near-term architecture using discrete VCSELs and PDs and three long-term integrated photonic architectures that use waveguide metal–semiconductor–metal (MSM) PDs and either EAM, RRM, or MZM sources. Section III discusses the optimization methodology, provides optical link performance comparisons in both 90- and 45-nm CMOS nodes, and also highlights the impact

Manuscript received October 29, 2009; revised February 6, 2010; accepted March 8, 2010. Date of current version May 14, 2010. This paper was recommended by Associate Editor V. Stojanovic.

The authors are with the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843 USA (e-mail: arunp_ece@neo.tamu.edu; spalermo@ece.tamu.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2010.2047319

TABLE I
OPTICAL DEVICE PARAMETERS (PARAMETERS IN PARENTHESES REFER TO THE 45-nm CMOS TECHNOLOGY)

Optical Device	Optical Device Parameters				
Tunnel Junction VCSEL [2]	CR = 5 dB	Ith = 0.5 mA	η = 0.28	Rs = 172 Ω	Cj = 130 fF
QWAFEM EAM [3]	CR = 5 dB	IL = 7.2 dB	Vbias = 2.4 V (2.2 V)	Vswing = 1.2 V (1.1 V)	Cmod = 200 fF
Waveguide EAM [4]	CR = 10 dB	IL = 5 dB	Vbias = 2.4 V (2.2 V)	Vswing = 1.2 V (1.1 V)	Cmod = 25 fF
Polymer based RR [6]	CR = 8dB	IL = 4 dB	Tuning Power =1mW	Vswing = 2.4 V (2.2 V)	Cmod = 10 fF
p-n diode based MZM [7]	V_π = 8 V	IL = 7 dB	Rload = 20 Ω		
Long wavelength PD [8]	PD Cap = 100 fF	Idark = 5 nA	Responsivity = 0.8 A/W		
Integrated PD [9]	PD Cap < 1fF	Idark = 100 μA	Responsivity = 0.9 A/W		

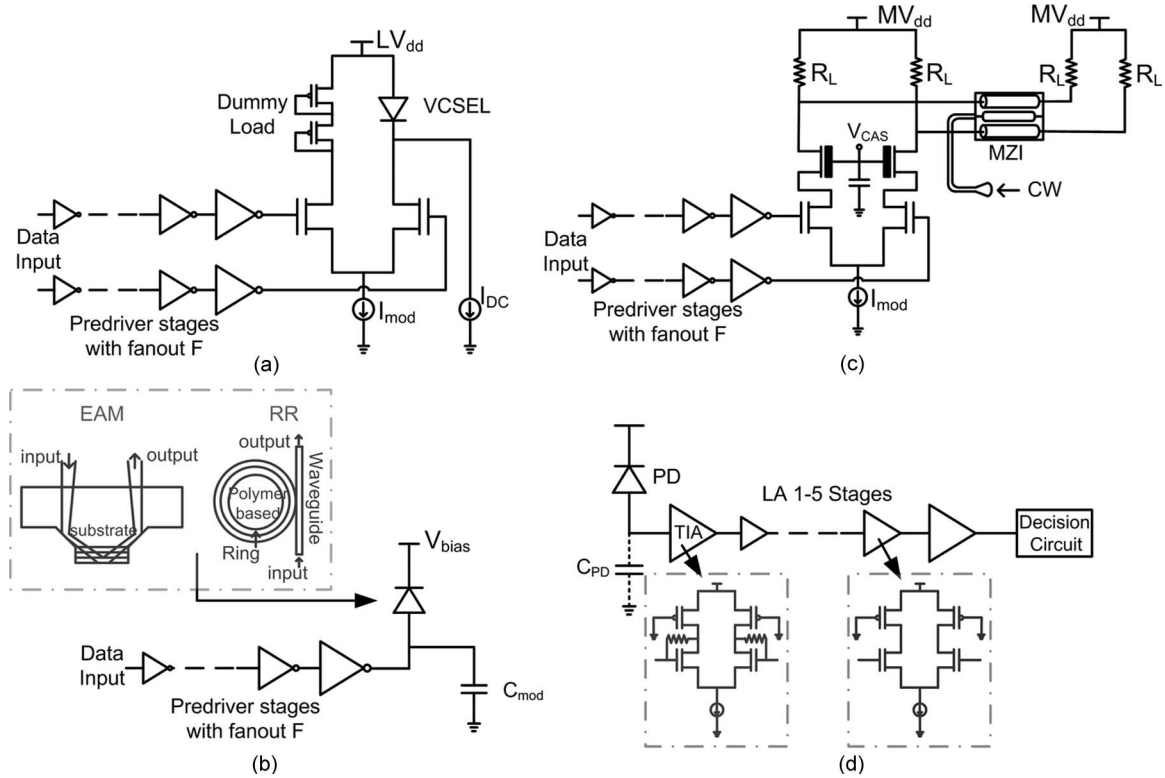

Fig. 1. Schematic of (a) VCSEL current mode driver, (b) EA modulator driver, (c) MZM driver, and (d) Transimpedance amplifier based receiver architecture.

of key optical parameters. The conclusions are summarized in Section IV.

II. OPTICAL LINK ARCHITECTURES

A. VCSEL

A high-speed 1.1-μm-range tunnel junction (TJ) VCSEL [2] is considered in this brief, parameters of which are given in Table I. Due to its linear optical power–current relationship beyond the threshold current $I_{\rm th}$, a differential current-mode driver [Fig. 1(a)] is used to modulate the VCSEL. The driver is driven by a set of cascaded predriver inverter stages with a fan-out of F, which in this analysis is optimized for transition times equal to one third of the bit period. A major constraint in the VCSEL is its bandwidth $\mathrm{BW}_{\rm VCSEL}$, which is dependent on the average current $I_{\rm avg}$ flowing through it, i.e.

$$\mathrm{BW}_{\rm VCSEL} \propto \sqrt{I_{\rm avg} - I_{\rm th}}. \quad (1)$$

B. EAM

To produce a modulated optical output signal, light originating from a continuous-wave source laser is absorbed in an EAM depending on the electric field strength through electrooptic (EO) effects such as the QCSE or the Franz–Keldysh effect. Two EAM devices were analyzed in this brief, namely, a quasi-waveguide angled-facet electroabsorption modulator (QWAFEM) surface normal device [3] and a waveguide modulator [4]. Table I summarizes the parameters of these devices, which includes increasing the reference waveguide EAM length for compatibility with nanometer CMOS voltage swings and using a smaller QWAFEM for lower capacitance. While the waveguide EAM achieves an excellent CR, it can suffer from poor misalignment tolerance due to coupling light into small waveguides. The QWAFEM structure combines features of surface normal and waveguide structures to achieve acceptable CRs at low voltage swings.

Modeled by a reverse-biased diode with a lumped capacitor, the EAM devices are driven by a voltage-mode driver consisting

of cascaded inverters [Fig. 1(b)]. Power dissipation [12], [13] consists of static absorbed photocurrent and dynamic switching components, in addition to external laser power. The swing voltage V_{swing} is assumed to be the nominal CMOS voltage supply V_{dd} for the given technology, and the prebias voltage V_{bias} is twice the supply voltage.

C. RRM

An EO polymer-based ring resonator (RR) [6] is used in this brief, which avoids carrier bandwidth limitations of a p-i-n diode-based RR [7]. Due to small dielectric constants and high confinement resonant ring structures, the polymer-based RR creates compact high-speed devices modeled as simple lumped-element capacitors. As polymer RRMs are still relatively immature, this brief assumes some improvements in EO coefficients to yield an 8-dB CR [9].

The RR is pseudodifferentially driven by two pairs of cascaded inverter stages to double the output swing and increase the CR. Power dissipation is similar to the EAM driver with slight modifications to account for the higher pseudodifferential output swing and the omission of the absorbed photocurrent term not present in the RRM. Due to the sensitivity of the RRM to process and temperature variations, additional tuning circuits are needed, whose power is assumed to be 1 mW (Table I) [14].

D. MZM

This brief analyzes an MZM based on the free-carrier plasma-dispersion effect, which has recently demonstrated 30-Gb/s operation [7]. Fig. 1(c) shows the MZM transmitter schematic [15]. Unlike smaller modulators that are treated as lumped capacitive loads, due to MZM length ($\sim$1 mm), the differential electrical signal is distributed using a pair of transmission lines terminated with a low impedance. To achieve the required phase shift and reasonable CR, long devices and large differential swings are required, necessitating a separate voltage supply $\mathrm{MV}_{\mathrm{dd}}$. Thick-oxide cascode transistors are used to avoid stressing driver transistors with the high supply. The output swing is optimized to minimize total power over data rate, with a 5-dB minimum CR constraint.

E. Receiver Architecture

Fig. 1(d) shows the transimpedance amplifier (TIA)-based receiver architecture consisting of the PD with its capacitance, TIA, limiting amplifier (LA) cells limited to a maximum of five stages, and finally ending in a decision circuit. A long-wavelength discrete p-i-n PD [8] with capacitance of 100 fF and dark current of 5 nA (Table I) is used in conjunction with the discrete TJ VCSEL link. For the other integrated CMOS photonic links based on modulators, an integrated waveguide MSM PD [9] with capacitance < 1 fF is used with a dark current level of 100 μA (Table I).

The decision circuit is assumed to have 20 $\mathrm{mV}_{\mathrm{pp}}$ input threshold ambiguity and 30 fF input capacitance, consistent with typical high-speed electrical deserializing decision circuit blocks [16].

III. Optimization and Comparison

A. Optimization Methodology

Obtaining accurate circuit modeling results requires accurate transistor parameters. These parameters are obtained from transistor-level simulations using a constant current density technique. Under fixed biasing conditions and finger sizing, the transistor drain current linearly increases with the transistor finger number, yielding a constant current density. Normalized transistor parameters (transconductance, output conductance, capacitance, etc.) are extracted at different biasing conditions corresponding to different transistor transition frequencies f_T.

The optimization objective is to minimize the total optical link power dissipation, including the receiver TIA and LA stages, transmitter predriver and driver circuits, RR tuning circuit power, static EAM power component, and external laser power. Clocking power common among all of the architectures, including clock synthesis, distribution, and recovery, is excluded in the reported power consumption. Using the normalized transistor parameters obtained from different bias points, the transmitter and the receiver are jointly modeled by iterating the design variables over the circuit and link constraints to satisfy particular data rate specifications at a given bit error rate (BER) of 10^{-12}. Multiple acceptable solutions are obtained, which correspond to differing circuit configurations, e.g., TIA with varying gain and LA stages, and optical transmitters with differing levels of optical output power. The minimum power solution is selected at each data rate from this matrix of acceptable link configurations.

The use of multiple biasing conditions in the different circuit blocks allows a wide design search space and provides a design solution where the transistors are biased near the optimum f_{T} to achieve the desired data rate for minimum power. The 90-nm process in this analysis achieves a peak f_{T} of 110 GHz at 0.4 $\mathrm{mA}/\mu\mathrm{m}$ current density, whereas scaling to the 45-nm process allows a 225-GHz peak f_{T} at 0.4 $\mathrm{mA}/\mu\mathrm{m}$.

B. Comparison of Different Optical Links

Optical device parameters and link budgets used in this brief are summarized in Tables I–III. The VCSEL average power is limited to 3 dBm maximum, whereas the external laser used in conjunction with the integrated modulators has an assumed 30% wall–plug efficiency and a maximum 10-mW electrical power, included in the total link power. CR power penalty and insertion loss are included based on each device's parameters. The lumped input capacitance of the discrete VCSEL-based link's receiver is 200 fF, which includes the 100-fF discrete PD and an assumed 100-fF bond-pad capacitance. The lumped input capacitance of the integrated link's receiver is 10 fF and is dominated by the interconnect capacitance. The receiver circuit input capacitance is added on top of these values to calculate the total input capacitance.

Using the previously discussed optimization methodology, the optimized power efficiency values for the optical links at various data rates are obtained. Fig. 2 compares the power efficiency of the TJ VCSEL-based link using the 90- and 45-nm CMOS processes. This link attained power efficiency values of

TABLE II
DISCRETE VCSEL-BASED OPTICAL LINK BUDGET

Max. Avg. VCSEL TX Power	3 dBm
VCSEL to MMF Coupling	- 1.1 dB
MMF to Photodetector Coupling	- 1.1 dB
Contrast Ratio (5 dB) Penalty	-2.844 dB
Margin	- 3 dB
Link Budget	- 8.044 dB
Required RX Sensitivity	- 5.044 dBm

TABLE III
INTEGRATED OPTICAL LINK BUDGET FOR EAM, MZM, AND RR

Max. Source CW Laser Power	4.8 dBm
Source Laser to SMF Coupling	- 2 dB
Modulator to SMF Coupling	- 2 dB
SMF to Photodetector Coupling	- 3 dB
Margin	- 3 dB
Contrast Ratio Penalty (CR_P)	depends on the device
Insertion Loss (IL)	depends on the device
Link Budget	- (10 + CR_P + IL) dB
Required RX Sensitivity	- (5.2 + CR_P + IL) dB

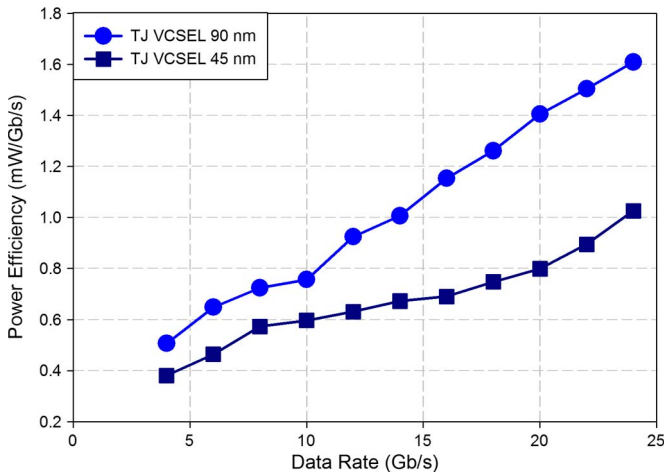

Fig. 2. Total power efficiency of VCSEL-based link versus data rate.

1.26 and 0.748 mW/Gb/s at a data rate of 18 Gb/s in 90- and 45-nm technologies, respectively. VCSEL bandwidth constraint (1) and maximum power levels limit the link performance at data rates higher than 24 Gb/s in both 90- and 45-nm nodes. Further improvements in increasing the VCSEL bandwidth by increasing device differential gain, reducing series resistance, and improving slope efficiency will result in improved power efficiency at higher data rates.

The waveguide EAM-based optical link achieves excellent power efficiency (Fig. 3) due to good CR, low swing and bias voltages, and small modulator capacitance. The other EAM structure, i.e., QWAFEM, has a reasonable CR at low voltage swings, but with relatively high insertion loss and large modulator capacitance, power dissipation is increased. The waveguide EAM achieves power efficiency values of 0.707 and 0.367 mW/Gb/s at 18 Gb/s in 90 and 45 nm in comparison with the QWAFEM structure, which achieves 1.29 and 0.727 mW/Gb/s power efficiency at the same data rate for the same technologies. Technology scaling yields higher transistor

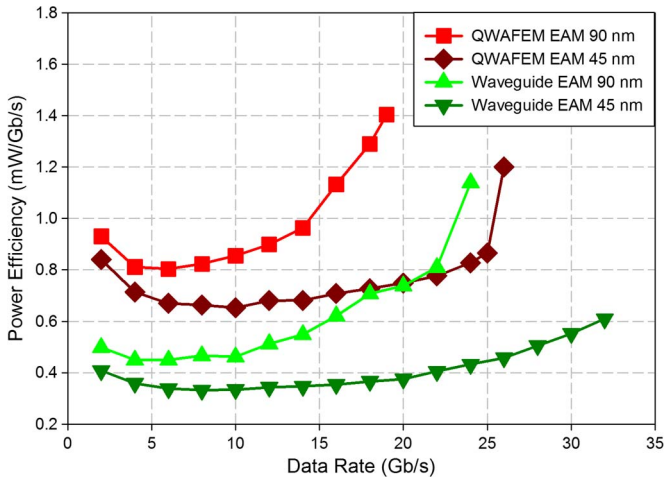

Fig. 3. Total power efficiency of EAM-based link versus data rate.

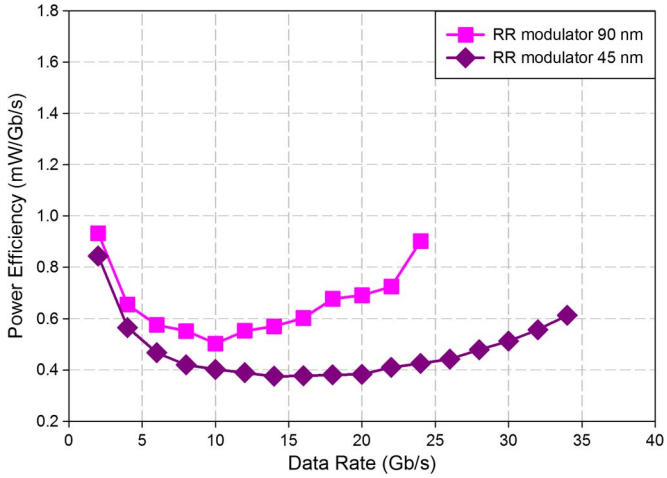

Fig. 4. Total power efficiency of RR-based link versus data rate.

f_T per current density, which allows the power efficiency of the integrated optical links to improve and the support of higher data rates. The maximum data rate extended from 24 to 32 Gb/s for the waveguide EAM and from 19 to 26 Gb/s for the QWAFEM EAM when scaling from 90 to 45 nm. When compared with the VCSEL link at 18 Gb/s, the waveguide EAM link attained 50% better power efficiency in the 45-nm node, whereas the QWAFEM link performance was similar to the VCSEL link. Improved alignment tolerance and coupling loss will further enhance the waveguide device's compatibility in high-volume applications, whereas QWAFEM structures with lower insertion loss and smaller capacitance would result in improved power efficiency.

The refractive RRM-based link achieves excellent power efficiency (Fig. 4) due to the good CR and ultralow modulator capacitance. At 18 Gb/s, it attains power efficiency values of 0.677 and 0.381 mW/Gb/s in 90- and 45-nm processes. Scaling from 90 to 45 nm has allowed the RRM data rate to increase from 10 to 30 Gb/s at power efficiency of 0.5 mW/Gb/s and extend the maximum operating data rate from 24 to 34 Gb/s. Comparing the RR link at 18 Gb/s in the 45-nm node, it achieved 50% improvement in power efficiency relative to the VCSEL and QWAFEM EAM and similar performance as the waveguide

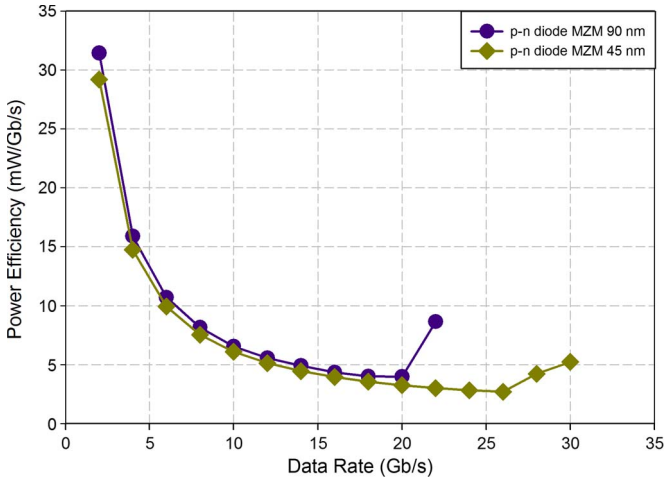

Fig. 5. Total power efficiency of MZM-based link versus data rate.

EAM. Although the RR-based link has very good power efficiency, RRs do have very low optical bandwidth (∼1 nm) [17] and are very sensitive to process and temperature variations. Efficient feedback tuning circuits and/or improvements in the device structure to allow less sensitivity to variations would enhance feasibility of these devices in high-density applications.

In contrast to the RR, the refractive MZM-based link has very wide optical bandwidth of around 100 nm [17] and improved tolerance to process and temperature fluctuations. While the voltage swing and CR were included in the power optimization, the resulting MZM link power efficiency was roughly one order of magnitude higher than the other optical links (Fig. 5). The achieved power efficiency values are 4.01 and 3.56 mW/Gb/s at 18 Gb/s data rate in the 90- and 45-nm processes. Technology scaling does not have a major impact, as the overall power is dominated by the voltage swing required for the low-impedance modulator. Methods to enhance the refractive index change are required to reduce device footprint and perhaps allow higher impedance termination.

IV. Conclusion

In conclusion, this brief has compared the power efficiency of different optical links proposed for high-density integration with CMOS chips and identified optical parameters critical to further power efficiency improvements. VCSEL bandwidth and maximum power levels limit the link performance in both 90- and 45-nm processes to 24 Gb/s. Among the integrated photonic links, the waveguide EAM and RR provide good power efficiency values attaining 0.5 mW/Gb/s in the 45-nm process at 28 and 30 Gb/s, respectively, while the misalignment-tolerant QWAFEM structure achieves 0.75 mW/Gb/s at 20 Gb/s. Although the MZM achieves wide optical bandwidth, significant improvements need to be made to obtain lower voltage swing and better power efficiency.

References

[1] D. A. B. Miller, "Physical reasons for optical interconnection," *Int. J. Optoelectron.*, vol. 11, no. 3, pp. 155–168, 1997.
[2] K. Yashiki, N. Suzuki, K. Fukatsu, T. Anan, H. Hatakeyama, and M. Tsuji, "1.1-μm-range high-speed tunnel junction vertical cavity surface emitting lasers," *IEEE Photon. Technol. Lett.*, vol. 19, no. 23, pp. 1883–1885, Dec. 2007.
[3] N. C. Helman, J. E. Roth, D. P. Bour, H. Altug, and D. A. B. Miller, "Misalignment-tolerant surface-normal low-voltage modulator for optical interconnects," *IEEE J. Sel. Topics Quantum Electron.*, vol. 11, no. 2, pp. 338–342, Mar./Apr. 2005.
[4] J. F. Liu *et al.*, "Ultralow energy, integrated GeSi electro-absorption modulators on SOI," in *Proc. 5th IEEE Int. Conf. Group IV Photonics*, Sep. 2008, pp. 10–12.
[5] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," *Nature*, vol. 435, no. 7040, pp. 325–327, May 2005.
[6] B. A. Block *et al.*, "Electro-optic polymer cladding ring resonator modulators," *Opt. Express*, vol. 16, no. 22, pp. 18 326–18 333, Oct. 2008.
[7] A. Liu *et al.*, "High-speed optical modulation based on carrier depletion in a silicon waveguide," *Opt. Express*, vol. 15, no. 2, pp. 660–668, Jan. 2007.
[8] PDCS20T, "Long wavelength 20 Gb/s photodiode chip," Albis OptoElectronic AG.
[9] I. Young *et al.*, "Optical I/O technology for tera-scale computing," *IEEE J. Solid-State Circuit*, vol. 45, no. 1, pp. 235–248, Jan. 2010.
[10] D. A. van Blerkom, C. Fan, M. Blume, and S. C. Esener, "Transimpedance receiver design optimization for smart pixel arrays," *J. Lightw. Technol.*, vol. 16, no. 1, pp. 119–126, Jan. 1998.
[11] P. Kapur, R. D. Kekatpure, and K. C. Saraswat, "Minimizing power dissipation in optical interconnects at low voltage using optimal modulator design," *IEEE Trans. Electron. Devices*, vol. 52, no. 8, pp. 1713–1721, Aug. 2005.
[12] H. Cho, P. Kapur, and K. C. Saraswat, "A modulator design methodology minimizing power dissipation in a quantum well modulator-based optical interconnect," *J. Lightw. Technol.*, vol. 25, no. 6, pp. 1621–1628, Jun. 2007.
[13] O. Kibar, D. A. van Blerkom, C. Fan, and S. C. Esener, "Power minimization and technology comparison for digital free-space optoelectronics interconnects," *J. Lightw. Technol.*, vol. 17, no. 4, pp. 546–555, Apr. 1999.
[14] C. Batten *et al.*, "Building manycore processor-to-DRAM networks with monolithic silicon photonics," in *Proc. 16th IEEE Symp. High Performance Interconnects*, Aug. 2008, pp. 21–30.
[15] B. Analui, D. Guckenberger, D. Kucharski, and A. Narasimha, "A fully integrated 20-Gb/s optoelectronic transceiver implemented in a standard 0.13-μm CMOS SOI Technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2945–2955, Dec. 2006.
[16] B. Casper *et al.*, "A 20 Gb/s forwarded clock transceiver in 90-nm CMOS," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 90–91.
[17] H.-W. Chen, Y.-H. Kuo, and J. E. Bowers, "High speed silicon modulators," in *Proc. OECC*, Hong Kong, Jul. 2009, pp. 1–2.