28.1 Optical I/O Technology for Tera-Scale Computing

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The microprocessor architecture transition from multi-core to many-core will drive increased chip-to-chip I/O bandwidth demands at processor/memory interfaces and in multi-processor systems. Future architectures will require bandwidths of 200GB/s to 1.0TB/s and will bring about the era of tera-scale computing. To meet these bandwidth demands, traditional electrical interconnect techniques require increases in circuit complexity and costlier materials. However, without lower loss electrical interconnects, this method of increasing I/O bandwidth in electrical links eventually comes at the cost of reducing interconnect link length, reducing signal integrity or increasing power consumption. Optical interconnect with its terahertz bandwidth, low loss, and low cross-talk has been proposed to replace electrical interconnect between chips [1]. This paper describes results for both near and long-term chip-to-chip optical interconnect architectures.

The near-term approach is a single package "hybrid" implementation [2] which avoids complex chip carrier packaging [3] and uses CMOS optical transceivers that are compatible with future integration in a microprocessor or logic die. Figure 28.1.1 shows the hybrid optical I/O package architecture that allows for up to 12 optical transmit or receive channels per optical connector. Linear 1×12 arrays of GaAs VCSELs and detectors are flip-chip bonded to the package substrate and polymer waveguides with 45° mirrors are embedded in the package substrate. In order to obtain adequate electrical signal integrity, the high-speed lines, which connect the VCSEL (photodiode) bumps to the transceiver chip's I/O bumps, are routed on the substrate surface as controlled 50Ω impedance microstrip traces. This avoids impedance discontinuities, while the close proximity between the transceiver chip and the optical elements minimizes frequency dependent loss. Power and bias planes are incorporated into the substrate to bias the optical elements.

An 8 channel prototype chip, shown in Fig. 28.1.7, was implemented in 90nm CMOS and includes 16 cells with VCSEL drivers, TIA receivers, and clock-data recovery (Fig. 28.1.2), which can be configured individually as optical TX/RX. The fully packaged prototype achieves open transmit and receive eye diagrams at up to 10Gb/s (Fig. 28.1.3). Higher data rates are possible with a combination of future packaging refinements aimed at reducing TIA input capacitance and circuit techniques, which extend VCSEL bandwidth. Electrical probe measurements of the TIA, which uses cross-coupled cascodes to boost gain and bandwidth [4], yields open eye diagrams at 12.5Gb/s and 18Gb/s with input capacitance of 260fF and 90fF, respectively. Implementing sub-bit interval pre-emphasis in the transmitter [4] allows for 18Gb/s operation with 122% vertical and 76% horizontal eye opening improvement with a 10Gb/s-class VCSEL. The optical receiver and driver energy efficiency is 11pJ/b at 10Gb/s, including the 38mW TIA/limiting amplifier and a reduced power 72mW transmitter that excludes pre-emphasis. In order to achieve higher data rates, switching to the 134mW pre-emphasis driver allows for a potential energy efficiency of 9.6pJ/b at 18Gb/s. Circuit simulation analysis on the full transceiver cell with the hybrid optical-electrical package architecture indicates that performance scaling offered by a 45nm or 32nm process provides the potential for operation at over 30Gb/s with sub-3pJ/b total transceiver energy efficiency including clock generation/recovery circuitry.

Our longer-term optimal approach to optical I/O uses fully monolithic, integrated single-mode silicon nitride optical waveguides, silicon nitride waveguide coupled metal-semiconductor-metal (MSM) Ge detectors, and electro-optical (EO) polymer based ring-resonator modulators on-die with the microprocessor/logic in a CMOS process [5]. The goal is to make optical components that can achieve very high bandwidth (100GB/s to TB/s links), high bandwidth density, and energy efficiency for an optical I/O link that is not only compatible with CMOS processing, but can be fabricated in the same process flow monolithically with the transistors without sacrificing transistor performance. The single mode ring-resonator architecture also enables WDM multiplexing and de-multiplexing providing TB/s interconnects. The monolithic architecture uses a single external off-chip CW laser source that is coupled to the on-die single-mode silicon nitride waveguides to distribute the optical power to electrically driven E-O ring-resonator modulators having typical ring diameters between 40 and 100μm.

The modulator design is an electro-optic (EO) polymer based modulator where the EO polymer is the top optical cladding to a silicon nitride waveguide. The linear EO effect is used to modify the index of the EO polymer and the optical mode effective index. This index change is exploited to modulate the intensity of light. The EO polymer based modulator technology has many desirable characteristics. First, electro-optic coefficients for chromophore polymers have been reported at values greater than 300 pm/V [6] or more than 10× that of LiNBO3, an optical industry standard modulator material. The mechanism creating the high electro-optic effect is a shuttling of the electrons within the molecular orbital of the EO chromophore material, which is inherently very fast and has been demonstrated in optical modulators at hundreds of GHz [7]. Additionally, the dielectric constant of the EO polymers is relatively low ($\varepsilon \sim 4$), and with the small size of the ring resonator leads to very low lumped capacitance. This makes it possible to realize a high speed modulator without the need for low loss traveling wave electrodes which consume considerable power [10]. Figure 28.1.4 shows the ring-resonator cross-section, which achieved 10GHz modulation at $2.7V_{pp}$ drive and, with an improved polymer and $8V_{pp}$ drive, 20Gb/s PRBS transmission. The EO polymer does not require high temperature processing enabling this modulator to be inserted into the backend of the CMOS process unlike [8] where the modulator must be fabricated with a thick BOX SOI wafer. Conventional copper damascene co-planar electrodes are used to apply the controlling electric field.

The integrated MSM Ge detector [9] layout and cross-section is shown in Figure 28.1.5. The Ge active material is grown directly on a SiO_2 interlayer dielectric (ILD) that is compatible with integration in the back-end metallization layers of a CMOS process. On typical devices, which are about 3μm long and 0.5 to 1.0μm wide, the measured responsivity was 0.9A/W at 1V bias and the bandwidth was 35GHz. High frequency probe measurement of the detector has an open eye with 20Gb/s PRBS NRZ data (Fig. 28.1.6).

Since CPU optical interconnect will first be introduced for the package-to-package optical I/O, the initial realization will be with "hybrid" single package technology. If the challenges of fully integrated optical elements in the CMOS process can be overcome, then monolithically integrated optical components will provide the path to the TB/s I/O data rates with the required energy efficiency near 1pJ/b.

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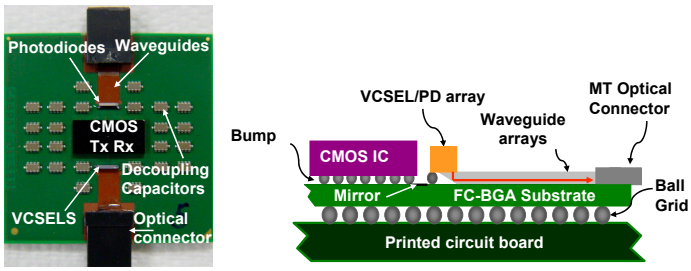

Figure 28.1.1: Fully assembled optical transceiver unit with side view of optical coupling of lasers / photo-detectors to waveguides through a 45° mirror.

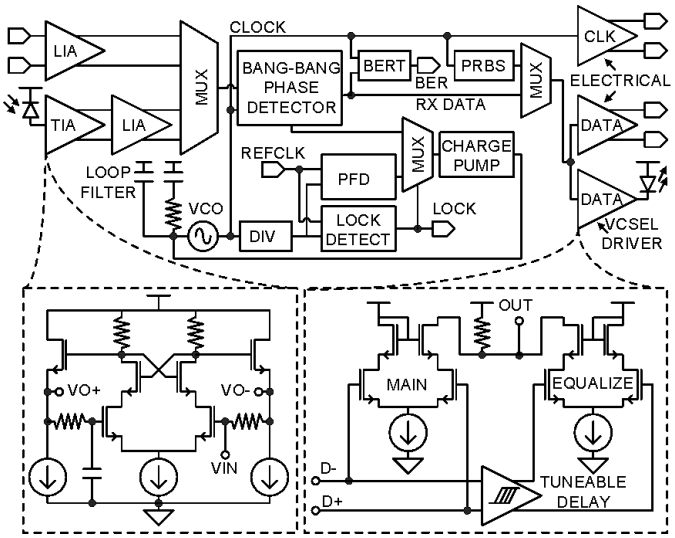

Figure 28.1.2: Optical transceiver cell.

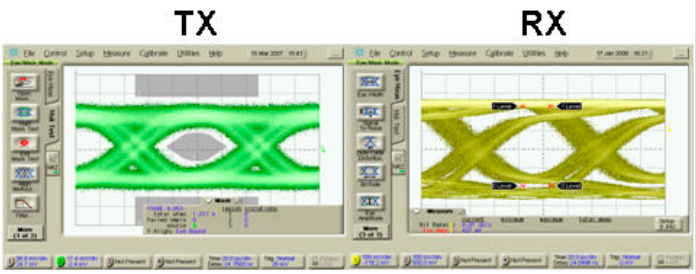

Figure 28.1.3: 10Gb/s eye diagrams from fully packaged VCSEL transmitter and optical receiver.

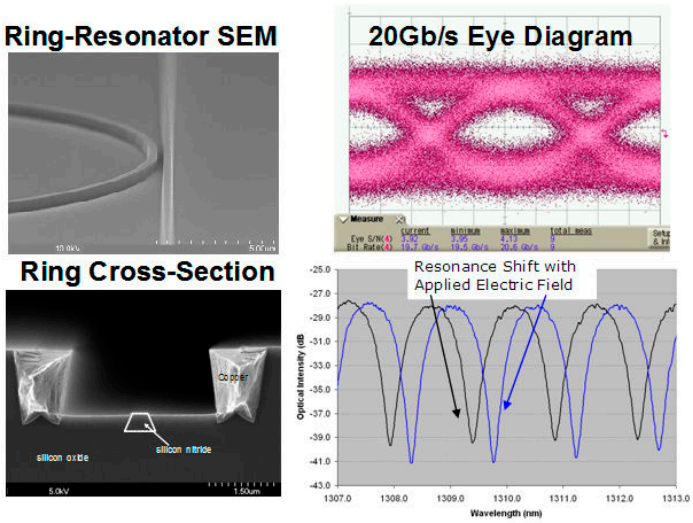

Figure 28.1.4: Ring-resonator electro-optic polymer modulator device structure and performance.

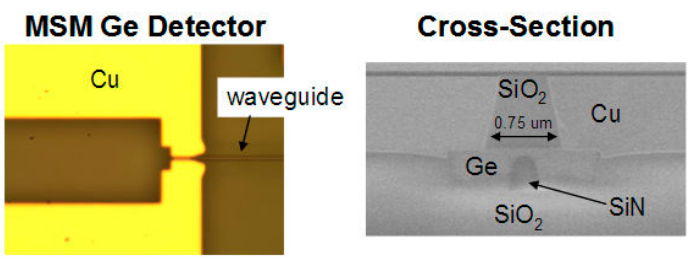

Figure 28.1.5: CMOS logic compatible waveguide coupled MSM Ge photodetector.

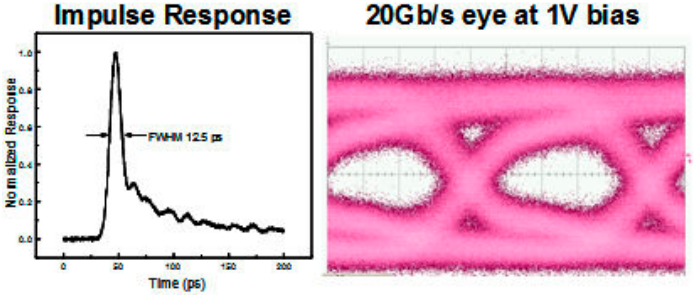

Figure 28.1.6: MSM Ge photodetector performance.

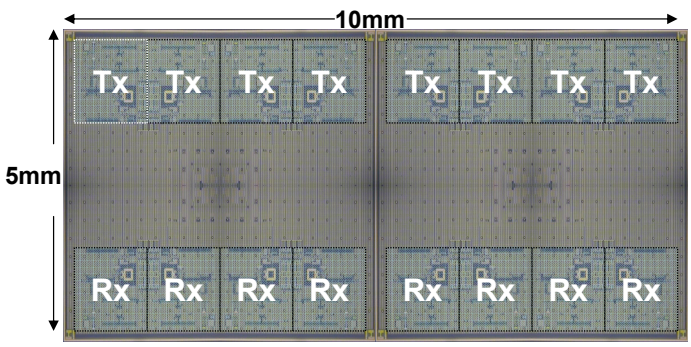

Figure 28.1.7: 8-channel optical transceiver die.

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