A 6-Gbit/s Hybrid Voltage-Mode Transmitter With Current-Mode Equalization in 90-nm CMOS

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***Abstract*—Low-power (LP) high-speed serial I/O transmitters which include equalization to compensate for channel frequency-dependent loss are required to meet the aggressive link energy-efficiency targets of future systems. This brief presents an LP serial-link-transmitter design that utilizes an output stage which combines a voltage-mode driver, which offers low static-power dissipation, and current-mode equalization, which offers low complexity and dynamic-power dissipation. The utilization of current-mode equalization decouples the equalization settings and termination impedance, allowing for a significant reduction in predriver complexity relative to segmented voltage-mode drivers. Proper transmitter series termination is set with an impedance control loop which adjusts the on-resistance of the output transistors in the driver voltage-mode portion. Further reductions in dynamic-power dissipation are achieved through scaling the serializer and local clock distribution supply with data rate. Fabricated in a 1.2-V 90-nm LP CMOS process, the transmitter supports an output swing range of 100–400 $\mathrm{mV_{ppd}}$ and up to 6 dB of equalization and includes output-duty-cycle control. The transmitter achieves 6-Gbit/s operation at 1.26-pJ/bit energy efficiency with 300-$\mathrm{mV_{ppd}}$ output swing and 3.72-dB equalization.**

***Index Terms*—Channel impedance matching, high-speed link, I/O, low power (LP), transmit equalization.**

I. Introduction

A LARGE percentage of serial-link power is often consumed in the transmitter, which must provide adequate signal swing on the low-impedance channel, maintain proper source termination, and include equalization to compensate for channel frequency-dependent loss. In low-power (LP) designs, the output driver often consumes the majority of the static power due to the low-impedance channel. This leads link architects to consider voltage-mode drivers to improve energy efficiency, as with differential receiver-side termination, these drivers have the potential to consume one-quarter of the output-stage power relative to conventional current-mode drivers [1].

While obtaining significant improvements in I/O energy efficiency will require improvements in electrical channel loss characteristics [1], the ability to efficiently include some transmit equalization allows for more loss compensation and increased flexibility in equalization circuitry partitioning. However, the potential power savings of voltage-mode drivers generally degrade with the introduction of transmit equalization and overheads associated with maintaining proper source termination. In order to generate the different output voltage levels for transmit equalization, significant output-stage segmentation is required in voltage-mode drivers which implement resistor divider [2]–[4] and channel shunting approaches [5]. This segmentation increases predriver complexity, resulting in degraded dynamic-power consumption. Additional output-stage segmentation is often implemented to digitally tune the driver termination to match the channel [5], further degrading energy efficiency. While analog control loops which scale the predriver supply can be utilized to set the driver output impedance [2], [6], [7], this does not allow independent optimization of the predriver supply to minimize dynamic power with data rate.

This brief presents a hybrid voltage-mode transmitter with current-mode equalization, which enables independent control over termination impedance, equalization settings, and predriver supply, allowing for a significant reduction in predriver complexity and power. Transmitter equalization techniques are reviewed in Section II, with a comparison of the hybrid transmitter with voltage- and current-mode drivers. Section III details the transmitter architecture, which includes local clocking circuitry with duty-cycle correction, low-complexity scalable-supply serialization and predriver, hybrid driver, and global impedance control. Experimental results from a 90-nm LP CMOS prototype are presented in Section IV. Finally, Section V concludes this brief.

II. Transmitter Equalization Techniques

Channel frequency-dependent loss, which causes intersymbol interference, is often compensated by equalization implemented at the transmitter in the form of an FIR filter. Fig. 1 shows examples of a two-tap FIR filter, with one main-cursor tap and one postcursor tap, in low-swing voltage-mode, current-mode, and proposed hybrid drivers. Assuming a standard two-tap high-pass FIR filter with a negative postcursor tap $[1-\alpha, -\alpha]$, the equalization coefficient α is

$$\alpha = \frac{1}{2} \cdot \left(1 - \frac{\mathrm{V_{ppd,min}}}{\mathrm{V_{ppd,max}}}\right) \tag{1}$$

and the amount of equalization peaking is

$$EQ\,[\mathrm{dB}] = 20 \cdot \log\left(\frac{1}{1-2\alpha}\right). \tag{2}$$

Two techniques to implement FIR equalization in the low-swing voltage-mode driver include a resistive voltage divider [Fig. 1(a)] [2]–[4] and the inclusion of an additional shunting

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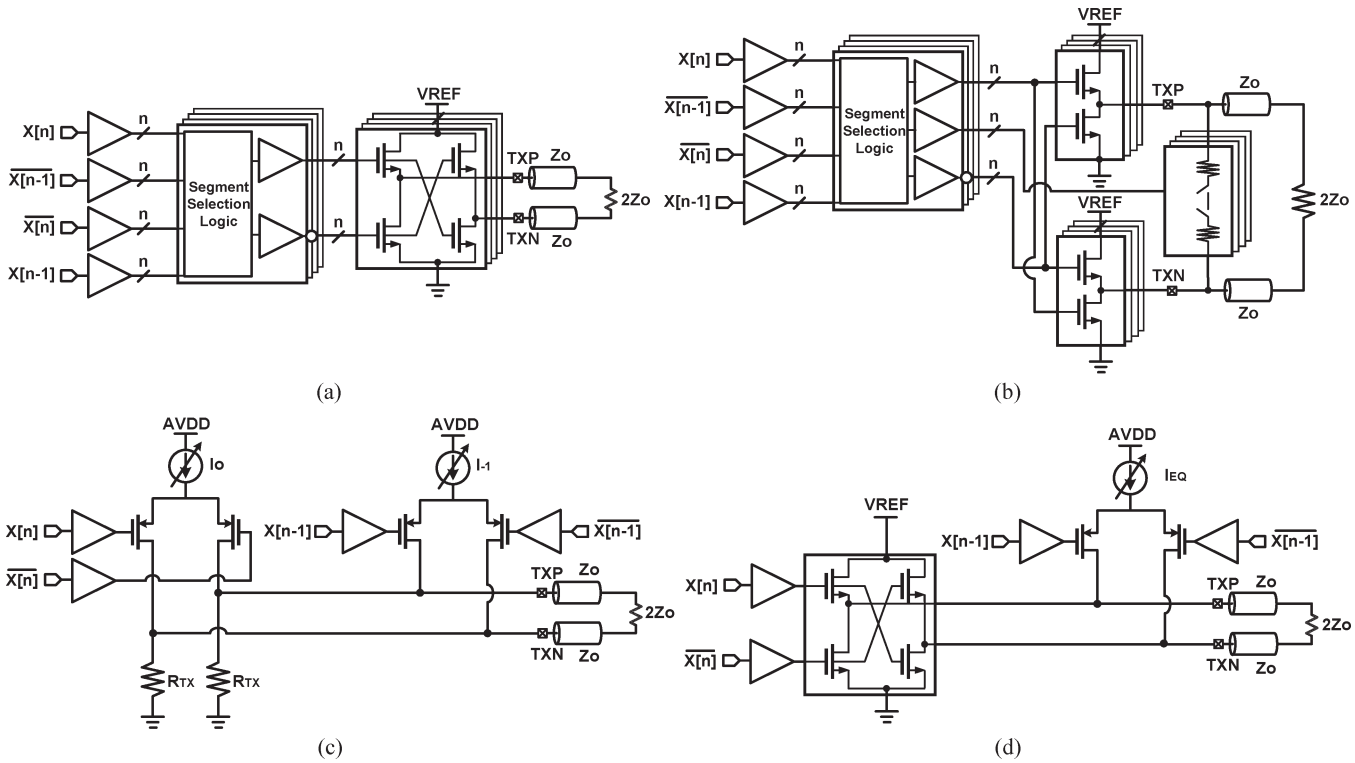

Fig. 1. Implementation of two-tap FIR equalization in (a) low-swing voltage-mode drivers with segmented resistive voltage divider [2]–[4], (b) low-swing voltage-mode driver with shunting resistor network [5], (c) current-mode driver [1], and (d) proposed low-swing voltage-mode driver with current-mode equalization.

TABLE I
TRANSMITTER TWO-TAP EQUALIZATION COMPARISONS ($V_{\mathrm{ppd,max}} = 400$ MV, $V_{\mathrm{ppd,min}} = 200$ MV, $\alpha = 0.25$, AND $Z_o = 50\ \Omega$)

	[2]		[3]		[5]		[1]		Proposed TX	
$I_{Vppd,max}$	$\frac{Vppd,max}{4Zo}$	2mA	$\frac{Vppd,max}{4Zo}$	2mA	$\frac{Vppd,max}{4Zo}$	2mA	$\frac{Vppd,max}{Zo}$	8mA	$\frac{Vppd,max}{4Zo}$	2mA
$I_{Vppd,min}$	$\frac{Vppd,max}{4Zo}(1+4\alpha(1-\alpha))$	3.5mA	$\frac{Vppd,max}{4Zo}(1-2\alpha)$	1mA	$\frac{Vppd,max}{4Zo}$	2mA	$\frac{Vppd,max}{Zo}$	8mA	$\frac{Vppd,max}{4Zo}(1+2\alpha)$	3mA
ΔI	$\frac{Vppd,max}{4Zo}(4\alpha(1-\alpha))$	1.5mA	$\frac{Vppd,max}{4Zo}(2\alpha)$	1mA	0	0	0	0	$\frac{Vppd,max}{4Zo}(2\alpha)$	1mA
R_{TX}	Zo	50Ω	Zo, $\frac{(1+2\alpha)}{(1-2\alpha)}$Zo	50,150Ω	Zo	50Ω	Zo	50Ω	Zo	50Ω
VREF	Vppd,max	400mV	Vppd,max	400mV	Vppd,max	400mV	-	-	Vppd,max(1 - α)	300mV
Pre Driver Complexity	High		High		High		Simple		Simple	

*Zo: channel characteristic impedance, α: equalization coefficient, $V_{ppd,max}$: differential peak-to-peak maximum swing, $V_{ppd,min}$: differential peak-to-peak minimum swing, $I_{Vppd,max}$: current with maximum differential output swing level, $I_{Vppd,min}$: current with minimum differential output swing level, $\Delta I = |I_{Vppd,max} - I_{Vppd,min}|$, R_{TX}: transmitter termination impedance, VREF: output driver reference voltage

resistor network [Fig. 1(b)] [5]. Here, both techniques utilize segmentation of the output driver to implement the different output voltage levels for equalization. In the design in [2] and [4], a $1-\alpha$ percentage of the output segments is controlled by the main-cursor tap, and an α percentage is controlled by the postcursor tap, with the output segments sized to ensure that all parallel combinations maintain proper source termination. Note that, as shown in Table I, the current drawn from the output driver supply V_{REF} varies with the output level, with all current flowing out into the channel during the maximum output swing and a portion being sunk at the transmitter during the de-emphasized level. This current variation can be a problem, as it necessitates more stringent voltage regulation of the V_{REF} supply. The design in [3] sacrifices a constant channel match and modulates the output impedance to achieve a lower output voltage level at a lower current level, while a constant current draw is achieved in [5] by switching a shunt resistor network in addition to the main output transistors.

The main drawback associated with these voltage-mode-driver designs involves the overhead in the predrive logic required to distribute the tap weights among the segments, which grows with equalization resolution. In contrast, as shown in Fig. 1(c), current-mode drivers offer the potential to implement high-resolution equalization without significant predriver complexity by setting the tap coefficients with tail-current-source digital-to-analog converters (DACs). If the output switches of the current steering stages are sized to handle the maximum tap current, only a single predrive buffer is required per

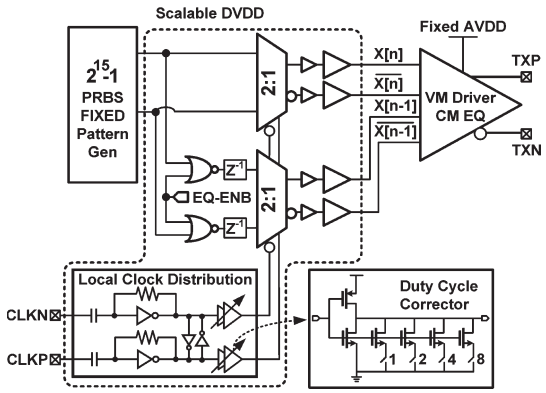

Fig. 2. TX block diagram.

equalization tap. However, this reduction in predrive dynamic power is greatly overshadowed by the four-times increase in output-stage static current due to the parallel termination scheme.

Fig. 1(d) shows a simplified schematic of the hybrid driver proposed in this brief which combines the low output current levels of a voltage-mode driver to implement the main tap and a parallel current-mode driver to implement the post-cursor tap with minimal predriver complexity. While parallel current drivers have previously been implemented with voltage-mode drivers as swing enhancers [4], this implementation improves driver energy efficiency by eliminating the voltage-mode-driver segmentation, as the equalization coefficient is set via the current-mode-driver tail-current DAC setting.

For the hybrid two-tap driver, the voltage-mode output-stage reference voltage is reduced to a value of $V^*_{\mathrm{ppd.max}}(1-\alpha)$, and the maximum swing is

$$V_{\mathrm{ppd,max}} = 2 \cdot \left[\frac{Z_o}{R_{\mathrm{TX}} + Z_o} \cdot V_{\mathrm{REF}} + (R_{\mathrm{TX}} // Z_o) \cdot I_{\mathrm{EQ}} \right] \quad (3)$$

where R_{TX} is the transmitter impedance and I_{EQ} is the equalization current. The minimum differential voltage swing is

$$V_{\mathrm{ppd,min}} = 2 \cdot \left[\frac{Z_o}{R_{\mathrm{TX}} + Z_o} \cdot V_{\mathrm{REF}} - (R_{\mathrm{TX}} // Z_o) \cdot I_{\mathrm{EQ}} \right]. \quad (4)$$

III. Transmitter Architecture

Fig. 2 shows the block diagram of the serial-link transmitter which utilizes two power supplies, a 1.2-V fixed $AVDD$, and a scalable $DVDD$. The local clock distribution, serialization muxes, and predriver buffers are powered from $DVDD$ which is scaled with data rate in order to improve the transmitter power efficiency. While an external supply was used for $DVDD$ in this design, an adaptive switching regulator [8] could efficiently generate this scalable supply. A fixed 1.2-V $AVDD$ supply is used to supply sufficient voltage headroom for the voltage-mode output-stage regulator, the current-mode equalizer stage, and the global impedance controller.

Two bits of parallel input data from on-die test circuitry capable of generating either a $2^{15}-1$ pseudorandom binary sequence (PRBS) or 16-bit fixed data pattern serves as the input to the half-rate output stage. The output stage includes two sets of 2:1 muxes to implement a two-tap FIR equalization filter, with the top mux driving the main-cursor voltage-mode driver and the bottom mux driving the postcursor current-mode

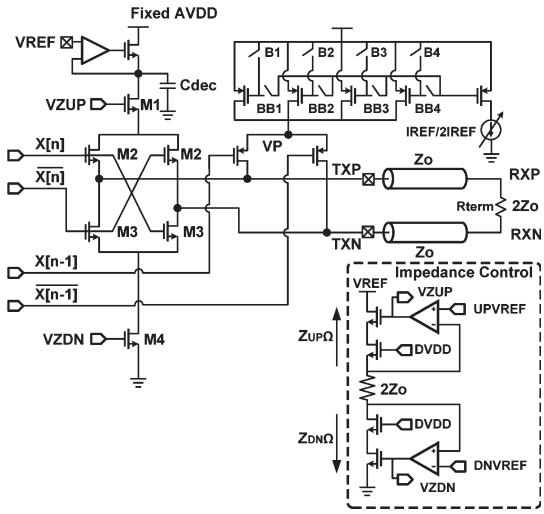

Fig. 3. Hybrid voltage-mode driver with current-mode equalization.

equalizer stage. In order to reduce power consumption for operation when equalization is not necessary, the data in the equalizer path are gated to disable the equalization serializer and any output equalization current.

In order to provide compatibility with low-swing global clock distribution present in LP multichannel link systems, an ac-coupled current mode logic (CML)-to-CMOS local clock distribution stage generates the serializer clocks. The transmitter utilizes inverter-based clock buffers with 4-bit digitally adjustable pMOS/nMOS size ratio in order to tune out errors in input duty cycle and clock distribution network mismatches, allowing the output duty cycle to be corrected to within $\pm 1\%$ over a data rate range of 2–6 Gbit/s.

After serialization with half-rate clocks, the main-cursor data signals drive the switches (M2 and M3) of an nMOS low-swing voltage-mode driver, while the delayed data signals drive the switches of a pMOS differential current-mode driver to implement the postcursor tap, which is shown in Fig. 3. Here, equalization adjustment is possible with minimal overhead, with the tail current source of the current-mode stage having 4-bit binary control. A reference current switchable between 60 and 120 μA allows for the addition of a total equalization current of 0.9–1.8 mA into the output stage at 4-bit resolution. The equalization current is steered between the driver outputs by switching the pMOS output switches, which are sized to handle the maximum equalization current setting. This allows the use of a single nonsegmented predriver to switch the pMOS output switches, greatly simplifying the output driver predrive complexity relative to other voltage-mode drivers which include equalization taps [2]–[5]. Higher resolution is achievable with ideally no power overhead simply by increasing the tail-current DAC bits. While this design is intended for low-/medium-loss channels, and thus only implemented two taps, the scheme is easily extendable to higher tap values with additional parallel current drivers.

The driver pull-up impedance Z_{UP} is set by the M2 top switches and an additional shared M1 transistor whose gate is controlled by $V_{Z_{\mathrm{UP}}}$, while the pull-down impedance Z_{DN} is set by the M3 bottom switches and an additional shared M4 transistor whose gate is controlled by $V_{Z_{\mathrm{DN}}}$. A global impedance control loop allows for both the driver Z_{UP} and Z_{DN}

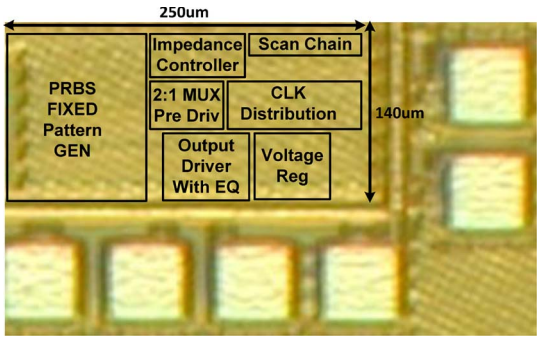

Fig. 4. Die photograph.

impedances to be set near the channel impedance by utilizing a replica transmitter with dual feedback amplifiers that forces $V_{Z_{\rm UP}}$ to a value consistent with a high output level of

$$UPV_{\rm REF} = \left(\frac{2Z_o + Z_{\rm DN}}{Z_{\rm UP} + 2Z_o + Z_{\rm DN}}\right) V_{\rm REF} \tag{5}$$

and sets $V_{Z_{\rm DN}}$ to a value consistent with a low output level of

$$DNV_{\rm REF} = \left(\frac{Z_{\rm DN}}{Z_{\rm UP} + 2Z_o + Z_{\rm DN}}\right) V_{\rm REF}. \tag{6}$$

In this design, an external supply was used for the adjustable reference voltage $V_{\rm REF}$ that sets the output driver swing, and an on-chip resistive divider generates the impedance control loop $UPV_{\rm REF}$ and $DNV_{\rm REF}$ signals from $V_{\rm REF}$.

While other voltage-mode impedance control schemes primarily utilize the predriver supply voltage [2], [6], [7], the method implemented in this work allows the predrive swing value ($DVDD$) to be decoupled from the impedance control, providing a degree of freedom to allow for potential predrive voltage scaling for improved energy efficiency. In order to reduce the gate capacitance of the switch transistors and save power, this design intentionally targets a 60-Ω single-ended output impedance. While not an exact channel match, this still provides a simulated low-frequency return loss of −22 dB, which meets the industry-standard return loss specifications [6]. Simulation results with backplane channels also indicate eye height degradation that is less than 3% relative to a 50-Ω design.

An on-chip linear voltage regulator sets the power supply of the voltage-mode driver to a value $V_{\rm REF}$, which is equal to the peak-to-peak differential output swing without equalization, and allows for an adjustable output swing from 100 to 400 $\rm mV_{ppd}$. The driver's low common-mode output voltage allows for the regulator to have a source-follower output stage, which offers improved supply-noise rejection relative to common-source output stages [6]. The low output impedance of the source follower allows for the use of a 40-pF decoupling capacitor to improve the power supply rejection ratio, while still maintaining stability.

IV. Experimental Results

The transmitter was fabricated in a 90-nm LP CMOS process. As shown in the die photograph in Fig. 4, the total transmitter active area is 250 μm × 140 μm.

Fig. 5(a) shows the low-frequency output patterns with a peak output swing near 400 $\rm mV_{ppd}$ and a maximum equalization value of 6 dB. The measured equalization settings match well with the linear value in decibels predicted by (2), with a slope of 0.4 dB/code for a 400-$\rm mV_{ppd}$ max swing and a 120-μA reference current setting [Fig. 5(b)]. In the hybrid driver, if the current-mode equalization settings are increased beyond 6 dB, the regulator is required to sink a portion of the equalization current. While this is not possible with the current regulator implementation, for LP serial-link transceivers which often also implement efficient receiver-side continuous-time linear equalizers, this level of transmit equalization is generally suitable for channels with 15–20 dB of loss at the Nyquist frequency. For increased equalization settings, the regulator output stage can be modified to sink a portion of the equalization current for equalization settings above 6 dB.

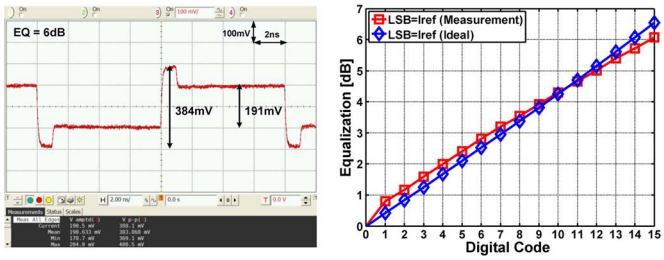

Fig. 5. (a) Low-frequency transmitter output waveform with 6-dB equalization. (b) Equalization peaking versus digital code for 400-$\rm mV_{ppd}$ peak output swing and 120-μA $I_{\rm REF}$.

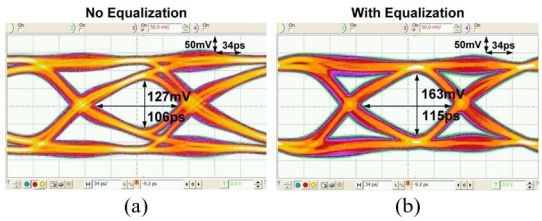

Fig. 6. Six-gigabit-per-second eye diagrams with a channel that has 4-dB loss at 3 GHz. (a) Without equalization. (b) With equalization.

The transmitter transient performance at a maximum of 6-Gbit/s data rate is verified in the $2^{15} - 1$ PRBS eye diagrams with operation over a 3-in FR4 channel with 4-dB loss at 3 GHz, shown in Fig. 6. By enabling the current-mode equalization, improvement is achieved in both eye height (127–163 mV) and eye width (106–115 ps). Testing with 3-GHz fixed clock patterns shows no significant degradation in output jitter with equalization enabled, 3.43-$\rm ps_{rms}$ jitter without equalization, and 3.17-$\rm ps_{rms}$ jitter with 6-dB equalization and the same 200-$\rm mV_{ppd}$ output swing. With the addition of an subminiature version A (SMA) cable to the 3-in FR4 channel, the total channel loss increases to 6 dB at 2.4 GHz, and the performance with maximum equalization settings is verified in the 4.8-Gbit/s eye diagram in Fig. 7. Again, improvement is achieved in both eye height (87–146 mV) and eye width (123–150 ps).

Fig. 8(a) shows how $Z_{\rm UP}$ and $Z_{\rm DN}$ vary as the output swing without equalization $V_{\rm REF}$ varies from 100 to 400 $\rm mV_{ppd}$. Relative to the 60-Ω target output impedance, $Z_{\rm UP}$ and $Z_{\rm DN}$ vary by maximum values of 7% and 10%, respectively. This is due to the driver output impedance increasing because of the reduced amplifier gain at the higher $V_{Z_{\rm UP}}$ and $V_{Z_{\rm DN}}$ output voltages required as the output swing increases.

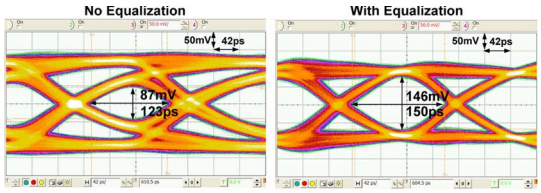

Fig. 7. 4.8-Gbit/s eye diagrams with a channel that has 6-dB loss at 2.4 GHz. (a) Without equalization. (b) With equalization.

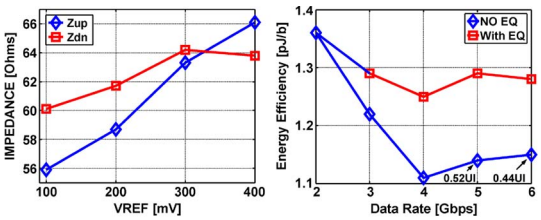

Fig. 8. (a) Measured transmitter output impedance versus V_{REF}. (b) Energy efficiency versus data rate for channel outputs of 50-mV eye height and 0.6-UI eye width.

Fig. 8(b) illustrates the efficiency of the equalization technique implemented in the hybrid driver. For the 3-in FR4 channel and cable used in the Fig. 7 eye diagrams, transmitter energy efficiency versus data rate for minimum channel outputs of 50-mV eye height and 0.6-UI eye width is shown with and without equalization. For data rates of 4 Gbit/s and lower, equalization is not required for the target eye opening, and a 1.11-pJ/bit optimal energy efficiency is achieved at 4 Gbit/s. Including equalization improves the overall eye margins and is necessary above 4 Gbit/s to achieve 0.6-UI eye width. Activating the equalization circuitry to achieve the target eye margins raises the energy efficiency by less than 0.2 pJ/bit up to 6 Gbit/s.

Table II shows a measured power breakdown at different data rates and equalization conditions. For the 6-Gbit/s settings used in the eye diagram in Fig. 6, 1.26-pJ/bit energy efficiency is achieved, with the largest power consumption from the 1.2-V $DVDD$ supply. As the data rate is dropped to 2 Gbit/s, significant $DVDD$ power savings are achieved by reducing the supply to 0.8 V. However, the total transmitter energy efficiency is dominated by the output-stage power, and 1.36 pJ/bit is achieved with 100-$\mathrm{mV_{ppd}}$ output swing and no equalization. Table III shows a comparison of this design with other low-swing voltage-mode transmitters. Relative to the design in [7] which was implemented in a similar process, the presented design allows for higher data rate operation with the efficient inclusion of two-tap FIR equalization and four times the output swing. The efficiency of the equalization is evident by comparing this work with that in [2], which implemented two-tap output equalization via a segmented resistor divider approach.

V. Conclusion

This brief has presented a hybrid voltage-mode transmitter with current-mode equalization, which enables independent control over termination impedance, equalization settings, and predriver supply. By controlling the equalization settings with a tail-current-source DAC in the parallel current-mode driver, segmentation is eliminated in the voltage-mode output stage, allowing for significant reduction in predriver complexity and power. Output impedance control is maintained in a manner that is compatible with supply scaling with additional series transistors in the voltage-mode output stage which are controlled by a global impedance control loop. These techniques allow for efficient transmit equalization over a wide range of data rates, supply voltages, and output swing levels.

TABLE II
Transmitter Performance Summary

	6Gbps	4Gbps	2Gbps
TX swing	300mV with 3.72dB EQ	300mV	100mV
Analog power Supply	1.2V	1.2V	1.2V
LDO & Output Driver	3.22mW	2.84mW	1.96mW
Global Impedance Control (amortized across 8 TX)	219uW	236uW	187uW
DVDD	1.2V	1V	0.8V
Serializer, Pre-drivers, Clocking	4.1mW	1.79mW	0.56mW
Energy Efficiency	1.26pJ/b	1.22pJ/b	1.36pJ/b

TABLE III
Transmitter Performance Comparisons

	[7]	[2]	This Work
Technology	90nm CMOS	0.18um CMOS	90nm CMOS
Supply Voltage	1.2V	1.8V	0.8~1.2V
Data Rate	0.5~4Gb/s	3.6Gb/s	2~6Gb/s
TX Swing	100mVppd	250mVpps	100mVppd~ 400mVppd
Equalization	None	2-Tap FIR	2-Tap FIR
Energy Efficiency	0.6p/b @3.2Gb/s	2.68pJ/b @3.6Gb/s	1.26pJ/b @6Gb/s

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