Embedded Equalization for ADC-Based Serial I/O Receivers

Ayman Shafik, Keytaek Lee, Ehsan Zhian Tabasy, and Samuel Palermo
Department of Electrical and Computer Engineering
Texas A&M University, College Station, TX, USA
aameen@neo.tamu.edu, spalermo@ece.tamu.edu

***Abstract*– In this paper, the performance impact of embedding partial equalization in ADC-based receivers is analyzed. A hybrid ADC receiver architecture which includes embedded equalization and selective digital equalization power-down based on threshold detection is proposed.**

Keywords- ADC-based receiver; embedded equalization; DFE; FFE; statistical BER.

I. INTRODUCTION

Operation at high data rates over standard electrical channels is challenging due to excessive frequency-dependent channel attenuation which causes large amounts of inter-symbol interference (ISI). In order to operate reliably over such channels at high data rates, equalizer circuits are usually employed. These are often implemented at the transmitter or the receiver in the form of continuous time linear (CTLE), feed-forward (FFE) or decision-feedback (DFE) equalizers [1]. I/O systems can incur significant increases in mixed-signal circuitry power as the equalization complexity required for acceptable performance increases with channel loss.

CMOS technology scaling allows for the efficient implementation of powerful on-chip digital signal processing (DSP) algorithms for equalization and symbol detection. This motivates the use of Analog to digital converter (ADC)-based analog front ends in I/O receiver design [2], as shown in Fig. 1. Here, the incoming data is quantized, allowing the ISI cancellation to be implemented in the digital domain. This digital equalization offers robustness to PVT variations and is easier to re-configure than mixed-signal equalization circuitry. Moreover, an ADC-based receiver also allows for more spectrally-efficient modulation schemes such as duobinary or PAM4, and more complicated equalization methods such as sequence estimation. Despite these advantages, ADC-based receivers are generally more complex and consume higher power than binary receivers. Even with state of the art multi-GS/s ADC implementations [3], power is often prohibitive for many systems where link power efficiency is the key metric. The digital equalization that follows the ADC can also consume significant power, comparable to the power of the ADC [2].

This paper evaluates different equalization options for ADC-based receivers, including digital equalization only and embedding partial equalization in the ADC, with the aid of statistical BER simulation techniques. An overview of the embedded equalization strategies for ADC-based links is given in Section II. Section III presents statistical BER simulation results which show performance advantages with embedded equalization over an all-digital equalization implementation, quantified in terms of ADC resolution and DSP complexity. A new hybrid ADC receiver architecture which includes embedded equalization and selective digital equalization power-down based on threshold detection is proposed and analyzed in Section IV. Finally, Section V concludes the paper.

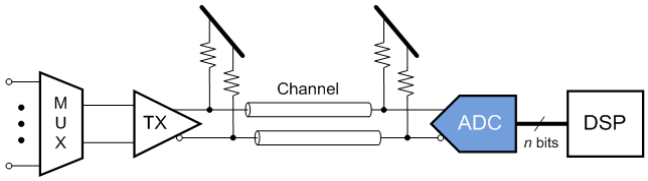

Fig. 1. High speed serial I/O link with ADC-based receiver.

II. EMBEDDED EQUALIZATION IN ADC-BASED LINKS

With embedded equalization, ISI subtraction is implemented before ADC quantization, as shown in Fig. 2 for two types of equalization: feed forward equalization (FFE) and decision feedback equalization (DFE). Unlike digital equalization, where the resolution is set by the ADC, embedded equalization applies the equalization taps to the un-quantized analog input.

Some recent examples of ADCs with embedded equalization include [4] and [5]. In [4], FIR/IIR equalization is embedded in the cap-DAC of a successive approximation register (SAR) ADC through selective sampling, at the cost of reduced ADC conversion rate. The implementation in [5] embeds one tap of equalization into a 4.8GS/s pipelined ADC. However, for the resolutions typically required in high-speed I/O systems, pipeline architectures are generally not the power optimal choice. Other recent ADC-based link systems suggest optimizing comparator thresholds to improve equalization performance [6], [7]. In [6], the authors propose a reduced slicer partial response DFE receiver, in which the thresholds of flash ADC comparators are optimized to minimize ISI. The authors note that it is preferable for their implementation to leave the FFE in the analog domain, since the DFE and FFE have contradicting requirements on the ADC quantization thresholds. With the hybrid architecture proposed in this paper, embedded equalization is combined with digital equalization to improve energy efficiency, without imposing any limitation over the digital FFE implementation. The authors in [7] suggest that by

This work was supported by SRC grant 1836.040

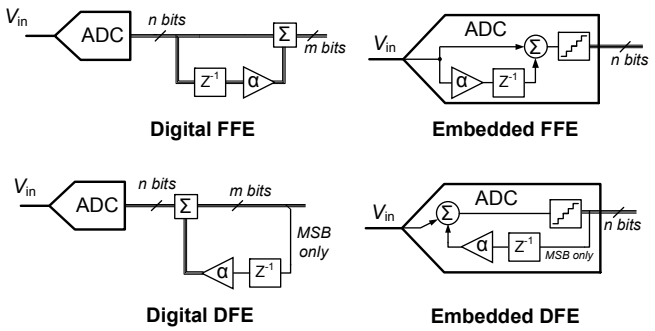

Fig.2. Block diagrams of embedded and digital equalization.

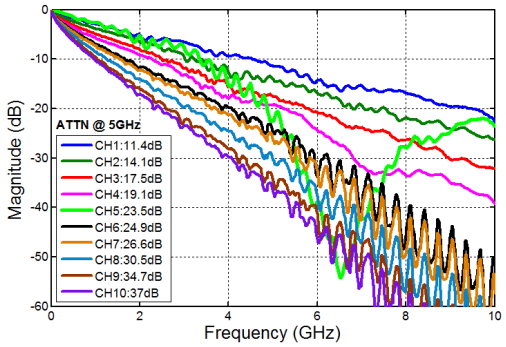

Fig. 3. Magnitude response for 10 backplane channels.

adapting the ADC full-scale range (FSR), savings in ADC complexity can be achieved. This technique is leveraged in the modeling results of the embedded equalization systems in the following section, where partial ISI cancellation before the ADC quantization reduces input amplitude and results in smaller ADC FSR.

III. Statistical Simulation of ADC-Based Receivers

In order to see the impact of embedded equalization on receiver performance, a statistical BER model is utilized which includes the effects of channel ISI, ADC and digital quantization noise, thermal noise, and receiver jitter. The presented results constrain DSP resolution to one bit higher than the ADC resolution and assume $1mV_{rms}$ receiver input thermal noise and receiver sampling jitter with a 0.02UI deterministic component (DJ) in the form of duty cycle distortion and a $0.02UI_{rms}$ random component (RJ). Ten backplane channels [8] are analyzed for 10Gbps operation, with loss ranging from 11 to 37dB at the 5GHz Nyquist frequency (Fig. 3).

Fig. 4 shows ADC resolution requirements to achieve a BER better than 10^{-12} for different conditions of digital equalization complexity, quantified in number of digital equalization taps. Note that these results, and the remainder of this paper's results, assume link equalization occurs only at the receiver, i.e. no transmit equalization. As channel loss increases, a larger amount of digital equalization taps and higher ADC resolution is required, with more than 2-taps of digital equalization necessary for channels with loss greater than 20dB. Channel 5, which displays a resonant null near 7GHz, requires higher ADC resolution and equalization relative to the other smooth loss channels with similar loss at the Nyquist frequency. In order to achieve the target BER with channel loss near 35dB, at least 8-bits of ADC resolution are required with 5-taps of equalization, while increasing to 7-taps allows for a savings of 1-2 ADC bits. This trade-off in ADC resolution and digital equalization complexity implies that the optimum receiver architecture from an energy efficiency perspective is a function of the relative power consumption of the ADC and digital equalization implementation.

In order to relax this system trade-off, partial equalization can be embedded inside the ADC and not be limited by the ADC resolution, as discussed in Section II. The following subsections discuss implementations of different embedded equalization architectures and their performance impact.

A. Embedded FFE

Embedded feed forward equalization (FFE) is first considered. In order to implement embedded FFE at the ADC front-end, a mechanism to delay, scale and sum analog signals is required. High-speed implementation of these functions in the analog domain can be complex, requiring active or passive analog delay lines and current mode adders which can consume considerable amounts of area and power [9]. An alternative mixed-signal approach is switched-capacitor equalization, which can be implemented efficiently as part of a capacitive DAC to perform signal addition and scaling [4]. A possible implementation of embedded FFE in a 4-bit SAR ADC is shown in Fig. 5, which improves upon [4] by leveraging time-interleaved front-end sampling to implement the FFE delay and avoids multiple sampling capacitors. To implement a 2-tap FFE with a main cursor and a post-cursor tap, during sampling a portion of the capacitor bank is applied to the post-cursor input sample and the remainder sample the cursor input. Charge sharing performs signal scaling and summation, followed by ADC conversion.

Fig. 6 shows the ADC resolution requirements including 2-taps of embedded FFE with a main cursor tap and a post-cursor tap. Note that while the tap coefficient resolution is limited by the ratio of the DAC unit capacitance to the total capacitance, and thus ADC resolution, applying the equalization to the un-quantized input signal allows for a reduced overall ADC resolution compared to the all-digital equalization requirements of Fig. 4. Including 2-taps of embedded FFE allows the null channel 5 to operate with only 2

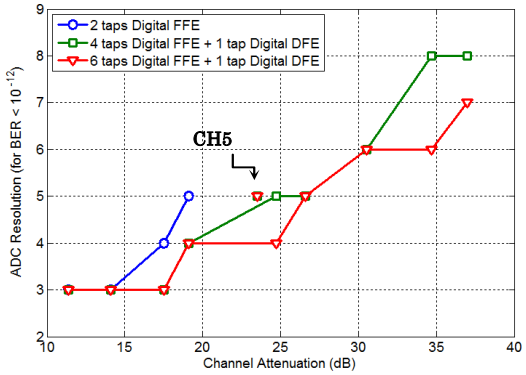

Fig. 4. ADC resolution requirements for ADC-based 10Gbps receiver with all-digital equalization.

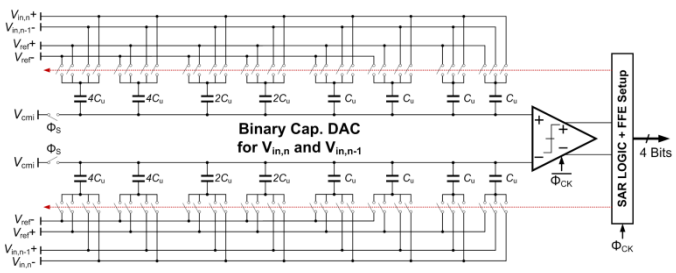

Fig. 5. 2-taps FFE embedded in the CAP DAC of a SAR ADC.

additional taps of digital FFE and a resolution savings of at least 2 bits for the four highest loss channels.

B. Embedded DFE

High speed binary receivers with DFE usually implement a loop-unrolling technique to overcome the critical 1 unit interval (UI) feedback path [10]. The straight forward implementation of a flash ADC with embedded 1-tap loop-unrolled DFE is shown in Fig. 7. Unlike FFE, embedding DFE inside the ADC requires only the "sign" of the past input (assuming PAM2 modulation), which corresponds to the MSB of the previous symbol. This MSB is fed back to decide the correct sign of ISI cancellation tap for the current symbol. One way to implement the DFE subtraction is by modifying the comparators threshold voltages. As with binary receivers, loop-unrolling results in almost a doubling of the hardware.

Another implementation of embedded 1-tap DFE using a SAR architecture as the front-end ADC is shown in Fig. 8. For a SAR ADC, each bit is resolved in a different clock cycle, which results in N+1 cycles for an N-bit ADC. Time interleaving of N+1 parallel converters is assumed to achieve the same conversion rate as the flash ADC. To implement DFE, loop-unrolling is only required in the first clock cycle, where the MSB is evaluated. Since other bits are evaluated in the following clock cycles, no unrolling is required. This implies that the unused comparator can be reset, minimizing the power overhead. Here, the DFE subtraction can either be implemented by modifying the comparators threshold voltages similar to the flash implementation or it can be realized by changing the reference voltages of the capacitive DAC.

Fig. 9 shows BER performance with 1-tap embedded DFE.

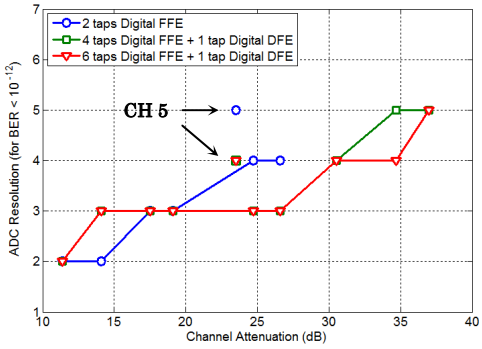

Fig. 6. ADC Resolution requirements for ADC-based 10Gbps receiver with 2-taps embedded FFE and differing digital equalization complexity.

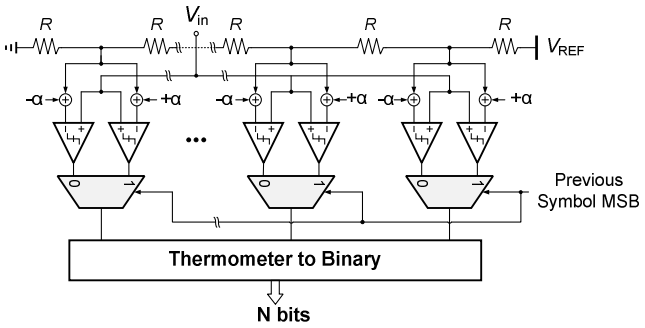

Fig. 7. Flash ADC with embedded loop-unrolled 1-tap DFE.

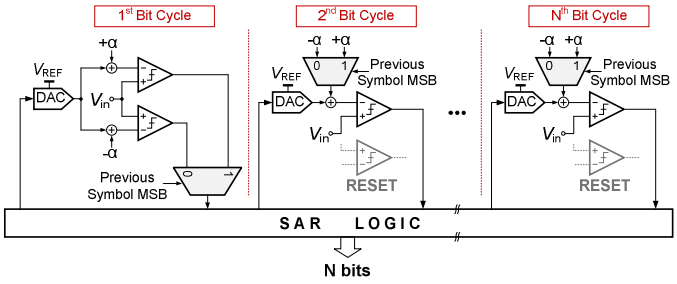

Fig. 8. SAR ADC with embedded loop-unrolled 1-tap DFE.

For low attenuation channels, where 1-tap DFE is enough to obtain an eye opening, the target 10^{-12} BER can be achieved. However, as any wrong DFE decision made due to residual ISI cannot easily be corrected by further digital equalization, receiver performance is limited by the BER at the ADC output. One method to improve overall BER is to merge the aforementioned 2-tap embedded FFE with the DFE tap, allowing for operation with near 30dB loss for the smooth channels. Another method to improve receiver BER, while still leveraging embedded DFE, involves distinguishing between reliable and unreliable DFE decisions and applying additional digital equalization. This approach is discussed in the next section with the proposed hybrid receiver architecture.

IV. Proposed Hybrid-ADC Receiver Architecture

While embedded DFE and 2-tap FFE provides improved BER performance, additional equalization is required to support channels with loss greater than 30dB. A technique that allows for additional post-DFE digital equalization is to use an erasure

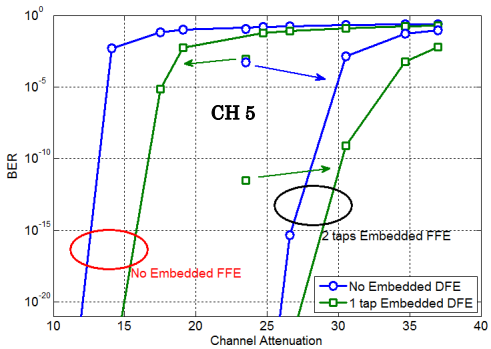

Fig. 9. Impact of 1-tap embedded DFE on BER performance of ADC-based receiver.

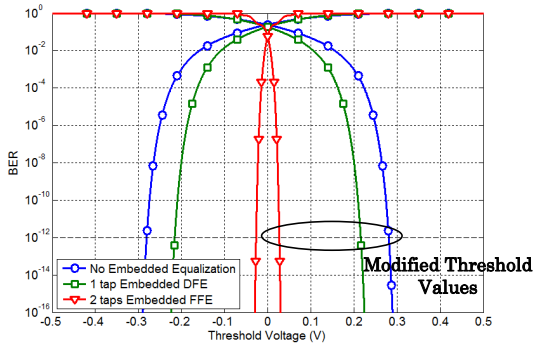

Fig. 10. Channel 9 BER versus receiver threshold under different equalization conditions and $1V_{ppd}$ input amplitude.

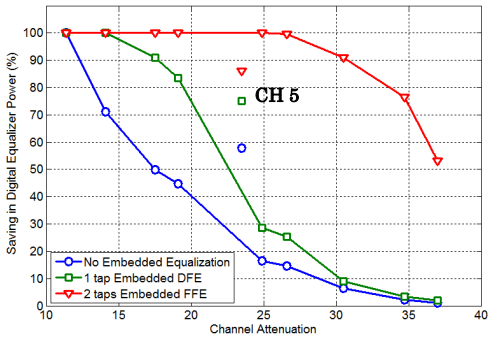

Fig. 12. Potential digital power savings with proposed hybrid-ADC receiver architecture.

scheme for erroneous DFE decisions [11]. In this scheme, a DFE decision is considered reliable only if the signal exceeds a certain differential threshold, which can also serve as an indication that further equalization is necessary on a sample-by-sample basis.

Fig. 10 illustrates for channel 9 that the BER at the normal zero threshold is very high, resulting in many unreliable DFE decisions. If the threshold is adjusted to a value corresponding to the target error rate, 280mV for channel 9 with no equalization, then the ADC MSB yields a reliable decision. For these reliable decisions, any additional digital equalization is not necessary and can be frozen, translating into potential power savings due to the reduced activity factor. Adding embedded 1-tap DFE or 2-tap FFE to the ADC reduces this threshold value to 220mV and 27mV, respectively, further improving digital equalization power efficiency.

The proposed hybrid ADC receiver architecture is shown in Fig. 11. Any samples which are below the necessary performance threshold level, as indicated by the threshold detector, are passed through the digital equalizer, while samples which exceed the threshold are treated as reliable decisions. For systems with embedded DFE, the effect of DFE subtraction is reversed in the digital domain in order to not limit the BER performance.

The performance of the proposed architecture in terms of potential power savings of digital equalization is shown in Fig. 12. The percentage of digital equalization power saving is given by the probability that the output exceeds the BER=10^{-12} threshold value, quantized to the minimum ADC resolution of Fig. 4 for the cases of no embedded ADC equalization and embedded DFE equalization and Fig. 6 for embedded FFE equalization. With embedded FFE equalization, saving of more than 50% of digital equalization power is possible for up to

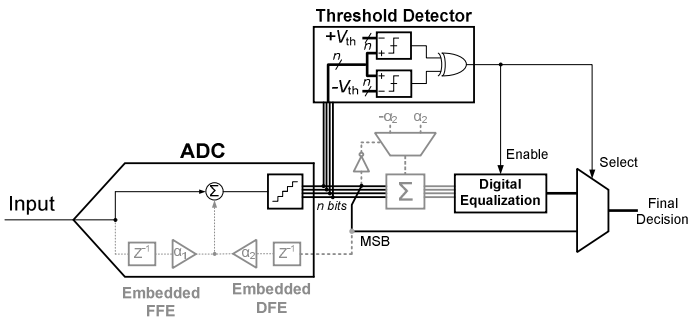

Fig. 11. Proposed hybrid ADC architecture with modified threshold

37dB of attenuation at Nyquist frequency.

V. Conclusion

In this paper, performance of ADC-based analog front-ends with embedded equalization was evaluated. It was shown that embedded FFE results in savings of ADC resolution and that embedded DFE can also provide improved BER performance. A new hybrid ADC receiver architecture is proposed which employs embedded equalization and a reliable decision threshold for enabling additional digital equalization. By enabling the digital equalizer only when necessary, this architecture is capable of achieving more than 50% of potential savings in digital equalization power.

References

[1] J.F. Bulzacchelli *et al.*, "A 10-Gb/s 5-tap DFE/4-tap FFE transceiver in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2885–2900, Dec. 2006.

[2] J. Cao *et al.*, "A 500 mW ADC-based CMOS AFE with digital calibration for 10 Gb/s serial links over KR- backplane and multimode fiber," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1172-1185, June 2010.

[3] P. Schvan *et al.*, "A 24GS/s 6b ADC in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 544-634, Feb. 2008.

[4] D.T. Lin, L. Li, S. Farahani, and M.P. Flynn, "A flexible 500MHz to 3.6GHz wireless receiver with configurable DT FIR and IIR filter embedded in A 7b 21MS/s SAR ADC," *IEEE Custom Integrated Circuits Conference,* pp.1-4, Sept. 2010.

[5] A. Varzaghani, and C.-K. K. Yang, "A 4.8 GS/s 5-bit ADC-based receiver with embedded DFE for signal equalization", *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 901, March 2009.

[6] J. Kim *et al.*, "Equalizer design and performance trade-offs in ADC-based serial links," *IEEE Custom Integrated Circuits Conference*, pp.1-8, Sept. 2010.

[7] E. Chen *et al.*, "Adaptation of CDR and full scale range of ADC-based SerDes receiver," *Symp. VLSI Circuits*, pp. 12-13, June 2009.

[8] IEEE P802.3ap task force - channel model material: http://www.ieee802.org/3/ap/public/channel_model/

[9] A. Momtaz and M. Green., "An 80 mW 40 Gb/s 7-tap T/2-spaced feed-forward equalizer in 65 nm CMOS *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 629-639, March 2010.

[10] S. Kasturia, and J.H Winters, "Techniques for high-speed implementation of nonlinear cancellation," *IEEE J. Selected Areas in Comm.*, vol. 9, no. 5, pp. 711-717, June 1991.

[11] M. Chiani, "Introducing erasure in decision feedback equalization to reduce error propagation," *IEEE Trans. Commun.*, vol. 45, no. 7, pp.757-760, Jan. 1998.