Samuel Palermo

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RESEARCH OVERVIEW

My research focuses on developing novel, energy-efficient, high-performance mixed-signal integrated circuit architectures in nanometer CMOS technologies. Specifically, my research interests cover the following areas: 1) High-speed electrical and optical chip-to-chip and on-chip interconnect architectures, 2) Radiation-hardened electronics, 3) RF and analog photonic systems, 4) Sensor circuits for emerging applications.

EDUCATION

Stanford University	Electrical Engineering	Ph.D. 2007
Texas A&M University	Electrical Engineering	M.S. 1999
Texas A&M University	Electrical Engineering	B.S. 1997

RESEARCH AND PROFESSIONAL EXPERIENCE

Texas A&M University, *College Station, TX* 2009 - present
Professor, Department of Electrical and Computer Engineering

Intel Corp., *Hillsboro, OR* 2006 - 2008
Senior Design Engineer, Advanced Circuits and Technology Integration Group

Stanford University, *Stanford, CA* 2000 - 2006
Research Assistant, Computer Systems Laboratory

Texas Instruments, Inc., *Dallas, TX* 1999 - 2000, Summer 2002
Design Engineer, High-Speed Serial Interfaces Group

Texas A&M University, *College Station, TX* 1997 - 1999
Research Assistant, Analog & Mixed-Signal Design Group

Motorola, Inc., Austin, *TX* Summer 1997
Design Intern, Microcontroller Design Group

Texas Instruments, Inc., *Dallas, TX* Summer 1995, Spring & Fall 1996
Design & Test Co-op, ASIC Design & Test Groups

TEACHING EXPERIENCE

Texas A&M University, Department of Electrical and Computer Engineering

Electronics (ECEN325) Taught 11 times, last in Spring 2020

In this course, students are introduced to electronic systems. Linear circuits, operational amplifiers, semiconductor-based electronic devices (diodes, bipolar junction and field effect transistors), and analog circuit design concepts are covered. The course includes a semester-long measurement and design lab and concludes with a final multi-stage amplifier design project.

Electronic Circuits (ECEN326) Taught 2 times, last in Fall 2017

This course covers the basic circuits used in analog electronic systems. Differential and multi-stage amplifiers, output stages and power amplifiers, frequency response, feedback circuits, stability, and analog integrated circuit basics are covered. The course includes a semester-long measurement and design lab.

(Analog) VLSI Circuit Design (ECEN474/704) Taught 5 times, last in Spring 2018

This course covers analog CMOS integrated circuit design. Basic transistor models, layout techniques, and analog design methodologies are covered. The course includes a semester-long CAD design lab with current IC design tools and concludes with a final transistor-level design project.

Network Theory (Broadband Circuit Design) (ECEN620) Taught 6 times, last in Fall 2020

This course covers broadband CMOS integrated circuit design. Phase-locked loops (PLLs), clock-and-data recovery (CDR) systems, broadband amplifiers, and high-speed logic are covered. A comprehensive final design project includes transistor-level design of a high-speed frequency synthesizer, CDR, or broadband amplifier in a nanometer CMOS technology.

Seminar (ECEN681) Taught 3 times, last in Fall 2016

This graduate seminar has weekly guest speakers on topics relevant to analog integrated circuits and systems.

Special Topics in Optical Interconnects Circuits & Systems (ECEN689) Taught 2 times, last in Spring 2020

This graduate course developed by Prof. Palermo covers high-speed optical interconnect (links) circuits and systems issues. Optical channel properties and modeling, link measurements and communications techniques, and drivers, receivers, equalizers, and synchronization circuits are covered. A comprehensive final design project includes systems analysis and circuit design of key link circuit blocks.

High-Speed Links Circuits and Systems (ECEN720) Taught 8 times, last in Spring 2019

This graduate course developed by Prof. Palermo covers high-speed serial and parallel wireline interfaces (links) circuits and systems issues. Electrical and optical channel properties and modeling, link measurements and communications techniques, and drivers, receivers, equalizers, and synchronization circuits are covered. A comprehensive final design project includes systems analysis with a statistical bit-error-rate simulator and circuit design of key link circuit blocks.

Electronics (ECEN325), Teaching Assistant Taught 2 times, last in Summer 1999

Electrical Circuit Theory (ECEN214), Teaching Assistant Taught once in Fall 1997

PUBLICATIONS

Peer-Reviewed Journal Articles

1. G. Zoppo**, A. Korkmaz*, F. Marrone**, **S. Palermo**, F. Corinto, and R. S. Williams, "Analog Solutions of Discrete Markov Chains via Memristor Crossbars," submitted to *IEEE Transactions on Circuits and Systems-I*.

2. A. Kumar*, Z. Huang, X. Zeng, B. Wang, D. Liang, W. Sorin, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "Design Considerations for Energy Efficient DWDM PAM4 Transceivers Employing Avalanche Photodiodes," *Laser & Photonics Reviews*, DOI: 10.1002/lpor.202000142, 2020.

** This indicates a student from another group within TAMU or other institution.
* This indicates a MS or PhD student in my group.

3. D. Liang, A. Roshan-Zamir*, Y.-H. Fan*, C. Zhang, B. Wang, A. Descos, W. Shen**, K. Yu, C. Li, G. Fan, G. Kurczveil, Y. Hu, Z. Huang, M. Fiorentino, S. Kumar, **S. Palermo,** and R. Beausoleil, "Fully-Integrated Heterogeneous DML Transmitters For High-Performance Computing," *IEEE-OSA Journal of Lightwave Technology*, vol. 38, no. 13, pp. 3322-3337, July 1, 2020.

4. Y.-H. Fan*, A. Kumar*, T. Iwai, A. Roshan-Zamir*, S. Cai*, B. Sun, and **S. Palermo**, "A 32 Gb/s Simultaneous Bidirectional Source-Synchronous Transceiver with Adaptive Echo Cancellation Techniques," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 2, pp. 439-451, Feb. 2020.

5. B. Wang, Q. Huang, K. Chen, J. Zhang, G. Kurczveil, D. Liang, **S. Palermo**, M. R. T. Tan, R. G. Beausoleil, and S. He, "Modulation on Silicon for Datacom: Past, Present, and Future (Invited Review)," *Progress In Electromagnetics Research*, Vol. 166, 119-145, 2019.

6. S. Kiran**, A. Shafik*, E. Zhian Tabasy*, S. Cai*, K. Lee*, S. Hoyos, and **S. Palermo**, "Modeling of ADC-Based Serial Link Receivers with Embedded and Digital Equalization," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 3, pp. 536-548, Mar. 2019.

7. A. Roshan-Zamir*, T. Iwai, Y.-H. Fan*, A. Kumar*, H.-W. Yang*, L. Sledeski, J. Hamilton, S. Chandramouli, A. Aude, and **S. Palermo**, "A 56 Gb/s PAM4 Receiver with Low-Overhead Threshold and Edge-Based DFE FIR- and IIR-Tap Adaptation Techniques," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 672-684, Mar. 2019.

8. S. Kiran**, S. Cai*, Y. Luo*, S. Hoyos, and **S. Palermo**, "A 52Gb/s ADC-Based PAM-4 Receiver with Comparator-Assisted 2bit/Stage SAR ADC and Partially-Unrolled DFE," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 659-671, Mar. 2019.

9. G. Choo**, C. Madsen, **S. Palermo**, and K. Entesari, "Automatic Monitor-Based Tuning of a Silicon Photonic 1X4 Asymmetric Binary Tree True-Time-Delay Beamforming Network," *IEEE-OSA Journal of Lightwave Technology*, vol. 36, no. 22, pp. 5263-5275, Nov. 15, 2018.

10. A. Tyagi*, T. Iwai, K. Yu*, B. Wang, W. Sorin, S. Mathai, M. Tan, and **S. Palermo**, "A 50 Gb/s PAM-4 VCSEL Transmitter with 2.5-Tap Nonlinear Equalization in 65nm CMOS," *IEEE Photonics Technology Letters*, vol. 30, no. 13, pp. 1246-1249, July 1, 2018.

11. G. Choo**, S. Cai*, B. Wang*, C. Madsen, K. Entesari, and **S. Palermo**, "Automatic Monitor-Based Tuning of Reconfigurable Silicon Photonic APF-Based Pole/Zero Filters," *IEEE-OSA Journal of Lightwave Technology*, vol. 36, no. 10, pp. 1899-1911, May 15, 2018.

12. C.-Y. Chen*, C. Li, M. Fiorentino, and **S. Palermo**, "A LIDAR Sensor Prototype with Embedded 14-bit 52ps Resolution ILO-TDC Array," *Analog Integrated Circuits and Signal Processing*, vol. 94, no. 3, pp. 369-382, Mar. 2018.

13. A. Roshan-Zamir*, O. Elhadidy*, H.-W. Yang*, and **S. Palermo**, "A Reconfigurable 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 9, pp. 2430-2447, Sept. 2017.

14. S. Cai*, Y. Zhu*, S. Kiran**, S. Hoyos, and **S. Palermo**, "Reference Switching Pre-Emphasis-Based SAR ADC with Enhanced DAC Settling," *IET Electronics Letters,* vol. 53, no. 20, pp. 1352-1354, Sept. 2017.

15. S. Cai*, E. Zhian Tabasy*, A. Shafik*, S. Hoyos, and **S. Palermo**, "A 25GS/s 6b TI Two-Stage Multi-Bit Search ADC with Soft-Decision Selection Algorithm in 65nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2168-2179, Aug. 2017.

16. C. Briseno-Vidrios**, A. Edward**, A. Shafik*, **S. Palermo**, and J. Silva-Martinez, "A 75 MHz Continuous-time Sigma-Delta Modulator Employing A Broadband Low-power Highly Efficient Common-gate Summing Stage," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 657-668, Mar. 2017.

17. B. Wang*, W. Sorin, **S. Palermo**, and M. Tan, "Comprehensive Vertical-Cavity Surface-Emitting Laser Model for Optical Interconnect Transceiver Circuit Design," *SPIE Optical Engineering*, vol. 55, no. 12, 126103, Dec. 2016.

18. K. Yu*, C. Li, H. Li**, A. Titriku*, A. Shafik*, B. Wang*, Z. Wang*, R. Bai**, C.-H. Chen, M. Fiorentino, P. Chiang, and **S. Palermo**, "A 25Gb/s Hybrid-Integrated Silicon Photonic Source-Synchronous Receiver with Microring Wavelength Stabilization," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2129-2141, Sept. 2016.

19. Z. Huang, C. Li, D. Liang, K. Yu*, C. Santori, M. Fiorentino, W. Sorin, **S. Palermo**, and R. Beausoleil, "25Gbps Low-Voltage Waveguide Si-Ge Avalanche Photodiode," *OSA Optica*, vol. 3, no. 8, pp. 793-798, Aug. 2016.
20. B. Wang*, C. Li, C.-H. Chen, K. Yu*, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "A Compact Verilog-A Model of Silicon Carrier-Injection Ring Modulators for Optical Interconnect Transceiver Circuit Design," *IEEE-OSA Journal of Lightwave Technology*, vol. 34, no. 12, pp. 2996-3005, June 15, 2016.
21. A. Shafik*, E. Zhian Tabasy*, S. Cai*, K. Lee, S. Hoyos, and **S. Palermo**, "A 10Gb/s Hybrid ADC-Based Receiver with Embedded Analog and Per-Symbol Dynamically-Enabled Digital Equalization," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 671-685, Mar. 2016.
22. B. Min*, N. H.-W. Yang*, and **S. Palermo**, "10Gb/s Adaptive Receive-Side Merged Near-End and Far-End Crosstalk Cancellation Circuitry in 65 nm CMOS," *Analog Integrated Circuits and Signal Processing*, DOI: 10.1007/s10470-016-0699-z, Feb. 2016.
23. H. Li**, Z. Xuan**, A. Titriku*, C. Li, K. Yu*, B. Wang*, A. Shafik*, N. Qi, Y. Liu, R. Ding, T. Baehr-Jones, M. Fiorentino, M. Hochberg, **S. Palermo**, and P. Chiang, "A 25 Gb/s, 4.4 V-Swing, AC-Coupled Ring Modulator-Based WDM Transmitter with Wavelength Stabilization in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3145-3159, Dec. 2015.
24. O. Elhadidy*, S. Shakib**, K. Krenek**, **S. Palermo**, and K. Entesari, "A Wide-Band Fully-Integrated CMOS Ring-Oscillator PLL-Based Complex Dielectric Spectroscopy System," *IEEE Transactions on Circuits and Systems-I*, vol. 62, no. 8, pp. 1940-1949, Aug. 2015.
25. Y.-H. Song*, H.-W. Yang*, H. Li**, P. Chiang, and **S. Palermo,** "An 8-16Gb/s, 0.65-1.05pJ/b, Voltage-Mode Transmitter with Analog Impedance Modulation Equalization and sub-3ns Power-State Transitioning," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2631-2643, Nov. 2014.
26. E. Zhian Tabasy*, A. Shafik*, K. Lee*, S. Hoyos, and **S. Palermo,** "A 6b 10GS/s TI-SAR ADC with Low-Overhead Embedded FFE/DFE Equalization for Wireline Receiver Applications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2560-2574, Nov. 2014.
27. C. Li*, R. Bai**, A. Shafik*, E. Zhian Tabasy*, B. Wang*, G. Tang*, C. Ma**, C.-H. Chen, P. Zhen, M. Fiorentino, R. Beausoleil, P. Chiang, and **S. Palermo,** "Silicon Photonic Transceiver Circuits with Microring Resonator Bias-Based Wavelength Stabilization in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 6, pp. 1419-1436, June 2014.
28. C. Li*, M. Browning**, P. Gratz, and **S. Palermo,** "LumiNOC: A Power-Efficient, High-Performance, Photonic Network-on-Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 6, pp. 826-838, June 2014.
29. E. Zhian Tabasy*, M. Kamarei, S. Ashtiani, and **S. Palermo,** "Sequential Correlated Level Shifting: A Switched-Capacitor Approach for High-Accuracy Systems," *IEEE Transactions on Circuits and Systems-II*, vol. 60, no. 12, pp. 857-861, Dec. 2013.
30. O. El-Hadidy*, M. Elkholy**, A. A. Helmy**, **S. Palermo**, and K. Entesari, "A CMOS Fractional-N PLL-Based Microwave Chemical Sensor with 1.5% Permittivity Accuracy," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 9, pp. 3402-3416, Sept. 2013.
31. E. Zhian Tabasy*, A. Shafik*, S. Huang*, N. Yang*, S. Hoyos, and **S. Palermo,** "A 6b 1.6GS/s ADC with Redundant Cycle 1-Tap Embedded DFE in 90nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 8, pp. 1885-1897, Aug. 2013.
32. A. Palaniappan* and **S. Palermo**, "A Design Methodology for Power Efficiency Optimization of High-Speed Equalized-Electrical I/O Architectures," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 21, no. 8, pp. 1421-1431, Aug. 2013.
33. Y. Song*, R. Bai**, K. Hu**, H.-W. Yang*, P. Chiang, and **S. Palermo,** "A 0.47-0.66pJ/bit, 4.8-8Gb/s I/O Transceiver in 65nm-CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1276-1289, May 2013.
34. C. Li* and **S. Palermo,** "A Low-Power 26-GHz Transformer-Based Regulated Cascode SiGe BiCMOS Transimpedance Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1264-1275, May 2013.

35. B. Min*, K. Lee*, and **S. Palermo,** "A 20Gb/s Triple-Mode (PAM-2, PAM-4, and Duobinary) Transmitter," *Microelectronics Journal*, vol. 43, no. 10, pp. 687-696, Oct. 2012.
36. X. Chen**, E. Sobhy**, Z. Yu**, S. Hoyos, J. Silva-Martinez, **S. Palermo**, and B. Sadler, "A Sub-Nyquist Rate Compressive Sensing Data Acquisition Front-End," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 3, pp. 542-551, Sept. 2012.
37. J. Zhou**, M. Ramirez**, **S. Palermo**, and S. Hoyos, "Digital-Assisted Asynchronous Compressive Sensing Front-End," *IEEE Journal of Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 3, pp. 482-492, Sept. 2012.
38. K. Hu**, R. Bai**, T. Jiang**, C. Ma**, A. Ragab*, **S. Palermo,** and P. Chiang, "0.16-0.25pJ/bit, 8Gb/s Near-Threshold Serial Link Receiver With Super-Harmonic Injection-Locking," *IEEE Journal of Solid-State Circuits*, vol. 47, no.8, pp. 1842-1853, Aug. 2012.
39. Y. Song* and **S. Palermo,** "A 6Gb/s Hybrid Voltage-Mode Transmitter with Current-Mode Equalization in 90nm CMOS," *IEEE Transactions on Circuits and Systems-II*, vol. 59, no. 8, pp. 491-495, Aug. 2012.
40. V. Sekar**, W. Torke*, **S. Palermo**, and K. Entesari, "A Self-Sustained Microwave System for Dielectric Constant Measurement of Lossy Organic Liquids," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 5, pp. 1444-1455, May 2012.
41. A. Ragab*, Y. Liu*, K. Hu**, P. Chiang, and **S. Palermo**, "Receiver Jitter Tracking Characteristics in High-Speed Source Synchronous Links," *Journal of Electrical and Computer Engineering*, vol. 2011, Article ID 982314, 2011.
42. S. Hoyos, S. Pentakota**, Z. Yu**, E. Sobhy**, X. Chen**, R. Saad**, **S. Palermo**, and J. Silva-Martinez, "Clock-Jitter Tolerant Wideband Receivers: An Optimized Multi-Channel Filter-Bank Approach," *IEEE Transactions on Circuits and Systems-I*, vol. 58, no. 2, pp. 253-263, Feb. 2011.
43. A. Palaniappan* and **S. Palermo**, "Power Efficiency Comparisons of Inter-chip Optical Interconnect Architectures," *IEEE Transactions on Circuits and Systems-II*, vol. 57, no. 5, pp. 343-347, May 2010.
44. I. Young, E. Mohammed, J. Liao, A. Kern, **S. Palermo,** B. Block, M. Reshotko, and P. Chang, "Optical I/O Technology for Tera-Scale Computing," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 235-248, Jan. 2010.
45. **S. Palermo**, A. Emami-Neyestanak, and M. Horowitz, "A 90nm CMOS 16Gb/s Transceiver for Optical Interconnects," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1235-1246, May 2008.
46. J. Roth, **S. Palermo**, N. Helman, D. Bour, D. Miller, and M. Horowitz, "An Optical Interconnect Transceiver at 1550nm using Low Voltage Electroabsorption Modulators Directly Integrated to CMOS," *IEEE-OSA Journal of Lightwave Technology*, vol. 25, no. 12, pp. 3739-3747, Dec. 2007.

Peer-Reviewed Conference Proceedings

1. Y.-H. Fan*, S. Srinivasan, Y. Hu, D. Liang, R. Liu*, A. Kumar*, E. Li, Z. Huang, R. Beausoleil, and **S. Palermo**, "A 22 Gb/s Directly Modulated Optical Injection-Locked Quantum-Dot Microring Laser Transmitter with Integrated CMOS Driver," *IEEE International Symposium on Circuits and Systems*, Oct. 2020.
2. Y. Zhu*, S. Cai*, S. Kiran**, Y.-H. Fan*, P.-H. Chang*, S. Hoyos, and **S. Palermo**, "A 1.5GS/s 8b Pipelined-SAR ADC with Output Level Shifting Settling Technique in 14nm CMOS," *IEEE Custom Integrated Circuits Conference*, Mar. 2020.
3. J. Gomez Diaz**, S. Kiran**, **S. Palermo**, and S. Hoyos, "Jitter-Robust Multicarrier ADC-Based Serial Link Receiver Architecture," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2019.
4. Y.-H. Fan*, A. Kumar*, T. Iwai, A. Roshan-Zamir*, S. Cai*, B. Sun, and **S. Palermo**, "A 32 Gb/s Simultaneous Bidirectional Source-Synchronous Transceiver with Adaptive Echo Cancellation in 28nm CMOS," *IEEE Custom Integrated Circuits Conference*, Apr. 2019.
5. Y.-H. Fan*, D. Liang, A. Roshan-Zamir, C. Zhang, B. Wang, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "A Directly Modulated Quantum Dot Microring Laser Transmitter with Integrated CMOS Driver," *OSA Optical Fiber Communication Conference*, Mar. 2019.

6. C. Li, K. Yu*, J. Rhim, K. Zhu, N. Qi, M. Fiorentino, T. Pinguet, M. Peterson, V. Saxena, and **S. Palermo**, "A 3D-Integrated 56 Gb/s NRZ/PAM4 Reconfigurable Segmented Mach-Zehnder Modulator-Based Si-Photonics Transmitter," *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium*, Oct. 2018.
7. S. Kiran**, S. Cai*, S. Hoyos, and **S. Palermo**, "Statistical Modeling of Non-Linearity in Decision Feedback Equalizer-Based Mixed-Signal Receivers," *IEEE Conference on Electrical Performance of Electronic Packaging and Systems*, Oct. 2018.
8. G. Choo**, C. Madsen, **S. Palermo**, and K. Entesari, "Automatic Monitor-Based Tuning of RF Silicon Photonic True-Time-Delay Beamforming Networks," *IEEE International Microwave Symposium*, June 2018.
9. A. Roshan-Zamir*, T. Iwai, Y.-H. Fan*, A. Kumar*, H.-W. Yang*, L. Sledjeski, J. Hamilton, S. Chandramouli, A. Aude, and **S. Palermo**, "A 56 Gb/s PAM4 Receiver with Low-Overhead Threshold and Edge-Based DFE FIR and IIR-Tap Adaptation in 65nm CMOS," *IEEE Custom Integrated Circuits Conference*, Apr. 2018.
10. S. Kiran**, S. Cai*, Y. Luo*, S. Hoyos, and **S. Palermo**, "A 32 Gb/s ADC-Based PAM-4 Receiver with 2-bit/Stage SAR ADC and Partially-Unrolled DFE," *IEEE Custom Integrated Circuits Conference*, Apr. 2018. **[Outstanding Student Paper Award**].
11. A. Roshan-Zamir*, K. Yu*, D. Liang, C. Zhang, C. Li, G. Fan*, B. Wang, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "A 14 Gb/s Directly Modulated Hybrid Microring Laser Transmitter," *OSA Optical Fiber Communication Conference*, Mar. 2018.
12. D. Liang, C. Zhang, A. Roshan-Zamir*, K. Yu*, C. Li, G. Kurczveil, Y. Hu, W. Shen, M. Fiorentino, S. Kumar, **S. Palermo**, and R. Beausoleil, "A Fully-integrated Multi-λ Hybrid DML Transmitter," *OSA Optical Fiber Communication Conference,* Mar. 2018.
13. H.-W. Yang*, A. Roshan-Zamir*, Y.-H. Song, and **S. Palermo**, "A Low-Power Dual-Mode 20-Gb/s NRZ and 28-Gb/s PAM-4 Voltage-Mode Transmitter," *IEEE Asian Solid State Circuits Conference*, Nov. 2017.
14. G. Choo**, C. Madsen, K. Entesari, and **S. Palermo**, "A Reconfigurable Silicon Photonic 4th-order Filter for Synthesizing Butterworth, Chebyshev, and Elliptic Responses," *IEEE Avionics and Vehicle Fiber-Optics and Photonic Conference*, Nov. 2017.
15. J. Rhim, K. Yu*, P.-H. Chang*, **S. Palermo**, C. Li, M. Fiorentino, R. Beausoleil, and M.-J. Lee, "Guard-Ring Dependence of Noise Characteristics for Single-Photon Avalanche Diodes in a Standard CMOS Technology," *IEEE International Conference on Group IV Photonics*, Aug. 2017.
16. A. Roshan-Zamir*, B. Wang*, K. Yu*, S. Telaprolu*, C. Li, M. A. Seyedi, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "A 40Gb/s PAM4 Optical DAC Silicon Microring Resonator Modulator Transmitter," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2017.
17. A. Roshan-Zamir*, B. Wang*, S. Telaprolu*, K. Yu*, C. Li, M. A. Seyedi, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "A Two-Segment Optical DAC 40 Gb/s PAM4 Silicon Microring Resonator Modulator Transmitter in 65nm CMOS," *IEEE Optical Interconnects Conference*, June 2017.
18. G. Choo**, S. Cai*, B. Wang*, C. Madsen, K. Entesari, and **S. Palermo**, "Automatic Monitor-Based Tuning of Reconfigurable Silicon Photonic 2nd-Order APF-Based Pole/Zero Filters," *OSA Conference on Lasers and Electro-Optics*, May 2017.
19. J. Okyere*, K. Yu*, K. Entesari, and **S. Palermo**, "A Fifth-Order Polynomial Predistortion Circuit for Mach-Zehnder Modulator Linearization in 65nm CMOS," *IEEE Texas Symposium on Wireless and Microwave Circuits and Systems*, Mar. 2017.
20. **S. Palermo**, K. Yu*, A. Roshan-Zamir*, B. Wang*, C. Li, M. Ashkan Seyedi, M. Fiorentino, and R. Beausoleil, "PAM4 Silicon Photonic Microring Resonator-Based Transceiver Circuits," *SPIE Photonics West*, Jan. 2017.
21. A. Roshan-Zamir*, O. Elhadidy*, H.-W. Yang*, and **S. Palermo**, "A 16/32 Gb/s Dual-Mode NRZ/PAM4 SerDes in 65nm CMOS," *IEEE Compound Semiconductor IC Symposium*, Oct. 2016.
22. C.-Y. Chen*, C. Li, M. Fiorentino, and **S. Palermo**, "A 52 ps Resolution ILO-Based Time-to-Digital Converter Array for LIDAR Sensors," *IEEE Dallas Circuits and Systems Conference*, Oct. 2016. [**Best Student Paper Award**].

23. S. Cai*, E. Zhian Tabasy*, A. Shafik*, S. Kiran*, S. Hoyos, and **S. Palermo**, "A 25GS/s 6b TI Binary Search ADC with Soft-Decision Selection in 65nm CMOS," *SRC Techcon*, Sept. 2016.
24. Z. Huang, C. Li, D. Liang, K. Yu*, C. Santori, M. Fiorentino, W. Sorin, **S. Palermo**, and R. Beausoleil, "A 25Gbps Low-Voltage Waveguide Si-Ge Avalanche Photodiode," *OSA Conference on Lasers and Electro-Optics*, June 2016.
25. A. Roshan-Zamir*, B. Wang*, S. Telaprolu*, K. Yu*, C. Li, M. A. Seyedi, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "A 40 Gb/s PAM4 Silicon Microring Resonator Modulator Transmitter in 65nm CMOS," *IEEE Optical Interconnects Conference*, May 2016.
26. S. Cai*, G. Choo**, B. Wang*, K. Entesari, and **S. Palermo**, "Comprehensive Adaptive Tuning of Silicon RF Photonic Filters," *IEEE Texas Symposium on Wireless and Microwave Circuits and Systems*, Mar. 2016.
27. **S. Palermo**, P. Chiang, K. Yu*, R. Bai**, C. Li, C.-H. Chen, M. Fiorentino, R. Beausoleil, H. Li**, A. Shafik*, and A. Titriku*, "Adaptive Gain, Equalization, and Wavelength Stabilization Techniques for Silicon Photonic Microring Resonator-Based Optical Receivers," *SPIE Photonics West*, Feb. 2016.
28. **S. Palermo**, P. Chiang, C. Li, C.-H. Chen, M. Fiorentino, R. Beausoleil, H. Li**, K. Yu*, B. Wang*, R. Bai**, A. Shafik*, and A. Titriku*, "Silicon Photonic Microring Resonator-Based Transceivers for Compact WDM Optical Interconnects," *IEEE Compound Semiconductor Integrated Circuit Symposium*, Oct. 2015.
29. A. Shafik*, E. Zhian Tabasy*, S. Cai*, K. Lee, S. Hoyos, and **S. Palermo**, "A 10Gb/s Hybrid ADC-Based Receiver with Embedded 3-Tap Analog FFE and Dynamically-Enabled Digital Equalization in 65nm CMOS," *SRC Techcon*, Sept. 2015. [**Best in Session Award**].
30. K. Yu*, C. Li, T.-C. Huang, A. Seyedi, D. Zhou, C. Wilson, D. Berkram, **S. Palermo**, J. Smela, M. Fiorentino, and R. Beausoleil, "56 Gb/s PAM-4 Optical Receiver Frontend in an Advanced FinFET Process," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2015.
31. S. Cai*, G. Choo*, E. Zhian Tabasy, B. Wang*, K. Entesari, and **S. Palermo**, "Adaptively-Tunable RF Photonic Filters," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2015.
32. B. Wang*, K. Yu*, H. Li**, P. Chiang, and **S. Palermo**, "Energy Efficiency Comparisons of NRZ and PAM4 Modulation for Ring-Resonator-Based Silicon Photonic Links," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2015.
33. T.-C. Huang, C. Li, R. Wu, C.-H. Chen, M. Fiorentino, K.-T. Cheng, **S. Palermo,** and R. Beausoleil, "DWDM Nanophotonic Interconnects: Toward Terabit/s Chip-Scale Serial Link," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2015.
34. S. Song, J. Xu, F. Cai, X. Ma, Z. Yang, M. Becker, B. Kim, L. Tate, **S. Palermo**, and B. Bowhill, "An Input Pole Tuned Switching Equalization Scheme for High-speed Serial Links," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2015.
35. S. Cai*, E. Zhian Tabasy*, A. Shafik*, S. Kiran**, S. Hoyos, and **S. Palermo**, "A 25GS/s 6b TI Binary Search ADC with Soft-Decision Selection in 65nm CMOS," *IEEE Symposium on VLSI Circuits*, June 2015.
36. O. Elhadidy*, A. Roshan-Zamir*, H.-W. Yang*, and **S. Palermo**, "A 32 Gb/s 0.55 mW/Gbps PAM4 1-FIR 2-IIR Tap DFE Receiver in 65-nm CMOS," *IEEE Symposium on VLSI Circuits*, June 2015.
37. C. Briseno-Vidrios**, A. Edward**, A. Shafik*, **S. Palermo**, and J. Silva-Martinez, "A 75 MHz 68dB DR CT-ΣΔ Modulator with MFB SAB and Low Power TIA Summing Node," *IEEE Symposium on VLSI Circuits*, June 2015.
38. B. Wang*, C. Li, C.-H. Chen, K. Yu*, M. Fiorentino, R. Beausoleil, and **S. Palermo**, "Compact Verilog-A Modeling of Silicon Carrier-Injection Ring Modulators," *IEEE Optical Interconnects Conference*, Apr. 2015.
39. C.-H. Chen, C. Li, R. Bai, K. Yu*, J.-M. Fedeli, S. Meassoudene, M. Fournier, S. Menezo, P. Chiang, **S. Palermo**, M. Fiorentino, and R. Beausoleil, "DWDM Silicon Photonic Transceivers for Optical Interconnect," *IEEE Optical Interconnects Conference*, Apr. 2015.
40. K. Yu*, C.-H. Chen, C. Li, H. Li**, A. Titriku*, B, Wang*, A. Shafik*, Z. Wang**, M. Fiorentino, P. Chiang, and **S. Palermo**, "25Gb/s Hybrid-Integrated Silicon Photonic Receiver with Microring Wavelength Stabilization," *OSA Optical Fiber Communication Conference*, Mar. 2015.

41. A. Shafik*, E. Zhian Tabasy*, S. Cai*, K. Lee, S. Hoyos, and **S. Palermo**, "A 10Gb/s Hybrid ADC-Based Receiver with Embedded 3-Tap Analog FFE and Dynamically-Enabled Digital Equalization in 65nm CMOS," *IEEE International Solid-State Circuits Conference*, Feb. 2015. [**Premier Integrated Circuits Conference, 35% Acceptance Rate**].
42. K. Yu*, H. Li**, C. Li, A. Titriku*, B, Wang*, A. Shafik*, Z. Wang**, R. Bai**, C.-H. Chen, M. Fiorentino, P. Chiang, and **S. Palermo**, "A 24Gb/s, 0.71pJ/b, Si-Photonic Source-Synchronous Receiver with Adaptive Equalization and Microring Wavelength Stabilization," *International Solid-State Circuits Conference*, Feb. 2015. [**Premier Integrated Circuits Conference, 35% Acceptance Rate**].
43. H. Li**, Z. Zuan**, A. Titriku*, K. Yu*, B, Wang*, N. Qi**, A. Shafik*, C. Li, M. Fiorentino, M. Hochberg, **S. Palermo**, and P. Chiang, "A 25Gb/s 4.4V Swing AC-Coupled Si-Photonic Microring Transmitter with 2-Tap Asymmetric FFE and Dynamic Thermal Tuning in 65nm CMOS," *International Solid-State Circuits Conference*, Feb. 2015. [**Premier Integrated Circuits Conference, 35% Acceptance Rate**].
44. S. Kiran**, S. Hoyos, and **S. Palermo**, "A Single Parity Check Forward Error Correction Method for High Speed I/O," *IEEE Global Conference on Signal and Information Processing*, Dec. 2014.
45. S. Cai*, A. Shafik*, S. Kiran**, E. Zhian Tabasy*, S. Hoyos, and **S. Palermo**, "Statistical Modeling of Metastability in ADC-Based Serial I/O Receivers," *IEEE Conference on Electrical Performance of Electronic Packaging and Systems*, Oct. 2014.
46. R. Jay* and **S. Palermo**, "Resonant Coupling Analysis for a Two-Coil Wireless Power Transfer System," *IEEE Dallas Circuits and Systems Conference*, Oct. 2014.
47. O. Elhadidy*, S. Shakib*, K. Krenek*, **S. Palermo**, and K. Entesari, "A 0.18-μm CMOS Fully Integrated 0.7-6 GHz PLL-Based Complex Dielectric Spectroscopy System," *IEEE Custom Integrated Circuits Conference*, Sept. 2014.
48. O. Elhadidy* and **S. Palermo**, "A 10 Gb/s 2-IIR-Tap DFE Receiver with 35 dB Loss Compensation in 65-nm CMOS," *SRC Techcon*, Sept. 2014.
49. B. Min*, N. H.-W. Yang*, and **S. Palermo**, "10Gb/s Adaptive Receive-Side Near-End and Far-End Crosstalk Cancellation Circuitry," *IEEE International Midwest Symposium on Circuits and Systems*, August 2014. [**Best Student Paper Award**].
50. N. Narku-Tetteh*, A. Titriku*, and **S. Palermo**, "A 15b, Sub-10ps Resolution, Low Dead Time, Wide Range Two-Stage TDC," *IEEE International Midwest Symposium on Circuits and Systems*, Aug. 2014.
51. H. Li**, S. Chen**, L. Yang**, R. Bai**, W. Hu, F. Zhong, **S. Palermo**, and P. Chiang, "A 0.8V, 560fJ/bit, 14Gb/s Injection-Locked Receiver with Input DCD Tolerable Edge-Rotating 5/4X Sub-Rate CDR in 65nm CMOS," *IEEE Symposium on VLSI Circuits*, June 2014.
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54. J. Zhou**, **S. Palermo**, J. Silva-Martinez, and S. Hoyos, "Asynchronous Compressive Radar," *Government Microcircuit Applications & Critical Technology Conference*, Apr. 2014.
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77. I. Young, E. Mohammed, J. Liao, A. Kern, **S. Palermo,** B. Block, M. Reshotko, and P. Chang, "Optical I/O Technology for Tera-Scale Computing," *IEEE International Solid-State Circuits Conference*, Feb. 2009. [**Premier Integrated Circuits Conference, 35% Acceptance Rate, Outstanding Technology Directions Paper Award**].
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79. **S. Palermo**, A. Emami-Neyestanak, and M. Horowitz, "A 90nm CMOS 16Gb/s Transceiver for Optical Interconnects," *IEEE International Solid-State Circuits Conference*, Feb. 2007. [**Premier Integrated Circuits Conference, 35% Acceptance Rate**].
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81. **S. Palermo** and M. Horowitz, "High-Speed Transmitters in 90nm CMOS for High-Density Optical Interconnects," *IEEE European Solid-State Circuits Conference*, Sep. 2006.
82. D. Miller, A. Bhatnagar, **S. Palermo**, A. Emami-Neyestanak, and M. Horowitz, "Opportunities for Optics in Integrated Circuits Applications," *IEEE International Solid-State Circuits Conference*, Feb. 2005. [**Premier Integrated Circuits Conference, 35% Acceptance Rate**].
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85. **S. Palermo** and J. Pineda de Gyvez, "A Multi-Band Single-Loop PLL Frequency Synthesizer with Dynamically-Controlled Switched Tuning VCO", *IEEE Midwest Symposium on Circuits and Systems*, Aug. 2000.
86. B. Provost, **S. Palermo**, E. Sánchez-Sinencio, and S.H.K. Embabi, "Built-In Self Test for Pipeline ADCs", *IEEE International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, July 1998.

Magazine Articles

1. K. Entesari, S. Palermo, C. Madsen, G. Choo**, S. Cai*, and B. Wang*, "Programmable Microwave Silicon Photonics Filters and Beamformers," accepted in *IEEE Microwave Magazine*. **[Peer Reviewed]**
2. S. Kiran**, S. Cai*, Y. Zhu*, S. Hoyos, and **S. Palermo**, "Digital Equalization with ADC-Based Receivers" *IEEE Microwave Magazine,* vol. 20, no. 5, pp. 62-79, May 2019. **[Peer Reviewed]**
3. **S. Palermo**, S. Hoyos, S. Cai*, S. Kiran*, and Y. Zhu*, "Analog-to-Digital Converter-Based Serial Links: An Overview," *IEEE Solid-State Circuits Magazine,* vol. 10, no. 3, pp. 35-47, Summer 2018.
4. **S. Palermo**, S. Hoyos, A. Shafik*, E. Zhian Tabasy*, S. Cai*, S. Kiran*, and K. Lee*, "CMOS ADC-Based Receivers for High-Speed Electrical and Optical Links," *IEEE Communications Magazine,* vol. 54, no. 10, pp. 168-175, Oct. 2016. **[Peer Reviewed]**
5. C. Li, C.-H. Chen, B. Wang*, **S. Palermo**, M. Fiorentino, and R. Beausoleil**,** "Design of an Energy-Efficient Silicon Microring Resonator-Based Photonic Transmitter," *IEEE Design and Test*, vol. 31, no. 5, pp. 46-54, Oct. 2014. **[Peer Reviewed]**
6. I. Young, E. Mohammed, J. Liao, A. Kern, **S. Palermo,** B. Block, M. Reshotko, and P. Chang, "Optical Technology for Energy Efficient I/O in High Performance Computing," *IEEE Communications Magazine*, vol. 48, no. 10, pp. 184-191, Oct. 2010. **[Peer Reviewed]**

Book Chapters

1. **S. Palermo**, "Encyclopedia of Modern Optics (Second Edition)," Chapter: CMOS Transceiver Circuits for Optical Interconnects, vol. 4, pp. 254-263, Elsevier, 2018.
2. C. Li, P. Gratz, and **S. Palermo**, "More than Moore Technologies for Next Generation Computer Design," Chapter 7: Nano-Photonic Networks-on-Chip for Future Chip Multiprocessors, Springer, 2015.

3. R. Saad**, S. Hoyos, and **S. Palermo**, "MATLAB - A Fundamental Tool for Scientific Computing and Engineering Applications - Volume 1," Chapter 17: Analysis and Modeling of Clock-Jitter Effects in Delta-Sigma Modulators, Intech, 2012.
4. **S. Palermo**, "CMOS Nanoelectronics Analog and RF VLSI Circuits," Chapter 9: High-Speed Serial I/O Design for Channel-Limited and Power-Constrained Systems, McGraw-Hill, 2011.

Patents

1. "High speed voltage mode differential digital output driver with edge-emphasis and pre-equalization," R. Payne, C. Chan, **S. Palermo**, U.S. Patent #6,624,670, Issued September 23, 2003.

Theses

1. Y.-H. Fan*, "Design Techniques for High Pin Efficiency Wireline Transceivers," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2020.
2. H.-W. Yang*, "Design of Low-Power NRZ/PAM-4 Wireline Transmitters," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2018.
3. A. Kumar*, "Clocking and Skew-Optimization for Source Synchronous Simultaneous Bidirectional Links," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2018.
4. S. Cai*, "Design of High-Speed Power-Efficient A/D Converters for Wireline ADC-Based Receiver Applications," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2018.
5. A. Roshan Zamir*, "High Speed Reconfigurable NRZ/PAM4 Transceiver Design Techniques," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2018.
6. K. Yu*, "Integrated Circuit Design for Silicon Photonic Interconnects," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2018.
7. A. Tyagi*, "A PAM-4 VCSEL Transmitter with 2.5 Tap Non-Linear Equalizer in 65nm CMOS," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2017.
8. R. Gupta*, "Wide Dynamic Range Image Sensor Prototype Based on Digital Readout Integrated Circuit," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2017.
9. B. Min*, "Design Techniques for High Performance Serial Link Transceivers," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2017.
10. J. Okyere*, "Fifth-Order Polynomial Predistortion for Mach-Zehnder Modulator Linearization," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, May 2017.
11. C.-Y. Chen*, "A Sub-Centimeter Ranging Precision LIDAR Sensor Prototype Based on ILO-TDC," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, Aug. 2016.
12. A. Shafik*, "Equalization Architectures for High Speed ADC-Based Serial I/O Receivers," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2016.
13. B. Wang*, "Modeling of Photonic Devices and Photonic Integrated Circuits for Optical Interconnect and RF Photonic Front-End Applications," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2016.
14. R. Jay*, "Wirelessly-Powered CMOS Front End for Locomotive IC Applications," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, May 2016.
15. O. Elhadidy*, "Design of Integrated Microwave Frequency Synthesizer-Based Dielectric Sensor Systems," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, Aug. 2015.
16. E. Zhian Tabasy*, "Design of Energy-Efficient A/D Converters with Partial Embedded Equalization for High-Speed Wireline Receiver Applications," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2015.
17. A. Titriku*, "Efficient Wavelength Tuning Techniques for Integrated Silicon Photonics," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2014.

18. Y.-H. Song*, "Design Techniques for Energy Efficient Multi-Gb/s Serial I/O Transceivers," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, May 2014.
19. C. Li*, "Design of Optical Interconnect Transceiver Circuits and Network-on-Chip Architectures for Inter- and Intra-Chip Communication," *Ph.D. Dissertation*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2013.
20. N. Narku-Tetteh*, "A Sub-10ps Time-to-Digital Converter with 204ns Dynamic Range for Time-Resolved Imaging and Ranging Applications," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, May 2014.
21. H. Huang*, "Impedance Spectroscopy Front-End Suitable for Biomedical Cell Impedance Measurement," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, May 2013.
22. K. Lee*, "High-Speed Link Modeling: Analog/Digital Equalization and Modulation Techniques," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, May 2012.
23. W. Torke*, "A PLL-Based Frequency Shift Measurement System for Chemical and Biological Sensing," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2011.
24. Y. Liu*, "Jitter Tracking Bandwidth Optimization Using Active-Inductor-Based Bandpass Filtering in high-Speed Forwarded Clock Transceivers," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, May 2011.
25. A. Palaniappan*, "Modeling, Optimization and Power Efficiency Comparison of High-Speed Inter-Chip Electrical and Optical Interconnect Architectures in Nanometer CMOS Technologies," *M.S. Thesis*, Texas A&M University, Department of Electrical and Computer Engineering, Dec. 2010.
26. **S. Palermo**, "Design of High-Speed Optical Interconnect Transceivers," *Ph.D. Dissertation*, Stanford University, Department of Electrical Engineering, Sep. 2007.
27. **S. Palermo**, "A Multi-Band Phase-Locked Loop Frequency Synthesizer," *M.S. Thesis*, Texas A&M University, Department of Electrical Engineering, Aug. 1999.

HONORS AND AWARDS

IEEE Custom Integrated Circuits Conference Outstanding Student Paper Award, 2018

IEEE Dallas Circuits and Systems Conference Best Student Paper Award, 2016

Semiconductor Research Corporation TECHCON Best in Session Award, 2015

Texas A&M University Engineering Faculty Fellow Award, 2015

Texas A&M University Department of Electrical and Computer Engineering Outstanding Professor Award, 2014

IEEE International Midwest Symposium on Circuits and Systems Best Student Paper Award, 2014

Semiconductor Research Corporation TECHCON Best in Session Award, 2013

IEEE Transactions on Circuits and Systems II Best Associate Editors Award, 2012-2013

International Solid-State Circuits Conference Outstanding Technology Directions Paper Award, 2009

NSF Graduate Research Fellowship, 1999

INVITED TALKS AND SEMINARS

1. 2020 Intel SERDES and I/O Summit – Intel – Online – Fall 2020
2. High-Speed Interface Group - Marvell – Online – Fall 2020
3. PhotonIcs & Electromagnetics Research Symposium Invited Talk – Xiamen, China – Fall 2019
4. 2019 Intel SERDES and I/O Summit - Intel – San Jose, CA – Fall 2019

5. High-Speed Interface Group - Marvell – Santa Clara, CA – Fall 2019
6. High-Speed Interface Group - NXP Semiconductors – Eindhoven, The Netherlands – Fall 2019
7. IEEE Photonics Society Summer Topicals Meeting Series Invited Talk – Fort Lauderdale, FL – Summer 2019
8. International Symposium on Ultrafast Photonic Technologies Invited Talk – Napa, CA – Summer 2019
9. IEEE SSCS Webinar – Fall 2018
10. IEEE IMS Digital Pre-Distortion and Post-Correction from DC to mm-Wave for Wireline and Optical Communications Workshop – Philadelphia, PA – Summer 2018
11. North American Workshop on Silicon Photonics for High Performance Computing – CSU – Fort Collins, CO – Spring 2018
12. Electrical and Computer Engineering Seminar – EPFL – Lausanne, Switzerland – Spring 2018
13. High-Speed Interface Group - Qualcomm – San Diego, CA – Spring 2018
14. IEEE ISSCC Conference Tutorial – San Francisco, CA – Spring 2018
15. 2017 Intel SERDES and I/O Summit - Intel – San Jose, CA – Fall 2017
16. Electrical and Computer Engineering Seminar – USC – Los Angeles, CA – Fall 2017
17. IEEE ISOCC Conference Invited Talk – Seoul, South Korea – Fall 2017
18. IEEE EPEPS Conference Tutorial – San Jose, CA – Fall 2017
19. IEEE SSCS Distinguished Lecture – HKUST – Clear Water Bay, Hong Kong – Summer 2017
20. IC Café Lecture – Shanghai, China – Summer 2017
21. IC Café Lecture – Nanjing, China – Summer 2017
22. IEEE SSCS Distinguished Lecture – Columbia University – New York, NY – Fall 2016
23. IEEE SSCS Distinguished Lecture – Princeton University – Princeton, NJ – Fall 2016
24. IEEE SSCS Distinguished Lecture – Lehigh University – Bethlehem, PA – Fall 2016
25. IEEE SSCS Distinguished Lecture – Brigham Young University – Provo, UT – Fall 2016
26. ECEN Electrical Engineering Department Seminar - Texas A&M University - College Station, TX – Fall 2016
27. Analog and Mixed-Signal Design Group – Cirrus Logic – Austin, TX - Summer 2016
28. IEEE SSCS Distinguished Lecture – UT-Austin – Austin, TX – Spring 2016
29. SRC-GRC Technology Transfer e-Workshop – University of Texas, Dallas – Dallas, TX - Spring 2016
30. IEEE SSCS Toronto Seminar - Toronto, Canada - Spring 2016
31. ECEN Computer Engineering Seminar - Texas A&M University - College Station, TX – Spring 2016
32. PHYS Institute for Quantum Science & Eng. Seminar - Texas A&M University - College Station, TX – Fall 2015
33. High-Speed Interface Group - Maxlinear - Carlsbad, CA - Summer 2015
34. High-Speed Interface Group - Broadcom Corp. - Irvine, CA - Spring 2015
35. High-Speed Interface Group – Altera Corp. – San Jose, CA - Spring 2015
36. ECEN Biomedical Engineering Seminar - Texas A&M University - College Station, TX – Spring 2015
37. High-Speed Interface Group – Qualcomm Technologies, Inc. – San Diego, CA - Summer 2014
38. Electrical and Computer Engineering Seminar – UC-San Diego – La Jolla, CA – Summer 2014
39. High-Speed Interface Group – Cisco Systems, Inc. – San Jose, CA - Spring 2014

40. High-Speed Interface Group – Xilinx Inc. – San Jose, CA - Spring 2014
41. Berkeley Wireless Research Center – UC-Berkeley – Berkeley, CA – Spring 2014
42. IEEE Forum for Leading Researchers – Austin, TX – Fall 2013
43. IEEE CICC Future of High-Speed Device Data Transfer Panel – San Jose, CA – Fall 2013
44. NSERC Silicon Photonics Tutorial - University of British Columbia – Vancouver, Canada - Fall 2013
45. High-Speed Interface Group - Texas Instruments, Inc. - Dallas, TX - Summer 2013
46. Enrichment Experiences in Engineering - Texas A&M University – College Station, TX - Summer 2013
47. Society of Women Engineers Summer Camp - Texas A&M University – College Station, TX - Summer 2013
48. IEEE Workshop on Microelectronics & Electron Devices Tutorial – Boise St. University – Boise, ID - Spring 2013
49. Texas Emerging Technology Fund - University of Texas, Dallas – Dallas, TX - Fall 2012
50. IEEE CICC Conference Tutorial – San Jose, CA – Fall 2012
51. High-Speed Interface Group - Fujitsu Laboratories of America Inc. - Sunnyvale, CA - Summer 2012
52. SRC-GRC Technology Transfer e-Workshop – University of Texas, Dallas – Dallas, TX - Spring 2012
53. IEEE VLSI-DAT Conference Tutorial – Hsinchu, Taiwan – Spring 2012
54. Industrial Technology Research Institute– Hsinchu, Taiwan – Spring 2012
55. High-Speed Interface Group - Samsung – South Korea - Summer 2011
56. High-Speed Interface Group - Broadcom Corp. - Irvine, CA - Spring 2011
57. ECEN Computer Engineering Seminar - Texas A&M University - College Station, TX – Spring 2011
58. SRC-GRC Technology Transfer e-Workshop – University of Texas, Dallas – Dallas, TX - Summer 2010
59. IEEE RFIC Power Management for Integrated RF Circuits Workshop – Anaheim, CA – Spring 2010
60. IEEE RFIC Future of High-Speed I/O Panel – Anaheim, CA – Spring 2010
61. ECEN Computer Engineering Seminar - Texas A&M University - College Station, TX - Fall 2009
62. VLSI Research Group - Sun Microsystems - Menlo Park, CA - Spring 2009
63. Photonics Technology Lab - Intel Corp. - Santa Clara, CA - Spring 2009
64. Wireless Analog/RF Design Group - Texas Instruments, Inc. - Dallas, TX - Spring 2009
65. CMOS Emerging Technologies Workshop - Banff, Canada - Spring 2009
66. Analog Circuit Group Workshop - Texas A&M University - College Station, TX - Fall 2008
67. ECEN Seminar - Texas A&M University - College Station, TX - Spring 2008
68. IEEE SSCS Santa Clara Valley Seminar - Santa Clara, CA - Spring 2008
69. IEEE Photonics Society High Speed Interconnects Workshop - Santa Fe, New Mexico - Spring 2007
70. Circuits & Photonics Research Groups - IBM TJ Watson Research Center - Yorktown Heights, NY - Spring 2006
71. High-Speed Interface Group - Intel Corp. - Hillsboro, OR - Spring 2006
72. High-Speed Interface Group - Texas Instruments, Inc. - Dallas, TX - Spring 2006

SHORT COURSES

Advanced High-Speed Serial Links Circuit Design Techniques – AMD Inc., Online, Summer 2020

Wireline SERDES Transceivers – MEAD Education, Online, Summer 2020

SERDES Design for Wireline and Optical Communications – Lynne Consulting, Shanghai, China, Summer 2019

Advanced High-Speed Serial Links Circuit Design Techniques – Mellanox Tech., Yokneam, Israel, Summer 2019

High-Speed Links Circuit Design Techniques – NXP Semiconductors, Chandler, AZ, Spring 2019

High-Speed Links Circuit Design Techniques – Lynne Consulting, Shanghai, China, Summer 2017

High-Speed Links Circuits and Systems – Qualcomm Inc., San Diego, CA, Summer 2015

FUNDING

Grants

SRC Global Research Collaboration, "Multi-Carrier DAC-Based Transmitter Architectures For 100+Gb/s Serial Links," PI: **S. Palermo**, co-PI: S. Hoyos, 09/2020-12/2023, $310,000 (50% of funds)

Southwestern Ohio Council for Higher Education, "A Wide-Range Radiation Hard PLL with Self-Healing Techniques," PI: **S. Palermo**, 09/2020-09/2021, $75,000 (100% of funds)

Southwestern Ohio Council for Higher Education, "A 20-50 GHz Frequency-Agile Silicon Photonic Receiver with Jammer Suppression," PI: K. Entesari, co-PI: **S. Palermo**, 09/2020-09/2021, $75,000 (50% of funds)

National Security Agency, "Scalable All-To-Date Optical Interconnect," PI: S. J. B Yoo (UC-Davis), Co-PI: **S. Palermo**, 07/2020-06/2021, $180,000 (100% of TAMU Portion)

Department of Energy, "Phase II: Energy-Efficient Reconfigurable Universal Accelerator Interconnect," PI: S. J. B Yoo (UC-Davis), Co-PI: **S. Palermo**, 04/2020-04/2021, $150,000 (100% of TAMU Portion)

Defense Advanced Research Projects Agency, “High-Efficiency Lasers with Integrated External Modulators for Petabit-Class Interconnects (HELIEM PCI)”, PI: M. Wood (Sandia National Labs), co-PI: **S. Palermo**, 09/2019-01/2021, $325,000 (100% of TAMU portion)

National Science Foundation, “Jitter-Tolerant Multi-Carrier ADC-Based Serial Link Architectures,” PI: S. Hoyos, co-PI: **S. Palermo**, 09/2019-08/2022, $390,000 (50% of funds)

Army Research Office, "Cacheless Computer Architecture with Massively Parallel Optically Interconnected Memory for Scaleable, Low-Latency, Energy-Efficient, and High-Productivity Computing," PI: S. J. B Yoo (UC-Davis), Co-PI: **S. Palermo**, 09/2019-09/2020, $25,000 (100% of TAMU Portion)

NXP, "Development of a 56/112 Gb/s Linear Redriver in a 0.13μm BiCMOS Process," PI: **S. Palermo**, 04/2019-10/2020, $106,441 (100% of funds)

Department of Energy, "Energy-Efficient Reconfigurable Universal Accelerator Interconnect," PI: S. J. B Yoo (UC-Davis), Co-PI: **S. Palermo**, 02/2019-02/2020, $223,500 (23.5% of funds)

National Science Foundation, “SpecEES: Spectrum and Energy Efficient Silicon Photonic Millimeter-wave Remote Antenna Units for Radio over Fiber Application,” PI: K. Entesari, co-PIs: C. Madsen and **S. Palermo**, 09/2018-08/2021, $675,000 (33.3% of funds)

National Science Foundation, “A Wideband Silicon Photonic Millimeter-wave Beam-forming Transmitter with Automatic Beam Calibration,” PI: K. Entesari, co-PI: **S. Palermo**, 08/2018-07/2021, $360,000 (50% of funds)

SRC Global Research Collaboration, "Frequency-Domain ADC-Based Serial Link Receiver Architectures for 100+Gb/s Serial Links," PI: **S. Palermo**, co-PI: S. Hoyos, 01/2018-12/2020, $180,000 (50% of funds)

United States Air Force Research Laboratory, "Photonic-Electronic Co-Design of Energy Efficient Silicon Photonic Interconnects," PI: S. J. B Yoo (UC-Davis), Co-PI: **S. Palermo**, 08/2017-08/2020, $1,223,704 (45% of funds)

Qualcomm Technologies, "Low-Power High-Speed Chip-to-Chip Serial Link PHY," PI: **S. Palermo**, 01/2017-08/2018, $176,000 (100% of funds)

National Science Foundation, “EARS: A Wideband Frequency-Agile Silicon Photonic mm-Wave Receiver with Automatic Jammer Suppression via Rapidly Reconfigurable Optical Notch Filters,” PI: **S. Palermo**, co-PIs: K. Entesari and C. Madsen, 09/2015-08/2019, $625,000 (33.3% of funds)

SRC Global Research Collaboration (Intel Member Specific Research Funding), "Digitally-Oriented Equalization Techniques for +40Gb/s Electrical and Optical Links," PI: **S. Palermo**, co-PI: S. Hoyos, 01/2015-12/2017, $300,000 (50% of funds)

SRC Global Research Collaboration (TI Custom Funding), "Design Techniques for Modulation-Agile and Energy-Efficient 60+Gb/s Receiver Front-Ends," PI: **S. Palermo**, 02/2014-01/2017, $165,000 (100% of funds)

National Science Foundation, "CAREER: Process, Voltage, and Temperature (PVT)-Tolerant CMOS Photonic Interconnect Transceiver Architectures," PI: **S. Palermo**, 5/2013-12/2018, $400,000 (100% of funds)

SRC Global Research Collaboration, "Advanced ADC-Based Serial Link Receiver Architectures," PI: **S. Palermo**, co-PI: S. Hoyos, 08/2012-07/2015, $270,000 (50% of funds)

National Science Foundation, "Advanced Modeling and Design of High-Performance ADC-Based Serial Links," PI: **S. Palermo**, 05/2012-04/2015, $360,000 (100% of funds)

Hewlett Packard, "Energy Efficient Electronics for Nanophotonic Interconnects," PI: **S. Palermo**, 10/2011-09/2020, $1,132,500 (100% of funds)

SRC Global Research Collaboration, "Design Techniques for Scalable, Sub-1mW/Gbps Serial I/O Transceivers," PI: **S. Palermo**, co-PI: P. Chiang (Oregon State University), 08/2010-07/2013, $180,000 (68.5% of funds)

SRC Global Research Collaboration, "A Fully-Integrated CMOS Platform for Microwave-Based Label-Free DNA Sensing," PI: K. Entesari, co-PI: **S. Palermo**, 08/2010-07/2013, $180,000 (50% of funds)

SRC Global Research Collaboration, "Energy Efficient CMOS 10GS/s 6-bit ADC with Embedded Equalization," PI: **S. Palermo**, 08/2009-07/2012, $180,000 (100% of funds)

Gifts

Marvell, "High Speed Interfaces," PI: **S. Palermo**, 4/2020, $30,000 (100% of funds)

Xilinx, "High Speed Interfaces," PI: **S. Palermo**, 6/2018, $15,000 (100% of funds)

NXP, "Design and Equalization Techniques for Energy-Efficient Serial Link Redrivers," PI: **S. Palermo**, 12/2017, $15,079 (100% of funds)

Hewlett Packard Enterprise, "Energy Efficient Electronics for Nanophotonic Interconnects," PI: **S. Palermo**, 1/2016, $10,000 (100% of funds)

Hewlett Packard, "Energy Efficient Electronics for Nanophotonic Interconnects," PI: **S. Palermo**, 1/2014, $10,000 (100% of funds)

PROFESSIONAL SERVICE

Membership

Senior Member, Institute of Electrical and Electronics Engineers (IEEE)
- Circuits and Systems Society
- Photonics Society
- Solid-State Circuits Society

Editorship

Associate Editor, IEEE Solid State Circuits Letters (2017-present)

Associate Editor, IEEE Transactions on Circuits and Systems II: Express Briefs (2011-2015)

Distinguished Lecturer

IEEE Solid-State Circuits Society (2016-2017)

Funding Agency Proposal Review

Canadian Foundation for Innovation Proposal Review (CFI), 2016 (1 proposal)

Department of Energy SBIR Phase II Proposal Review (ASCR), 1/12/16 (1 proposal)
Ghent University Industrial Research Fund (IOF-Stepstone), 2016 (1 proposal)
Ghent University Industrial Research Fund (IOF-Advanced), 2015 (1 proposal)
National Science Foundation Proposal Review Panel (CCSS), Feb. 27-28, 2014 (7 proposals)
Department of Energy SBIR Phase I Proposal Review Panel (HEP), 11/25/13 (1 proposal)
Department of Energy SBIR Phase I Proposal Review Panel (ASCR), 11/27/12 (3 proposals)
National Science Foundation Proposal Review Panel (CCSS), Sept. 27-28, 2012 (7 proposals)
National Science Foundation Proposal Review Panel (CCSS), May 9-10, 2012 (8 proposals)
Quebec New Researchers Start-up Program of Fonds, 2010 (1 proposal)

Reviewing (Journals and Conferences)

IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)
IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
IEEE Journal of Solid-State Circuits (JSSC)
IEEE Journal of Lightwave Technology (JLT)
IEEE Transactions on Biomedical Circuits and Systems (TBioCAS)
IEEE Transactions on Microwave Theory and Techniques (MTT)
IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
IEEE Transactions on Components, Packaging and Manufacturing Technology (CPMT)
IEEE Electron Device Letters (EDL)
IEEE Photonics Technology Letters (PTL)
IEEE Microwave and Wireless Components Letters (MWCL)
IEEE Design and Test (D&T)
IEEE Transactions on Industrial Electronics (TIE)
OSA Optics Express
OSA Optica
Biomedical Microdevices
Integration, the VLSI Journal
Light: Science & Applications (LSA)
Scientific Reports
IET Electronics Letters (Electron Lett)
Analog Integrated Circuits and Signal Processing (AICSP)
Microelectronics Journal (MEJ)
SPIE Optical Engineering (OE)
International Journal of Circuit Theory and Applications
IEEE Asian Solid-State Circuits Conference (A-SSCC)
IEEE Custom Integrated Circuits Conference (CICC)

IEEE International Solid-State Circuits Conference (ISSCC)

IEEE International Symposium on Circuits and Systems (ISCAS)

IEEE International Midwest Symposium on Circuits & Systems

IEEE Optical Interconnects Conference (OIC)

IEEE Texas Symposium on Wireless & Microwave Circuits & Systems

IEEE/OSA Optical Fiber Communication Conference (OFC)

ISQED Asia Symposium on Quality Electronic Design (ASQED)

General Co-Chair

IEEE Optical Interconnects Conference (2016)

Circuits and Systems for Medical and Environmental Applications Workshop (2012)

Program Co-Chair

IEEE Optical Interconnects Conference (2015)

Special Sessions Co-Chair

IEEE International Midwest Symposium on Circuits and Systems (2019)

Technical Program Co-Chair

IEEE Custom Integrated Circuits Conference (2020-2021)

Technical Program Committee

IEEE Custom Integrated Circuits Conference (2012-present)

IEEE Optical Interconnects Conference (2015-present)

IEEE International Solid-State Circuits Conference (2016-2020)

IEEE Group IV Photonics Conference (2019)

IEEE/OSA Optical Fiber Communication Conference (2016-2019)

IEEE Asian Solid-State Circuits Conference (2016-2017)

IEEE International Midwest Symposium on Circuits and Systems (2013-2014)

Interdisciplinary Engineering Design Education Conference (2012)

ISQED Asia Symposium on Quality Electronic Design (2009-2011)

CMOS Emerging Technologies Workshop (2009-2011)

Steering Committee

IEEE International Midwest Symposium on Circuits and Systems (2014-present)

Session Chair

IEEE/OSA Optical Fiber Communication Conference (2018-2019)

IEEE International Solid-State Circuits Conference (2017)

IEEE Asian Solid-State Circuits Conference (2016)

IEEE Custom Integrated Circuits Conference (2013)

IEEE International Midwest Symposium on Circuits and Systems (2011, 2013-2015)

CMOS Emerging Technologies Workshop (2009, 2011)

Publication Chair

IEEE International Midwest Symposium on Circuits and Systems (2014)

Circuits and Systems for Medical and Environmental Applications Workshop (2010)

Other

IEEE Circuits and Systems Society Board of Governors Member (2011-2012)

Faculty Mentor in Enrichment Experiences in Engineering (E^3) Teacher Summer Research Program (2014)

Faculty Mentor in ECE Unplugged Summer Engineering Camp (2010-2013)