

Analysis and Modeling of Clock-Jitter Effects in Delta-Sigma Modulators

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Abstract

Random variation in the timing of clock edges (namely, clock-jitter) is a critical problem that is becoming the main limitation in the performance of state-of-the-art data-converters. The problem of clock-jitter is a very critical issue and can significantly deteriorate the achievable signal-to-noise ratio (SNR) of an analog-to-digital converter (ADC) or a digital-to-analog converter (DAC) by several dBs. For example, nowadays, the limitation on increasing the ADC performance in terms of SNR and speed is a clock-jitter specification of 0.1 picoseconds (ps) on the sampling-clock. Given that delta-sigma ($\Delta\Sigma$) ADCs are attractive candidates for state-of-the-art wideband and high SNR wireless receivers, thus in the process of designing a $\Delta\Sigma$ ADC, it is instructive to have robust models and estimation for the errors caused by clock-jitter. This is critical in extracting the requirements on clock-jitter for a given target performance and also to be able to explore efficient solutions and techniques that can remedy the effects of clock-jitter on the ADC performance. In this context, this chapter is intended to provide a comprehensive background and study for the effects of clock-jitter in the sampling-clocks of $\Delta\Sigma$ modulators. The study includes detailed analysis for the effects of clock-jitter on various waveforms and signals provided by different types of DACs used in $\Delta\Sigma$ modulators. Also, efficient Matlab/Simulink® models for additive errors induced by clock-jitter in $\Delta\Sigma$ modulators are shown so that to help designers characterize the sensitivities of various types of $\Delta\Sigma$ architectures to clock-jitter. The robustness of the adopted models is demonstrated through illustrative examples based on system-level simulations using Matlab/Simulink.

Keywords: Analog-to-digital converter (ADC), clock-jitter, continuous-time, data-conversion, delta-sigma ($\Delta\Sigma$) modulator, digital-to-analog converter (DAC), modeling, noise shaping, non-return to zero, return-to-zero, simulink, switched-capacitor (SC) DAC.

1. Introduction

The quest for higher data rates in state-of-the-art wireless standards and services calls for wideband and high-resolution data-converters in wireless transceivers. While modern integrated circuits (IC) technologies provide high cut-off frequencies (f_T) for transistors and hence allow the operation at higher speeds, the main limitation against increasing speed of operation of data-converters is the problem of clock-jitter. Clock-jitter is a common problem associated with clock generators due to uncertainty in the timing of the clock edges caused

by the finite phase-noise (PN) in the generated clock waveform. Particularly, noise components induced by several noise sources in the system providing the clock (e.g. phase-locked loop, PLL) add to the clock waveform and cause uncertainty in the timing of the zero-crossing instants from cycle to cycle. Figure 1 shows a survey chart of the analog-to-digital converter (ADC) implementations reported in IEEE International solid-state circuits conference (ISSCC) and VLSI Symposium since 1997 [1]. The straight lines show the limitation on the achievable signal-to-noise ratio (SNR) by clock-jitter for jitter root-mean square (rms) values of 1ps and 0.1ps. As can be seen from the chart, the performance of most ADCs falls below the line corresponding to 1ps rms jitter, few ADCs reside in the range between 1ps and 0.1ps, and almost all ADC implementations reported so far are beyond the 0.1ps rms jitter line. This means that the main limitation on increasing the ADC performance in terms of SNR and speed is the specification on the clock-jitter of 0.1ps.

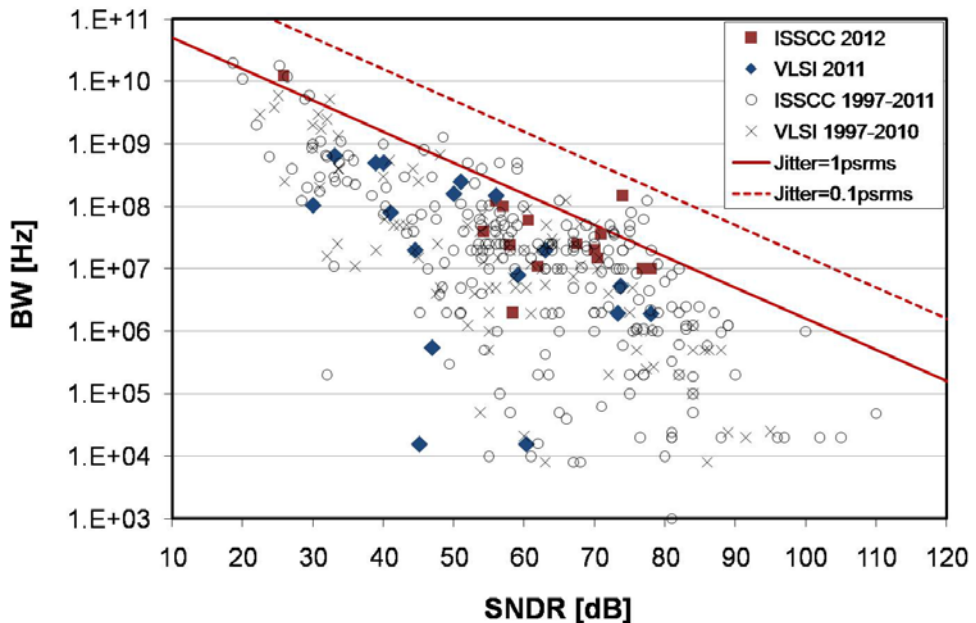


Figure 1. ADC Performance Survey 1997-2012 [1]

Delta-sigma ($\Delta\Sigma$) ADCs are the convenient choice in low power and state-of-the-art multi-standard wireless receivers for two main reasons. First, they trade DSP for relaxed analog circuit complexity. Particularly, $\Delta\Sigma$ ADC implementations span analog and digital domains ($\Delta\Sigma$ pulse density modulation + digital decimation and filtering, as shown in Figure 2) and hence exploit DSP to relax hardware requirements on analog blocks. Thus, the simplified analog part ($\Delta\Sigma$ modulator) and the digital filtering can be efficiently reconfigured to fulfill performance requirements of different standards at minimum power consumption. Second, $\Delta\Sigma$ modulators use oversampling and hence trade speed for resolution. Specifically, for a given $\Delta\Sigma$ modulator and channel bandwidth (BW), higher effective number of bits (ENOB) can be achieved by increasing the oversampling ratio (OSR). This qualifies $\Delta\Sigma$ ADCs to

benefit from increasing speeds of operation offered by advanced deep submicron CMOS technologies (maximum cutoff-frequency $f_T > 300 \text{ GHz}$ in 45nm [2]) to meet higher resolution requirements for modern and future wireless services at minimum power overhead.

Continuous-time (CT) $\Delta\Sigma$ ADCs are widely used in wideband low power wireless receivers [3, 4]. The CT operation of the loop filter relaxes the requirements on the gain-bandwidth product (GBW) of the adopted amplifiers and hence allows the operation at higher speeds or lower power consumption compared to discrete-time (DT) implementations. Also, CT loop filters offer inherent anti-aliasing and thus save the need for explicit anti-aliasing filter before the ADC. The requirements on the sample-and-hold (S/H) circuitry are also relaxed because the sampling is performed after the loop filter and hence the sampling errors experience the maximum attenuation offered by the loop (similar to quantization noise). However, CT $\Delta\Sigma$ modulators suffer from high sensitivity to clock-jitter in the sampling-clock of the digital-to-analog converters (DACs) in the feedback.

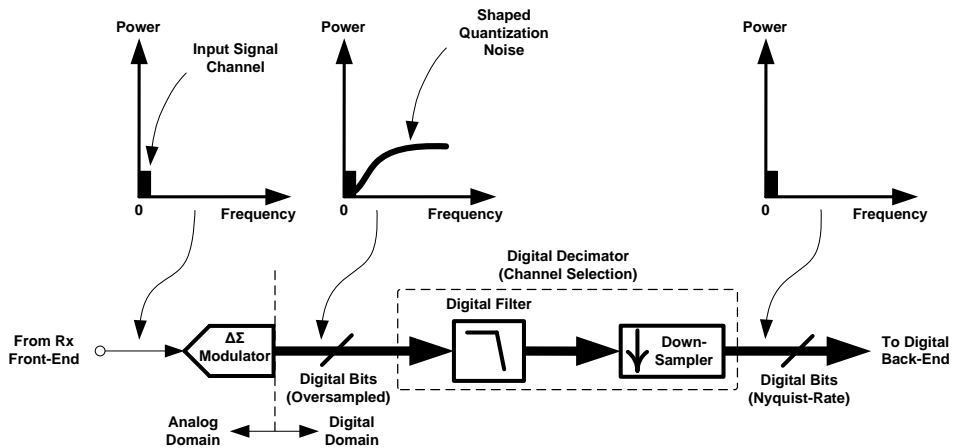


Figure 2. $\Delta\Sigma$ ADC ($\Delta\Sigma$ pulse density modulation + digital decimation and filtering).

In this context, this chapter is intended to provide a comprehensive background and study for the effects of clock-jitter in the sampling-clocks of $\Delta\Sigma$ modulators. Also, Matlab/Simulink models for additive errors induced by clock-jitter in $\Delta\Sigma$ modulators are given so that to help designers characterize the sensitivities of various types of $\Delta\Sigma$ architectures to clock-jitter. The material in this chapter is organized as follows. Section 2 gives a general background about the types of errors caused by clock-jitter in different classes of switched circuits and signal waveforms. The critical sources of jitter induced errors in a $\Delta\Sigma$ loop are identified for DT and CT $\Delta\Sigma$ modulators and a comparison between the two types, in terms of sensitivity to clock-jitter, is done in Section 3. Section 4 provides detailed sensitivity analysis for CT $\Delta\Sigma$ modulators to clock-jitter in the feedback DAC sampling-clock. In Section 5, Simulink models, based on the analysis of Section 4, for the additive errors generated by clock-jitter in CT $\Delta\Sigma$ modulators are shown and the robustness of these models is verified by CT simulations in Matlab/Simulink. Simulations results show good agreement with the theoretical expectations. Finally, conclusions are drawn in Section 6.

2. Jitter Problems: Background

Since digital data is always available in DT form, then any process of converting information from analog form to digital bit-stream or vice versa entails sampling. However, the clock signals driving sampling switches suffers clock-jitter due to the noise components that accompany the clock waveform. Figure 3 shows the PN density in a typical voltage-controlled oscillator (VCO)¹. In the time-domain, the integrated effect of these noise components results in random variations in the phase of the generated clock signal. In data-converters, the problem of clock-jitter is a very critical issue and can significantly deteriorate the achievable SNR by several dBs. The problems resulting from clock-jitter are classified as follows:

Phase Noise, dBc/Hz

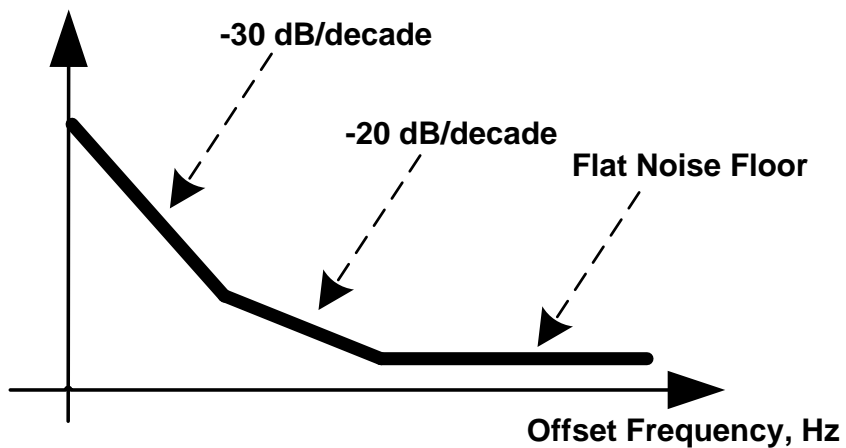


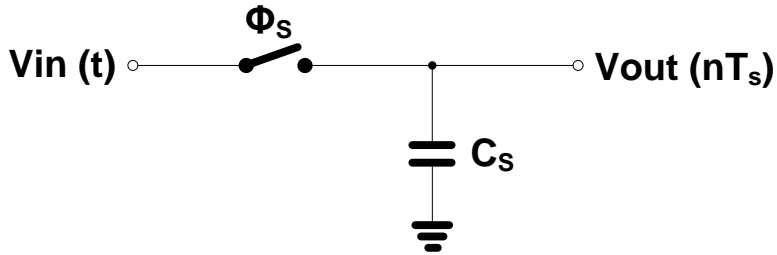
Figure 3. Typical Phase-Noise profile in a VCO.

2.1. Aperture Jitter: Voltage Sampling Errors

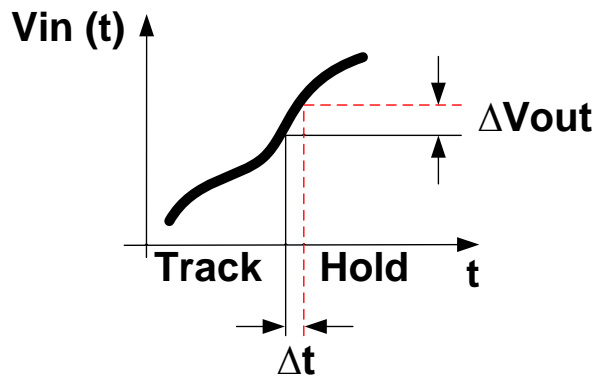
In ADCs, it is desirable to convert CT voltage signals into DT form. Figure 4(a) shows a common track-and-hold (T/H) circuit based on a switch driven by a clock signal (sampling-clock) and a sampling capacitor C_S . Errors in the sampled voltage (during the tracking phase) value is one of the most common problems resulting from timing uncertainty Δt (clock-jitter) in the sampling-clock. Particularly, on sampling an input voltage signal, random variations in the timing of the clock edges can result in an incorrect sampled signal, as illustrated in Figure 4(b). This effect is called aperture jitter. The noise induced by aperture jitter can be illustrated as follows. Suppose that a sinusoidal signal $A \sin(\omega t)$, where A is the amplitude and ω is the angular frequency, is to be sampled using a T/H circuit. Then, the error in the n^{th} sample of the sampled signal due to a timing error $\Delta t(n)$ is given by

¹ The design of clock generators and the mechanisms of PN generation in PLLs are not within the scope of the material given in this chapter.

Sampling-Clock, Φ_S 



(a)



(b)

Figure 4. T/H Circuit. (a) Schematic view and clock waveform. (b) Effect of aperture jitter on sampled values.

$$e(n T_s) = A \{ \sin[\omega(n T_s + \Delta t(n))] - \sin(\omega n T_s) \}$$

$$\approx A \omega \Delta t(n) \cos(n T_s). \quad (1)$$

where T_s is the sampling-period. If σ_j^2 is the variance of the timing error Δt , then the error power is given by

$$\sigma_e^2 = E(e^2) = \frac{(A \omega \sigma_j)^2}{2}. \quad (2)$$

Since the signal power of the sinusoid is given by $A^2/2$, the SNR due to aperture jitter is given by

$$SNR|_{\text{Due to aperture jitter}} = 10 \text{ Log} \left(\frac{1}{\omega^2 \sigma_j^2} \right) = 10 \text{ Log} \left(\frac{1}{4 \pi^2 f^2 \sigma_j^2} \right), \quad (3)$$

where $f = \omega/2\pi$ is the frequency. From (3) the SNR has the worst value at the edge of the signal band (largest value of frequency, f_{max}). The plots in Figure 5 show the limitation on the achievable SNR vs. the signal frequency due to aperture jitter for different values of the rms jitter σ_j .

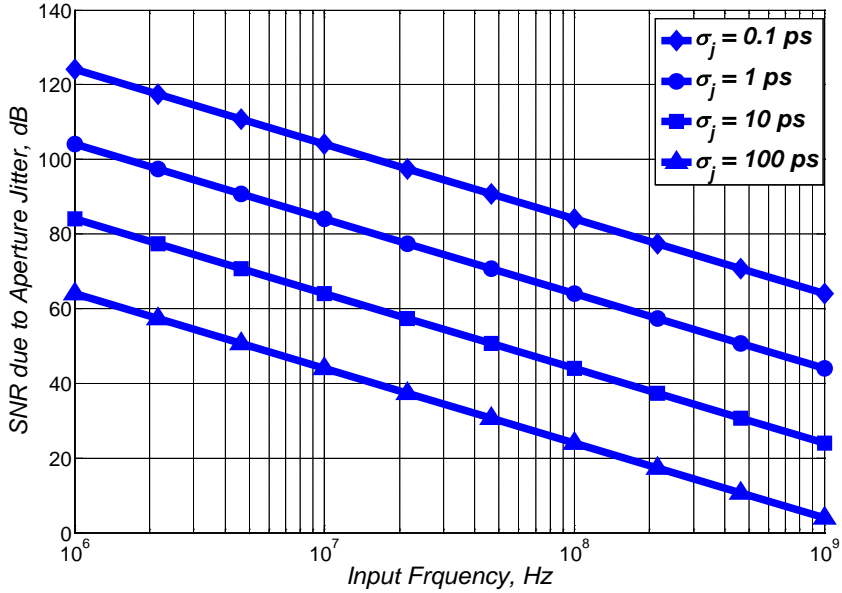


Figure 5. SNR variation with the input frequency due to aperture jitter for different rms jitter values.

2.2. Charge Transfer Jitter

Another effect of clock-jitter, called charge transfer jitter, shows up in circuits whose operation is based on charge transfer by switching. In particular, switched-capacitor (SC) circuits commonly used in DT ADCs and DACs suffer from charge transfer errors due to clock-jitter in the sampling clocks. Consider the simple non-inverting SC integrator in Figure 6(a). As shown by the time-domain waveforms in Figure 6(b), during integrating phase ϕ_2 , the charge stored in a sampling capacitor C_s is transferred to an integrating capacitor C_I

through the ON resistance (R_{ON}) of the switch. The discharging of C_S takes place in an exponentially-decaying rate.

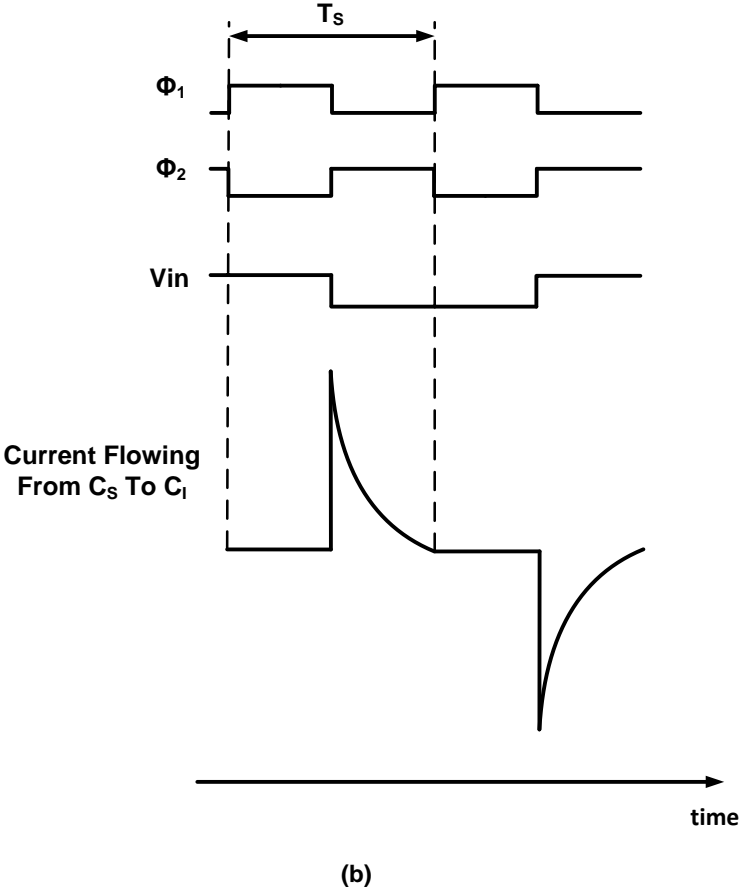
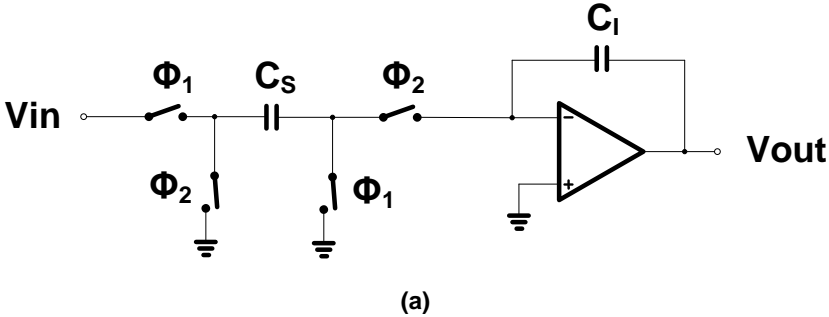


Figure 6. (a) Non-inverting switched-capacitor discrete-time integrator. (b) Time-domain waveforms for clock phases, input signal, and charge flow from C_S to C_I .

For a given clock-cycle n , the instantaneous exponentially-decaying current $I_n(t)$ resulting from the charge transfer from C_S to C_I can be derived as follows:

$$I_n(t) = \begin{cases} I_p e^{-\frac{(t-\alpha)T_s}{\tau}} & , \quad \alpha T_s < t < \beta T_s, 0 \leq \alpha \leq \beta \leq 1 \\ 0 & , \quad \text{otherwise} \end{cases} \quad (4)$$

where I_p is the value of the peak current at the beginning of the pulse, α and β are the start and end times of the exponentially-decaying pulse normalized to the sampling period T_s and τ is the discharging time-constant and is given by the product $R_{ON}C_S$. The values of α and β are determined by the duty-cycle of the clock. In typical SC circuits, $\alpha = 0.5$ and $\beta = 1$. Recall that the input voltage is sampled on C_S during the first clock half-cycle (when ϕ_1 is high) and then the charge on C_S is transferred to C_I during the second clock half-cycle (when ϕ_2 is high). For a total charge of Q_n to be transferred during ϕ_2 of clock-cycle n ,

$$Q_n = \int_{\alpha T_s}^{\beta T_s} I_n(t) dt = \int_{\alpha T_s}^{\beta T_s} I_p e^{-\frac{(t-\alpha)T_s}{\tau}} dt = -\tau A e^{-\frac{(t-\alpha)T_s}{\tau}} \Big|_{\alpha T_s}^{\beta T_s} = \tau A \left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}} \right) \quad (5)$$

Thus,

$$I_p = \frac{Q_n}{\tau \left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}} \right)}. \quad (6)$$

Substituting with (6) in (4) yields

$$I_n(t) = \begin{cases} \frac{Q_n}{\tau \left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}} \right)} e^{-\frac{(t-\alpha)T_s}{\tau}} & , \quad \alpha T_s < t < \beta T_s, 0 \leq \alpha \leq \beta \leq 1. \\ 0 & , \quad \text{otherwise.} \end{cases} \quad (7)$$

However, in presence of timing error $\Delta t(n)$ in the pulse-width of the discharging phase ϕ_2 , the resulting error in the integrated charge in the n^{th} clock-cycle is given by

$$\begin{aligned} e_j(n) &= \frac{Q_n}{\tau \left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}} \right)} \int_{\beta T_s}^{\beta T_s + \Delta t(n)} e^{-\frac{(t-\alpha)T_s}{\tau}} dt = \frac{-Q_n}{\left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}} \right)} e^{-\frac{(t-\alpha)T_s}{\tau}} \Big|_{\beta T_s}^{\beta T_s + \Delta t(n)} \\ &= \frac{Q_n}{\left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}} \right)} \left[e^{-\frac{(\beta-\alpha)T_s}{\tau}} - e^{-\frac{(\beta-\alpha)T_s - \Delta t(n)}{\tau}} \right] \\ &= \frac{Q_n}{\left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}} \right)} e^{-\frac{(\beta-\alpha)T_s}{\tau}} \left[1 - e^{-\frac{\Delta t(n)}{\tau}} \right], \end{aligned} \quad (8)$$

which for $\Delta t_n \ll \tau$ can be approximated by

$$e_j(n) \approx \frac{Q_n}{\tau \left(1 - e^{-\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{-\frac{-(\beta-\alpha)T_s}{\tau}} \Delta t(n). \quad (9)$$

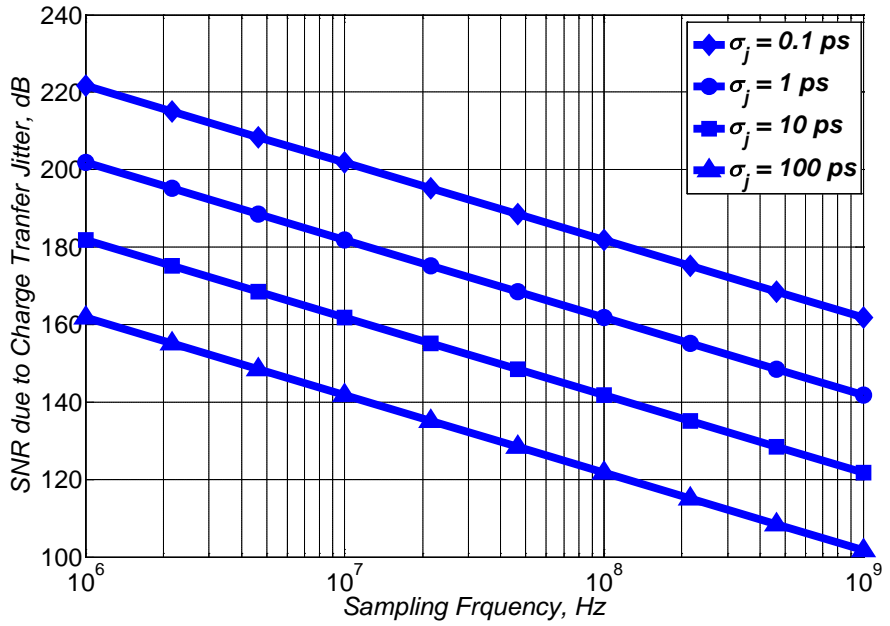
If σ_j^2 the variance of the timing error $\Delta t(n)$, then the error power is given by

$$\sigma_e^2 = E(e^2) = \left(\frac{Q_{rms}}{\tau \left(1 - e^{-\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{-\frac{-(\beta-\alpha)T_s}{\tau}} \right)^2 \sigma_j^2, \quad (10)$$

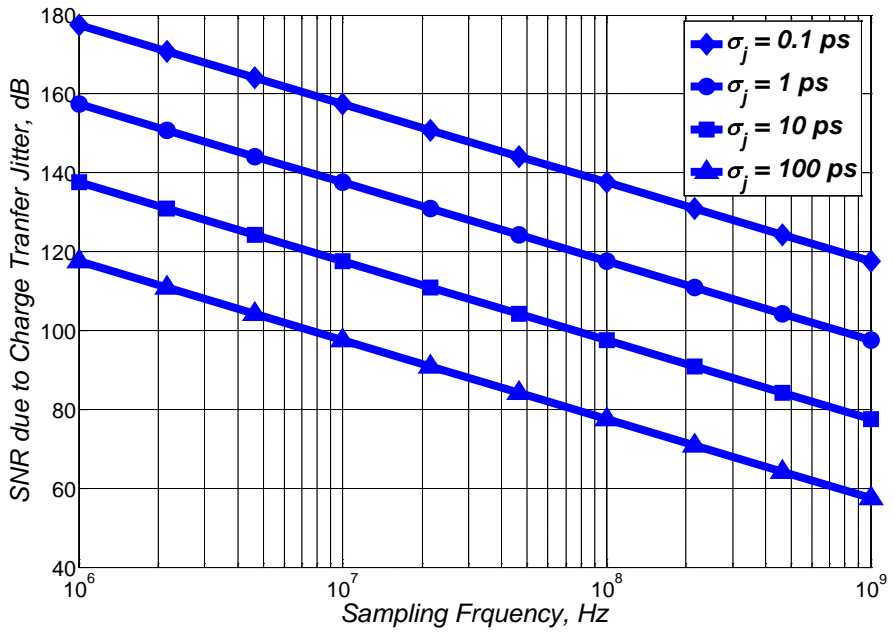
where Q_{rms} is the rms charge sampled on the sampling capacitor C_S . Thus, the SNR due to charge transfer jitter caused by charge transfer jitter is given by

$$\begin{aligned} SNR|_{Due\ to\ charge\ transfer\ jitter} &= 10 \text{ Log} \left(\frac{Q_{rms}^2}{\left(\frac{Q_{rms}}{\tau \left(1 - e^{-\frac{-(\beta-\alpha)T_s}{\tau}}\right)} e^{-\frac{-(\beta-\alpha)T_s}{\tau}} \right)^2 \sigma_j^2} \right) \\ &= 10 \text{ Log} \left(\frac{\tau^2 \left(1 - e^{-\frac{-(\beta-\alpha)T_s}{\tau}}\right)^2}{\left(e^{-\frac{-(\beta-\alpha)T_s}{\tau}} \right)^2} \frac{1}{\sigma_j^2} \right). \end{aligned} \quad (11)$$

The plots in Figure 7 show the limitation on the achievable SNR vs. the signal frequency due to charge transfer jitter for different values of the rms jitter σ_j . Typical values of $\alpha = 0.5$ and $\beta = 1$ have been considered. The results are provided for $\tau = 0.05 T_s, 0.1 T_s$, and $0.2 T_s$. As can be seen from the plots in Figure 7, for a given clock frequency, the SNR limitation due to charge transfer jitter is much more relaxed compared to the aperture jitter error (Figure 5). This result was expected because from equation (11), the effect of the jitter induced noise is reduced by an exponential factor indicating that charge transfer error in SC circuits should be less critical. This also can also be explained intuitively by noting that for the exponentially-decaying waveform in Figure 8, the amplitude of the pulse is rather low at the end of the clock-cycle and hence the amount of charge that varies over one clock period due to jitter is significantly reduced. However, for a given rms jitter and sampling frequency, the SNR limitation due to charge transfer jitter degrades as the discharging time-constant τ increases. This is because the value of the charge transfer current at the end of the clock-cycle (discharge phase) is varying exponentially with τ , thus for a given timing error Δt , the error in the amount of charge transferred is higher.



(a)



(b)

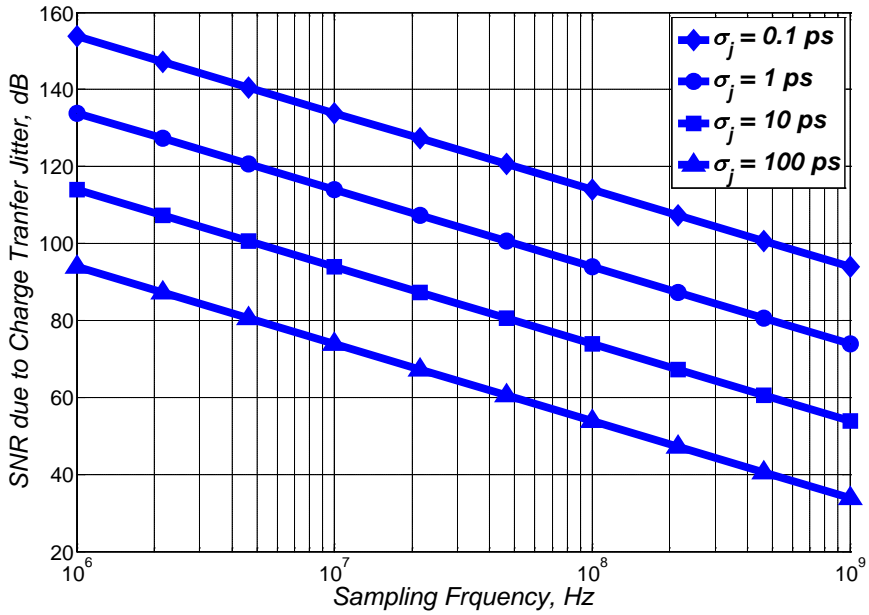


Figure 7. SNR variation with the input frequency due to charge transfer jitter for different rms jitter values. (a) $\tau = 0.05 T_s$. (b) $\tau = 0.1 T_s$. (c) $\tau = 0.2 T_s$.

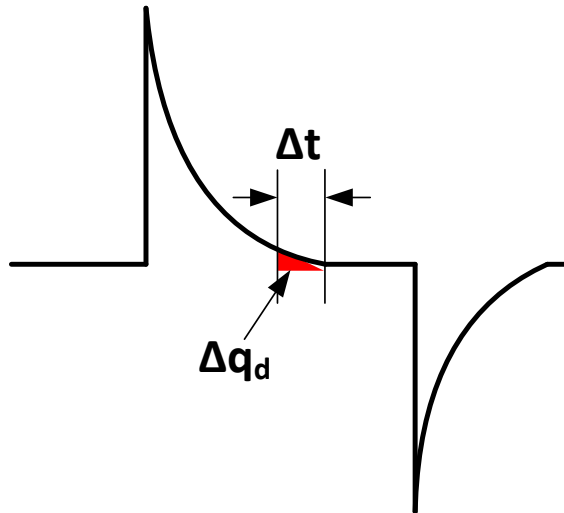


Figure 8. Jitter-tolerant exponentially-decaying waveform.

2.3. Pulse-Width Jitter

Continuous-time current-steering DAC, shown in Figure 9(a), is used to convert digital signals into CT analog pulses. Clock-jitter in the sampling-clock of a CT DAC modulates the pulse-width of the waveform at the DAC output. Called pulse-width jitter (PWJ), this problem generally shows up in circuits whose operation is based on current-switching, e.g. current-steering DACs, charge sampling circuits, and charge pumps. In systems using CT DACs (e.g. audio transmitters and CT $\Delta\Sigma$ modulators), the DAC is loaded by a CT filter stage that integrates the output current pulse from the DAC. The error in the amount of integrated charges is directly proportional to the timing error Δt in the pulse-width, as illustrated by the time-domain waveform in Figure 9(b). If the clock-jitter causes timing errors Δt with variance σ_j^2 and the switched-current levels are $\pm I_s$, the variance of the charge transferred per clock-cycle T_s is

$$\sigma_e^2 = \sigma_j^2 I_s^2. \quad (12)$$

For a sinusoidal signal, the maximum signal power in terms of the integrated charge signal per clock-cycle is given by

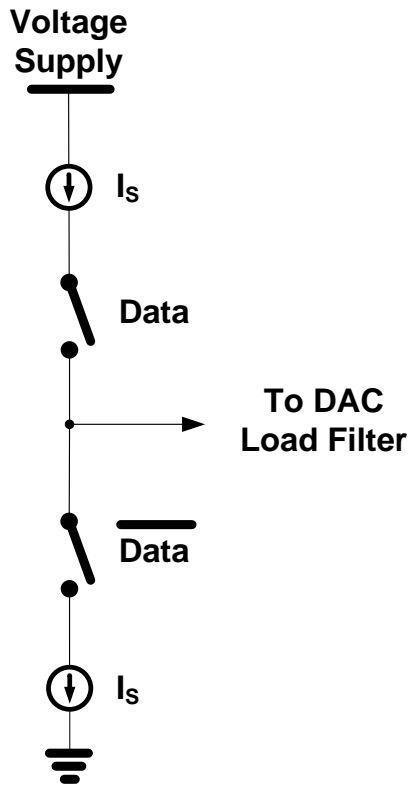
$$\sigma_{signal}^2 = \frac{I_s^2 T_s^2}{2}. \quad (13)$$

Thus, the maximum SNR against PWJ is given by

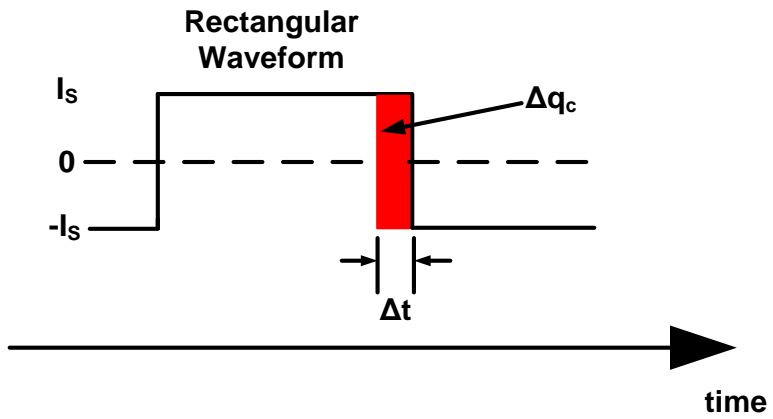
$$SNR|_{Due\ to\ pulse-width\ jitter} = 10 \text{ Log} \left(\frac{T_s^2}{2 \sigma_j^2} \right), \quad (14)$$

Thus, the SNR degradation by PWJ is less than that of the aperture jitter by a factor of $2\pi^2$. The plots in Figure 10 show the limitation on the achievable SNR vs. the signal frequency due to PWJ problem for different values of the rms jitter σ_j .

Figure 11 provides a comparative insight about the SNR limitation imposed by each one of the clock-jitter induced problems discussed above. It is worth noting that these plots are for Nyquist-rate sampling; however the foregoing analysis and results can be easily extended to include the effect of oversampling in oversampled circuits. As can be observed from the plots in Figure 11, for a given sampling frequency, the maximum limitation on the achievable SNR is caused by aperture jitter. However, the charge transfer jitter limits the SNR at very high frequencies; for example for an SNR of 80 dB, the charge transfer jitter starts to limit the achievable SNR at sampling frequency $F_s \geq 1 \text{ GHz}$ for $\tau = 0.1 T_s$, and as mentioned before more robustness to charge transfer jitter at high frequencies can be obtained by reducing the discharging time-constant τ .



(a)



(b)

Figure 9. Pulse-width jitter in switched-current circuits.

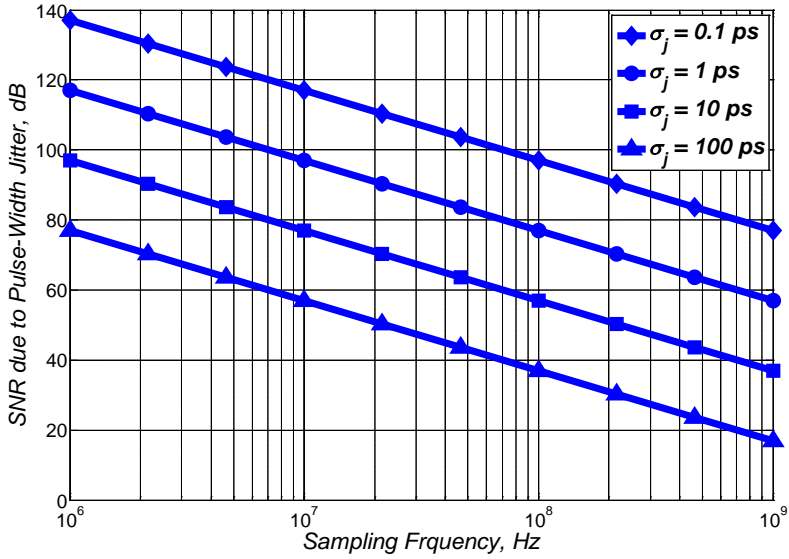


Figure 10. SNR variation with the input frequency due to pulse-width jitter for different rms jitter values.

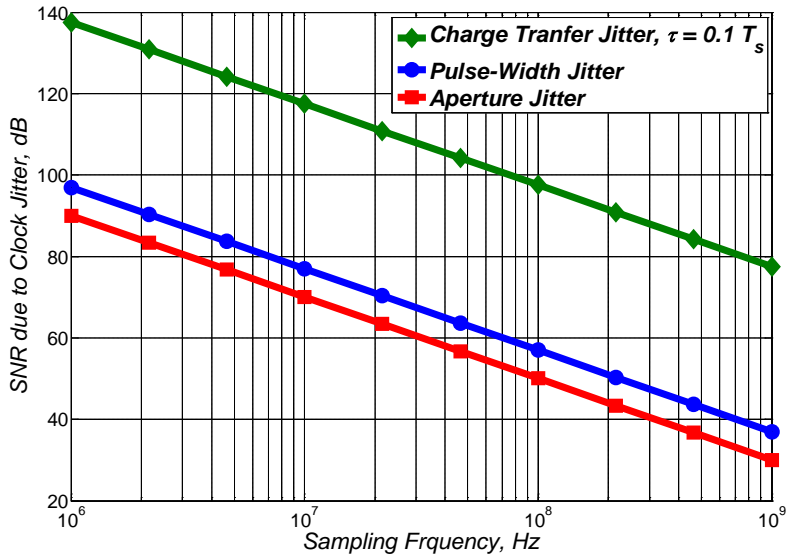


Figure 11. SNR variation with the sampling frequency due to different types of jitter induced errors for a rms jitter of 10 ps.

3. Sensitivity of $\Delta\Sigma$ Modulators to Clock-Jitter

The purpose of this section is to address the effects of clock-jitter in the two main classes of $\Delta\Sigma$ modulators, shown in Figure 12, and provide a comparison between them in terms of sensitivity to clock-jitter. In order to determine the performance sensitivity to clock-jitter in DT and CT modulators, the critical sources of jitter induced errors in the loop should be identified in each one. The most critical clock-jitter errors in a $\Delta\Sigma$ modulator are those generated at the modulator input and in the feedback path through the outermost DAC feeding the first stage in the loop filter (recall that errors generated at inner nodes in the loop are suppressed by the previous stages of the loop filter).

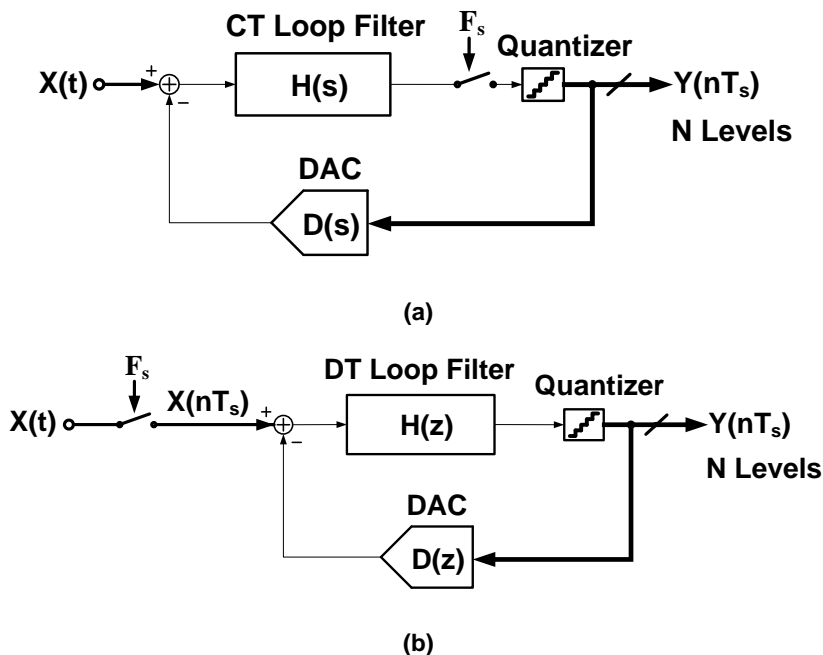


Figure 12. $\Delta\Sigma$ Modulators. (a) Continuous-Time. (b) Discrete-Time.

The feedback signal is carrying a digital data (coming from the loop quantizer) and hence it is robust to aperture jitter². However, depending on the type of the adopted feedback DAC, the feedback signal in a $\Delta\Sigma$ loop can suffer one of the other two kinds of jitter induced errors (namely, charge transfer jitter and PWJ). The effect of feedback jitter can be further discussed in the frequency domain with the aid of Figure 13 as follows. Recall that the modulator feedback signal includes the in-band desired signal (input signal) and the high-pass shaped noise. Since the sampling process ideally is a multiplication in time, the spectra of the analog input signal and the clock signal convolve. Thus, the error generated by DAC clock PN has two main components, as illustrated by Figure 13. First, the clock PN

² Since the digital data coming in the feedback is usually sampled at the middle of the clock-cycle, sampled signal in the feedback can suffer aperture jitter only if the clock-jitter is $\geq T_s/2$.

components close to the clock frequency modulates the in-band desired signal resulting in signal sidebands in the same manner like the PN of an upfront sampler [5]. Second, the wideband clock PN, modulates the high-pass shaped noise components and the modulation products fall over the desired band and hence elevate the in-band noise level.

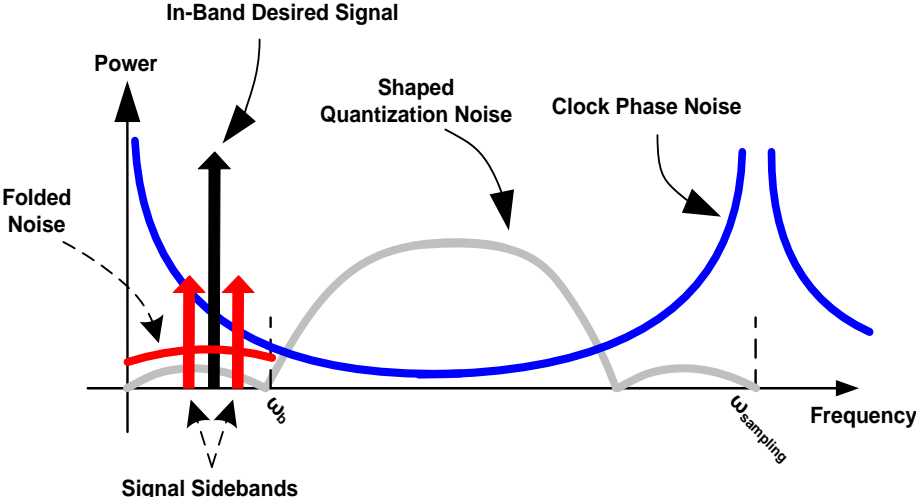


Figure 13. Modulation of in-band desired signal and shaped quantization noise by phase-noise in the DAC sampling clock.

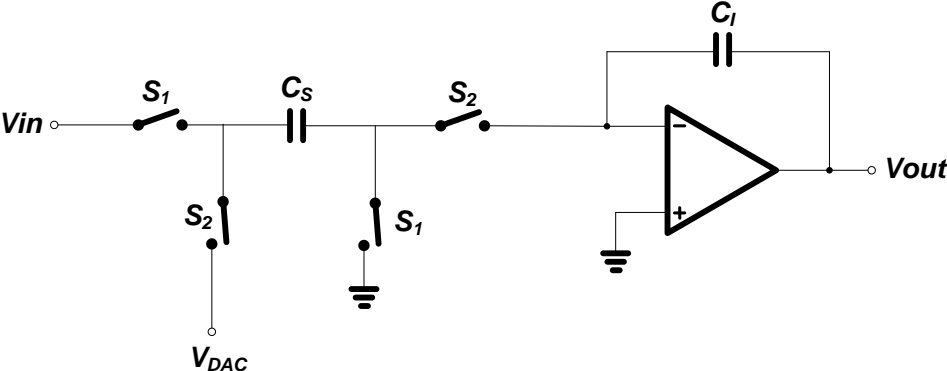


Figure 14. Non-inverting switched-capacitor discrete-time integrator.

3.1. DT ΔΣ Modulators

In DT ΔΣ modulators, the sampling takes place at the modulator input. The SC integrator in Figure 14 is commonly used as an input stage for DT loop filters in ΔΣ modulators. The sampling aperture jitter errors due to the sampling switch (S_1) will be added to the signal at

the input and hence will directly appear at the modulator output without any suppression. As mentioned earlier, the feedback signal (V_{DAC}) doesn't experience aperture jitter because the feedback signal is DT and also it has discrete amplitude levels. Thus, timing errors cannot result in a sampled value that is different from the original feedback one. Timing errors at switch S_2 cause charge transfer jitter errors being added at the input stage. However, the charge transfer jitter errors at S_2 are very small owing to the high robustness of the exponentially-decaying waveform to clock-jitter and moreover R_{ON} of the switches are usually very small resulting in a small time-constant τ which gives more jitter robustness to the waveform (recall the analysis given in the previous section).

According to the above discussion, the jitter induced noise in DT $\Delta\Sigma$ modulators is mainly dominated by the aperture error at S_1 . At a given sampling speed, the only way to improve the performance of DT $\Delta\Sigma$ modulators is to improve the jitter performance of the clock generator which translates into significant increase in the total power consumption in case of $\Delta\Sigma$ ADCs targeting high resolution. On the other hand, for a given rms jitter, if the sampling frequency is reduced for the sake of improving tolerance to jitter errors, then to achieve high resolution at the resulting low OSR, the filter order and/or the quantizer levels need to be increased. This translates into significant power penalty too. Moreover, this approach wouldn't work for state-of-the-art wireless standards with continuously increasing channel bandwidths.

3.2. CT $\Delta\Sigma$ Modulators

In CT $\Delta\Sigma$ modulators, sampling occurs after the loop filter and hence sampling errors including aperture jitter are highly suppressed when they appear at the output because this is the point of maximum attenuation in the loop. However, CT $\Delta\Sigma$ implementations suffer from jitter errors added to the feedback signal. Particularly, in a CT $\Delta\Sigma$ modulator the DAC converts the quantizer output DT signal into CT pulses. The waveform coming from the CT DAC is fed to the loop filter to be integrated in the CT integrator stages. Thus, PWJ in the DAC waveform causes uncertainty in the integrated values at the outputs of the loop filter integrators. Rectangular waveform DACs are commonly used in CT $\Delta\Sigma$ structures due to their simple implementation and the relatively relaxed slew-rate (SR) requirement they offer for the loop filter amplifiers. Return-to-zero (RZ) DACs are the most sensitive to feedback PWJ because the random variations are affecting the rising and falling edges of the waveform at every clock-cycle. The jitter sensitivity can be slightly reduced by using a NRZ DAC because in this case, the clock-jitter will be effective only during the clock edges at which data is changing. The equivalent input-referred errors induced by clock jitter in RZ and NRZ waveforms for a certain sequence of data are illustrated in Figure 15.

As mentioned earlier, clock-jitter errors added in the feedback path are the most critical because they entail random phase-modulation that folds back high-pass shaped noise components over the desired channel. For typical wideband CT $\Delta\Sigma$ modulators with NRZ current steering DACs in the feedback, the error induced by the PWJ in the DAC waveform can be up to 30% - 40% of the noise budget [3, 4, 6].

Convenience for low power implementations: CT $\Delta\Sigma$ modulators have gained significant attention in low power and high speed applications because they can operate at higher speed or lower power consumption compared to DT counterparts. Recall the relaxed gain bandwidth (GBW) product requirements they add on the loop filter amplifiers compared to

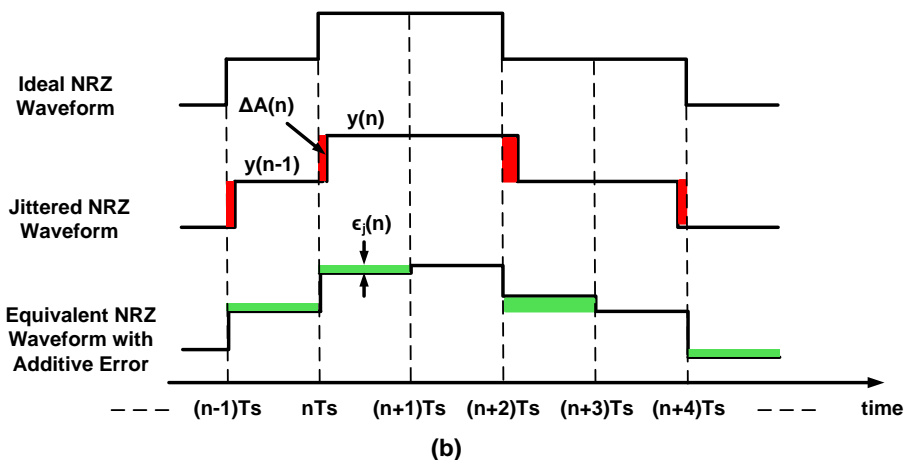
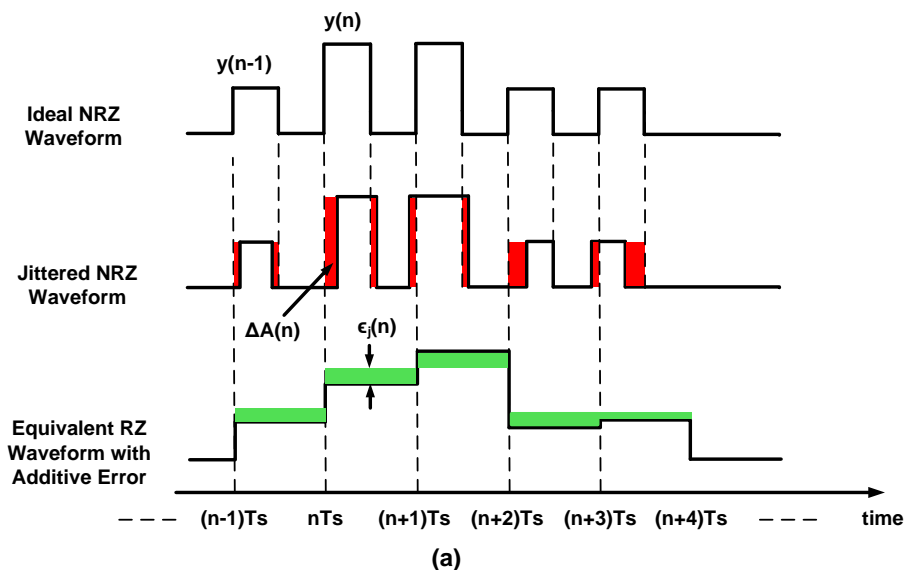


Figure 15. Equivalent input referred error induced by pulse-width jitter [7]. (a) RZ DAC. (b) NRZ DAC.

DT implementations in which the loop filter is processing a DT signal and hence a GBW requirement on the amplifier is typically in the range of five times the sampling frequency. Moreover, sensitivity of CT $\Delta\Sigma$ modulators to DAC clock-jitter can be minimized by processing the DAC pulse or modifying its shape so as to alleviate the error caused by the DAC clock jitter [7]. That is, the achievable SNR of a CT $\Delta\Sigma$ modulator can be improved against clock-jitter without having to improve the jitter performance of the clock generator or to reduce the sampling speed and increase the order of the loop filter or the quantizer resolution. This definitely translates into power savings because it avoids increasing the

complexity of the clock generator or the $\Delta\Sigma$ modulator and hence avoiding extra power penalties³.

4. Analysis of Jitter Effects in CT $\Delta\Sigma$ Modulators

This section provides detailed analysis for the effects of DAC clock-jitter on the performance of CT $\Delta\Sigma$ modulators for the most commonly used DAC types.

4.1. Return-To-Zero DAC Waveforms

Return-to-zero DAC waveforms are known to be robust to even-order nonlinearities resulting from mismatch between rise and fall times, as well as less sensitive to excess loop delay in the quantizer compared to NRZ waveforms [3]. However, as mentioned in previous section, they are the most sensitive to PWJ because the additive jitter induced errors are linearly proportional to the random timing errors at the rise and fall edges every clock-cycle, as illustrated in Figure 15(a). The equivalent error induced by PWJ in a RZ DAC waveform is given by

$$\epsilon_j(n) = \frac{\Delta A(n)}{T_s} = y(n) \frac{T_s}{T_c} \frac{(\Delta t_r(n) + \Delta t_f(n))}{T_s}, \quad (15)$$

where $\Delta A(n)$ is the area difference resulting from the error in the total integrated charge per one clock period T_s between the ideal and the jittered waveforms, $y(n)$ is the modulator output at the n^{th} clock cycle, T_c is the duty-cycle of the RZ pulse, and $\Delta t_r(n)$ and $\Delta t_f(n)$ are the random timing errors in the rise and fall edges, respectively, of the n^{th} DAC pulse. The amplitude of the DAC pulse varies inversely proportional with the pulse duty-cycle so that to supply a constant amount of charge (determined by Full-Scale (FS) voltage level of the quantizer) to the loop filter per clock-cycle. Following the procedure in [7], for a single tone $V_{sig} \cdot \sin(\omega_{sig} t)$ at the input of the $\Delta\Sigma$ modulator, the integrated in-band jitter-induced noise power (IBJN) for a RZ DAC is given by

$$IBJN|_{RZ} = \frac{2}{OSR} \left(\frac{\sigma_j}{T_c}\right)^2 \left[\frac{V_{sig}^2}{2} + \frac{\Delta^2}{12} \cdot \frac{1}{2\pi} \int_{-\pi}^{\pi} |NTF(e^{j\omega})|^2 d\omega \right]. \quad (16)$$

where σ_j is the rms jitter in the DAC sampling-clock, OSR is the oversampling ratio of the modulator, Δ is the quantization step of the loop quantizer, and NTF is the noise transfer-function of the modulator. From equation (16), the expressions for the IBJN due to input signal and shaped quantization noise can be written as follows

³ This is provided that the solution adopted to improve the DAC tolerance to clock jitter errors is not adding high power overhead and thus not increasing the total power consumption.

$$IBJN|_{RZ, \text{due to input signal}} = \frac{V_{sig}^2}{OSR} \left(\frac{\sigma_j}{T_C} \right)^2. \quad (17)$$

$$IBJN|_{RZ, \text{due to shaped noise}} = \frac{1}{OSR} \left(\frac{\sigma_j}{T_C} \right)^2 \frac{\Delta^2}{12\pi} \int_{-\pi}^{\pi} |NTF(e^{j\omega})|^2 d\omega. \quad (18)$$

From the expression in (16), it is evident that the IBJN decreases proportionally with the OSR and the duty cycle of the DAC pulse. Particularly, 1) as the OSR increases, the power spectral density (PSD) of the PWJ induced errors is reduced and hence the resulting integrated in-band noise is decreased accordingly, 2) the additive error in the amount of integrated charge in the loop filter varies linearly with the PWJ at the rise and fall edges by a factor roughly equal to the pulse amplitude (Figure 15(a)), which is inversely proportional to T_C . The IBJN due to in-band signal component, given in (17), causes sidebands of the input signal to appear in the desired band. Also, from (18), PWJ randomly modulating shaped noise results in noise folding back over the desired band and hence elevating the in-band noise level. In (16) and (18), the effect of the quantizer resolution is implicitly included in Δ^2 .

4.2. Non-Return-To-Zero DAC Waveforms

Non-return-to-zero DACs are known to be highly sensitive to excess loop delay and also they result in even-order nonlinearities due to mismatch between rise and fall times, in contrast to RZ DAC waveforms. However, they are commonly used in CT $\Delta\Sigma$ modulators due to their simple implementation, relaxed SR requirement on the integrating amplifiers, and lower sensitivity to clock-jitter compared to RZ DACs. As illustrated by Fig. 15(b), in NRZ waveforms the clock-jitter will be effective only during the clock edges at which data is changing. Equivalent error induced by clock-jitter in a NRZ waveform is given by

$$\epsilon_j(n) = \frac{\Delta A(n)}{T_s} = (y(n) - y(n-1)) \frac{\Delta t(n)}{T_s}, \quad (19)$$

where $\Delta t(n)$ is the random timing error in the clock edge of the n^{th} clock-cycle. From [7], for a single tone $V_{sig} \cdot \sin(\omega_{sig} t)$ at the input of the $\Delta\Sigma$ modulator, the total IBJN for a NRZ DAC is given by

$$\begin{aligned} IBJN|_{NRZ} &= 4 \cdot OSR \cdot BW^2 \cdot \sigma_j^2 \cdot \left[\frac{\pi^2}{2} \left(\frac{V_{sig}^2}{OSR_{sig}^2} \right) + \frac{\Delta^2 \cdot \sigma_{NTF,RMS}^2}{12} \right] \\ &\leq 2\pi^2 \frac{V_{sig}^2 \cdot BW^2 \cdot \sigma_j^2}{OSR} + \frac{OSR \cdot BW^2 \cdot \Delta^2 \cdot \sigma_{NTF,RMS}^2 \cdot \sigma_j^2}{3}. \end{aligned} \quad (20)$$

where BW is the input signal bandwidth, OSR_{sig} is the ratio of the sampling frequency to double the input signal frequency, and $\sigma_{NTF,RMS}^2 = \frac{1}{\pi} \int_{-\pi}^{\pi} [|NTF(e^{j\omega})|^2 \cdot (1 - \cos \omega)] d\omega$. Thus, the expressions for the IBJN due to input signal and shaped quantization noise can be written as follows

$$IBJN|_{NRZ, \text{due to signal}} \leq 2\pi^2 \frac{V_{sig}^2 \cdot BW^2 \cdot \sigma_f^2}{OSR}. \quad (21)$$

$$IBJN|_{NRZ, \text{due to shaped noise}} = \frac{OSR \cdot BW^2 \cdot \Delta^2 \cdot \sigma_{NTF,RMS}^2 \cdot \sigma_f^2}{3}. \quad (22)$$

From the expression in (21), the IBJN due to signal is inversely proportional with the OSR because, intuitively, as the OSR increases, less signal-related transitions will occur at the modulator output and hence less additive jitter noise will be generated. This note is applicable only to transitions at the modulator output in the frequency range of the input signal. For example, in case of DC inputs, the modulator output will exhibit limit cycles and yields discrete tones at the output spectrum [8]; however, these transitions at the output waveform are due to the shaped quantization noise and not the input signal. On the other hand, from (22), the IBJN due to shaped noise increases proportionally with the OSR because a higher OSR means more OOB shaped noise components will be modulated and fold back over the desired channel by the PN components at their respective frequencies. Therefore, the OSR needs to be optimized for better robustness to PWJ according to the contribution of each component (in-band signal and shaped noise). Also, the IBJN due to shaped noise is proportional to $\sigma_{NTF,RMS}^2$, and thus to minimize the PWJ, the aggressiveness of the NTF needs to be relaxed. This gives a trade-off between quantization noise suppression and sensitivity to PWJ and hence a compromise is needed.

4.3. Switched-Capacitor-Resistor DACs with Exponentially-Decaying Waveforms

A commonly used solution to alleviate DAC sensitivity to PWJ is the switched-capacitor-resistor (SCR) DAC with exponentially-decaying waveform, shown in Figure 16. The exponentially-decaying waveform (Figure 8) of the SCR DAC makes the amount of charge transferred to the loop per clock-cycle less dependent on the exact timing of the DAC clock-edges [4, 9].

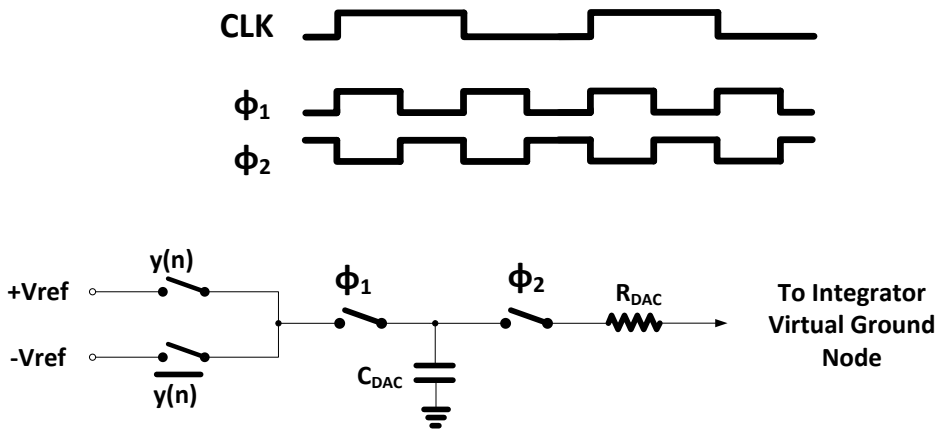


Figure 16. SCR DAC.

For a given clock-cycle n , the instantaneous exponentially-decaying current $I_n(t)$ resulting from the charge transfer is given by equation (4). Recall that the feedback value is sampled on C_{DAC} during the first clock half-cycle (when ϕ_1 is high) and then the sampled voltage is transferred to loop filter during the second clock half-cycle (when ϕ_2 is high). For a total integrated charge of $k_{DAC} \cdot y(n) \cdot T_S$ to be delivered by the SCR DAC during ϕ_1 of clock-cycle n ,

$$k_{DAC} \cdot y(n) \cdot T_S = \int_{\alpha T_S}^{\beta T_S} I_P e^{\frac{-(\beta-\alpha)T_S}{\tau}} dt = \tau I_P \left(1 - e^{\frac{-(\beta-\alpha)T_S}{\tau}}\right). \quad (23)$$

where k_{DAC} is the feedback DAC gain coefficient. Therefore,

$$I_P = \frac{k_{DAC} \cdot y(n) \cdot T_S}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_S}{\tau}}\right)}. \quad (24)$$

However, in presence of timing error $\Delta t(n)$ in the pulse-width of the discharge phase ϕ_2 in the n^{th} clock cycle, the equivalent input-referred additive error in the integrated charge is given by

$$\begin{aligned} \epsilon_j(n) &= \frac{1}{T_S} \frac{k_{DAC} \cdot y(n) \cdot T_S}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_S}{\tau}}\right)} \int_{\beta T_S}^{\beta T_S + \Delta t(n)} e^{\frac{-(t-\alpha)T_S}{\tau}} dt \\ &= \frac{k_{DAC} \cdot y(n)}{\left(1 - e^{\frac{-(\beta-\alpha)T_S}{\tau}}\right)} e^{\frac{-(\beta-\alpha)T_S}{\tau}} \left[1 - e^{-\frac{\Delta t(n)}{\tau}}\right], \end{aligned} \quad (25)$$

which for $\Delta t(n) \ll \tau$ can be approximated by

$$\epsilon_j(n) \approx \frac{k_{DAC} \cdot y(n)}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_S}{\tau}}\right)} e^{\frac{-(\beta-\alpha)T_S}{\tau}} \Delta t(n). \quad (26)$$

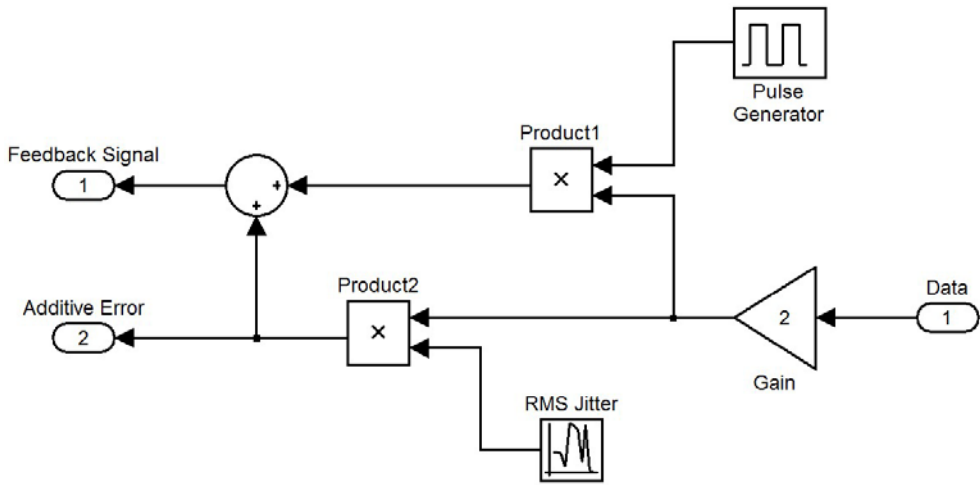
If σ_j^2 is the variance of the timing error $\Delta t(n)$, then for a single tone $V_{sig} \cdot \sin(\omega_{sig} t)$ at the input of the $\Delta\Sigma$ modulator, the power of the input-referred IBJN is given by

$$IBJN|_{SCR} = \frac{1}{OSR} \cdot \left[\frac{e^{\frac{-(\beta-\alpha)T_S}{\tau}}}{\tau \left(1 - e^{\frac{-(\beta-\alpha)T_S}{\tau}}\right)} \right]^2 \cdot \sigma_j^2 \cdot \left[\frac{V_{sig}^2}{2} + \frac{\Delta^2}{12} \cdot \frac{1}{2\pi} \int_{-\pi}^{\pi} |NTF(e^{j\omega})|^2 d\omega \right]. \quad (27)$$

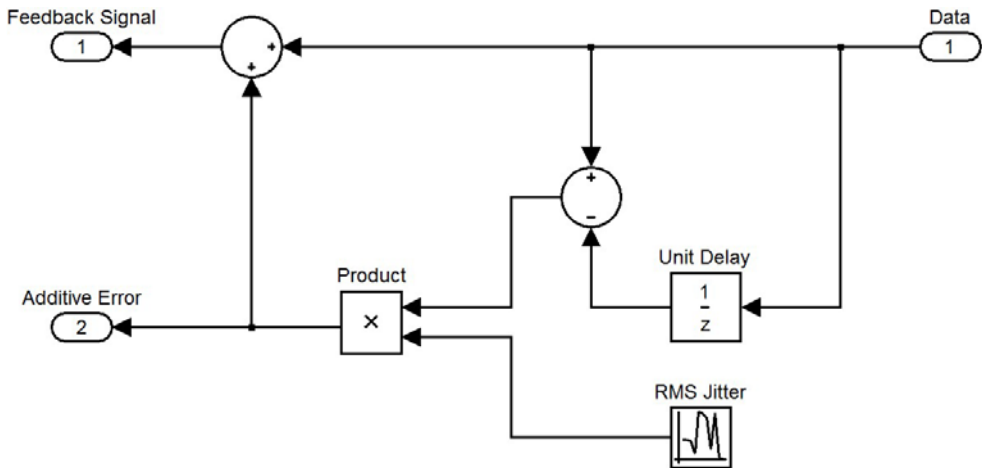
The expressions for the IBJN due to input signal and shaped quantization noise are given by

$$IBJN|_{SCR, \text{due to input signal}} = \frac{1}{OSR} \cdot \left[\frac{e^{-\frac{(\beta-\alpha)T_s}{\tau}}}{\tau \left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}}\right)} \right]^2 \cdot \sigma_j^2 \cdot \frac{V_{sig}^2}{2}. \quad (28)$$

$$IBJN|_{SCR, \text{due to shaped noise}} = \frac{1}{OSR} \cdot \left[\frac{e^{-\frac{(\beta-\alpha)T_s}{\tau}}}{\tau \left(1 - e^{-\frac{(\beta-\alpha)T_s}{\tau}}\right)} \right]^2 \cdot \sigma_j^2 \cdot \frac{\Delta^2}{12} \cdot \frac{1}{2\pi} \int_{-\pi}^{\pi} |NTF(e^{j\omega})|^2 d\omega. \quad (29)$$



(a)



(b)

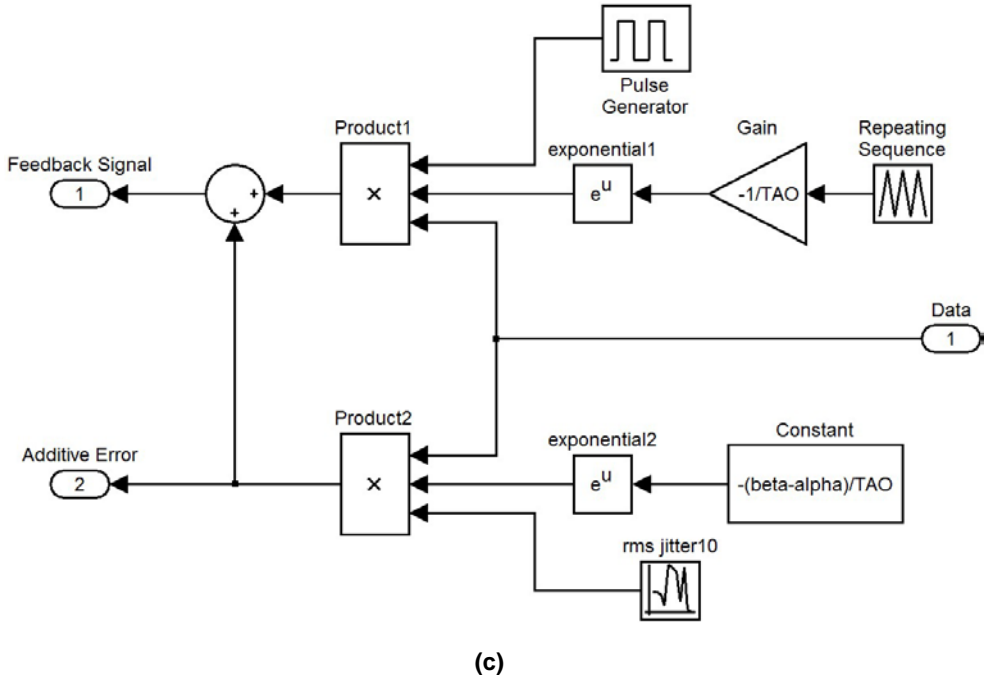


Figure 17. Simulink Modeling for DACs and jitter induced additive errors in the feedback of a CT $\Delta\Sigma$ modulator. (a) RZ DAC. (b) NRZ DAC. (c) SCR DAC.

As expected, the sensitivity of SCR DACs to PWJ, given by (32)-(34) is the same as the RZ DAC case (16)-(18) but exponentially reduced. However, the increased peak current of the SCR DAC, given by (28), adds higher requirements on the SR and the GBW of the loop filter integrator [4, 10]. Moreover, CT $\Delta\Sigma$ modulators using SCR DACs have poor inherent anti-aliasing compared to those using current-steering DACs [11] due to the loading of the SCR DAC on the integrating amplifier input nodes. The hybrid SI-SCR DAC solution in [12] provides suppression to PWJ noise equivalent to that offered by SCR DACs without adding extra requirements on the SR or GBW of the integrating amplifier.

5. Modeling and Simulation of Jitter Effects in CT $\Delta\Sigma$ Modulators Using Matlab/Simulink

In this section, Matlab/Simulink models for the jitter induced errors in different DAC types are shown. The models are based on the expressions of the additive jitter errors developed in the previous section and will be verified by simulations. Figure 17 shows the Simulink models for RZ, NRZ and SCR DACs, including the additive jitter errors based on the expressions in (15), (19), and (25), respectively. Note that these additive errors in the feedback should be multiplied by the gain coefficient of their respective feedback path. These models are examined through simulations in Matlab/Simulink to verify their accuracy and compliance with the developed analysis. The feed-forward third-order single-bit CT $\Delta\Sigma$

modulator in Figure 18 is used as a test vehicle for the system-level simulations. The modulator operates at an OSR of 100 with a target ENOB of 13 bits over a baseband channel bandwidth of 1.92 MHz for the WCDMA standard. The noise budgeting for the ADC to achieve the required ENOB is given in Table 1. Table 2 lists the specifications and summary of the achievable performance of the modulator when an SCR DAC model is used with DAC time-constant $\tau = 0.1 T_s$. Recall that an SCR DAC is a convenient option to provide robustness to clock-jitter and maintain the low percentage of the jitter induced noise in the noise budget. The dynamic-range (DR) and PSD plots of the modulator are given in Figure 19 and Figure 20. The maximum signal-to-noise-plus-distortion ratio (SNDR) is calculated as 80dB.

To examine the sensitivity of the modulator to clock-jitter for different DAC types by simulations, the appropriate model for the feedback DAC including the additive jitter errors is chosen from the ones in Figure 17, according to the adopted DAC type (RZ, NRZ, or SCR), and is added to the Simulink model of the complete modulator. The plots in Figure 21 imply that for sufficiently large rms jitter in the DAC sampling-clock, the IBJN increases significantly and dominate the total in-band noise (IBN). For the SCR DAC, it can be seen from the plots in Figure 21(c) that the robustness to clock-jitter degrades proportionally with the DAC time-constant τ , as discussed earlier in the analysis. To compare the robustness to clock-jitter in the three DAC types, IBJN plots are combined together in Figure 22, and it is evident that the SCR DAC is the most tolerant to DAC jitter while RZ DAC is the most sensitive.

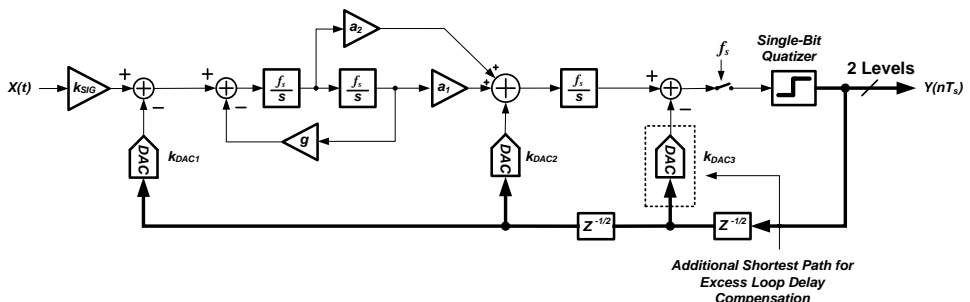


Figure 18. Adopted modified feed-forward CT single-bit $\Delta\Sigma$ modulator.

Table 1. Modulator noise budget

Noise/Distortion Source	Noise Budget	Signal-to-Noise-Ratio (SNR)
Quantization Noise	10%	90 dB
Thermal Noise	50%	83 dB
Jitter Induced Noise	10%	90 dB
Nonlinearity induced Distortion	20%	87 dB
Others	10%	90 dB

Table 2. Modulator specifications and performance summary

Property	Value
Sampling Frequency	384 MHz, <u>RMS Jitter 10 ps</u>
Signal Bandwidth	1.92 MHz
Oversampling Ratio (OSR)	100
ENOB	13
Peak SNDR	80 dB
Dynamic Range	84 dB
SFDR	83 dB

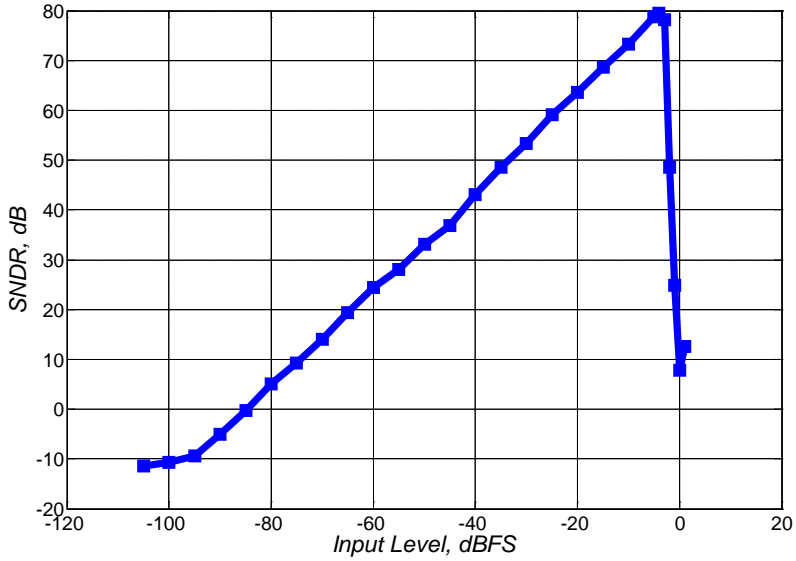


Figure 19. Dynamic-range of the adopted $\Delta\Sigma$ modulator.

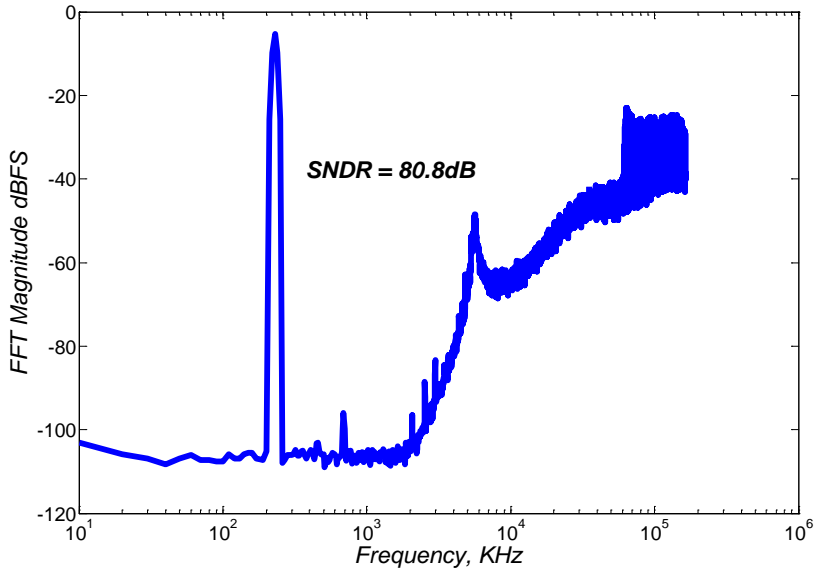
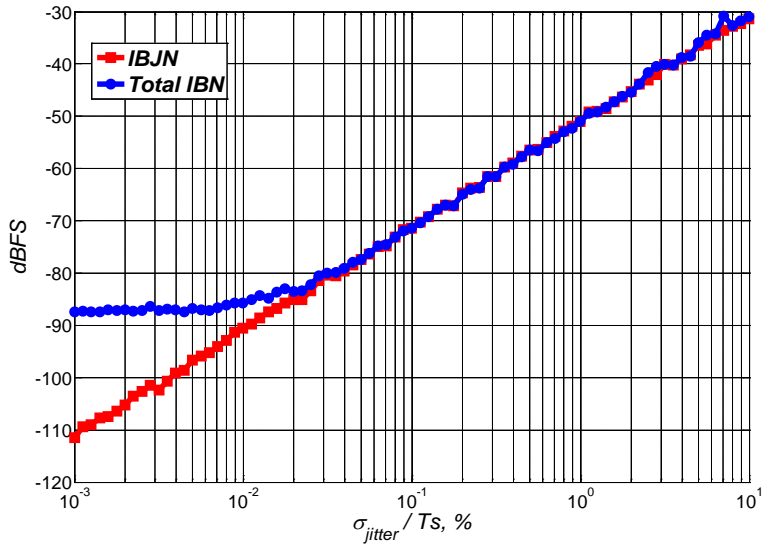
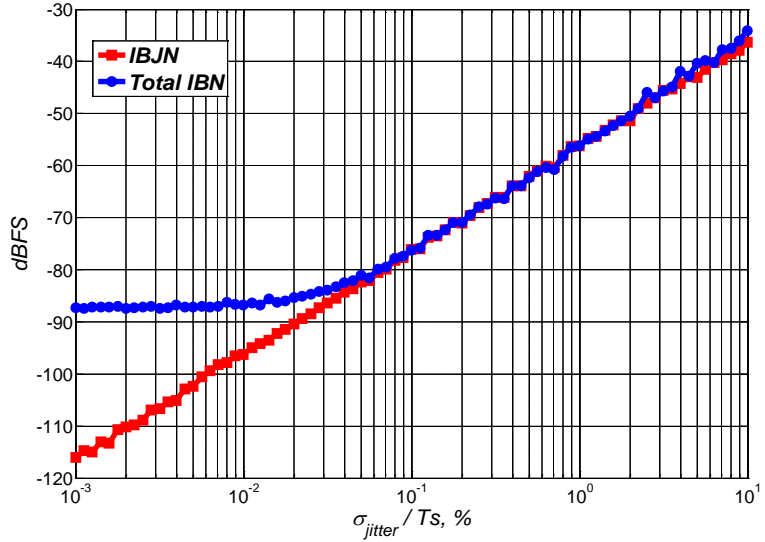


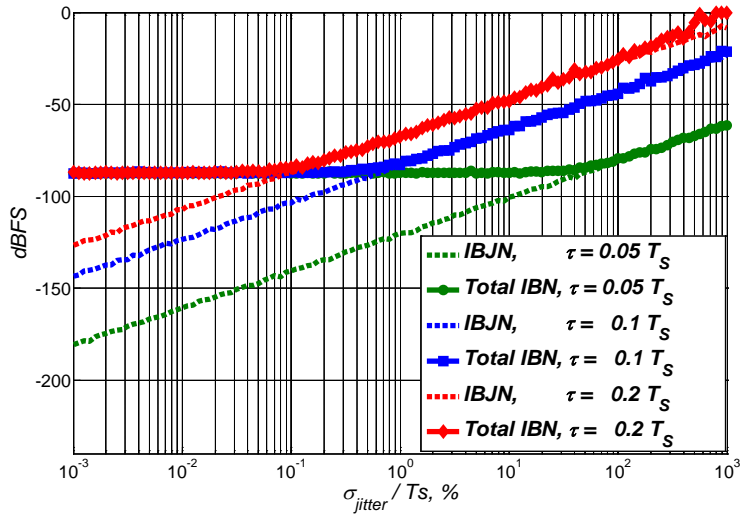
Figure 20. PSD at the modulator output calculated using 32768 FFT points with 16 averages. *Signal Amplitude* = -4 dBFS, *Signal Frequency* = 270 KHz.



(a)



(b)



(c)

Figure 21. Sensitivity plots of the $\Delta\Sigma$ modulator in Figure 18 to clock-jitter in the DAC. *Signal Amplitude = -4 dBFS, Signal Frequency = 1.9 MHz.* (a) RZ DAC. (b) NRZ DAC. (c) SCR DAC.

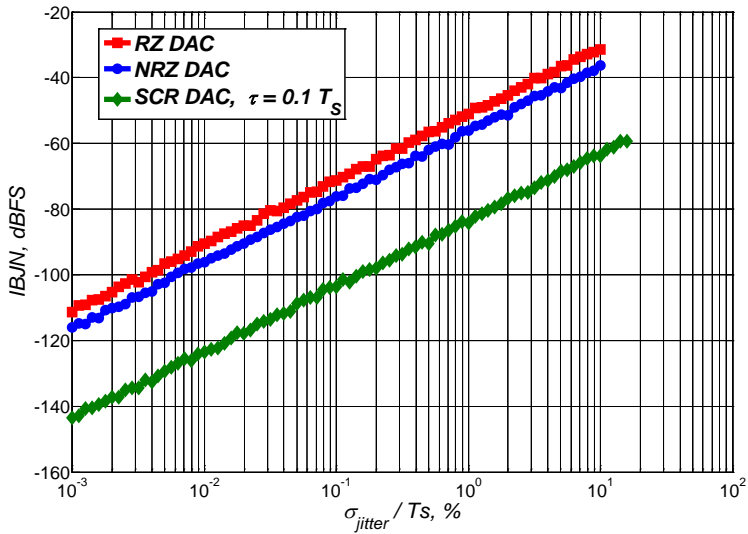


Figure 22. IBJN plots for the $\Delta\Sigma$ modulator in Figure 18 using different DAC types. *Signal Amplitude = -4 dBFS, Signal Frequency = 1.9 MHz.*

6. Conclusion

In this chapter, the effects of clock-jitter in the sampling-clocks of $\Delta\Sigma$ modulators are analyzed and studied in details. The critical sources of jitter induced errors in a $\Delta\Sigma$ loop are discussed for $\Delta\Sigma$ modulators with DT and CT loop filters. The comparison between DT and CT modulators showed that CT architectures are more sensitive to clock-jitter than DT counterparts due to PWJ in the feedback signal caused by clock-jitter in the DAC sampling-clock. In essence, PWJ in the feedback waveform entails random phase-modulation that folds back high-pass shaped noise components over the desired channel bandwidth. Thus, a detailed analysis for the sensitivities of various signal waveforms provided by different types of CT DACs to clock-jitter is given thereafter. Also, efficient Matlab/Simulink models for additive errors induced by clock-jitter in the feedback DACs are shown so that to help designers characterize the sensitivities of various types of CT $\Delta\Sigma$ architectures to clock-jitter and obtain the specification requirement on the rms jitter of the sampling-clock for a given target performance. Furthermore, these models are beneficial for system-level simulations adopted in the process of developing efficient solutions and modulator or DAC architectures that can remedy the effects of clock-jitter on the $\Delta\Sigma$ modulator performance. The robustness of these models is verified by CT simulations in Matlab/Simulink and simulations results show good agreement with the theoretical expectations.

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