Clock-Jitter-Tolerant Wideband Receivers: An Optimized Multichannel Filter-Bank Approach

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***Abstract*—Clock jitter is one of the most fundamental obstacles in realizing future generations of wideband receivers. Stringent jitter specifications in the sampling clocks of high-performance single-channel and multichannel time-interleaved analog-to-digital converters severely limit the evolution of baseband receivers. This paper presents an analytical framework for the design of clock-jitter-tolerant low-order multichannel filter-bank receivers, with techniques to dramatically lower the sampling-clock-jitter specifications. Although it is well understood that high-order frequency-channelized receivers provide higher tolerance to sampling jitter, this paper shows that low-order bandwidth-optimized multichannel receivers can achieve similar sampling-jitter tolerance. Additionally, this paper presents design tradeoffs and specifications of an example multichannel receiver that can process a 5-GHz baseband signal with 40 dB of signal-to-noise-ratio using sampling clocks that can tolerate up to 5 $\mathrm{ps_{rms}}$ clock jitter. In comparison, existing architectures based on time-interleaving require 0.5 $\mathrm{ps_{rms}}$ clock jitter for the given specifications. This extreme jitter tolerance allows for relaxed design of clocking systems, which averts a major roadblock in future wideband-communication-receiver development and provides the potential to enable several high-data-rate communication applications.**

***Index Terms*—Baseband receivers, channel bank filters, jitter.**

I. Introduction

IMAGINE the potential offered if electronic devices, such as computers, cell phones, digital cameras, MP3 players, flat panels, and external hard disks wirelessly connect to each other at speeds similar to the processing capabilities of modern computers. Although it is clear that advances in the semiconductor industry provide some of the tools for these ideas to become reality [millimeter-wave radio (mmWR) [1], [2], software-defined radio [3], [4], cognitive radio (CR) [5], [6], [54] and multistandard radio [4], [7]], there remain challenging issues that prevent wireless multichannel systems from coming to fruition. For instance, in applications such as power-spectral-density estimation for CRs [6], [8] and future mmWR standards, several gigahertz of bandwidth with high dynamic-range requirements need to be received and detected by the wireless receiver. Also, as the number of radio-frequency (RF) channels in magnetic-resonance-imaging systems massively increases to achieve very fast scan times, the bandwidth and information rate quickly reach several gigahertz [9]–[12]. Demanding wireless transmission and reception speeds impose severe challenges for the analog baseband multichannel circuits needed in these applications [57]–[63]. In particular, higher signal resolution and bandwidth impose very aggressive clock-jitter requirements in traditional parallel-path approaches, such as time-interleaved analog-to-digital converters (ADCs), resulting in prohibitively expensive complexity and power consumption in clock generation and distribution circuitry. This motivates fundamentally different receiver architectures that reduce the clock-jitter requirements of these wireless data-communication systems.

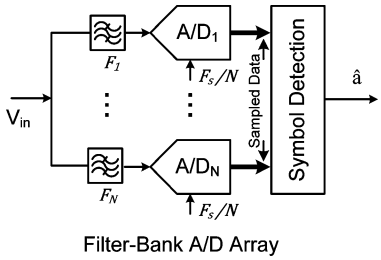

Fig. 1. Basic block diagram of a multichannel filter-bank ADC array.

Multichannel sampling concepts were first introduced in [17], and their interference-rejection capabilities among other advantages have been investigated in [18]–[21]. Fig. 1 shows a multichannel filter-bank ADC array, where the filters F_1, $F_2 \ldots F_N$ channelize the input-signal bandwidth into N bands processed by N ADCs. This architecture offers the advantages of both a lower sampling-clock frequency and, as detailed in this paper, robustness to clock jitter.

Jitter tolerance has been extensively reported in the context of multichannel serial-link communications, where the signal is digital [usually binary or 4-PAM (pulse amplitude modulation)], and the channels are independent. In this application, the tolerance to clock jitter is straightforward, but the implementation is challenging [22]–[25], [67], [68]. Clock jitter in classical communication systems has also been analyzed [26], [27]. CMOS implementations [65], [66] of high-order multichannel receivers have been reported. However, to the authors' knowledge, there is no literature showing that low-order bandwidth-optimized multichannel receivers can provide the same sampling-jitter tolerance offered by high-order channelized receivers.

This paper is organized as follows. Section II gives an overview of the state of the art in multichannel time-inter-

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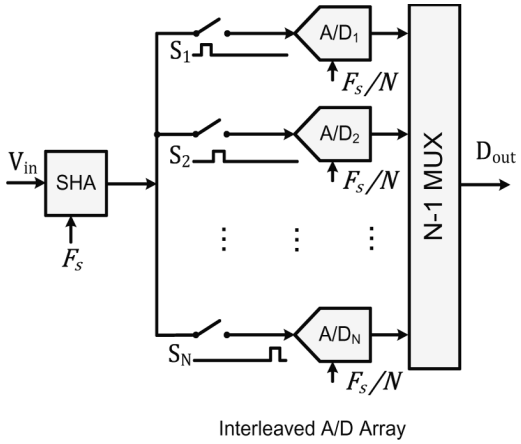

Fig. 2. Basic block diagram of a conventional time-interleaved ADC.

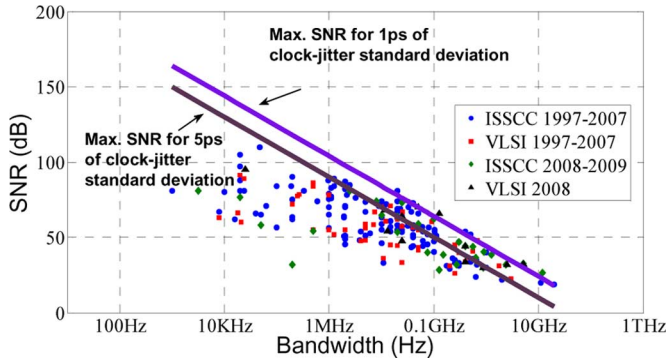

Fig. 3. SNR versus bandwidth of latest published ADCs [13].

leaved ADCs and identifies the fundamental performance limitation imposed by clock jitter. In Section III, the proposed bandwidth-optimized jitter-tolerant receiver architecture is presented, and Monte Carlo simulations are given to illustrate the potential of the proposed low-order multichannel receivers in terms of clock-jitter robustness. The receiver model and design framework are derived in Section IV. Section V presents a design example for a multichannel receiver that can process a 5-GHz baseband signal with 40 dB of signal-to-noise-ratio (SNR) with sampling clocks that can tolerate up to 5-ps$_{\rm rms}$ clock jitter. Finally, conclusions are drawn in Section VI.

II. Rationale and Background

A receiver chain can be split into three main parts: the RF front end, the analog baseband, and the digital baseband. The ADC provides the interface between the analog and digital basebands. Parallelization in the design of receivers has been conventionally realized using sampling multiplexing through the time-interleaved ADC architecture. Fig. 2 shows 1-to-N analog multiplexing scheme where N switches are clocked by N uniformly spaced clock phases. Each clock is running N times slower than the Nyquist rate, which relaxes the sampling rate of the N parallel ADCs but still requires a front-end sample-and-hold amplifier (SHA) sampling at full Nyquist rate (F_s).

A. State-of-the-Art Conventional Multichannel ADCs: Time-Interleaved ADC

Fig. 3 shows the SNR versus bandwidth performance of some of the latest reported single-channel and time-interleaved ADCs [13], [37]–[53]. The figure shows also a line with the theoretical maximum achievable SNR for 1 and 5 ps of clock-jitter standard deviation in the SHA. The plot shows that clock jitter has become an impediment in the design of practical high-performance ADCs, with implementations demanding better than 1 ps rms jitter. This translates into high-power consumption in the clock-generation circuits as well as significant silicon area. ADCs operating with subpicosecond clock jitter are often demonstrated using cutting-edge bulky equipment and in stand-alone configurations to avoid interference from adjacent devices. This setup is not practical in many portable applications, which require high levels of integration and miniaturization. The lack of robustness to jitter in the sampling clocks of time-interleaved ADCs has become a critical problem for parallel-channel ADCs that are envisioned to support future generations of wideband systems [14].

B. Fundamental Limitation: Clock Jitter

The fundamental clock-jitter limitation can be understood and quantified by a well-known equation in the field of data converters. If an ADC is sampling a sinusoidal signal of amplitude A at full Nyquist rate ($F_s = 2B$), a sampling-clock jitter of variance σ_j^2 introduces an equivalent additive noise of variance $\sigma_j^2 = (\sqrt{2}\pi BA\sigma_j)^2$ [15]. Therefore, the signal quality degrades quadratically with the signal frequency. This leads to very stringent requirements on the clock jitter for the next generation of signal bandwidths and resolutions. For instance, consider a baseband signal bandwidth of $B = 5$ GHz and $b = 7$ bits of resolution, which, using the fundamental data-converter relationship SNR $= 6.02b + 1.76$ dB [16], is equivalent to an SNR requirement of around 44 dB. The SNR dependence on the clock jitter can be written directly as SNR $= 1/(2\pi B\sigma_j)^2$. Solving for σ_j, we obtain 201 fs $(201 \times 10^{-15}$ s). Note that this is also an issue in medium-bandwidth high-resolution applications, with the same jitter specification obtained for $B = 50$ MHz and SNR $= 84$ dB ($b \sim 14$ bits of resolution). Such a jitter standard-deviation requirement, if not impossible to achieve in many circuit technologies, will greatly increase area and power consumption of the phase-locked-loop (PLL) circuit and buffers that generate and drive the sampling clocks. It is important to note that the aforementioned simple clock-jitter requirement analysis is valid only for a single-tone signal[1] that drives any Nyquist-rate ADC [16]. Although the sampling clocks of a time-interleaved ADC run at a fraction of the Nyquist-rate frequency, every channel still produces jitter-induced noise from sampling the full input-signal bandwidth. Therefore, although the sampling rate in each channel of a time-interleaved ADC is relaxed by the number of channels, the jitter requirement is the same as in a single-channel ADC. This issue has become one of the fundamental obstacles preventing advances in wideband data-communication receivers.

[1]The clock-jitter requirement for a multitone signal is less stringent because the energy is not concentrated at the maximum frequency $Fs/2$ but distributed in the whole bandwidth B.

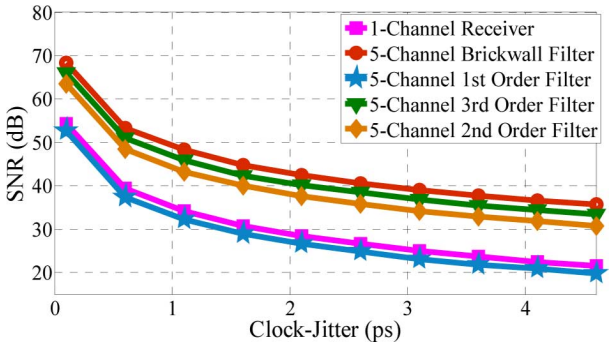

Fig. 4. SNR versus clock-jitter standard deviation for uniformly channelized first-, second-, and third-order and brickwall filter banks. Input signal is OFDM with $S = 128$ and $B = 5$ GHz.

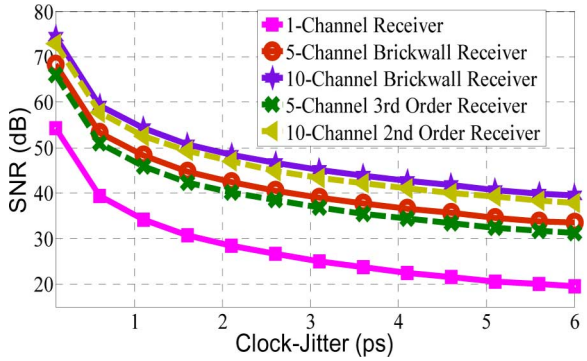

Fig. 5. Clock-jitter relaxation of bandwidth-optimized multichannel approach for an OFDM input signal with $S = 128$ and $B = 5$ GHz.

III. Optimal Jitter-Tolerant Multichannel Receiver

This section develops an analysis in the context of orthogonal-frequency-division-multiplexing (OFDM) [28]–[34] signals, which are the preferred signaling scheme of wideband standards such as ultrawideband and 60-GHz ECMA-387. Clock jitter in conventional single-channel OFDM systems has been analyzed in [27], which provide a foundation that will be adopted for the evaluation and comparison of the results obtained from this analysis. In order to motivate the analytical framework derived in Section IV, this section provides a heuristic discussion of the key results.

Consider again the general N-channel receiver structure in Fig. 1. The filters F_1, $F_2 \ldots F_N$ channelize the input-signal bandwidth into N bands. For an ideal "brickwall" type of filter, the signal bandwidth in each channel is reduced N times, leading to an additive-noise variance that can be obtained directly from the elementary equation $\sigma_n^2 = (\sqrt{2}\pi\sigma_j BA/N)^2$, which is N^2 times lower than the one for a time-interleaved ADC. However, filters with finite rolloffs do not provide perfect channel separation, leaving attenuated out-of-band signal at each channel. Thus, the jitter-induced noise is not only a function of the in-band signal but also of the aliased-attenuated out-of-band signal. This has been considered a serious drawback of filter banks in the data-conversion community. Indeed, as Fig. 4 shows, if a signal is uniformly channelized with N first-order filters, each with bandwidth B/N, the effect of clock jitter is worse than if a single channel or time-interleaved ADC is used.

An OFDM signal with $S = 128$ carriers and bandwidth $B = 5$ GHz is used to examine the multichannel architecture's jitter tolerance. Fig. 5 shows Monte Carlo simulation results which show the symbol-detection SNR at the output of the receiver versus the clock-jitter standard deviation for the conventional one-channel OFDM receiver and multichannel receiver topology with $N = 5$ and $N = 10$ channels. Note that in both Figs. 4 and 5, the filters' bandwidth has been optimized using the analytical tools developed in this paper to obtain the best possible clock-jitter robustness, as explained in Section IV. Fig. 5 shows that the ideal ten-channel brickwall-filter approach offers a 20-dB SNR enhancement, and a practical second-order multichannel receiver performs very close to the ideal curve. The plot also reveals that in order to achieve 7 bits of resolution (44 dB), the conventional OFDM receiver, based on a time-interleaved ADC or some other single-channel conventional ADC, requires a 0.345-ps clock jitter,[2] whereas the five-channel-receiver approach can tolerate 1.36 ps of clock-jitter standard deviation. Moreover, a ten-channel receiver can tolerate 3.5 ps. Additionally, the plot reveals that if an SNR of 40 dB is sufficient, the ten-channel-receiver approach can tolerate up to 5 ps of standard deviation, whereas the single-channel counterpart needs roughly 0.5 ps, a 10X improvement in clock-jitter tolerance. This degree of clock-jitter tolerance has the potential to enable wireless high-speed data-communication applications that are very difficult to achieve with conventional single-channel and time-interleaved topologies. Section IV makes a formal theoretical derivation of the results stated here and provides the analytical tools for the systematic design of multichannel filter-bank receivers.

IV. Receiver Analysis

Two figures of merit fully characterize and provide the basic analytical tools to understand the tolerance to clock jitter of the multichannel receiver: the sampled-data SNR, $\text{SNR}_{\text{sampled}}$, and the symbol-detection SNR. The sampled-data SNR measures the data quality at the output of the samplers right before the digital baseband. The symbol-detection SNR measures the data quality after the digital baseband. Both SNRs will be obtained in the context of OFDM signals with emphasis on their dependence on the number of channels N, which is the fundamental design parameter of the proposed receiver.

A. Analytical Derivation of the Sampled-Data SNR

Fig. 6 shows the basic block diagram used for modeling the OFDM signal transmission and reception. To facilitate the analysis, the model is introduced with a matrix notation. The transmitted signal is given by

$$\mathbf{x} = \mathbf{\Psi a} \tag{1}$$

where $\mathbf{a} = [a_1, a_2, \ldots, a_S]^{\mathbf{T}}$ and $\mathbf{\Psi} = [\Psi_1, \Psi_2, \ldots \Psi_S]$. This model is valid for any arbitrary transmitter that simultaneously processes S symbols. In the particular and important case of OFDM, the matrix $\mathbf{\Psi}$ is the set of complex exponential functions that represent the inverse discrete Fourier transform operation

[2]Note once again that this clock-jitter requirement is less stringent than the one for a single tone signal (201 ps).

with N points of an OFDM transmitter. The received signal is given by

$$\mathbf{r} = \mathbf{x} + \mathbf{n}_1 \tag{2}$$

where $\mathbf{n_1}$ is the noise added during the transmission. Consider an OFDM signal composed of M sinusoidal signals: $x(t) = \sum_{m=1}^{M} A_m \sin(m\Delta\omega t)$, where A_m is the symbol of the mth tone and $\Delta\omega$ is the tone-frequency spacing, which is equal to B/M. This signal is sampled at instances $tn = nT_s + \delta t$ by clocks of frequency $F_s = 1/T_s$ and clock jitter δt with variance σ_j^2. The clock jitter δt can be generally modeled as zero-mean Gaussian for a regular clock generator, such as a PLL in a locked steady state. Additionally, the clock phase noise can have some spectral shape around the clock frequency, usually referred as close-in skirts [64]. This phase noise can be modeled as $1/f^n$ decaying function and produces spectral shaping similar to the skirt shape and broadening of the analog signals [55], [64]. This, in turn, can produce overlapping among the OFDM carriers and between the OFDM signal and nearby interferers. As a practical design rule, the energy of the spectral overlapping must be $\sim$ 4–6 dB lower than the flat noise floor in order for the phase-noise skirts impact to be negligible in comparison with the flat wideband noise. This important specification has to be satisfied in the design of any sampling clock. Under this practical scenario, the Gaussian white-noise model is sufficient [56], [64]. The uncertainty produced by the clock jitter on the OFDM signal can be expressed as

$$x(t) = \sum_{m=1}^{M} A_m \left[\sin(m\Delta\omega t)\cos(m\Delta\omega\delta t) + \cos(m\Delta\omega t)\sin(m\Delta\omega\delta t)\right] \tag{3}$$

which, for a small δt, can be approximated as

$$x(t) \cong \sum_{m=1}^{M} A_m \sin(m\Delta\omega t) + \sum_{m=1}^{M} m\Delta\omega\delta t A_m \cos(m\Delta\omega t). \tag{4}$$

The error produced by the clock jitter is approximately given by

$$\varepsilon(t) = x(t) - \sum_{m=1}^{M} A_m \sin(m\Delta\omega n T_s) \cong \sum_{m=1}^{M} m\Delta\omega\delta t A_m \cos(m\Delta\omega t). \tag{5}$$

The variance of this additive error can be expressed as

$$\sigma_n^2 = \overline{\varepsilon^2(t)} = \overline{\delta t^2}\frac{\Delta\omega}{2\pi}\int_0^{\frac{2\pi}{\Delta\omega}} \left[\sum_{m=1}^{M} m\Delta\omega A_m \cos(m\Delta\omega t)\right]^2 dt \tag{6}$$

which, owing to the orthogonal nature of the OFDM signal, can be rewritten as

$$\sigma_n^2 = \sigma_j^2 \frac{\Delta\omega}{2\pi}\sum_{m=1}^{M}\int_0^{\frac{2\pi}{\Delta\omega}} [m\Delta\omega A_m \cos(m\Delta\omega t)]^2 dt, \text{ where}$$

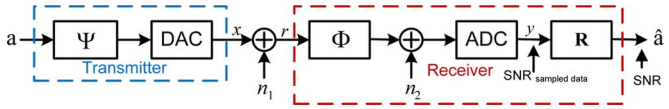

Fig. 6. Block diagram that models the transmitter and multichannel receiver, including noise sources, such as the clock jitter.

$\sigma_j^2 = \overline{\delta t}^2$. This expression simplifies to

$$\sigma_n^2 = \sigma_j^2 \sum_{m=1}^{M} \frac{m^2\Delta\omega^2 A_m^2}{2} = \frac{1}{2}\sigma_j^2\Delta\omega^2 \sum_{m=1}^{M} m^2 A_m^2. \tag{7}$$

Please note that the OFDM carriers remain orthogonal as long as the communication channel and the receiver remain linear. The linearity specification is set by the standard bit-error-rate requirement and is a necessary condition for any receiver to operate properly, unless nonlinear postcalibration techniques are used to correct for the nonlinearities. Since this topic is out of the scope of this paper, we assume that the receiver is linear. The $\text{SNR}_{\text{sampled data}}$ is found to be given by

$$\text{SNR}_{\text{sampled data}} = \sum_{m=1}^{M}\frac{A_m^2}{2} \Bigg/ \left[\frac{\sigma_j^2\Delta\omega^2}{2}\sum_{m=1}^{M} m^2 A_m^2\right] = \sum_{m=1}^{M} A_m^2 \Bigg/ \left[\sigma_j^2\Delta\omega^2 \sum_{m=1}^{M} m^2 A_m^2\right]. \tag{8}$$

Assuming $A_m = A$ for $m = 1, \ldots M$, the sampled-data SNR final expression is

$$\text{SNR}_{\text{sampled data}} = \frac{M}{\sigma_j^2\Delta\omega^2 \sum_{m=1}^{M} m^2}. \tag{9}$$

Therefore, the sampled-data SNR is inversely proportional to the clock-jitter variance, the squared value of the OFDM frequency spacing, and the term $\sum_{m=1}^{M} m^2$. This last term is critical in the performance enhancement of the multichannel receiver. For instance, consider a four-channel system using ideal brickwall type of filters. The original OFDM signal has 128 tones that are split with a bank of four filters into four channels with 32 tones each; defining SNR_{128} and SNR_{32} as the $\text{SNR}_{\text{sampled}}$ for the original signal and four-channel signal, the SNR enhancement of the multichannel approach is given by

$$\begin{aligned}\text{SNR}_{\text{Enhancement}} &= \text{SNR}_{32} - \text{SNR}_{128} \\ &= 10\log\left(\frac{32}{128}\right) - 10\log\left(\frac{\sum_{m=1}^{32} m^2}{\sum_{m=1}^{128} m^2}\right) \\ &\approx 12\text{ dB}.\end{aligned} \tag{10}$$

Fig. 7 shows this SNR enhancement for several numbers of channels. In principle, this enhancement can only be obtained if the OFDM tones are separated perfectly by brickwall filters. As real filters with finite rolloffs do not offer perfect channel separation, the architecture becomes sensitive to aliasing of out-of-band tones. The following analysis shows that optimized

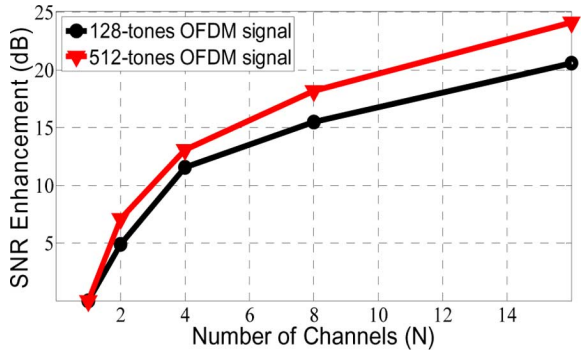

Fig. 7. Sampled data SNR enhancement of multichannel-receiver approach versus the number of brickwall-filter channels.

second-, and even first-order, filters are effective in providing tolerance to sampling-clock jitter.

B. Analytical Derivation of the Symbol-Detection SNR

Without loss of generality, the receiver diagram in Fig. 6 only models the analog and digital baseband processing. The matrix Φ represents the analog filter-bank transformation. For N channels, Φ will have N columns, one per channel. The number of rows of Φ corresponds to the number of samples per channel that the ADC takes for one block of S symbols a. The sampling rate should comply with the Nyquist sampling theory, i.e., the number of samples should be not less than S. The receiver can be represented by the following linear transformation:

$$\mathbf{y} = \mathbf{\Phi r} + \mathbf{n_2} = \mathbf{\Phi}(\mathbf{\Psi a} + \mathbf{n_1}) + \mathbf{n_2} \tag{11}$$

where $\mathbf{n_2}$ is the noise during sampling. Note that the effects of clock jitter from (7) are included in $\mathbf{n_1}$ and $\mathbf{n_2}$, and therefore, the digital-to-analog converter/ADC in the diagram are ideal. For brevity, (11) is rewritten as

$$\mathbf{y} = \mathbf{Ga} + \mathbf{n} \tag{12}$$

where $\mathbf{G} = \mathbf{\Phi\Psi}$ and $\mathbf{n} = \mathbf{\Phi n_1} + \mathbf{n_2}$.

This is an overdetermined system, and the least square (LS) estimation[3] [35], [36] of $\mathbf{a}$ is given by

$$\hat{\mathbf{a}} = \mathbf{Ry} = \mathbf{a} + \mathbf{Rn} \tag{13}$$

where $\mathbf{R} = \mathbf{G}^{\dagger} = (\mathbf{G}^H\mathbf{G})^{-1}\mathbf{G}^H$. The matrices $\mathbf{G}$ and $\mathbf{R}$ are the *Generation Matrix* and *Symbol-Detection Matrix*, respectively. Depending on the receiver's architecture, $\mathbf{G}$ and $\mathbf{R}$ vary, which result in different amplification of the noise $\mathbf{n}$ as shown in the following:

$$\begin{aligned} E\left[\|\mathbf{Rn}\|^2\right] &= E\left[\mathbf{n}^H\mathbf{R}^H\mathbf{Rn}\right] \\ &= E\left[\mathbf{n}^H\mathbf{Q}^H\Lambda\mathbf{Qn}\right] \\ &= E\left[\left(\sum_{i=1}^{S}\lambda_i n_i^*\mathbf{q}_i^H\right)\left(\sum_{j=1}^{S} n_j\mathbf{q}_j\right)\right] \\ &= E\left[\sum_{i=1}^{S}\sum_{j=1}^{S}\lambda_i n_i^* n_j \mathbf{q}_i^H\mathbf{q}_j\right] \\ &= \sum_{i=1}^{S}\sum_{j=1}^{S}\lambda_i E\left(n_i^* n_j\right)\mathbf{q}_i^H\mathbf{q}_j \\ &= \sum_{i=1}^{S}\lambda_i E\left(n_i^* n_i\right)\mathbf{q}_i^H\mathbf{q}_i \\ &= \sum_{i=1}^{S}\lambda_i E\left(\|n_i\|^2\right) \end{aligned} \tag{14}$$

where $\mathbf{Q} = [\mathbf{q_1^T}, \mathbf{q_2^T}, \ldots, \mathbf{q_S^T}]$ and $\mathbf{q_i^T}$ is the eigenvector of $\mathbf{R^H R}$ corresponding to the eigenvalue λi [36], i.e., the singular value of $\mathbf{R}$, and $\mathbf{Q^H Q} = \mathbf{I}$. Assuming that the noise is Gaussian with zero mean and variance σ_n^2, then

$$E[\|\mathbf{Rn}\|^2] = \sigma_n^2 \sum_{i=1}^{s}\lambda_i. \tag{15}$$

Therefore, the noise amplification of different multichannel receiver architecture is determined by the singular values of the reconstruction matrix $\mathbf{R}$. In the mutichannel architecture proposed here, the type of filters will change $\mathbf{G}$, which in turn changes $\mathbf{R}$, leading to a different digital and analog receiver structure.

Now, replacing σ_n^2 by the expression in (7), the SNR of the detected symbols can be expressed as

$$\text{SNR} = \frac{\|\mathbf{a}\|^2}{\frac{1}{2}\sigma_j^2\Delta\omega^2 \sum\limits_{m=1}^{M} m^2 A_m^2 \sum\limits_{i=1}^{S}\lambda_i}. \tag{16}$$

The Monte Carlo simulations shown in Fig. 4 illustrate this important result as was previously discussed. An additional design specification that is highly relaxed in the multichannel approach is the SNR to variations in the clock jitter. Fig. 5 shows that for SNR $= 40$ dB, the single-channel approach has an SNR sensitivity of -20 dB/ps, whereas the ten-channel approach has -2 dB/ps. This order-of-magnitude lower sensitivity to clock-jitter variations provides robustness to episodic clock-jitter spikes produced by interference or other unpredictable events.

The simulations shown in Fig. 8 for the same setup of Fig. 5 (an OFDM signal with $S = 128$ carriers and bandwidth $B = 5$ GHz) for a ten-channel receiver indicate that the filter's cutoff frequency can be optimized for first- and second-order filters but not for a third-order filter. The figure shows that the second-order receivers have an optimal SNR point at around 300 MHz. In addition to the higher clock-jitter tolerance, reducing the bandwidth in the first-order filters lowers the power consumption and circuit complexity.

The potential of low-order filters for obtaining clock-jitter robustness through bandwidth optimization can be intuitively explained by the following, and a rigorous mathematical proof is provided in the Appendix. The clock-jitter tolerance is primarily due to the attenuation of the high-frequency signal components which are beyond the channel band of interest ($|f| > B/2N$). Reducing the cutoff frequency of the filter, which is originally

[3]The minimum mean-squared error (mmse) solution is the optimal estimate of the data in the mean-squared error sense. The mmse can provide considerable improvements over the LS solution in the low-SNR regime, particularly if the noise is correlated. In the high-SNR regime both solutions offer similar performances.

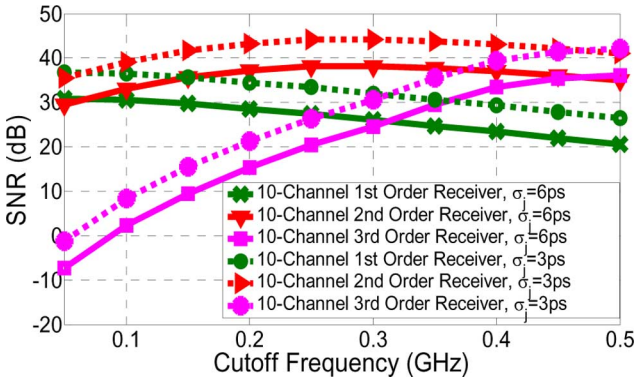

Fig. 8. Symbol-detection SNR versus cutoff frequency parameterized by the filter's order and the clock-jitter standard deviation (σ_j). Input signal is OFDM input signal with $S = 128$ and $B = 5$ GHz.

$(B/2N)$, implies higher attenuation for the signal components of frequency $|f| > B = 2N$, which translates into lower out-of-band convolution of the phase noise and signal which in turn implies lower aliasing after sampling. However, it also means that the signal components within the band of interest will be subjected to some attenuation since the cutoff frequency is less than $B/2N$. The reconstruction scheme (13) compensates for the in-band signal loss (gain and phase errors) that occurs due to reduction of the filter cutoff frequency. Even though the reconstruction scheme can correct the signal loss, there will be a limit after which the reconstruction performance degrades due to the high in-band signal loss. This sets an optimum cutoff frequency that has a maximum SNR. Reducing the cutoff frequency beyond this optimum point for second-order filters reduces the SNR, as is shown in Fig. 8. Moreover, the figure shows that when the first-order-filter cutoff frequency is reduced, the performance of the multichannel receiver gets better because the data construction is able to correct for the signal errors. When it comes to the case of the third-order filter, it is found that the optimum point is the original filter bandwidth $B/2N$.

This analytical derivation also represents a valuable design tool for these receivers because it saves long simulations times. For instance, the Monte Carlo simulation in Fig. 5 took four days using Matlab in a PC with a 2.13-GHz Pentium processor to obtain the SNR for clock jitters lower than 1 ps. It could take several more days if a circuit simulator like Spice were to be used to obtain the clock-jitter specifications. The lack of analytical tools has made the area of multichannel receiver poorly understood and its design noticeably cumbersome.

V. Receiver-Circuit Implementation Example

This section summarizes some implementation considerations and specifications in multichannel receivers suitable for a baseband OFDM input signal with 5 GHz of bandwidth and containing 128 tones. Fig. 9 shows the block diagram of a multichannel receiver with 5 I&Q parallel channels, an aggregated sampling rate of 10 GS/s, and 40 dB of resolution.

The signal is complex-valued and baseband, and therefore, I&Q processing is used. If a time-interleaved ADC topology is used to achieve these specifications, Fig. 5 shows that the clock-jitter standard-deviation requirement for a 128-tone signal is 0.5 ps, which entails prohibitively high power consumption. On the other hand, the multichannel system relaxes the standard deviation requirement to 2 ps, which greatly simplifies the sampling-clock generation, routing, and driving circuitry. Additionally, a ten-channel receiver would further relax the standard-deviation requirement to 5 ps.

A. Power Consumption and Area Overhead

The implementation of N filters for the multichannel approach instead of just one, as in a conventional time-interleaved ADC, may initially give the impression that this will result in extra power consumption and area overhead. The reality is that the power consumption of N filters of bandwidth B/N is either the same or lower than the power consumption of one filter with bandwidth B of the same order. This can be explained by realizing that in order to reduce the bandwidth by N times but maintain the dc gain, the filter's transconductance $G_m = \sqrt{KI_{\rm bias}W/L}$ needs to be reduced N times as well, which can be accomplished by lowering N times both the transistor width W and the bias current $I_{\rm bias}$. Since N filters are needed to cover the bandwidth B, then the total bias current and active-device area will, in principle, remain the same. Moreover, additional power savings can be achieved by lowering the bias current $I_{\rm bias}$ more than the width W. Thus, the N-channel approach offers an extra degree of flexibility that can be exploited to reduce the power consumption. Additionally, the resistor R_f needs to be increased N times to keep the gain constant. However, the passive-device area is smaller than the active-device area in the gigahertz-bandwidth domain addressed in this paper. In any case, this extra passive-device area and the additional routing will most likely introduce an overhead. This area overhead is not a critical drawback, and it is justified by the critical savings in the clock generation, routing, and driving circuits. There are other circuit-design considerations, including the rest of the circuit devices (for example, bypass capacitors, compensation capacitors, resistors, etc.) and the additional separation between filters for isolation purposes.

More importantly, as the bandwidth and dynamic-range requirements continue to increase for future systems, the proposed scheme provides a scalable solution, whereas conventional time-interleaved ADCs will soon not be feasible because of the prohibitive clock-jitter specifications.

B. Clock Generation

The multichannel receiver is achieved with low-complexity clock generation, as it requires a clock at 4 GHz (see Fig. 9). A simple divide-by-two circuit generates the 2-GHz clock for the second set of mixers and for the ADC sampling clocks. Note that if a front-end SHA is used in a time-interleaved architecture (see Fig. 1), it requires a 10-GHz sampling clock. In the proposed receiver, the middle channel is already centered at dc (0 Hz) and does not require frequency translation, although a dummy mixer is included for matching purposes. Simulations in Fig. 11 show that the effect of jitter on the local-oscillator (LO) clocks is less than the effect of clock jitter in the sampling clocks.

The nature of jitter in both cases have a completely different representation. In the case of the LOs, the jitter multiplies the input signal, which produces convolution in the frequency

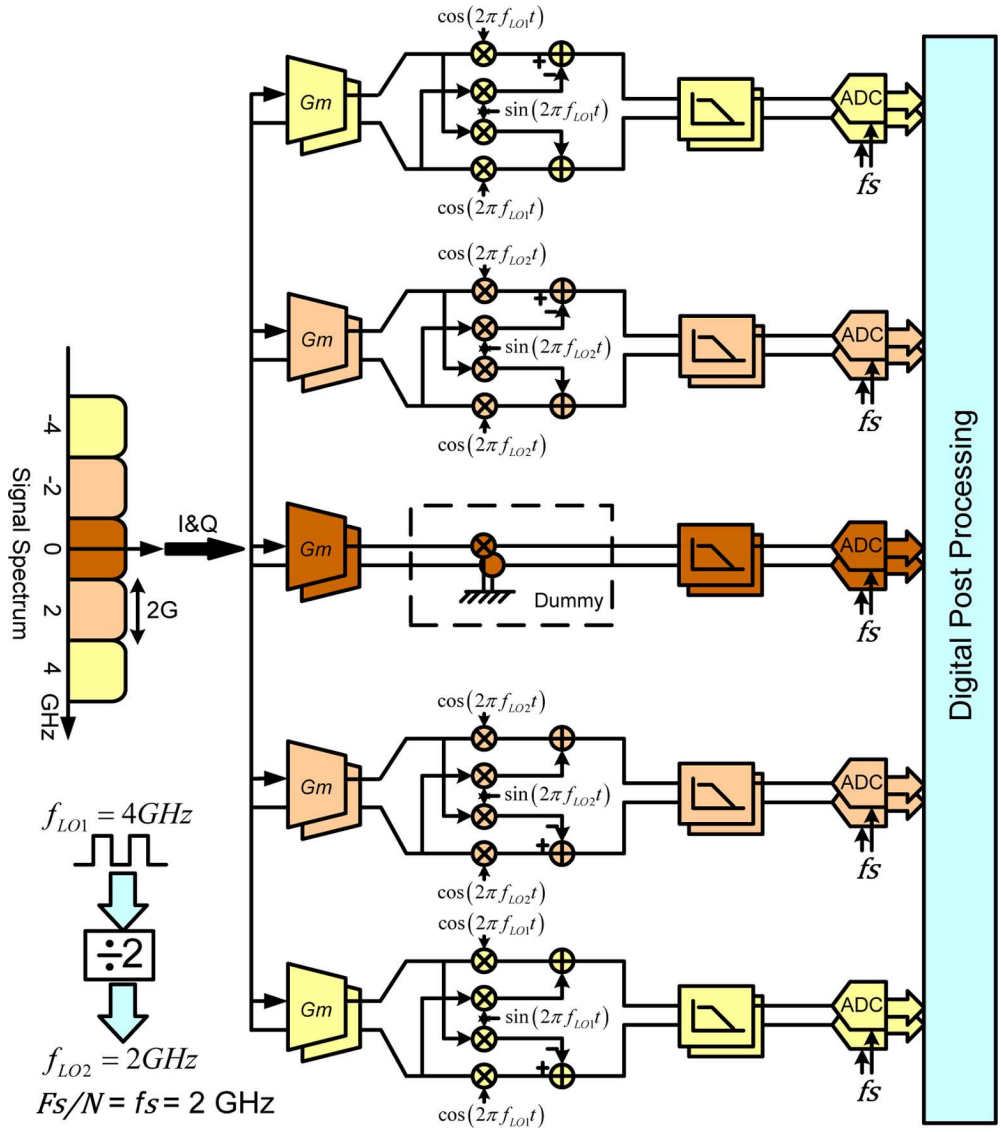

Fig. 9. Block diagram of a 5 I&Q multichannel receiver for processing a 5-GHz complex baseband signal.

domain. On the other hand, the jitter in the sampling clocks produces aliasing of high-frequency components contaminated with the noise produced by the clock-jitter itself. The filters limit the signal bandwidth, and the bandwidth optimization reduces the impact of this effect.

Thus, all the clocks will have very relaxed clock-jitter specifications as discussed throughout this paper. For the adopted receiver, a simple frequency divider by two is needed. This is an evidence of the low overhead in the extra LOs needed in the proposed approach.

C. Total Integrated Noise Added by N Filters

Another issue that could appear as a drawback of the multichannel scheme is the noise added by the N filters which, in principle, could degrade the overall receiver performance.

Fig. 10 shows a typical first-order filter based on a continuous-time lossy integrator. The output is at node Y, which drives the input of the following ADC. Assuming that the operational amplifier (Op-Amp) provides a perfect virtual ground at node X, the voltage at output node Y is equivalent to the voltage across the capacitor C. The transfer function of the filter $H(f)$ is

$$H(f) = \frac{GmR_f}{1 + j2\pi f R_f C}. \tag{17}$$

The noise generated by the Gm stage is modeled as the input reference noise $\overline{V_{n1}^2} = 4kt/Gm$. The total integrated noise introduced by $\overline{V_{n1}^2}$ at the output node Y is V_{Y1}^2

$$V_{Y1}^2 = \int_0^\infty \frac{4kt}{Gm}|H(f)|^2 df = \frac{kT}{C}GmR_f. \tag{18}$$

The noise current $\overline{I_n^2} = 4kt/R_f$ is generated by the resistor R_f. The total integrated noise introduced by $\overline{I_n^2}$ at the output node Y is V_{Y2}^2

$$V_{Y2}^2 \int_0^\infty \frac{4kT}{R_f}\left|\frac{R_f}{1 + j2\pi f R_f C}\right|^2 df = \frac{kT}{C}. \tag{19}$$

Loading at node Y needs to be introduced for exploring the impact of noise generated by the Op-Amp. Assume R_o and C_L represent the impedance that loads the Op-Amp. C_L is usually the sampling capacitor of the following ADC. The noise generated by the Op-Amp is modeled as the input reference noise voltage $\overline{V_n^2} = 4kt/gm$, where gm is the transconductance of the Op-Amp. The open-loop gain is

$$A(f) = \frac{gmR_0}{1 + sR_0C_L}. \tag{20}$$

Let $A_C(f)$ be the closed-loop noise transfer function from $\overline{V_{n2}^2}$ to the output

$$A_C(f) = \frac{A(f)}{1 + A(f)} = \frac{gmR_0}{1 + sR_0C_L + gmR_0}. \tag{21}$$

The introduced total integrated noise V_{Y3}^2 is

$$V_{Y3}^2 = \int_0^\infty \frac{4kT}{gm}|A_C(f)|^2 df = \frac{kT}{C_L}. \tag{22}$$

The overall integrated noise that goes into the ADC is $V_{n,\text{sampled}}^2$

$$V_{n,\text{sampled}}^2 = V_{Y1}^2 + V_{Y2}^2 + V_{Y3}^2 = \frac{kT}{C}(GmR_f + 1) + \frac{kT}{C_L}. \tag{23}$$

It shows that the N-channel approach offers an extra degree of flexibility that allows lowering either the noise at the filter output or the power consumption when the single filter is replaced by N filters with N times less bandwidth. Assuming that $C = C_L$, the total integrated noise at the output of each filter can be expressed as $\eta KT/C$, where η is a factor that depends on the amplifier topology. Then, the only way to lower the noise is by increasing the capacitance C. If the capacitance is increased N times while leaving fixed the open-loop gain G_mR_f, the filter will have an N times lower bandwidth $1/R_fC$ and the same power consumption. In this way, the N-channel topology introduces N times less noise at the expense of N times more power. Another option is to leave constant the capacitance C and lower N times the transconductance G_m. To keep the fixed gain, R_f is increased by N times; thus, the bandwidth is lowered by N times. In this case, it will lower the power of each filter by N times, leading to the same power consumption with the same total integrated noise $\eta KT/C$. Moreover, the power consumption can be lowered at the expense of some area overhead by reducing the bias current I_{bias} more than the transistor width W, as was explained before. Therefore, there are two extreme cases: one possessing N times larger power consumption and N times lower noise and the other offering lower power consumption, the same noise power, and some area overhead. The optimal point should be somewhere between these two extreme cases, which can offer some power/noise savings at the expense of some area overhead. Note that C should be of sufficient size such that the $\eta KT/C$ noise term is negligible in comparison with the additive noise derived in (7).

VI. Conclusion

This paper has exploited the relaxation of the clock-jitter specifications offered by multichannel filter banks. The analytical framework developed in this paper allows the optimal design of baseband low-order (first- and second-order) multichannel receivers with robustness to one of the most fundamental limitations in wideband communication receivers: clock jitter. The design example (see Fig. 9 of a multichannel receiver can process a 5-GHz baseband signal with 40 dB of SNR with sampling clocks that can tolerate up to 5 ps_{rms} of clock jitter, enabling several high-data-rate communication applications. Existing architectures based on time-interleaving require 0.5 ps_{rms} of clock jitter for those specifications, which has become a roadblock for future wideband communication receivers.

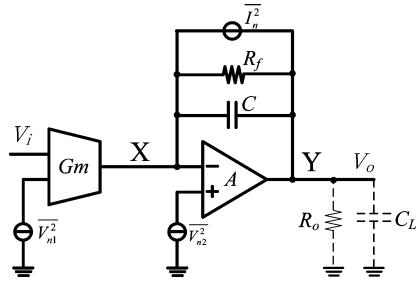

Fig. 10. Block diagram of a first-order filter based on a continuous-time lossy integrator.

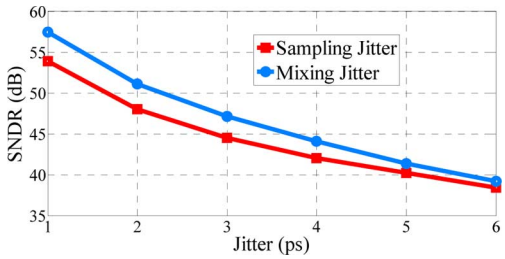

Fig. 11. Comparison between the performance impact of sampling jitter and LO mixing jitter for a ten-channel, second-order, and bandwidth-optimized receiver.

Appendix

Consider an OFDM signal composed of M complex sinusoidal signals of bandwidth B applied to the N-channel system in Fig. 9. Without loss of generality, assume Butterworth filtering with magnitude $|H(j\omega)| = 1/\sqrt{1 + (\omega/\omega_c)^{2\alpha}}$ and phase $\phi(\omega)$, where ω_c is the filter cutoff frequency and α is the filter order. After mixing and filtering, the signal in path i, for $i = 1, \ldots N$, is given by

$$v_i(t) = \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega - \omega_{\text{LO}i})} e^{j(m\Delta\omega - \omega_{\text{LO}i})t}}{\sqrt{1 + \left(\frac{m\Delta\omega - \omega_{\text{LO}i}}{\omega_c}\right)^{2\alpha}}} \tag{24}$$

where A_m is the symbol of the mth tone, $\Delta\omega$ is the tone-frequency spacing between the tones which is equal to B/M, and $\omega_{\text{LO}i}$ is the LO frequency in path i. This signal is sampled at instances $t_n = nT_s + \delta t$ by clocks of frequency $F_s = 1/T_s$ and clock jitter δT with variance σ_j^2. The uncertainty produced by the clock jitter on the OFDM signal can be obtained as (25),

$$v_i(n) = \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{\mathrm{LO}i})} e^{j(m\Delta\omega-\omega_{\mathrm{LO}i})nT_s} e^{j(m\Delta\omega-\omega_{\mathrm{LO}i})\delta t}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{\mathrm{LO}i}}{\omega_c}\right)^{2\alpha}}} \tag{25}$$

which is shown at the top of the page. For a small δt, this can be approximated as

$$v_i(n) \approx \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{\mathrm{LO}i})} e^{j(m\Delta\omega-\omega_{\mathrm{LO}i})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{\mathrm{LO}i}}{\omega_c}\right)^{2\alpha}}} \times[+j(m\Delta\omega-\omega_{\mathrm{LO}i})\delta t]. \tag{26}$$

The error produced by the clock jitter is approximately given by

$$\begin{aligned}\epsilon_i(n) &= v_i(n) \\ &\quad - \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{\mathrm{LO}i})} e^{j(m\Delta\omega-\omega_{\mathrm{LO}i})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{\mathrm{LO}i}}{\omega_c}\right)^{2\alpha}}} \\ &\approx \sum_{m=-M/2}^{M/2} \frac{A_m e^{j\varphi(m\Delta\omega-\omega_{\mathrm{LO}i})} e^{j(m\Delta\omega-\omega_{\mathrm{LO}i})nT_s}}{\sqrt{1+\left(\frac{m\Delta\omega-\omega_{\mathrm{LO}i}}{\omega_c}\right)^{2\alpha}}} \\ &\quad \times j(m\Delta\omega-\omega_{\mathrm{LO}i})\delta t. \end{aligned} \tag{27}$$

The variance of this additive error in the ith path can be expressed as

$$\overline{\epsilon_l^2(n)} = \frac{T_s\Delta\omega}{2\pi} \sum_{n=0}^{2\pi/T_s\Delta\omega} |\epsilon_i(n)|^2. \tag{28}$$

For the N paths, assuming uncorrelated noise, the total variance is given by

$$\overline{\epsilon^2(n)} = \sum_{i=1}^{N} \overline{\epsilon_i^2(n)}. \tag{29}$$

Following the same procedure from (11) to (15), the symbol-detection SNR is found to be

$$\mathrm{SNR} = \frac{\|\mathbf{a}\|^2}{\overline{\epsilon^2(n)} \sum_{i=1}^{S} \lambda_i}. \tag{30}$$

Monte Carlo simulations confirmed the validity of this expression. Fig. 8 shows the SNR as a function of the filter cutoff frequency ω_c parameterized by different filter orders.

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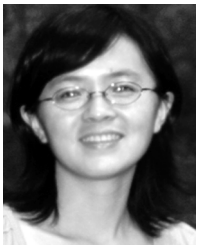

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