A Low-Power 26-GHz Transformer-Based Regulated Cascode SiGe BiCMOS Transimpedance Amplifier

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***Abstract*—Low-power high-speed optical receivers are required to meet the explosive growth in data communication systems. This paper presents a 26 GHz transimpedance amplifier (TIA) that employs a transformer-based regulated cascode (RGC) input stage which provides passive negative-feedback gain that enhances the effective transconductance of the TIA's input common-base transistor; reducing the input resistance and isolating the parasitic photodiode capacitance. This allows for considerable bandwidth extension without significant noise degradation or power consumption. Further bandwidth extension is achieved through series inductive peaking to isolate the photodetector capacitance from the TIA input. The optimum choice of series inductive peaking value and key transformer parameters for bandwidth extension and jitter minimization is analyzed. Fabricated in a 0.25-µm SiGe BiCMOS technology and tested with an on-chip 150 fF capacitor to emulate a photodiode, the TIA achieves a 53 dBΩ single-ended transimpedance gain with a 26 GHz bandwidth and 21.3 pA/$\sqrt{\text{Hz}}$ average input-referred noise current spectral density. Total chip power including output buffering is 28.2 mW from a 2.5 V supply, with the core TIA consuming 8.2 mW, and the chip area including pads is 960 µm x 780 µm.**

***Index Terms*—Bandwidth enhancement, BiCMOS, broad-band, inductive-series peaking, monolithic transformers, optical receiver, regulated cascode (RGC), transimpedance amplifier (TIA).**

I. Introduction

THE continuous growth of data volume due to increased multimedia applications and cloud computing services requires that the data rates of optical communication systems scale to supply this demand. This rapid expansion in data communication also necessitates improvements in optical transceiver circuitry power efficiency as these systems scale well past 10 Gb/s.

A typical optical receiver architecture is shown in Fig. 1. The photodetector detects the optical signal and converts it to electrical current. A transimpedance amplifier (TIA) then converts this current signal into a voltage which is passed through a limiting amplifier (LA) to achieve a signal sufficient for reliable operation of the subsequent clock and data recovery (CDR) circuits. After the CDR, a demultiplexer is used to generate multiple low-speed data streams for further processing.

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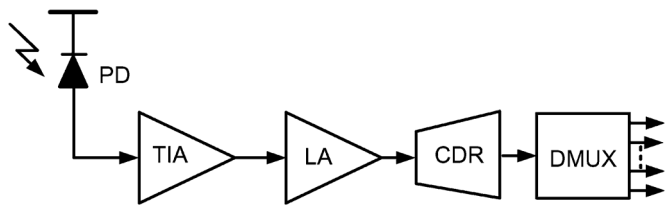

Fig. 1. Optical receiver system block diagram.

Transimpedance amplifiers typically determine the overall optical link performance, as their speed and sensitivity set the maximum data rate and tolerable channel loss. One TIA design challenge stems from the potentially large photodiode parasitic capacitance, which deteriorates both the bandwidth and noise performance of the system. Various input stages have been proposed [1]–[4] to relax this bandwidth limitation. A popular technique to obtain a very small input resistance involves modifying a conventional common-gate/common-base (CG/CB) input stage to a regulated cascode (RGC) architecture which employs active negative feedback gain to boost the input transconductance [1], [2]. This reduced input resistance pushes the input pole to a higher frequency, relaxing trade-offs between TIA gain and bandwidth. However, conventional RGC topologies require additional voltage headroom due to the cascode topology. Moreover, extra power is required in the feedback stage in order to avoid excessive TIA frequency peaking and obtain sufficient noise performance [1].

An efficient way to boost transistor transconductance involves passive transformer-based negative feedback. In this method, magnetic coupling between the transformer primary and secondary windings is utilized to realize negative feedback gain without introducing additional power or noise. While this approach has been employed in narrow-band LNA design [5], applying this in broad-band TIA design requires tight control on frequency peaking and group delay variation (GDV), particularly when combined with other bandwidth extension techniques [6].

Series inductive peaking is another technique for extending TIA bandwidth. Placing inductors in series between amplifier stages forms an equivalent π-network which isolates the capacitance of the stages [7], [8]. In TIA design, this is often used to isolate the photodetector capacitance from the TIA input capacitance. While this approach is effective, the inductance should be optimized to limit frequency peaking and group delay variation.

This paper presents a TIA design which employs both input transconductance boosting via transformer-based negative feedback and series inductive peaking in order to efficiently

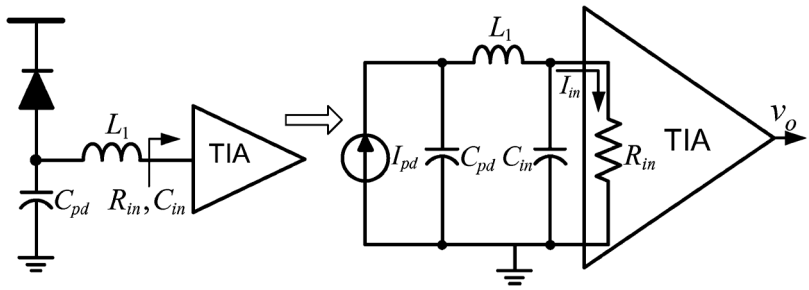

Fig. 2. Bandwidth enhancement by inserting a series inductor between the photodiode and the TIA.

obtain significant bandwidth extension and low-noise performance. Common bandwidth extension techniques, including series inductive peaking and the active regulated cascode topology, are reviewed in Section II. Section III discusses the transformer-based RGC input stage, where the mutual magnetic coupling of the on-chip transformer provides a negative feedback between the emitter and base terminals of the common-base input stage; improving the input transistor effective transconductance and allowing for extended bandwidth. The complete TIA topology is detailed in Section IV, along with analysis on the optimization of the series inductance and key transformer parameters to extend bandwidth, while limiting frequency peaking and group delay variation. Experimental results of the TIA, fabricated in a 0.25 μm SiGe BiCMOS technology, are presented in Section V. Finally, Section VI concludes the paper.

II. Bandwidth Extension Techniques

This section reviews the two key bandwidth extension techniques used in the presented TIA design, series inductive peaking and input transistor transconductance-boosting via the regulated cascode topology.

A. Series Inductive Peaking

Series inductive peaking [7]–[11] is an effective method to extend bandwidth in multi-stage amplifiers by isolating a stage's output capacitance from the subsequent stage's input capacitance. This technique is often leveraged in TIA design by interposing an inductor between the photodiode and the circuit input, as shown in Fig. 2. From the equivalent small-signal model, the series inductor L_1 isolates the two parasitic capacitors (C_{pd} and C_{in}), forming a π-network which extends the bandwidth relative to a lumped RC system. Following a similar approach as in [10], the current-mode transfer function of this π-network can be expressed as the following third-order expression.

$$\frac{I_{in}}{I_{pd}} = \frac{1}{s^3 R_{in} L_1 C_{pd} C_{in} + s^2 L_1 C_{pd} + s R_{in}(C_{pd}+C_{in}) + 1} = \frac{1}{\left(\frac{s}{\omega_0}\right)^3 \frac{k}{m}(1-k) + \left(\frac{s}{\omega_0}\right)^2 \frac{1-k}{m} + \frac{s}{\omega_0} + 1} \quad (1)$$

where $k = C_{in}/(C_{in}+C_{pd})$ and $m = R_{in}^2(C_{pd}+C_{in})/L_1$. Significant bandwidth extension ratios (BWER) can be achieved by choosing different k and m values, as shown in Fig. 3, where the frequency is normalized to the 3-dB frequency ($\omega_0 = 1/(C_{pd}+C_{in})R_{in}$) of the uncompensated case with $L_1 = 0$. However, it is important to avoid values which cause large gain ripple in the frequency response, as this introduces large group delay variation and results in significant signal distortion [8]. A more detailed analysis of the relationship between the bandwidth extension and group-delay variation in the proposed TIA can be found in Section IV.

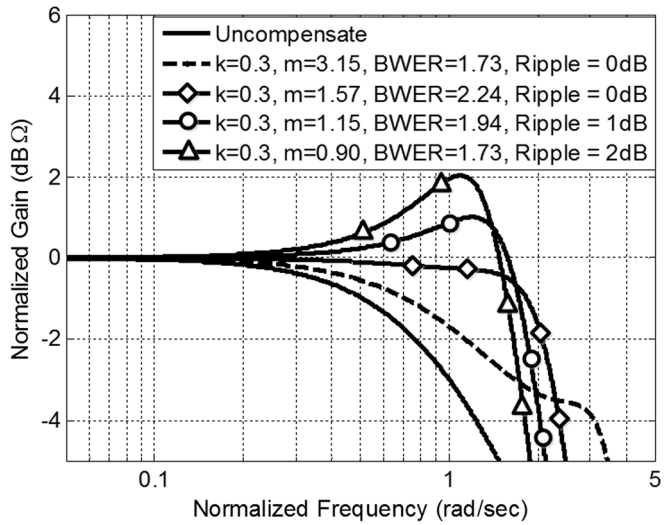

Fig. 3. Frequency response of inductive series peaking π-network for various m values ($k = 0.3$).

B. Conventional RGC Topology

TIA bandwidth extension can also be achieved by reducing the input resistance. The regulated cascode topology [1], shown in Fig. 4(a), achieves this by using a common-base input stage (Q_1) with local active feedback (Q_2) to boost the transconductance of Q_1 and provide a small signal input resistance of

$$R_{in} \simeq \frac{1}{g_{m1}(1+g_{m2}R_3)}. \quad (2)$$

An important feature of this gain-boosted common-base input stage is that it isolates the photodiode capacitance from subsequent amplifier stages. Used in combination with a subsequent feedback TIA, a high transimpedance can be achieved while maintaining stability over a wide input capacitance range.

However, a conventional RGC topology has a power overhead due to the headroom necessary to support the two base-emitter voltages and maintain a suitable frequency response. In addition, the local feedback stage introduces a zero (z_1) in the transimpedance transfer function. This zero can be estimated

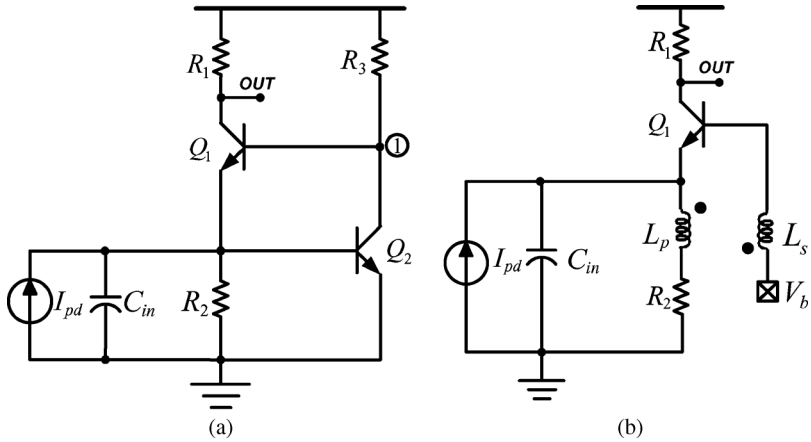

Fig. 4. Regulated cascode input stage: (a) conventional topology, (b) proposed transformer-based topology.

by $z_1 = (r_{\pi 1} \| r_{o2} \| R_3) C_{p1}$, where, $r_{\pi 1}$ is the base-emitter resistance of transistor Q_1, r_{o2} is the collector resistance of transistor Q_2, and C_{p1} is the total parasitic capacitance at node 1 of Fig. 4(a). In order to avoid the frequency peaking of transimpedance gain, a smaller resistor R_3 is normally used to set this zero in the roll-off region of the gain curve [12]. For a given negative-feedback gain and g_m-boosting factor, this results in an increased Q_2 bias current. In addition, the local feedback transistor can contribute substantial thermal noise at high frequency, thus degrading the system noise performance.

III. Transformer-Based RGC Input Stage

The TIA proposed in this work employs passive transformer-based negative feedback, shown in Fig. 4(b), in order to provide input g_m-boosting. Relative to a conventional RGC input stage, this approach trades off increased area from the large transformer to avoid the power and noise of an added active amplifier stage. Here the transformer consists of primary (L_p) and secondary inductors (L_s), with the bias voltage V_b provided externally. Feedback via mutual magnetic coupling in the transformer provides anti-phase operation between the emitter and base terminals, thus boosting the transconductance of the common-base transistor to

$$g'_m = (1 + nk) g_m. \tag{3}$$

Here the turn ratio n is

$$n = \sqrt{\frac{L_s}{L_p}} \tag{4}$$

and the coupling coefficient k is

$$k = \frac{M}{\sqrt{L_s L_p}} \tag{5}$$

where M is the mutual inductance between the primary and secondary windings [5]. The coupling coefficient indicates the magnetic coupling strength in the transformer and is intrinsically less than unity due to magnetic flux leakage. In order to effectively boost the transconductance of the input transistor, thus reducing the effective resistance at input node and extending the TIA bandwidth, the monolithic transformer should be designed to achieve a relatively high magnetic coupling coefficient over a wide frequency range. This implies careful design of the wires that comprise the transformer windings, the turn number, and the turn ratio. The details of transformer design for achieving considerable bandwidth extension and low deterministic jitter are described in Section IV.

IV. TIA Design

A. TIA Topology

The complete schematic of the transformer-based regulated cascode TIA is shown in Fig. 5. Both series inductive peaking (L_1) and input transistor g_m-boosting via transformer-based negative feedback are leveraged in order to extend TIA bandwidth. Table I gives the key parameters for the input-stage transformer. The g_m-boosted common-base input stage isolates the photodiode capacitance from the second-stage feedback TIA. This common-emitter gain stage, consisting of (Q_2 and R_4) with local shunt feedback resistor (R_f) connected between the base and collector terminals, provides the majority of the transimpedance gain. R_3 and C_1 are inserted in the second stage to provide an appropriate level shift for the DC voltage at emitter terminal. The final stage is a differential output buffer which converts the TIA's single-ended output to differential outputs and drives the 50 Ω load of the measurement equipment. Here shunt inductive peaking [14] is also used to achieve broadband operation. As this simple output buffer is not a major point of emphasis in this design, emitter degeneration is not included in the output buffer current mirror.

Assuming sufficiently large boosted g_{m1} and $g_{m2}R_f$ values, the low frequency transimpedance from the input to node B of Fig. 5 is approximately

$$Z_T(0) \simeq g_{m2} R_4 \left(R_1 \| \frac{R_f}{1 + g_{m2} R_4} \right) \tag{6}$$

At the input, since the (Q_1) transconductance is boosted by the negative feedback from the on-chip transformer, the resistance at the input node can be expressed as

$$R_{in}(s) \simeq \frac{1}{g_{m1}\left(1 + nk(s)\right)} \tag{7}$$

where $k(s)$ displays a high-pass response, as shown in Fig. 14. With turn ratio $n = 2$ and coupling coefficient k near 0.7 at 20 GHz, the input resistance can be reduced to a relatively low value. Note, this high-pass coupling coefficient can also be

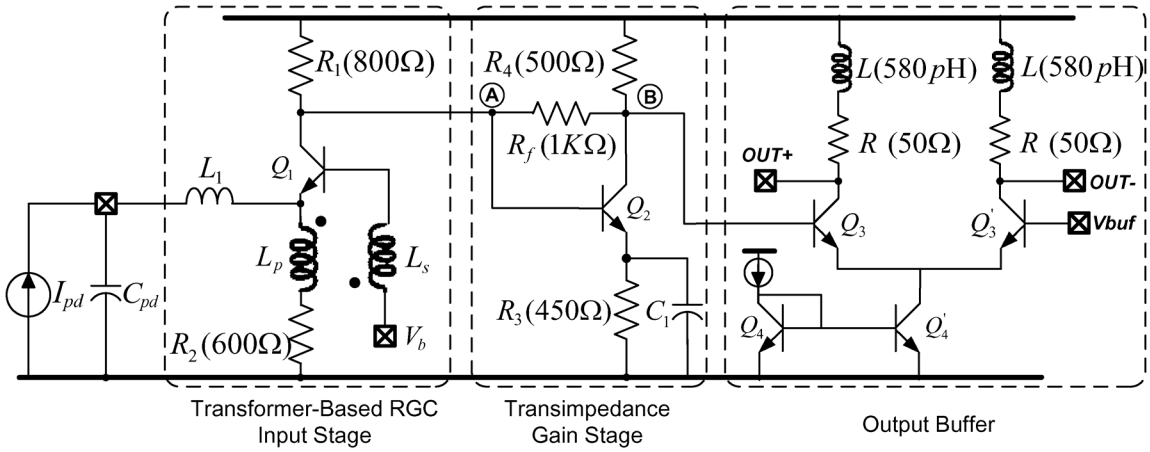

Fig. 5. Transformer-based RGC TIA schematic.

leveraged to compensate for bandwidth degradation caused by the circuits poles.

The trade-offs between input resistance, noise, and voltage headroom pose challenges in the design of a high-speed TIA based on a single common-base topology. In order to obtain a low input resistance the bias current needs to be large, which, for a given voltage headroom, limits the load resistor R_1 which sets the transimpedance gain and the TIA noise performance [18]. Moreover, a large load resistor reduces the TIA output bandwidth. The proposed TIA architecture alleviates these trade-offs by utilizing a transformer-based input stage that enhances the transconductance without increasing the bias current, thus reducing the input resistance. At node A of Fig. 5, the local shunt feedback lowers the node resistance down by the factor of the open loop gain of the second amplifier stage. Although the relatively low impedance caused by the local resistive shunt feedback sacrifices the transimpedance gain of first stage, it overcomes the bandwidth limit due to the large output impedance of the simple common-base topology. Finally, the effective resistance at node B is $(1/gm_2)\|R_4$, which is inherently small. Due to this TIA topology, all major signal path poles reside at relatively high frequencies, making this architecture suitable for wideband, high speed applications.

Since passive transformer-based negative feedback is utilized to boost the input transconductance, the noise penalty of the active feedback amplifier in the conventional RGC input stage is avoided. Considering transistor collector current shot noise and base resistance thermal noise [15], the input-referred noise current can be derived as

$$\overline{i_{n,in}^2} \simeq \frac{4kT}{R_1}+\frac{4kT}{R_2}+\frac{4kT}{R_f}+2kT\left(\frac{1}{g_{m2}}+2r_{b2}+\frac{2}{g_{m2}^2R_4}\right)\times\omega^2C_A^2+4kT\left(\frac{g_{m1}}{2}+r_{b1}g_{m1}^2+\frac{1}{R_f}+\frac{1}{R_1}\right)\frac{\omega^2C_{in}^2}{g_{m1}'^2} \quad (8)$$

where r_{b1} and r_{b2} are the base resistance of Q_1 and Q_2, respectively. Here, g'_{m1} is the boosted transconductance and C_{in} and C_A are the total parasitic capacitance at the input node and Q_1's collector, respectively. From (8), the boosted g'_{m1} value, which is a function of the feedback from the transformer comprised of L_p and L_s, should also provide a reduction in the last noise term at no power overhead.

B. Bandwidth Extension Analysis

While on-chip inductors and transformers can be used to enhance broadband amplifier bandwidth and overcome a given process's transimpedance limit, improperly designed inductor values can cause frequency peaking and lead to relatively large group delay variation and signal distortion. This has been well studied in the work of [8] and [16]. In this subsection, we model the frequency response of the proposed TIA, neglecting the output buffer (Fig. 6(a)), in order to select the series inductance value and transformer design parameters. We extend the approach of [16] for TIA modeling with series inductive peaking to include both the frequency-dependent response of the transformer-based g_m-boosting and a more accurate 2-pole and 1-zero feedback TIA model.

Fig. 6(b) shows the equivalent TIA small-signal model. The equivalent resistance seen into the emitter of transistor Q_1 is taken from (3). As shown in Fig. 6(c), the proposed TIA is then simplified to a passive π-network followed by the feedback TIA model. Including the transformer's primary inductor, the transfer function of this π-network can be written as a fourth-order expression. The feedback TIA is modeled with two poles located at nodes A and B in Fig. 6(a) and a zero from the parasitic capacitance in parallel with the local feedback resistor. Overall, the complete TIA transfer function is approximated as (9),

$$Z_T(s) \simeq \frac{R_1R_4}{R_1(1+g_{m2}R_4)+R_f}\times\frac{(sR_fC_f+1-g_{m2}R_f)}{(sR_AC_A+1)(sR_BC_B+1)}\times\frac{L_ps+R_2}{a_4s^4+a_3s^3+a_2s^2+a_1s+a_0} \quad (9)$$

where

$$\begin{aligned} a_0 &= R_2+R_{in}(s),\\ a_1 &= R_2R_{in}(s)(C_{pd}+C_{in})+L_p,\\ a_2 &= L_1C_{pd}(R_2+R_{in}(s))+R_{in}(s)L_p(C_{pd}+C_{in}),\\ a_3 &= L_1R_2R_{in}(s)C_{pd}C_{in}+L_1L_pC_{pd}, \end{aligned}$$

TABLE I
KEY PARAMETERS OF THE INPUT-STAGE TRANSFORMER

L_p	L_s	Turn Number	Turn Ratio (n)	Coupling Coefficient (k) at 20 GHz
0.28 nH	1.09 nH	2.5	2	0.68

$$a_4 \quad L_1 L_p C_{pd} C_{in} R_{in}(s),$$
$$R_A \quad R_1 \| (R_f/(1+g_{m2}R_4)),$$
$$R_B \quad (1/gm_2) \| R_4,$$
$$C_A \quad C_{cs1} + C_{be2} + C_f(1+g_{m2}R_4) + C_{bc1},$$
$$C_B \quad C_f + C_{cs2}.$$

Here C_{pd} denotes the parasitic photodiode capacitance and the bond pad capacitance, C_{cs1} and C_{bc1} are the Q_1 collector-substrate and base-collector capacitances, respectively, C_{be2} and C_{cs2} are the Q_2 base-emitter and collector-substrate capacitances, respectively, and C_f is the depletion capacitance of the collector-base junction of Q_2.

Using this model, the series peaking inductance and transformer design parameters are chosen for a flat frequency response, low group delay variation, and low deterministic jitter. The series inductance is selected to achieve a Butterworth response with maximally flat gain magnitude and the total TIA's response is optimized by varying the transformer turn number and turn ratio. As L_1, L_p, and L_s need to be jointly optimized, this iterative process is outlined in the following steps.

Step 1) Using initial reasonable transformer parameters (e.g. 2 turns and turn ratio of 2:1), optimize the series inductance L_1 for reasonable bandwidth extension, low jitter and group delay variation;
Step 2) Using the L_1 value found in Step 1 and the initial turn ratio, optimize the transformer turn number;
Step 3) Using the L_1 value found in Step 1 and turn number found in Step 2, optimize the transformer turn ratio;
Step 4) Using the transformer parameters found in Steps 2 and 3, re-optimize the series inductance;
Step 5) If necessary, re-optimize the transformer parameters and finalize the design.

The following sub-sections provide key design insights on how the series inductance and transformer parameters impact the TIA performance, with the assumption for each of the parameters that the other design parameters are already optimized.

1) Series Peaking Inductance: In order to achieve a flat frequency response, low group-delay variation, and low deterministic jitter, the inductance of L_1 in Fig. 5 needs to be carefully selected. The simulated TIA transimpedance frequency response is shown in Fig. 7(a) for various L_1 inductance values, with a finite-Q inductor model employed, and a 220 fF capacitance to model the photodetector and input bondpad. Also, an initial transformer design with 2 turns and a 2:1 turn ratio is assumed. Here both the transimpedance gain is normalized to one and the frequency axis is normalized to the 3-dB bandwidth without series inductive peaking ($L_1 = 0$). A Butterworth response with maximally flat magnitude and $1.8\times$ bandwidth extension is achieved when employing a proper series inductor value of $L_1 = 820$ pH. Note that higher inductance values also cause peaking in the frequency response, thus leading to relatively large group-delay variations, as shown in Fig. 7(b). The chosen series inductor value of $L_1 = 820$ pH and Q of $\sim$8 achieves a low group delay variation of $\pm$10% and, as shown in Fig. 8, minimal deterministic jitter with a 40 Gb/s $2^{31}-1$ PRBS pattern. Post-layout simulations indicate that this series inductance value is suitable for photodetector capacitance variations near $\pm$20%, while still maintaining $<$1 dB gain peaking and 5% bandwidth degradation. While an octagonal-shaped inductor is employed in the final design, this geometry choice is not essential, as post-layout simulations indicate that a Q of approximately three can be used without degrading the bandwidth more than 10%.

Realizing L_1 fully with an on-chip series peaking inductor value is directly applicable for an optical receiver with monolithically integrated photodetectors [19]. For optical receivers which have off-chip photodetectors, a portion of the series peaking inductor L_1 could be realized with the bondwire inductance between the photodetector and the TIA input pad. In this case, a smaller on-chip peaking inductor could still be included to isolate the bond pad capacitance from the TIA input capacitance for further bandwidth extension [8].

2) Transformer Turn Number: The total TIA response is optimized by setting the transformer turn number and ratio. Using the $L_1 = 820$ pH value to optimize the input π-network and assuming an initial 2:1 transformer turn ratio, the turn number is varied to observe how the change in coupling coefficient affects the TIA's frequency response. Here the transformer area is increased in order to increase the turn number, which results in increased parasitic resistance and capacitance. For example, the 3-turn transformer was designed by adding an extra turn to the 2-turn design, incurring a 72% area increase. As shown in Fig. 9, increasing turn number allows for bandwidth extension up to a point. However, when the transformer becomes large, as in the 3-turn case, the incurred parasitics cause a steep roll-off in the frequency response. A 2.5 turn number allows for a maximally flat bandwidth response, and, as shown in Fig. 8, minimal deterministic jitter with a 40 Gb/s $2^{31}-1$ PRBS pattern.

3) Transformer Turn Ratio: Transformer turn ratio is another important parameter which sets the amount of input transistor g_m-boosting. Using a 2.5-turn transformer value, the turn ratio is optimized for maximum bandwidth enhancement and minimum magnitude variation. As shown in Fig. 10, increasing turn ratio allows for bandwidth extension due to increased input transistor transconductance. However, again due to transformer size issues, the incurred parasitics cause excessive frequency peaking and a steep roll-off with $n = 3$. Also, as shown in Fig. 8, a large increase in deterministic jitter is observed for a turn ratio larger than two. The final transformer design uses $n = 2$ and 2.5 turns, which allows for a simulated TIA -3 dB-bandwidth of 32 GHz.

As mentioned previously, the overall design procedure is an iterative process to optimize the series peaking inductance and

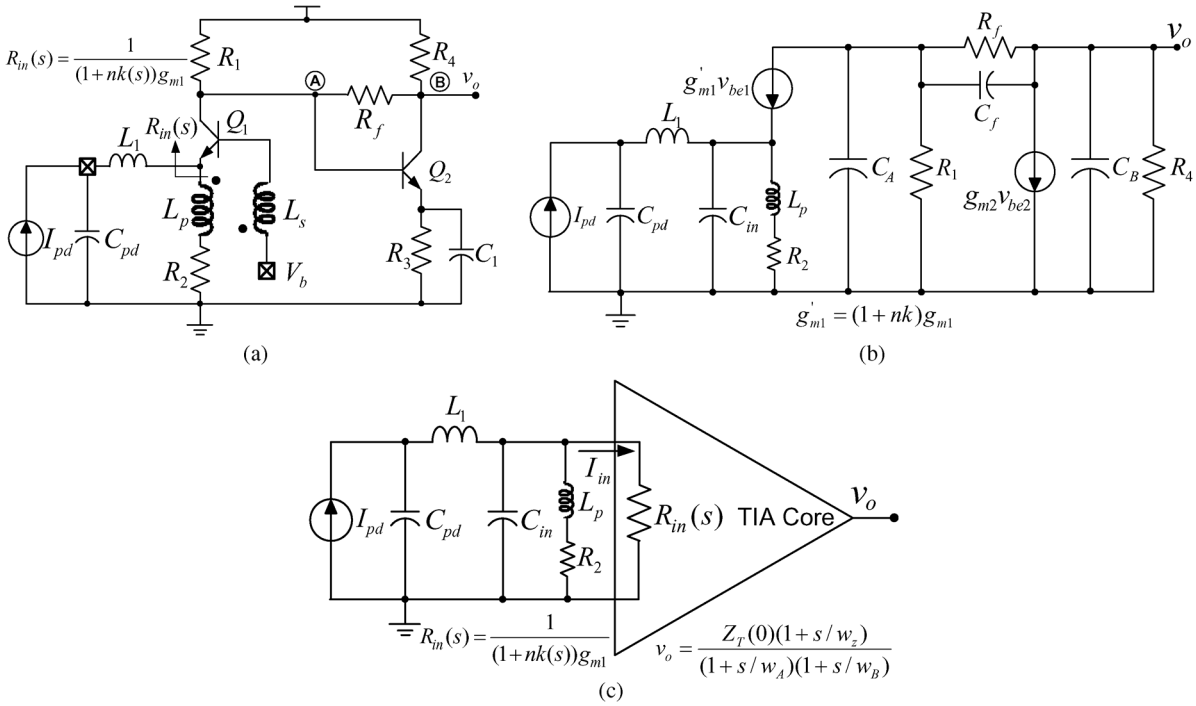

Fig. 6. (a) TIA schematic without the output buffer, (b) Equivalent small-signal model, (c) Equivalent analysis model.

key transformer parameters. Fig. 11 shows how the TIA bandwidth and group delay vary over a more complete design space of various series inductor values, normalized to the optimum 820 pH value, and transformer turn ratios. Overall, a turn ratio of two yields the maximum bandwidth and minimum group delay variation. Note that while a smaller value relative to the chosen 820 pH series inductor yields a potentially wider bandwidth, this would result in sub-optimum group delay variation.

C. Transformer Design

Trade-offs exist in the design of the wires that comprise the transformer windings. For a transformer with a given number of turns, magnetic flux coupled between windings increases as the metal width decreases. However, if the metal width is too narrow, this may lead to excessive ohmic losses. On the contrary, a larger width comes at the cost of relatively higher parasitic capacitance.

The monolithic transformer used in this work is shown in Fig. 12, where the two sections of primary winding are connected in parallel to form a 2:1 transformer and an inverting configuration is implemented in order to form the negative feedback for the transconductance boosting in the input stage. A simple square shape is utilized in order to more accurately control the turn ratio. As critical electromagnetic effects, such as substrate eddy currents and frequency-dependent metal loss need to be considered in the transformer design, an electromagnetic simulator, SONNET, is used to model the transformer. Each process layer is accurately modeled in SONNET according to the specifications in the 0.25-μm SiGe BiCMOS process design kit. In order to reduce the parasitic effects which cause high-frequency loss, the transformer is realized with the top metal layer (M6) which is the thickest and farthest from the substrate. The other metal layers (M3, M5) are used to facilitate convenient connections to other circuitry. Considering the wideband application of this design, the smallest linewidth (5 μm) is used to reduce the parasitic capacitance and the minimum line spacing (3 μm) allowed in the technology is used to achieve the best magnetic coupling. A grounded polysilicon bar shield is also introduced to provide increased isolation to the transformer from the silicon substrate, at the cost of increasing the capacitance to the shield to 10.5 fF from a potential value of 7.8 fF to the substrate. Note, as this design was implemented in a process with a high-resistivity substrate, the impact of the ground shield has a negligible impact on the quality factors of the inductors used to implement the transformer.

In addition to the physical size and spacing of metal wires, the number of turns is another important factor that affects the coupling coefficient. Fig. 13 shows the simulated transformer coupling coefficient k at 20 GHz versus turn number and for different turn ratios. While a large coupling coefficient improvement is observed from one to three turns, it tends to saturate around 0.8 with further increase in turn number. This is due to increased magnetic coupling between adjacent lines causing a large improvement in k-factor as the turn number is increased from one to two. However, as the turn number is increased further, the separation between the multiple parallel conductors increases and causes the k-factor to saturate near turn values of three to four [13]. Note that for multi-turn designs the turn ratio has little impact on the coupling coefficient in the 26 GHz frequency range of interest, with a lower turn ratio displaying only marginally better performance. However, at higher frequencies the k-factor of the 1:1 transformer falls off faster due to its lower self-resonant frequency.

It is seen from (3), that increasing the turn ratio between the secondary and primary windings can also boost the TIA input

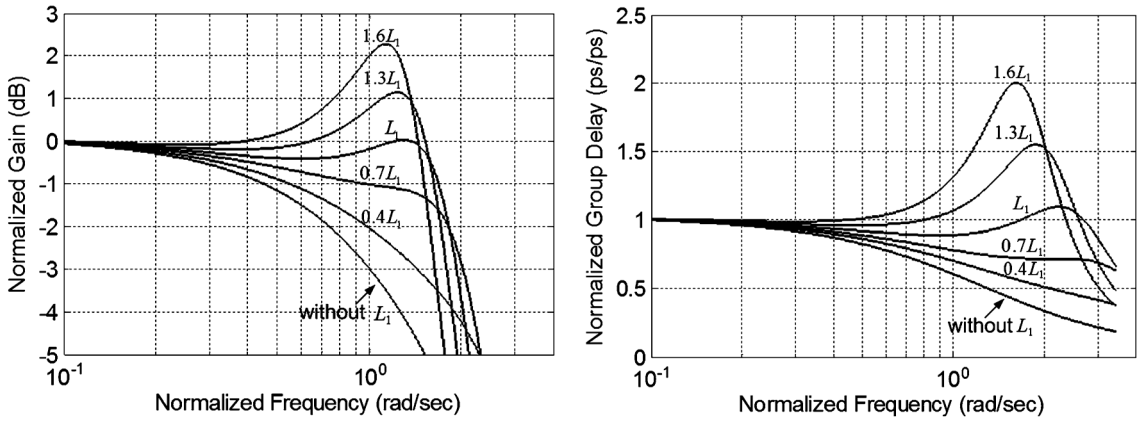

Fig. 7. Simulated TIA frequency response with various series inductance values: (a) normalized transimpedance gain, (b) group-delay of input π-network. The frequency axis in both curves is normalized to the 3-dB bandwidth without series inductive peaking.

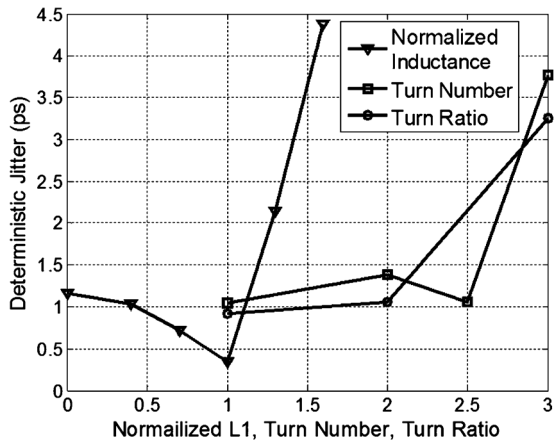

Fig. 8. Simulated 40 Gb/s deterministic jitter performance of the proposed TIA with a $2^{31}-1$ pattern.

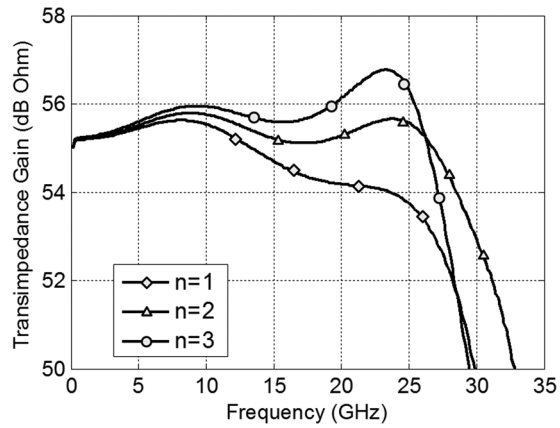

Fig. 10. Simulated transimpedance frequency response with different transformer turn ratio, transformer turn number is fixed at 2.5.

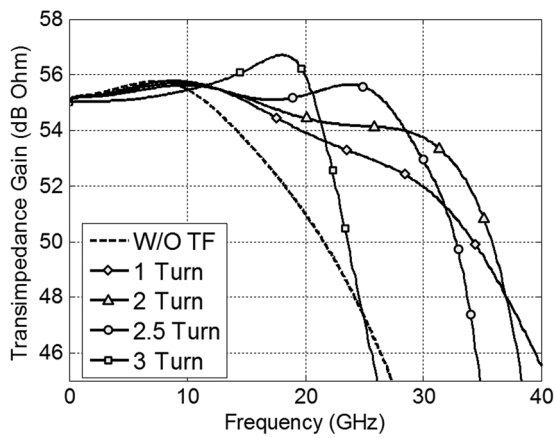

Fig. 9. Simulated transimpedance frequency response with different transformer turn number, transformer turn ratio is fixed at $n = 2$.

transconductance. For a monolithic transformer implemented by conductors interwound in the same plane, the mutual inductance of the transformer increases with the length of each winding. The simulated coupling coefficient of a 2.5-turn transformer versus frequency and for different transformer turn ratios is shown in Fig. 14, where the frequency response displays a high-pass shape that is mostly independent of turn ratio over the frequency range of interest. Therefore, a transformer with a turn ratio larger than one can be implemented with a single top-layer metal by sectioning the continuous primary winding into multiple individual turns [13]. While a larger turn ratio can further boost input transconductance, a transformer with turn ratio 2:1 is chosen in this work to balance TIA bandwidth extension and group-delay variation.

V. Experimental Results

The TIA was fabricated in a 0.25-μm SiGe BiCMOS technology with bipolar npn transistor peak f_t of 137 GHz. As shown in the die photograph of Fig. 15, the total chip area including pads is $960\ \mu\text{m} \times 780\ \mu\text{m}$. The chip is encapsulated in a QFN package only for connection of external power supply and DC voltage biases.

High frequency testing is performed with the package cover removed and the high-speed input/output signals and transistor base bias voltage applied via probing. Thus, there are no wire bonds on these critical signals. The S-parameters shown in Fig. 16 are measured using an Agilent N5230A network analyzer. In order to emulate the parasitic capacitance of a potential photodiode, a 150 fF on-chip metal capacitor is included in the

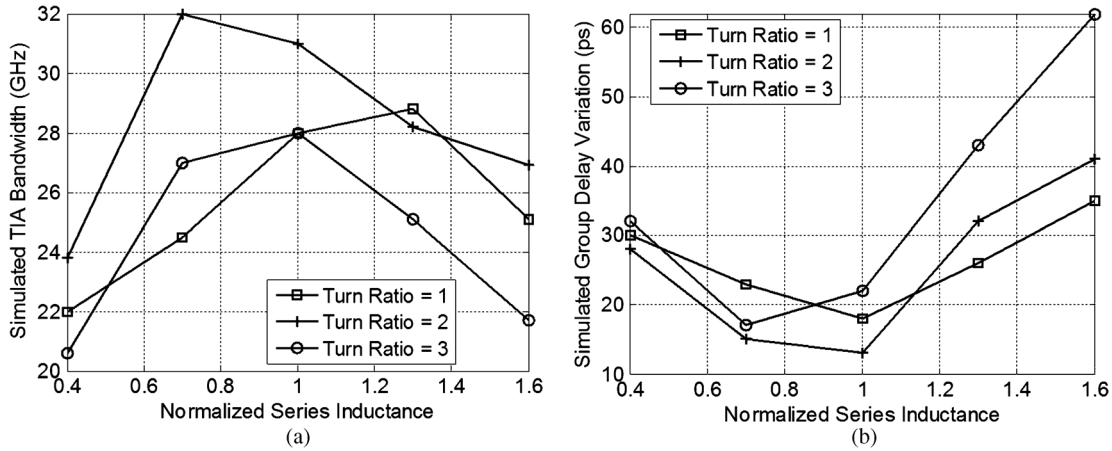

Fig. 11. Simulated TIA performance versus series inductance L_1 for different transformer turn ratios: (a) bandwidth, (b) group delay variation. Here the series inductance is normalized to the optimum value of 830 pH.

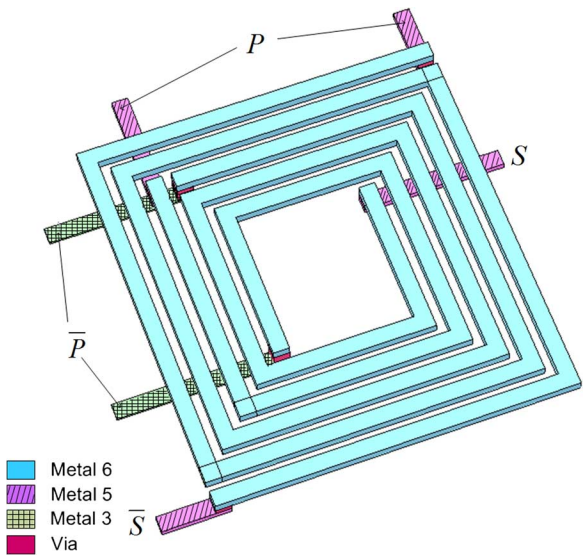

Fig. 12. Monolithic transformer used for input stage g_m-boosting.

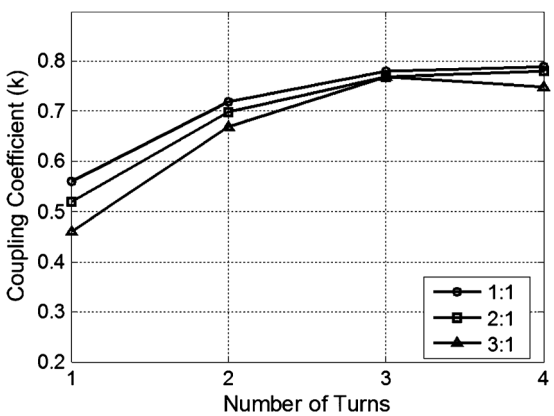

Fig. 13. Simulated transformer coupling coefficient at 20 GHz vs turn number with different turn ratios.

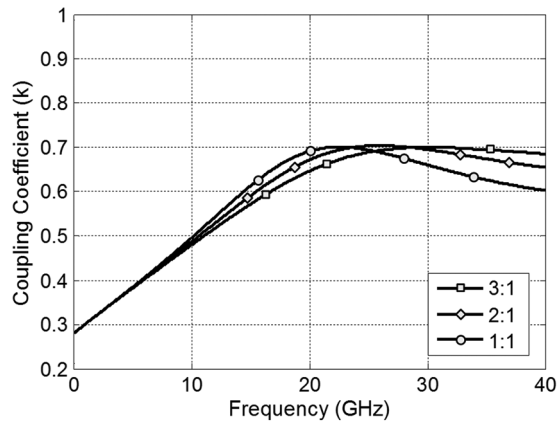

Fig. 14. Simulated 2.5-turn transformer coupling coefficient vs frequency with different turn ratios.

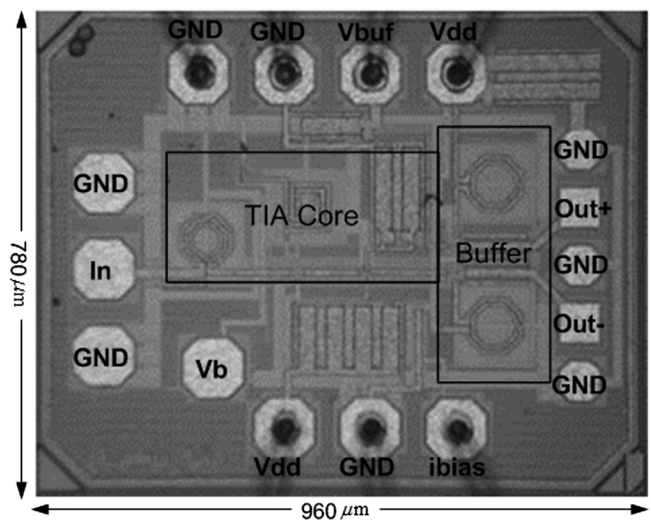

Fig. 15. Die photograph.

design. This capacitance, along with the 70 fF bondpad, yields a total effective C_{PD} of 220 fF. Due to equipment availability, testing is performed in single-ended mode with the unused ports terminated at 50 Ω. The differential transimpedance gain is calculated from the measured S-parameters based on

$$Z_t = \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}} \times Z_0 \qquad (10)$$

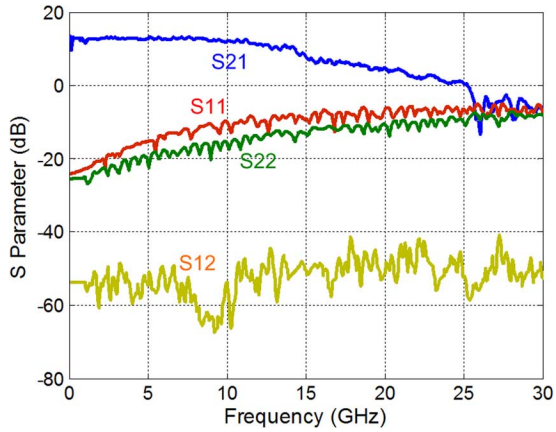

Fig. 16. Measured TIA single-ended S-parameters.

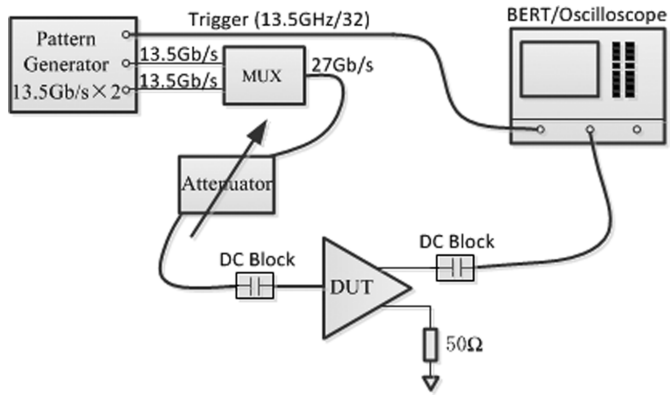

Fig. 18. Measurement setup for eye diagram and BER test.

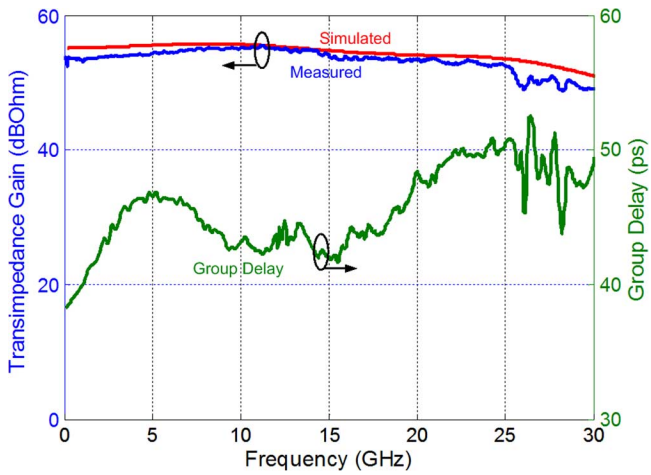

Fig. 17. Single-ended simulated/measured transimpedance gain and measured group delay.

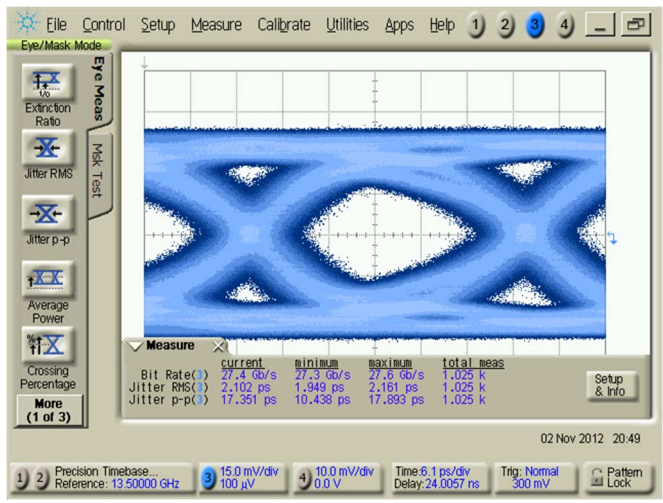

Fig. 19. Measured 27 Gb/s single-ended eye-diagram with a 125 μA_{pp} $2^{15}-1$ PRBS input signal.

where Z_0 is 50 Ω [20]. A single-ended transimpedance gain of 53 dBΩ with a −3 dB frequency of 26 GHz is achieved, as shown in Fig. 17. The TIA group delay is also extracted from the measured S-parameters, with group delay variation below 19 ps from near DC to 26 GHz. With data encoding schemes, the low-frequency cut-off frequency of interest is increased. If group delay values below 5 GHz are neglected [8], then the group delay variation is only 10 ps.

Fig. 18 illustrates the measurement setup for the high-speed eye diagram test. Two uncorrelated 13.5 Gb/s $2^{15}-1$ bit sequences from a pattern generator (Agilent N4872A) are multiplexed by a 2:1 MUX (SHF 23210A) to form a 27 Gb/s data sequence. A programmable step attenuator is then used to attenuate the input signal to an appropriate range for the TIA. The 27 Gb/s input/output signals pass through external DC blocks and are applied to the TIA via probing. Note that while this test setup is not optimal for TIA characterization, as the 50 Ω system has the potential to artificially increase the TIA bandwidth, this does not have a dramatic increase in the experimental results due to the transformer-based negative feedback at the input node reducing the TIA input impedance to near 15 Ω. Post-layout simulations indicate only a 2.7% bandwidth differential with the 50 Ω measurement system due to the low TIA input impedance and the contribution of other TIA poles setting the overall bandwidth. An improved test setup which better emulates a photodiode would include a large series resistor at the TIA input [21].

Fig. 19 shows a single-ended $2^{15}-1$ PRBS eye diagram obtained at 27 Gb/s with an estimated input current of 125 μA_{pp}. At this data rate the TIA output displays healthy margins, with the output rise/fall time mainly limited by the edge rate of the input signal, rather than the TIA circuit. Additionally, some bandwidth limitation is introduced by the microwave attenuators, connectors and cables. The TIA only introduces a small amount of jitter relative to the original input signal, as the measured output peak-to-peak jitter is 17 ps with an input signal that has 14 ps peak-to-peak jitter. While the available equipment limited testing at higher data rates, a post-layout simulated single-ended eye diagram at 40 Gb/s with a 100 μA_{pp} $2^{31}-1$ PRBS pattern, shown in Fig. 20, also achieves minimal vertical and horizontal eye closure.

The experimental setup of Fig. 18 was also used to perform BER testing. Fig. 21 shows a 25 Gb/s BER bathtub curve, with approximately 20% UI timing margin for a 150 μA_{pp} input

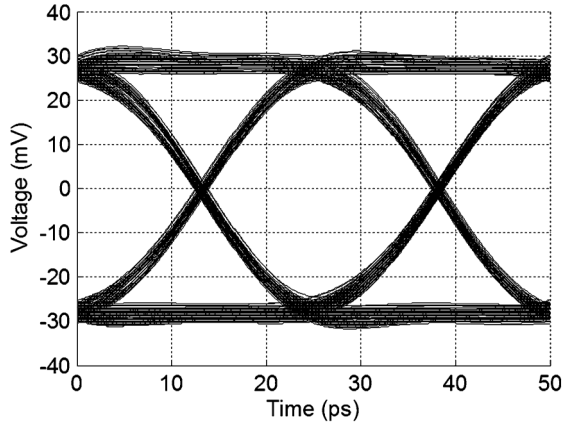

Fig. 20. Post-layout simulated single-ended 40 Gb/s eye-diagram of the proposed TIA with 100 μA_{pp} input current.

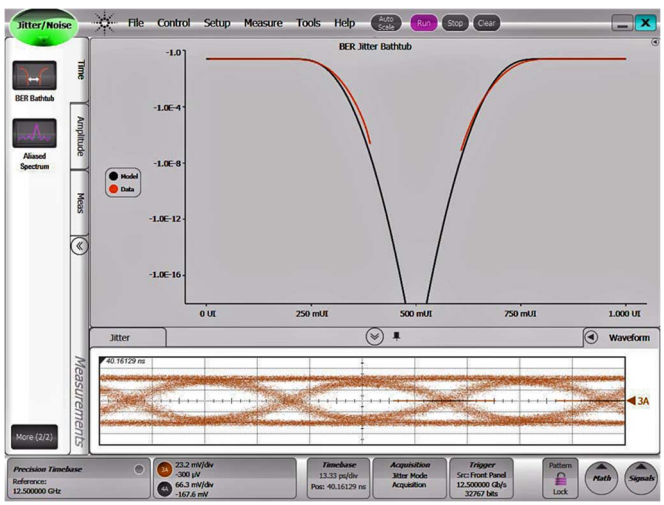

Fig. 21. BER jitter bathtub plot with 25 Gbps 150 μA_{pp} PRBS $2^{15}-1$ input.

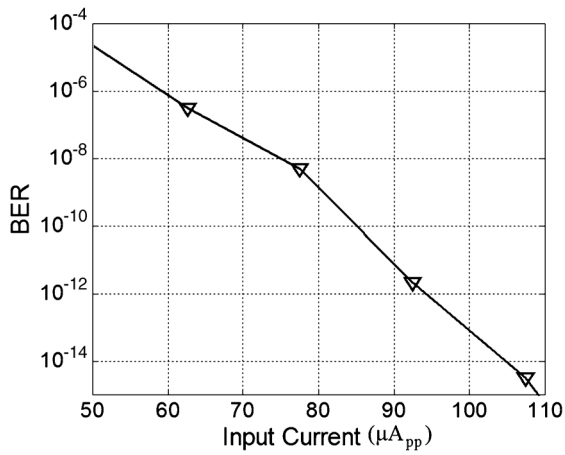

Fig. 22. Measured BER versus input current.

signal. A sensitivity of 93 μA_{pp} is achieved at a BER of 10^{-12}, as shown in Fig. 22.

The integrated single-ended output noise, measured via the oscilloscope histogram function with the absence of any input signal source, is shown in Fig. 23. After deconvolving the inherent oscilloscope noise of 0.476 mV_{rms}, the single-ended integrated output noise of the TIA is estimated at 1.54 mV. The integrated input-referred noise of the TIA's differential output can be calculated as

$$I_{n,in} = \frac{2\sqrt{(1.6125\ \text{mV})^2 - (0.476\ \text{mV})^2}}{59\ \text{dB}\Omega} = 3.45\ \mu\text{A}_{\text{rms}} \tag{11}$$

and the average input-referred noise current density is

$$I_{n,in,avg} = \frac{I_{n,in}}{\sqrt{BW}} = 21.3\ \text{pA}/\sqrt{\text{Hz}}. \tag{12}$$

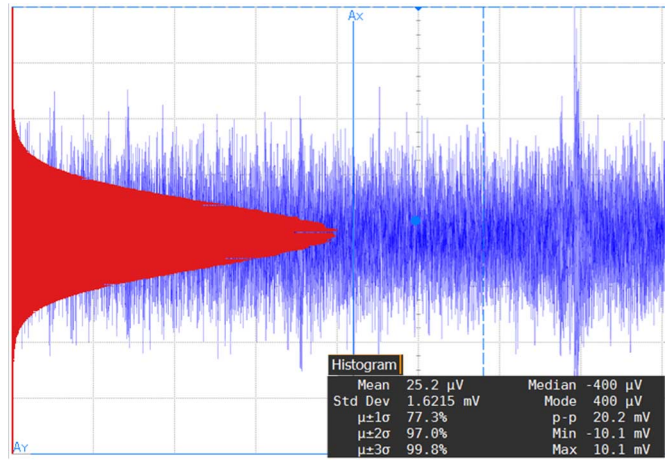

Fig. 23. Measured TIA single-ended integrated output noise.

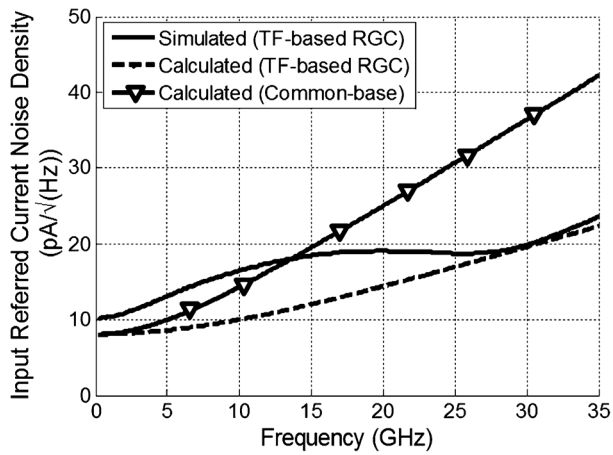

Fig. 24. Simulated and calculated input-referred current noise density for the proposed transformer-based RGC input-stage TIA and a simple common-base input-stage TIA.

This measured result matches well with the simulated input-referred noise current density, shown as the solid curve in Fig. 24, which is below 20 $\text{pA}/\sqrt{\text{Hz}}$ up to 30 GHz. Fig. 24 also compares the simulated input-referred current noise with the expressions for the proposed transformer-based RGC TIA (8) and a simple common-base input stage. The noise for a simple common-base input stage without any gain boosting increases at a relatively low frequency due to a reduced input pole frequency which effectively amplifies the input-referred current noise. Whereas the increased input bandwidth provided by the transformer-based RGC topology reduces the frequency-dependent slope of the last term in (8), and allows for a slower

TABLE II
TIA PERFORMANCE COMPARISONS

	[2]	[17]	[8]	This Work
BW (GHz)	28	42	29	26
Gain (dBΩ)	53.6	65	50	59 (diff)
Noise (pA/$\sqrt{Hz}$)	36.5	34.2	51.8	21.3
GDV (ps)	NA	10	16	13
Power (mW)	110.0	600.0	45.7	28.2
Area (mm^2)	0.56	1.0	0.4	0.75
Architecture	RGC	CE	CS	Transformer based RGC
Technology	0.13μm-BiCMOS	InP-InGaAs	0.13μm-CMOS	0.25μm-BiCMOS
f_t (GHz)	160	150	85	137

increase in the noise current with frequency. Note that the calculated noise level of the proposed transformer-based RGC TIA is lower than the simulated results at low frequencies due to neglecting the noise of the output buffer.

Table II compares this work with recent TIA designs. The use of passive transformer-based negative feedback to reduce the input resistance and extend TIA bandwidth allows the design to achieve a comparable transimpedance gain with a power consumption of only 28.2 mW from a 2.5 V power supply, of which the TIA core is only 8.2 mW. Also, since the passive transformer contributes little noise, superior noise performance is achieved.

VI. CONCLUSION

This paper presented a TIA design which employs two key bandwidth extension techniques; input g_m-boosting via transformer-based negative feedback and series inductive peaking. Utilizing mutual magnetic coupling of a passive on-chip transformer to provide negative feedback between the emitter and base terminals of a common-base input stage provides g_m-boosting in the input common-base stage, without the power and noise penalties associated with a conventional regulated cascode topology. Further bandwidth extension is achieved with series inductive peaking at the TIA input. This series inductive peaking value and key transformer design parameters were selected to obtain a broadband flat frequency response, low group delay variation, and low deterministic jitter. These techniques allow for relaxed voltage headroom, low power, improved system noise performance, and high bandwidth operation, making the proposed topology suitable for high-speed, low power, and low noise applications.

ACKNOWLEDGMENT

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