A Low-Power, 26-GHz Transformer-Based Regulated Cascode Transimpedance Amplifier in 0.25µm SiGe BiCMOS

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***Abstract* — A 26 GHz transimpedance amplifier (TIA) with transformer-based regulated cascode (RGC) input stage is proposed and analyzed. The transformer enhances the effective transconductance of the TIA's input common-base transistor; reducing the input resistance and providing considerable bandwidth extension. The TIA is implemented in a 0.25µm BiCMOS technology. Measurement shows the single-ended transimpedance gain of 53dBΩ with -3dB bandwidth of 26 GHz. Total chip power, including an output buffer, is 28.2mW from a 2.5V supply; while core TIA power is 8.2mW. The measured average input-referred noise current spectral density is 21.3 $pA/\sqrt{Hz}$. Total chip area, including pads, is 960µm×780µm.**

Index Terms* — *BiCMOS, Regulated Cascode (RGC), Transimpedace Amplifier (TIA), Common-Emitter (CE), Common-Base (CB), LNA (Low Noise Amplifier)

I. Introduction

As data networks scale to meet increasing bandwidth requirements, optical channels are being considered as replacements for copper channels. Transimpedance amplifiers (TIAs), which typically serve as an optical receiver system's input amplifier stage, determine the overall optical link performance; as their speed and sensitivity set the maximum data rate and tolerable channel loss.

One of the TIA design challenges stems from the large parasitic capacitance of the photodiode deteriorating the bandwidth and noise performance of the system. Various input stages have been proposed [1]-[4] to relax this bandwidth limitation. For example, by modifying a conventional common-base (CB) input stage to a regulated cascode (RGC) architecture [1], [2], the input resistance can be reduced to

$$R_{in} \cong \frac{1}{g_{m1}(1+g_{m2}R_2)} \quad (1)$$

where $g_{m2}R_2$ is the voltage gain of the local feedback stage in Fig. 1. Therefore, the pole at the input node can be pushed to higher frequency. However, conventional RGC topology requires additional voltage headroom due to the cascode architecture. Moreover, extra power is required for the cascode transistor to balance the frequency peaking and noise performance of the TIA [1].

Utilization of negative feedback through transformer to control the node impedance and system noise performance has been discussed in LNA design [5]. In this work, we propose a transformer-based RGC input stage to improve the power and noise performance of the conventional RGC architecture. Section II provides an overview of the TIA circuit design, where the mutual magnetic coupling of the on-chip transformer provides a negative feedback between the emitter and base terminals of the common-base input stage, improving the input transistor effective transconductance and allowing for extended bandwidth with excellent high frequency noise performance. Measurement results of the TIA, fabricated in a 0.25µm SiGe BiCMOS technology, are presented in Section III. Finally, Section IV concludes the paper.

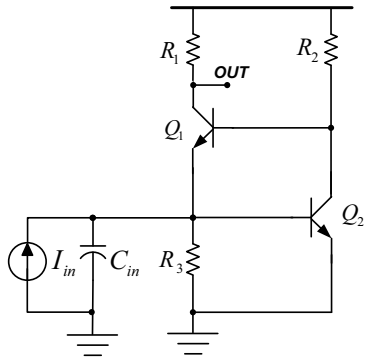

Fig. 1. Schematic of conventional RGC TIA.

II. Circuit Design

A. TIA with Transformer-based RGC Input Stage

The conventional RGC structure is shown in Fig. 1. In this topology, a common base amplifier (Q_1) with local active feedback (Q_2) is adopted to reduce the input impedance, thus isolating the bandwidth-limiting photodiode's parasitic capacitance. However, in this topology, the headroom of at least two base-emitter voltages is required; leading to relatively high power consumption. In addition, the local feedback transistor contributes substantial thermal noise at high frequency, thus degrading the system noise performance.

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To overcome these issues discussed above, the transformer based RGC architecture is proposed and shown in Fig. 2, which is composed of a transformer-based negative local feedback input stage (Q_1, L_P and L_s) followed by a common-emitter gain stage with local shunt feedback resistor. The on-chip transformer consists of the primary (L_P) and secondary inductors (L_s), with the bias voltage V_b provided externally. Feedback via the mutual magnetic coupling in the transformer provides anti-phase operation between the emitter and base terminals, thus boosting the transconductance of the common-base transistor. The boosted transconductance can be expressed as

$$g_m^{'} = (1+nk)g_m \qquad (2)$$

where k is the coupling coefficient of the transformer and the turn ration $n = \sqrt{L_s / L_p}$ [5]. Series peaking inductor L_1 is also inserted to achieve additional bandwidth extension.

The RGC input stage is transparent to the photodiode current, which flows through the feedback resistor R_f and is converted to the output voltage signal. Therefore, the transimpedance gain is roughly decided by the shunt-feedback resistor.

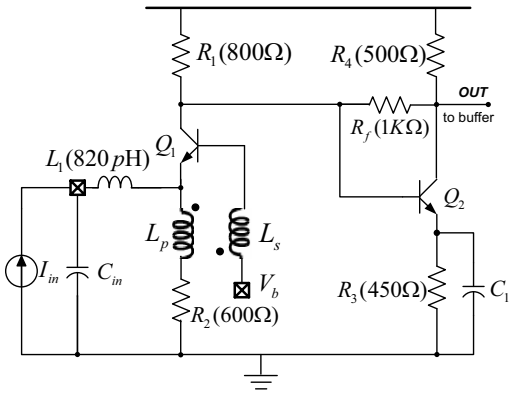

Fig. 2. Schematic of transformer based TIA.

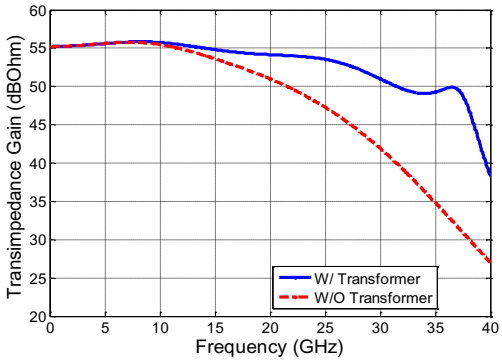

Fig. 3. Simulated frequency response of TIA, with/without transformer based RGC.

Fig. 3 shows the simulated impact of the transformer-based local feedback on transimpedance gain. These results show a bandwidth extension ratio of 160% has been achieved with the transformer-based RGC input stage.

B. Transformer Design

The performance of the transformer-based RGC architecture depends on the mutually-coupled inductors' high-frequency response. An electromagnetic simulator, SONNET, is used to model various non-ideal passive effects, such as parasitic routing paths and finite component quality factor. In order to reduce these parasitic effects which cause high frequency loss, the transformer is realized with the top metal layer which is the thickest and farthest from the substrate.

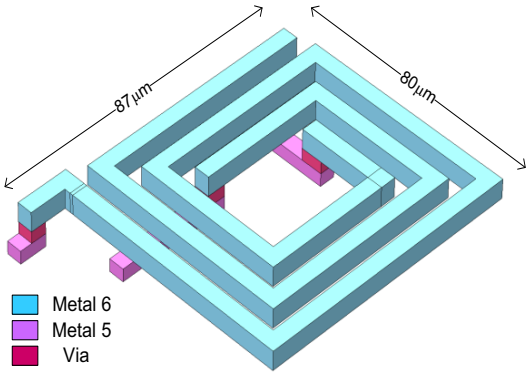

Fig. 4. Monolithic transformer.

Fig. 4. shows the on-chip transformer designed in SONNET. The square spiral layout consists of two interwound inductors to promote mutual coupling. The line width and spacing between the two inductors are optimized to achieve a coupling coefficient of 0.67. The simulated coupling coefficient for the on-chip transformer is show in Fig. 5.

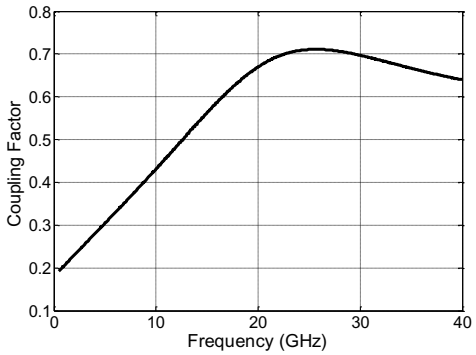

Fig. 5. Simulated coupling coefficient of transformer.

Terminals for the primary and secondary windings are optimized to facilitate connection to the other circuitry. An inverting configuration [6] is implemented in order to form the negative feedback for the transcodunctance boosting in the input stage.

C. Output Buffer

The function of the output buffer is to drive the 50Ω load of the measurement equipment. To achieve a broad bandwidth, a simple differential pair with shunt inductive peaking is used in the design. The schematic of the output buffer is shown in Fig. 6.

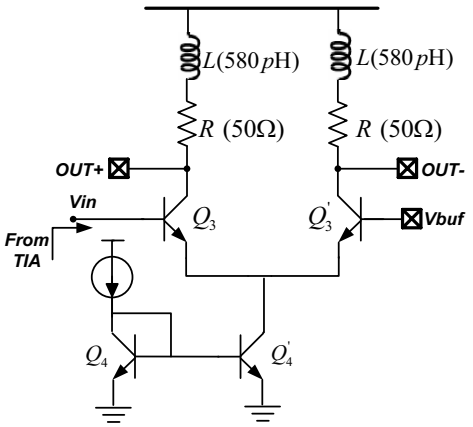

Fig. 6. Schematic of output buffer.

III. Results and Discussion

The developed TIA was fabricated in a 0.25µm SiGe BiCMOS technology with bipolar npn transistor peak f_T of 137GHz. The die micrograph is shown in Fig. 7, where the total chip area including the pads is 960µm×780µm. The chip is encapsulated in a quad flat no leads (QFN) package for connection of external power supply and DC voltage biases. The total power consumption of the circuit is about 28.2mW with 2.5V power supply, of which 8.2mW is consumed by the TIA core.

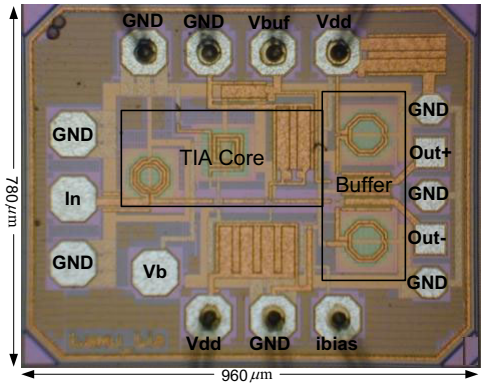

Fig. 7. Chip Micrograph.

The signal is applied and measured by on-wafer probing station and Agilent N5230A S-parameter analyzer. 150fF capacitance is added in the circuit to emulate the parasitic capacitance of the photodiode. Due to equipment availability, testing is performed in single-ended mode with the unused ports terminated at 50Ω. Fig. 8 presents the measured S parameters of the TIA. The transimpedance gain Z_t without photodetector was calculated from measured S-parameters based on the equation (3), where Z_0 is 50Ω.

$$Z_t = \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{21}S_{12}} \times Z_0 \qquad (3)$$

The TIA exhibits a single-ended transimpedance gain of 52.8dBΩ with –3dB frequency of 26GHz, which is shown in Fig. 9. 6dB is added on single-ended gain to represent the differential gain. The group delay is measured from the S-parameters. Measure results show group delay variation is below 10ps up to 26GHz.

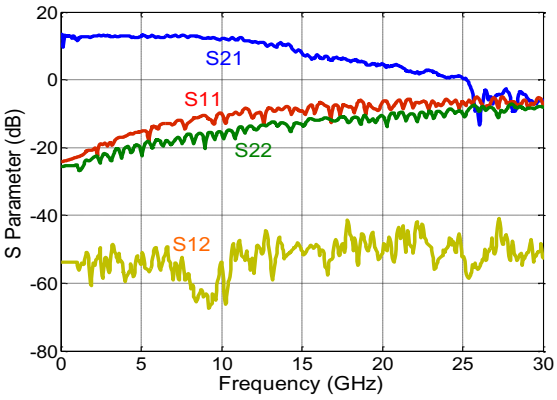

Fig. 8. Single-ended measured S-parameters.

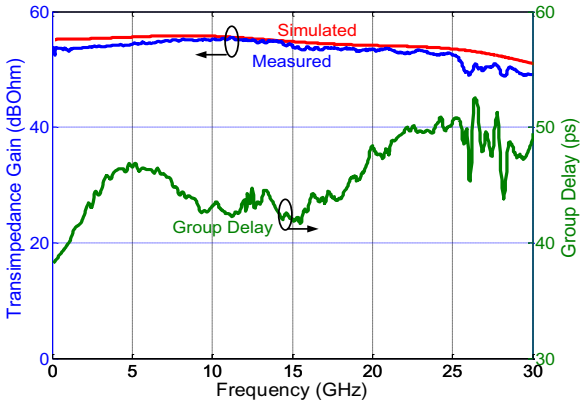

Fig. 9. Single-ended simulated/measured trans-impedance gain and measured group delay.

Fig. 10 shows the integrated single-ended output noise measured with the oscillopscope histogram function and with the absence of any input signal source. The single-ended integrated output noise of the TIA after deconvolving oscilloscope noise is 1.54mV. The integrated input-referred noise of the TIA's differential output can be calculated as

$$I_{n,in} = \frac{2\sqrt{(1.6125mV^2 - 0.476mV^2)}}{59dB\Omega} = 3.45\mu A_{rms} \qquad (4)$$

where the 0.476mV$_{rms}$ is the noise contributed by the oscilloscope. The average input-referred noise current density is

$$I_{n,in,avg} = \frac{I_{n,in}}{\sqrt{BW}} = 21.3 pA/\sqrt{Hz} \quad (5)$$

Simulated input-referred noise current density is shown in Fig. 11, which is below $20 pA/\sqrt{Hz}$ up to 30GHz.

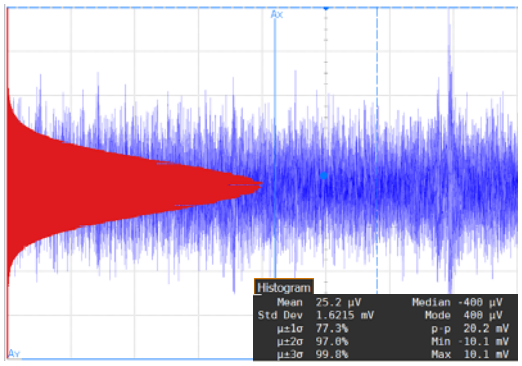

Fig. 10. Measured integrated output noise of TIA (single-ended).

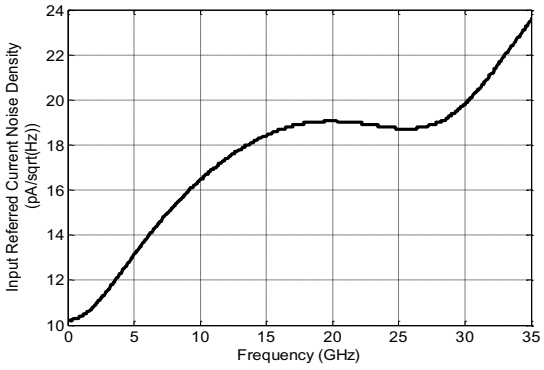

Fig. 11. Simulated input-referred noise current density

Table 1. compares this work with recent TIA designs. The proposed design consumes 28.2mW from a 2.5V power supply, of which the TIA core is only 8.2mW. Since the passive transformer contributes little noise compared to the other designs with extra transistors, superior noise performance is achieved.

IV. CONCLUSION

A low power, transformer-based RGC TIA for an optical receiver system is designed and implemented in a 0.25µm SiGe BiCMOS technology. Replacing the active local feedback in the conventional RGC architecture with the proposed transformer-based local feedback allows for relaxed voltage headroom, lower power, improved system noise performance, and high bandwidth operation.

ACKNOWLEDGEMENT

The authors would like to thank NXP Semiconductor for fabricating the chip. The authors also acknowledge Dr. Kamran Entesari for use of measurement equipment. They would also like to thank Younghoon Song for useful discussions and assistance during chip measurements.

TABLE I
MEASURED PERFORMANCE COMPARED WITH PRIOR PUBLISHED TIAS

	[2]	[7]	[8]	This Work
BW (GHz)	28	42	29	26
Gain (dBΩ)	53.6	65	50	59 (diff)
Noise ($pA/\sqrt{Hz}$)	36.5	34.2	51.8	21.3
Power (mW)	110.0	600.0	45.7	28.2
Chip Area (mm^2)	0.56	1.0	0.4	0.75
Architecture	RGC	CE	CS	Transformer-based RGC
Technology	0.13µm BiC-MOS	InP-InGaAs	0.13µm CMOS	0.25µm BiCMOS
f_T (GHz)	160	150	85	137

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