Silicon Photonic Transceiver Circuits With Microring Resonator Bias-Based Wavelength Stabilization in 65 nm CMOS

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***Abstract*—Photonic interconnects are a promising technology to meet the bandwidth demands of next-generation high-performance computing systems. This paper presents silicon photonic transceiver circuits for a microring resonator-based optical interconnect architecture in a 1 V standard 65 nm CMOS technology. The transmitter circuits incorporate high-swing ($2\mathrm{V_{pp}}$ and $4\mathrm{V_{pp}}$) drivers with nonlinear pre-emphasis and automatic bias-based tuning for resonance wavelength stabilization. An optical forwarded-clock adaptive inverter-based transimpedance amplifier (TIA) receiver trades off power for varying link budgets by employing an on-die eye monitor and scaling the TIA supply for the required sensitivity. At 5 Gb/s operation, the $4\mathrm{V_{pp}}$ transmitter achieves 12.7 dB extinction ratio with 4.04 mW power consumption, excluding laser power, when driving wire-bonded modulators designed in a 130 nm SOI process, while a 0.28 nm tuning range is obtained at 6.8 μW/GHz efficiency with the bias-based tuning scheme implemented with the $2\mathrm{V_{pp}}$ transmitter. When tested with a wire-bonded 150 fF p-i-n photodetector, the receiver achieves -9 dBm sensitivity at a $\mathrm{BER} = 10^{-9}$ and consumes 2.2 mW at 8 Gb/s. Testing with an on-die test structure emulating a low-capacitance waveguide photodetector yields 17 $\mu\mathrm{A_{pp}}$ sensitivity at 10 Gb/s and more than 40% power reduction with higher input current levels.**

***Index Terms*—Electrooptic modulators, optical interconnects, optical receiver, pre-emphasis, ring resonator, transimpedance amplifier (TIA).**

I. Introduction

OPTICAL channels provide the potential to overcome key interconnect bottlenecks and greatly improve data transfer efficiency due to their flat channel loss over a wide frequency range and also relatively small crosstalk and electromagnetic noise [1]. Another important feature of optical interconnects is the ability to combine multiple data channels on a single waveguide via wavelength-division-multiplexing (WDM) and greatly improve bandwidth density. In order to take advantage of these attractive properties, silicon photonic platforms are being developed to enable tightly integrated optical interconnects and future photonic interconnect network architectures [2]–[18]. One promising photonic device is the silicon ring resonator [2]–[6], which can be configured either as an optical modulator or WDM drop filter. Silicon ring resonator modulators/filters offer advantages of small size, relative to Mach–Zehnder modulators [7], [8], and increased filter functionality, relative to electro-absorption modulators [9].

Silicon photonic links based on ring resonator devices provide a unique opportunity to deliver distance-independent connectivity whose pin-bandwidth scales with the degree of wavelength-division multiplexing. As shown in Fig. 1, multiple wavelengths ($\lambda_{1\text{-}4}$) generated by an off-chip continuous-wave (CW) laser are coupled into a silicon waveguide via an optical coupler. This off-chip laser can either be a distributed feedback (DFB) laser bank [19], which consists of an array of DFB laser diodes, or a comb laser [20], which is able to generate multiple wavelengths simultaneously. Implementing a DFB laser bank for dense WDM (DWDM) photonic interconnects (e.g., 64 wavelengths) is quite challenging due to area and power budget constraints. This motivates a single broad-spectrum comb laser source, such as InAs–GaAs quantum dot comb lasers which can generate a large number of wavelengths in the 1100 to 1320 nm spectral range with typical channel spacing of 50–100 GHz and optical power of 0.2–1 mW per channel [20]. While operating near the common 1310 nm wavelength (O-band) does have slightly higher optical loss versus a 1550 nm (C-band) system, this has negligible impact in short-reach interconnect applications. After coupling the CW laser light, transmit-side ring modulators insert data onto a specific wavelength through electrooptical modulation. These modulated optical signals propagate through the waveguide and arrive at the receiver side where ring filters drop the modulated optical signals of a specific wavelength at a receiver channel with photodetectors (PDs) that convert the signals back to the electrical domain.

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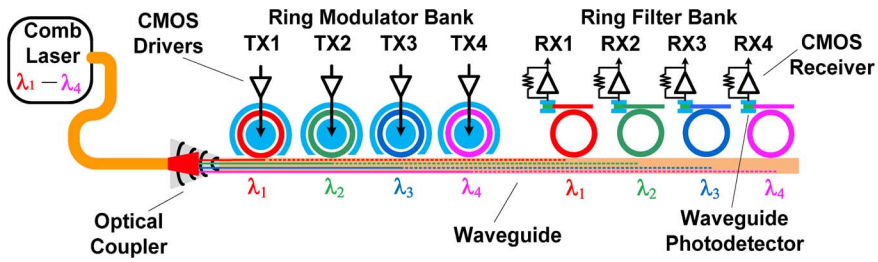


Fig. 1. Silicon ring resonator-based WDM link.

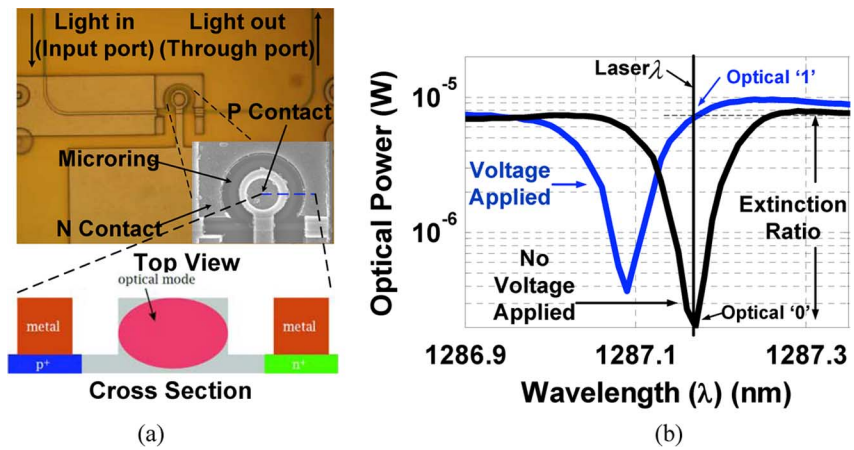


Fig. 2. (a) Top and cross-sectional views of carrier-injection silicon ring resonator modulator. (b) Optical spectrum at through port.

A basic silicon ring resonator consists of a straight waveguide coupled with a circular waveguide, as shown in Fig. 2(a). Input light at the resonance wavelength mostly circulates in the circular waveguide, with only a small amount of optical power observed at the through port, resulting in the ring's spectrum at the through port displaying a notch-shaped characteristic [Fig. 2(b)]. This resonance wavelength of the ring device is periodic, repeating over a free spectral range (FSR), and can be shifted by changing the effective refractive index of the waveguide through the free-carrier plasma dispersion effect [5]. Two common implementations of silicon ring resonator modulators include p-i-n junction-based carrier-injection devices [3], [4], operating primarily in forward-bias, and carrier-depletion devices [6], operating primarily in reverse-bias. Although a depletion ring generally achieves higher modulation speeds relative to a carrier-injection ring due to the ability to rapidly change the depletion width, its modulation depth is limited due to the relatively low doping concentration in the waveguide to avoid excessive loss. In contrast, carrier-injection ring modulators can provide large refractive index changes and high modulation depths, but are limited by long minority carrier lifetimes.

While ring-resonator-based photonic interconnects have the potential to offer both improved power efficiency and bandwidth density, reliability and robustness are major barriers to widespread adoption of ring-based silicon photonics [10]. A key challenge is the variation in resonance wavelength with temperature changes and fabrication tolerances. For example, Fig. 3 shows that, while a high quality factor is maintained for nine 2.5 μm radius ring resonators spread across an 8 in 130 nm

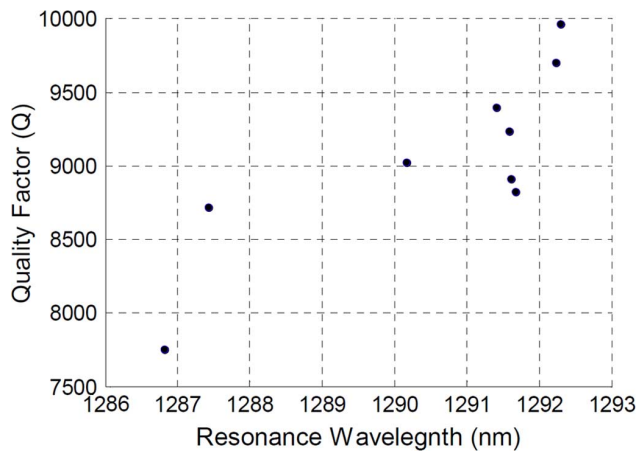


Fig. 3. Measured quality factor and resonance wavelength of nine 2.5 μm radius silicon ring modulators fabricated on an 8 in 130 nm CMOS SOI wafer.

CMOS-compatible silicon-on-insulator (SOI) wafer, the 5.48 nm resonance wavelength variation implies the need for a potentially wide resonance tuning range for robust operation. In order to relax this, system-level WDM channel-shuffling techniques are proposed that reduce the tuning to the order of FSR/N, where N is the WDM channel number [10], [15]. A commonly proposed resonance wavelength tuning technique is to adjust the device's temperature with a resistor implanted close to the photonic device to heat the waveguide, thus changing the refractive index [16], [17]. One potential issue with this approach is the tuning speed, which is limited by the device thermal time constant ($\sim$ms), may necessitate long

calibration time. Also, tuning power overhead can degrade overall link power efficiency [12], [17].

Achieving reliable and efficient operation in silicon photonic interconnect systems with large variations in link budget components, such as photonic device properties and interface parasitics, is another important consideration. The link budget determines the receiver sensitivity, with various front-end circuits proposed for optical interconnects, such as regulated-cascode transimpedance amplifiers (TIA) [21], [22], feedback TIAs [16], [18], [23], and integrating topologies [24], [25]. In the presence of variations, excessive sensitivity margins are often maintained for each channel to satisfy bit error rate (BER) under worst case conditions. Having individual scalability for each channel reduces necessary margins and, therefore, power consumption. One efficient approach to optimize receiver power efficiency versus data rate is to utilize supply scaling with CMOS inverter-based feedback TIAs [23]. However, in order to leverage this approach for large channel-count systems, efficient control loops with per-receiver voltage regulators are required that allow for self-adaptation to the desired data rate and link budget conditions.

While efficient clocking architectures for receiver-side data retiming and de-serialization are often neglected in optical interconnect designs [18], [23], they are necessary to form a complete link. One approach is to utilize a continuously running clock-and-data recovery (CDR) system [24] which allows the potential for plesiochronous operation between the transmitter and receiver. However, this generally consumes more power and area relative to mesochronous architectures which only require periodic training to optimize the receiver sampling position [16]. For mesochronous architectures, key considerations include achieving efficient receiver-side clock generation and sufficient jitter tracking of the incoming data to achieve the desired BER. Applying a forwarded-clock architecture, commonly used in electrical I/O systems [26], [27], in a photonic WDM system offers the potential for improved high frequency jitter tolerance with minimal jitter amplification due to the clock and data signals experiencing the same delay over the common low-dispersive optical channel.

This paper presents silicon photonic transceiver circuits for a ring resonator-based optical interconnect architecture that addresses limited modulator bandwidth, variations in ring resonator resonance wavelength and link budget, and efficient receiver clocking. The architecture of the transceiver circuits prototype is outlined in Section II. Section III describes transmitters with independent dual-edge pre-emphasis to compensate for the bandwidth limitations of the carrier-injection microring resonators used in this work. A novel bias-based resonance wavelength stabilization scheme for the modulators that offers advantages in tuning speed at comparable efficiency levels is presented in Section IV. Section V discusses an optical forwarded-clock adaptive sensitivity-power receiver that accommodates variations in input capacitance, modulator/photodetector performance, and link budget. Experimental results of the electrical transceiver circuits prototype, fabricated in a 65 nm CMOS technology and integrated via wire-bonding to photonic devices fabricated in a 130 nm SOI process, are presented in Section VI. Finally, Section VII concludes the paper.

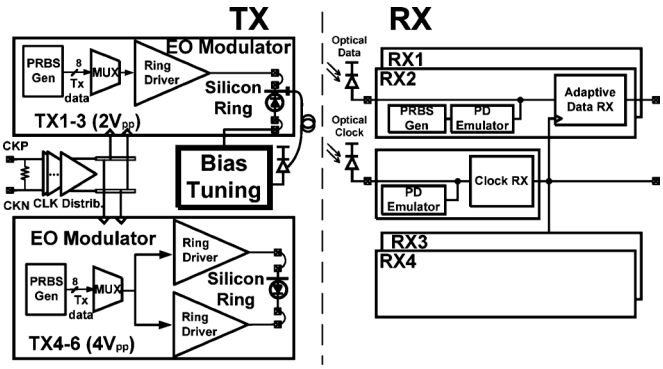


Fig. 4. Photonic transceiver circuits prototype block diagram.

II. Transceiver Circuits Prototype Architecture

Fig. 4 shows a block diagram of the CMOS photonic transceiver circuits prototype, with six transmitter and five receiver modules integrated in a 2 mm^2 65 nm CMOS die. At the transmitter side, a half-rate CML clock is distributed to the six transmitter modules where 8-bit parallel data is multiplexed to the full output data rate before being buffered by the modulator drivers. Two versions of the drivers are implemented. A differential driver, with approximately 0 V average bias level, provides a $4\mathrm{V_{pp}}$ output swing to allow for high-speed operation, while a single-ended driver provides a $2\mathrm{V_{pp}}$ output swing on the modulator cathode and utilizes a bias-tuning DAC on the anode for an adjustable DC-bias level. These drivers are wire-bonded to carrier-injection silicon ring resonator modulators (Fig. 2), where continuous wavelength light near 1300 nm from a tunable laser is vertically coupled into the photonic device's input port. The modulated light is then coupled from the modulator's through port into a single-mode fiber for routing to the bias-based tuning photodetector used to stabilize the resonant wavelength and to the optical receiver modules for high-speed data recovery. At the receiver side, data is recovered by adaptive inverter-based TIA front-ends that trade-off power for varying link budgets by employing on-die eye monitors and scaling the TIA supplies for the required sensitivity. The receive-side sampling clocks are produced from an optically-forwarded quarter-rate clock which is amplified by a fixed-supply TIA before being passed to an injection-locked oscillator which produces four quadrature clocks that are routed to the four receiver data channels.

III. Nonlinear Pre-Emphasis Modulator Driver Transmitters

While carrier-injection silicon ring modulators are capable of high extinction ratio operation in a low area footprint, the operating speed is limited by relatively slow carrier dynamics in forward-bias and parasitic contact resistance in reverse-bias. Fig. 5 shows device model simulation results of the carrier-injection silicon microring modulators used in this work, with positive and negative 200 ps pulse responses overlaid. Observe that a simple $2\mathrm{V_{pp}}$ waveform yields a high extinction ratio, but the optical rise time is excessively long due to the carrier recombination lifetime [3]. Increasing the modulation voltage to $4\mathrm{V_{pp}}$ dramatically improves the optical rise time at the expense of

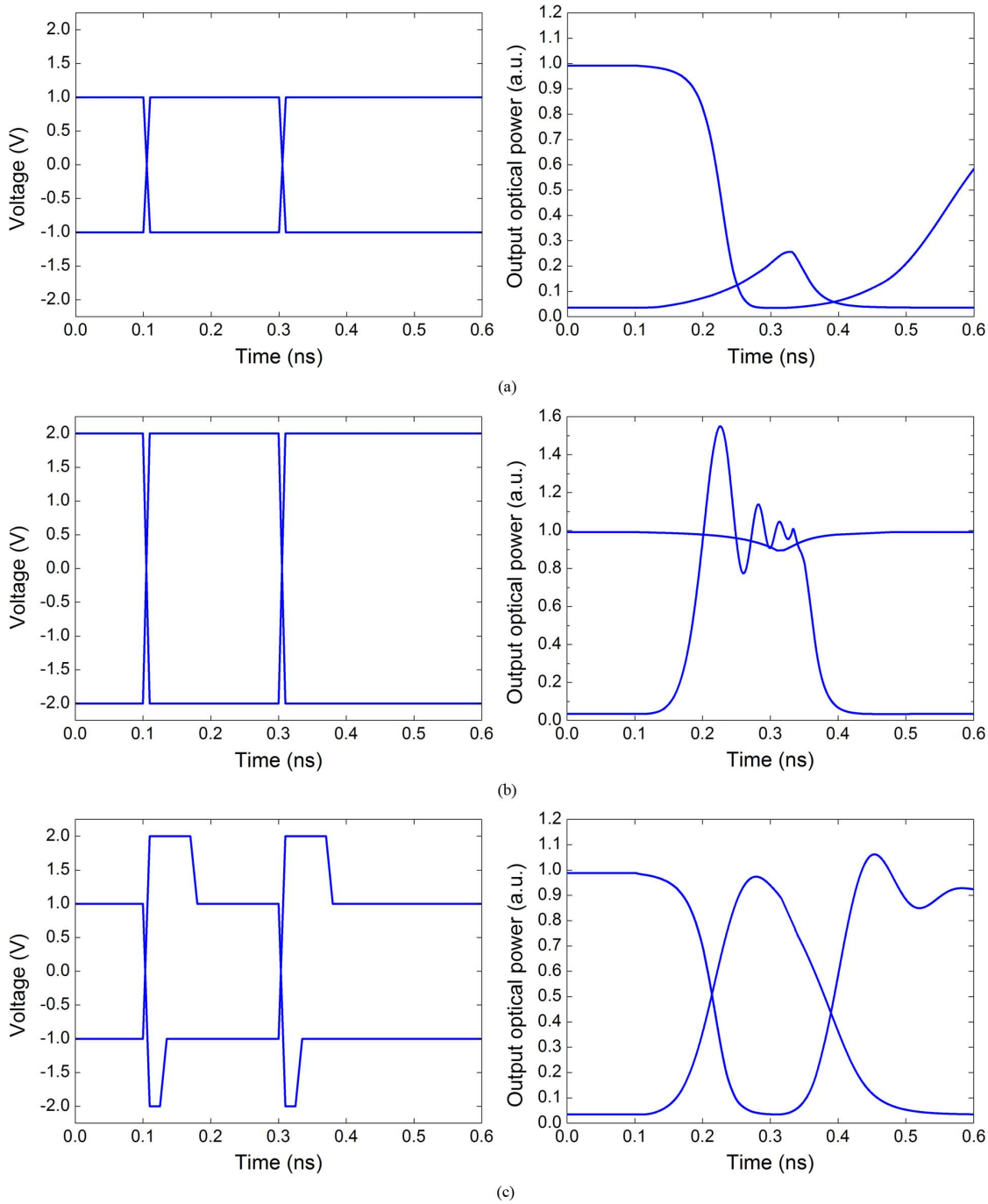


Fig. 5. Simulated carrier-injection ring resonator modulator response to 200 ps data pulses with: (a) $2V_{pp}$ simple modulation, (b) $4V_{pp}$ simple modulation, and (c) $4V_{pp}$ modulation with pre-emphasis.

high-level ringing and a high steady-state charge value. Unfortunately, this large amount of charge results in a slow optical fall time due to the modulator's series resistance limiting the drift current to extract the excess carriers in the junction. The conflicting requirements for fast rising and falling transitions are addressed through the use of a pre-emphasis waveform [3]. During a rising-edge transition the positive voltage overshoots (2 V) for a fraction of a bit period to allow for a high initial charge before settling to a lower voltage (1 V) corresponding to a reduced steady-stage charge. A similar shaped waveform is used for the falling-edge transition to increase the drift current to extract the carriers. As the rising and falling-edge time constants are different, a nonlinear modulation waveform is applied. This work adjusts the amount of over/under-shoot time of the pre-emphasis waveform for a specific modulator, with the rising-edge pre-emphasis pulse typically wider than the falling-edge. Adjusting the pre-emphasis time, rather than utilizing different voltage levels, allows the optimization of the transient response to be decoupled from the steady-state extinction ratio value.

As shown in the block diagram of Fig. 6(a), two optical transmitter versions are developed to demonstrate high-speed operation with a differential $4V_{pp}$ output driver and explore

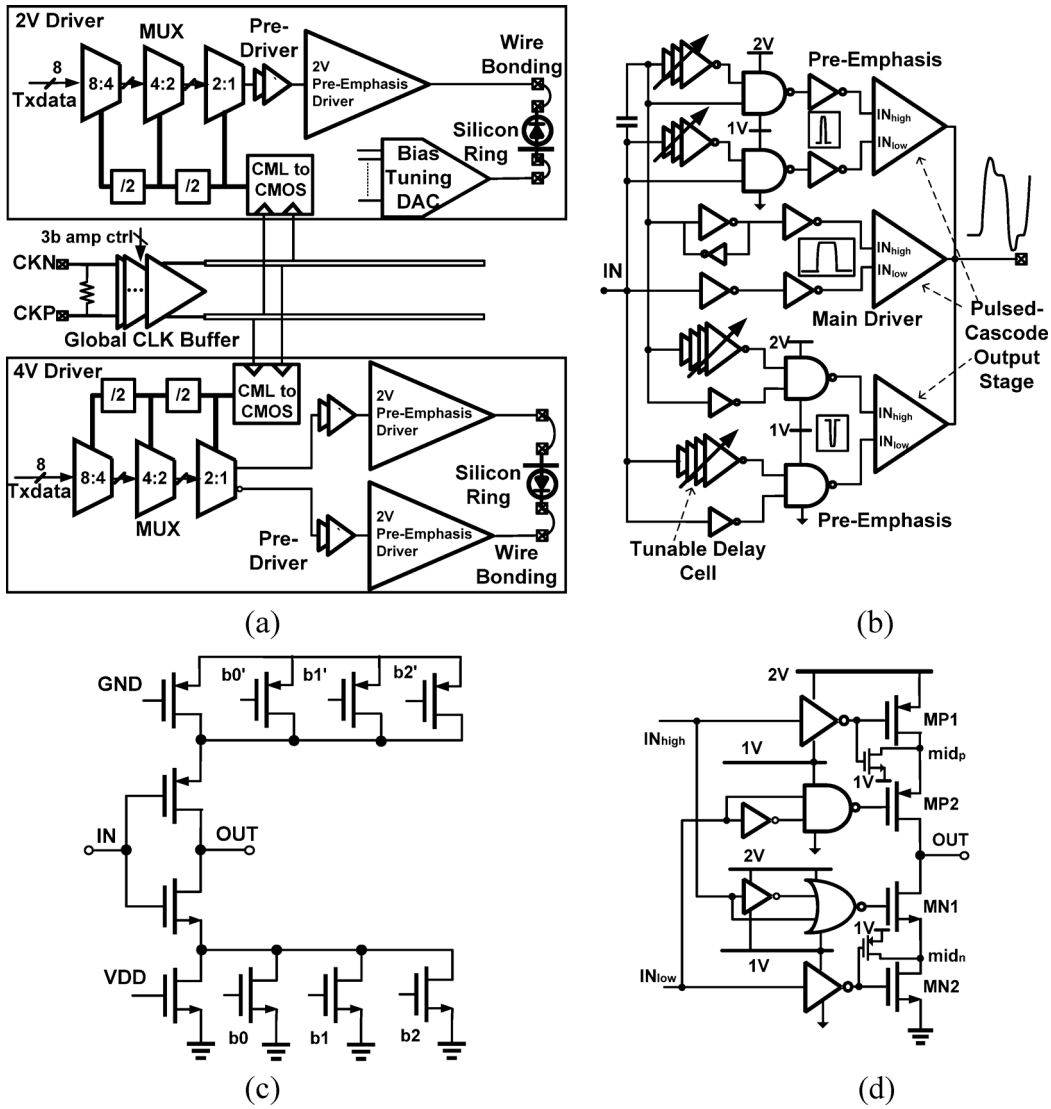
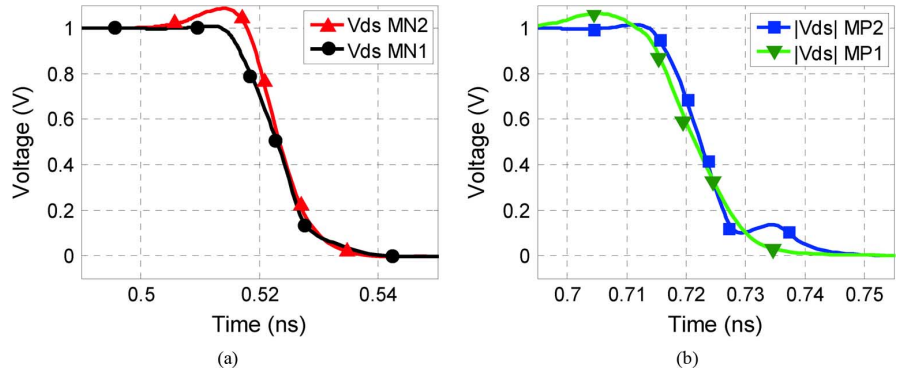


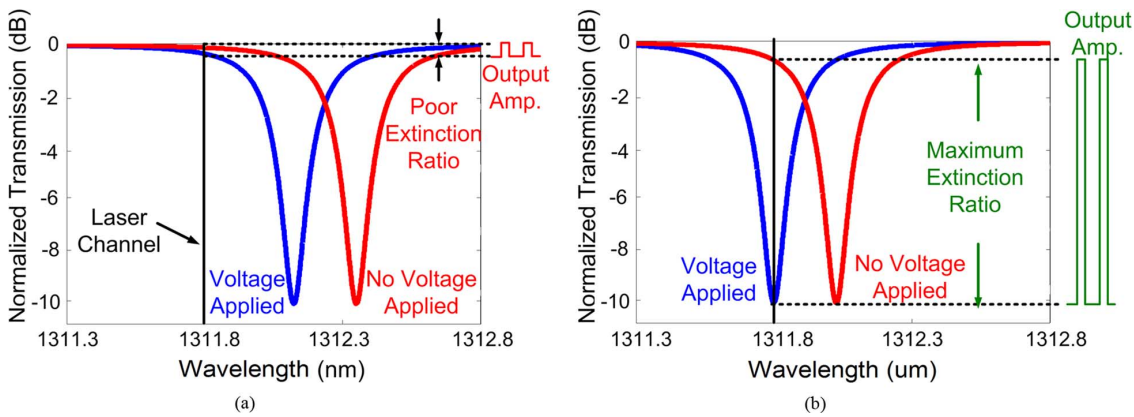
Fig. 6. Nonlinear pre-emphasis modulator driver transmitters: (a) transmitter block diagrams, (b) per-terminal 2 V pre-emphasis driver, (c) tunable delay cell, and (d) pulsed-cascode output stage.

bias-based modulator tuning capabilities with a single-ended $2V_{pp}$ output driver. Serialization of eight bits of parallel input data is performed in both transmitter versions with three 2:1 multiplexing stages, with the serialization clocks generated from a half-rate CML clock which is distributed to six transmitter modules, converted to CMOS levels, and subsequently divided to switch the mux stages. The serialized data is then transmitted by the modulator drivers, with both output stage versions utilizing a main driver, positive-edge and negative-edge pre-emphasis pulse drivers in parallel [Fig. 6(b)] to generate the pre-emphasis output waveform. Tunable delay cells, implemented with digitally adjustable current-starved inverters [Fig. 6(c)], allow for independent control of the rising and falling-edge pre-emphasis pulse duration over a range of 20–100 ps. While not implemented in this prototype, utilizing an adaptive tuning approach for the pre-emphasis settings can ensure robust operation across process, voltage, and temperature variations. This could potentially be implemented in a manner similar to transmit pre-emphasis tuning in electrical links with a back-channel [28] by utilizing threshold information available from the adaptive receiver eye monitor system, discussed in Section V. Finally, pulsed-cascode output stages [Fig. 6(d)] with only thin-oxide core devices [29] reliably provide a final per-terminal output swing of twice the nominal 1 V supply. A capacitive level shifter and parallel logic chain generate the signals $\mathrm{IN_{low}}$, swinging between GND and the nominal VDD, and $\mathrm{IN_{high}}$, level-shifted between VDD and 2*VDD, that drive the final pulsed-cascode output stages. During an output transition from high to low, the $\mathrm{IN_{low}}$ input switches MN2 to drive node $\mathrm{mid_n}$ to near Gnd and the $\mathrm{IN_{high}}$ input triggers a positive pulse from the level shifted NOR-pulse gate that drives the gate of MN1 to allow the output to begin discharging at roughly the same time that the MN1 source is being discharged. As shown in the simulation results of Fig. 7, the $\mathrm{V_{ds}}$ voltages of both output nMOS transistors does not exceed more than 10% of the nominal 1 V supply. Similarly, during an output transition from low to high, the $\mathrm{IN_{high}}$ input switches MP1 to drive node $\mathrm{mid_p}$ to near 2 V and the $\mathrm{IN_{low}}$ input triggers a negative pulse from the NAND-pulse gate that drives the gate of MP2 to allow the output to begin discharging



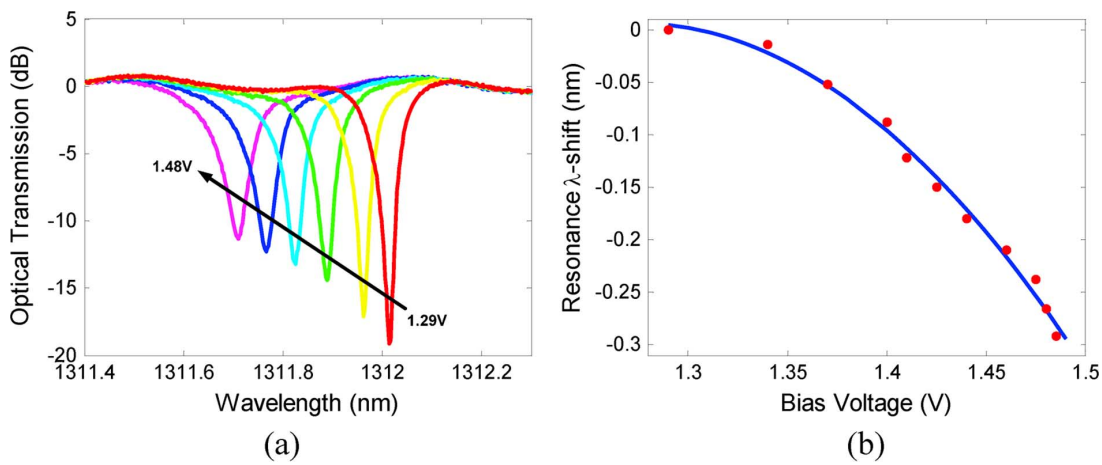
(a) (b)

Fig. 7. Transient simulation of pulsed-cascode output stage: (a) nMOS V_{ds} for output falling transition, and (d) pMOS $|V_{ds}|$ for output rising transition.



(a) (b)

Fig. 8. Ring resonator modulator transmission curves with high and low modulation voltage levels when (a) resonance wavelength is not aligned with input laser wavelength and (b) resonance wavelength is aligned with input laser wavelength.



(a) (b)

Fig. 9. Measured carrier-injection ring resonator modulator performance. (a) Optical transmission spectrum at different bias levels. (b) Resonance wavelength shift versus bias voltage.

at roughly the same time that the MP2 source is being charged. Simulations also verify that the $|V_{ds}|$ of both output pMOS transistors does not exceed more than 10% of the nominal 1 V supply.

IV. Automatic Bias-Based Wavelength Stabilization

One problem with silicon ring resonators is that their resonance wavelength is sensitive to temperature variation and fabrication tolerances. As shown in Fig. 8, a poor extinction ratio results when the modulator's resonance is not aligned with the input continuous-wave laser wavelength. Hence, a closed-loop adaptation scheme is therefore necessary to stabilize the ring's resonance to match the input laser. Thermal tuning schemes with closely integrated heating resistors [12], [17], [30]–[32], which red-shift the resonance wavelength as the device is heated up, are commonly proposed for this tuning. However, thermal time constants in the ms-range limit the speed of this tuning approach. Another important consideration is the tuning power

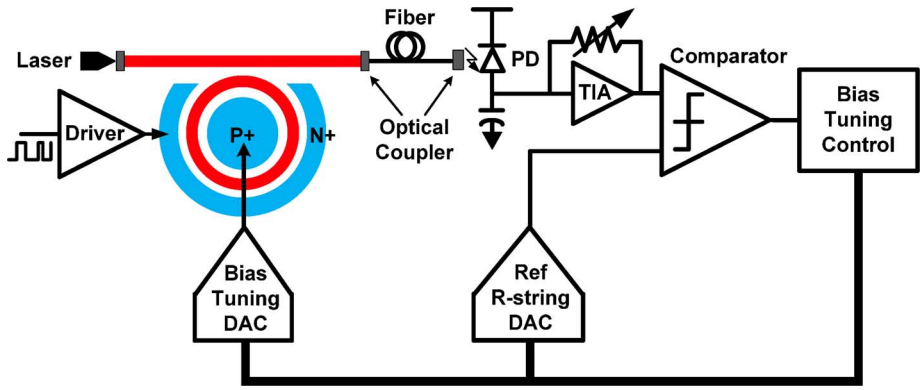


Fig. 10. Bias-based ring resonator modulator semi-digital wavelength stabilization loop.

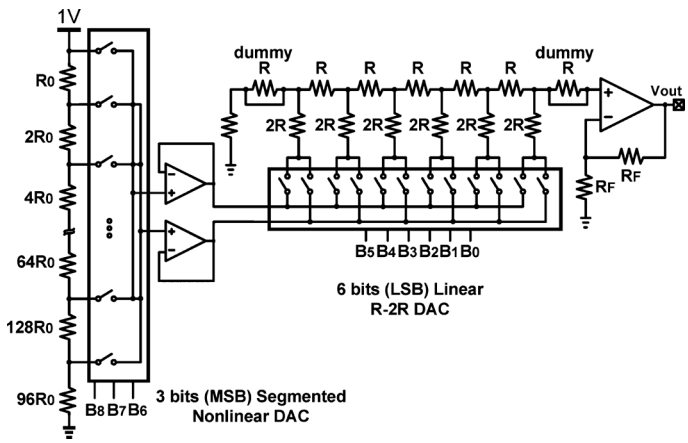


Fig. 11. 9-bit nonlinear bias tuning DAC.

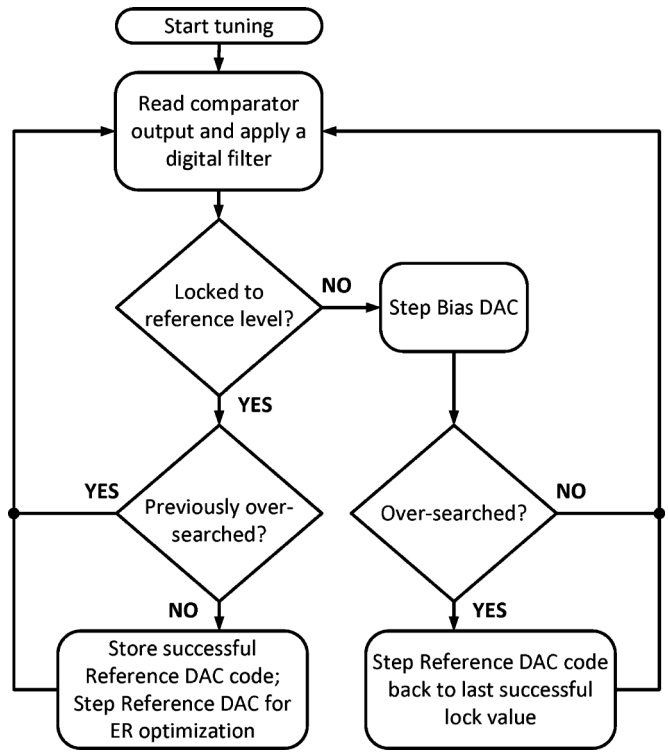


Fig. 12. Ring resonator bias-based tuning algorithm.

efficiency, which varies for thermal tuning depending on the fabrication complexity. Doping a section of the ring waveguide differently to realize a thermal resistor is relatively simple, but has been shown to have a relatively poor 42 μW/GHz tuning efficiency [12]. Improved efficiencies near 10–15 μW/GHz have been demonstrated using approaches such as substrate removal and transfer for an SOI process [30] and deep-trench isolation for a bulk CMOS process [17]. Finally, superior efficiencies in the 1.7–2.9 μW/GHz have been achieved with localized substrate removal or undercutting [31], [32], but this comes at the cost of complex processing steps.

Compared with the conventional heater-based tuning approaches, the proposed bias-based tuning method of this work has advantages of fast tuning speed and flexibility in the tuning direction, while displaying comparable tuning efficiency. As shown in Fig. 9, increasing the resonator p-i-n diode anode voltage causes the resonance wavelength to blue-shift to shorter wavelengths due to the accumulation of free carriers in the ring waveguide. This provides the potential for a very fast tuning mechanism. While some optical loss and quality factor reduction is observed with increased forward-bias due to the additional carriers, an extinction ratio in excess of 10 dB is achieved for a 190 mV tuning range. Note that at the bias point with a minimum $Q = 9100$, this allows for less than 1 dB crosstalk at a tight 24 GHz channel spacing or 0.2 dB crosstalk at a typical 50 GHz spacing. As the quality factor (Q) of a micro-cavity is mainly governed by the cavity loss (e.g., bending loss, intrinsic material loss, and scattering from surface roughness) and the external waveguide coupling, improved processing and careful design of the gap and waveguide width [33] can lead to higher Q values and either reduced crosstalk or tighter allowable channel spacing.

Fig. 10 shows the semi-digital control loop for the bias-based resonator tuning approach which is utilized with the $2V_{pp}$ transmitters. A monitor PD and low-bandwidth TIA is used to sense the average resonator power levels for comparison with a DAC-programmable reference level. This comparator output signal is digitally filtered by a bias tuning control finite-state machine that adjusts the setting of the bias tuning DAC that drives the resonator anode terminal, while the $2V_{pp}$ high-speed modulation signal is applied at the resonator cathode terminal. Fig. 11 shows the schematic of the 9-bit segmented bias DAC, which

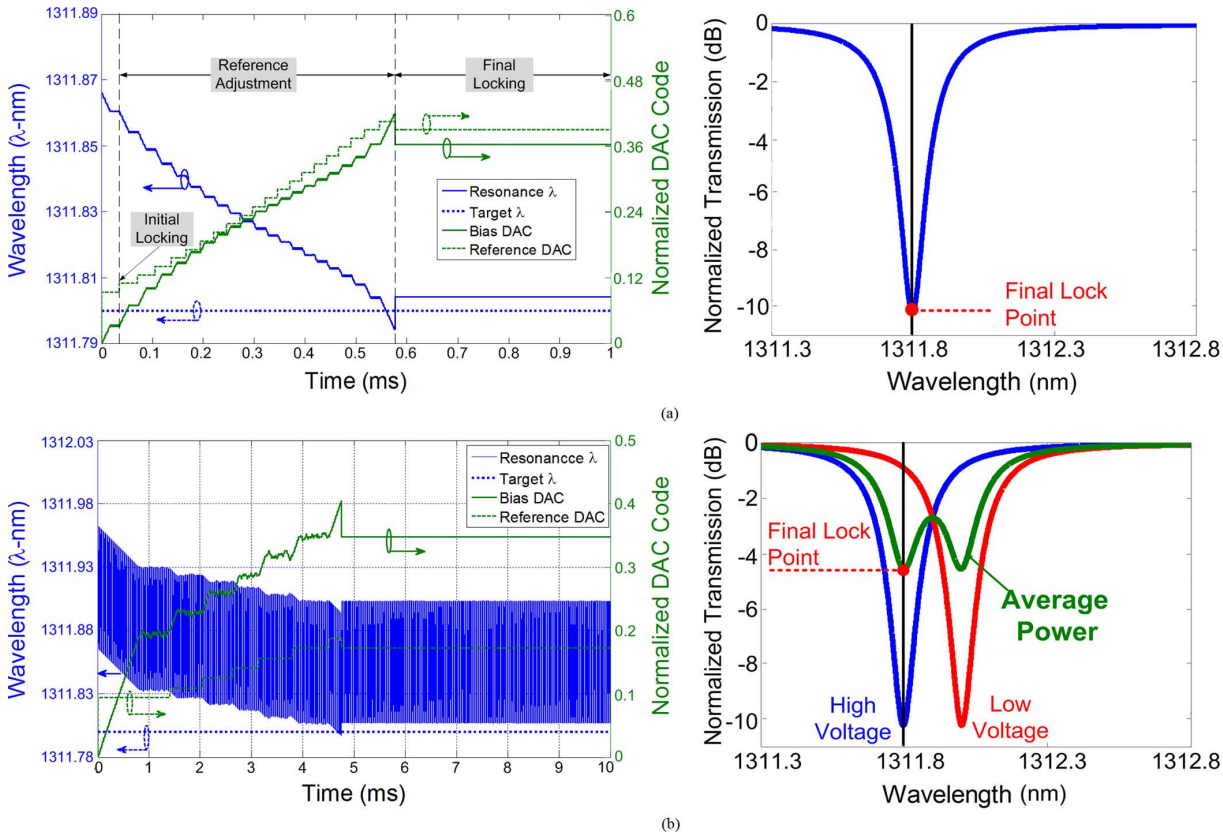


Fig. 13. Simulated tuning waveforms and final optical transmission curves for (a) static tuning mode and (b) dynamic tuning mode.

utilizes a coarse 3-bit nonlinear R-string DAC to match the p-i-n I–V characteristics and a fine 6-bit linear R-2R DAC.

The flowchart of Fig. 12 and simulation results of Fig. 13 summarize the bias tuning system operation, which can operate both in a static tuning mode with a constant maximum forward-bias across the modulator and a dynamic tuning mode with the modulator driven with a random data signal. For simplicity, first consider the static tuning of Fig. 13(a). The tuning system works by initially locking the monitor PD and low-bandwidth TIA output to a conservative reference DAC voltage that maps to a reliable point on the resonator curve. This implies that the voltage is not too high to avoid locking to any small fluctuations in the flat region of the resonator transmission curve and not too low such that it maps to below the resonance null value. After an initial lock is achieved, the reference DAC code is saved as a successful lock point and adjusted in order to maximize the extinction ratio. Since the current system monitors the modulator through-port power, the objective is to minimize the received power to obtain the maximum extinction ratio. As illustrated by the stair-step curves in the simulation results, the tuning procedure then undergoes several cycles of locking and reference level adjustment until the loop "over-searches" and can no longer lock to a minimum power point. The system then steps back to the last successful reference level to obtain the final lock point near the target resonance wavelength and achieve an extinction ratio near 10 dB with a 0.9 dB insertion loss. While not an issue with the carrier-injection ring resonator devices used in this work, in maximizing the extinction ratio this algorithm does has the potential to lock in a region with increased insertion loss. In the event this happens, it is possible to disable the extinction ratio optimization procedure and simply lock to a fixed DAC reference that maps to a point in the resonator transmission curve that balances extinction ratio and insertion loss. Tuning with randomly modulated data [Fig. 13(b)], which obviates bringing the link down, is achieved by utilizing the same procedure. Note that the convergence time increases due to higher digital filtering for sufficient optical power averaging. Also, in order to achieve a similar extinction ratio in dynamic-tuning mode, the modulated resonance shift, $\Delta\lambda_{\text{shift}}$, between data "0" and data "1" should be larger than the resonator's full-width half-maximum $\text{FWHM} = \lambda_0/Q$, as shown in Fig. 14.

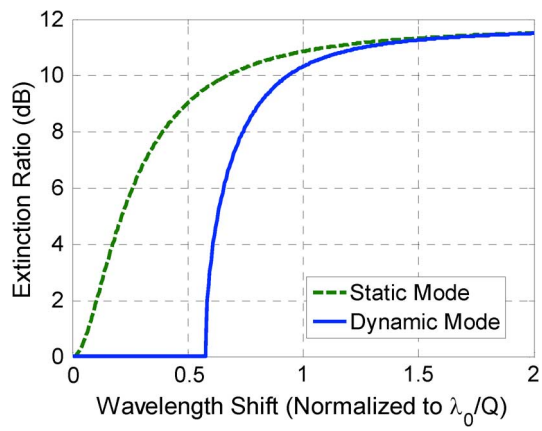


Fig. 14. Extinction ratio versus modulated wavelength shift for static and dynamic tuning modes.

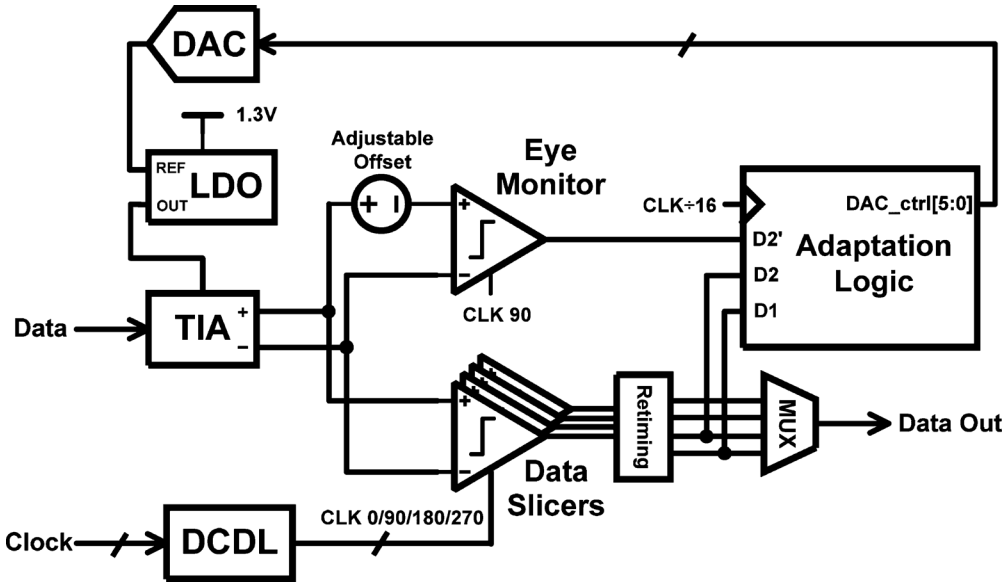


Fig. 15. Adaptive sensitivity-power data receiver.

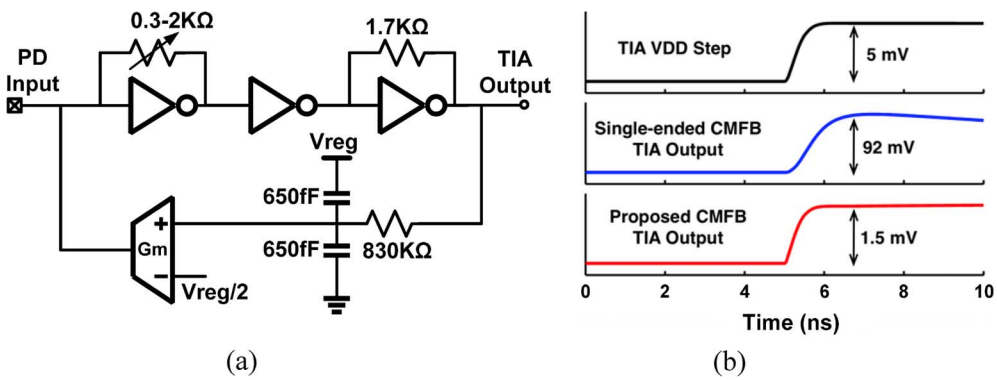


Fig. 16. Inverter-based TIA front-end. (a) Schematic. (b) Simulated TIA common-mode output response to a 5 mV power supply step.

Note that while these simulation results and the experimental tuning results of Section VI are obtained by monitoring the modulator through-port, perhaps a more efficient approach for silicon photonic systems is to use an additional drop-port waveguide coupled to the ring modulator that has a waveguide PD for local power monitoring. This is accommodated in the current tuning system state machine via digital control to switch to drop-port monitoring mode, where the optical power is maximized to lock to the resonance point.

V. Optical Forwarded-Clock Adaptive Receiver

As shown in Fig. 15, the data-channel receivers consist of an inverter-based TIA front-end followed by a bank of four quadrature-clocked comparators whose offsets are digitally calibrated to optimize receiver sensitivity. The quadrature sampling clocks, generated from an optical forwarded-clock receiver, are passed through a local digitally-controlled delay line for timing margin optimization and phase-spacing calibration. An additional parallel comparator with a 6 bit programmable threshold is introduced that serves as an eye monitor, setting the minimum voltage margin needed to correctly slice the input signal for a required BER. By comparing its output with the normal data comparator on the same clock phase, eye-closure can be detected before a bit error actually occurs. This information is used to control a 6 bit R-2R voltage DAC that sets the LDO-generated TIA supply voltage to the minimum level required to achieve the sensitivity and bandwidth for a given BER.

Fig. 16 shows the TIA front-end [23], which consists of three inverter stages with resistive feedback in the first and third stages. These inverter stages are biased around the trip-point for maximum gain with an offset control loop that subtracts the average photocurrent from the input node. The front-end's power supply level has a significant impact on gain, bandwidth, and noise performance [23], allowing for an efficient mechanism to trade-off receiver sensitivity with power consumption. However, excessive fluctuations can result in the front-end output common-mode variation if a simple single-ended low-pass filter is used in the offset control loop, which can impact overall receiver sensitivity. In order to reduce this common-mode variation, the feedback RC filter capacitor is split into equal decoupling to ground and the adaptive supply. The RC filter bandwidth is set to be 150 kHz, which is estimated to support a $2^{16} - 1$ PRBS pattern at 10 Gb/s. If a system is required to support longer run-length data patterns, techniques similar to the low-frequency equalizers [34] and baseline-wander correction circuits [35] used in electrical links offer potential solutions.

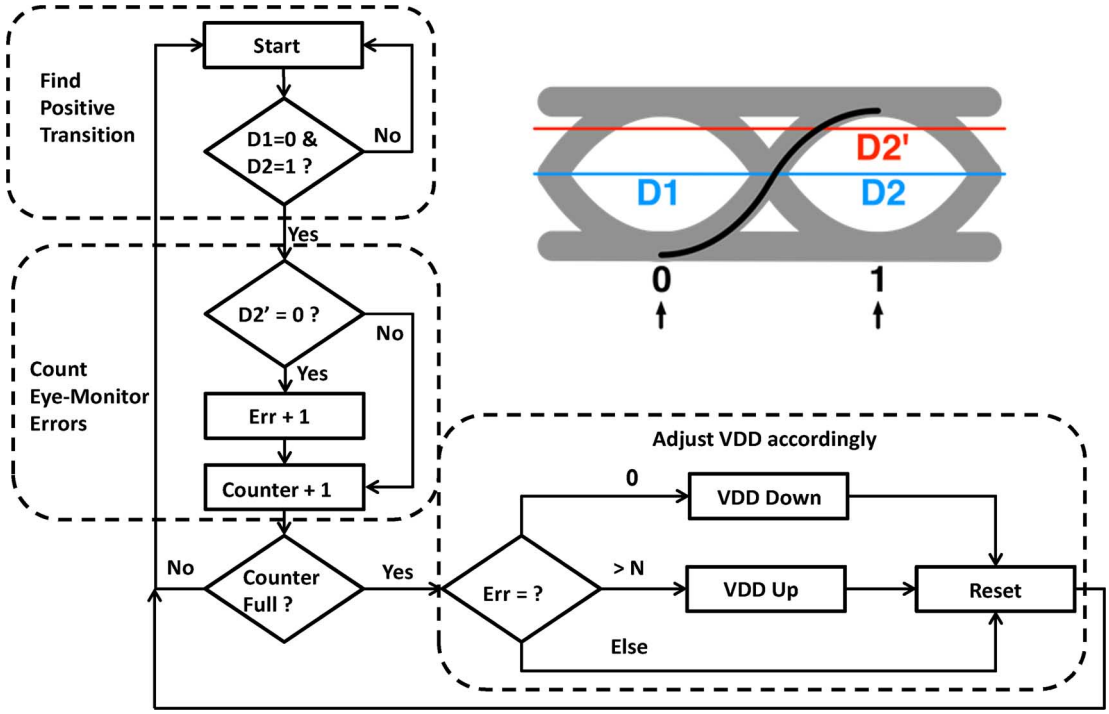


Fig. 17. Optical receiver sensitivity-power adaption algorithm.

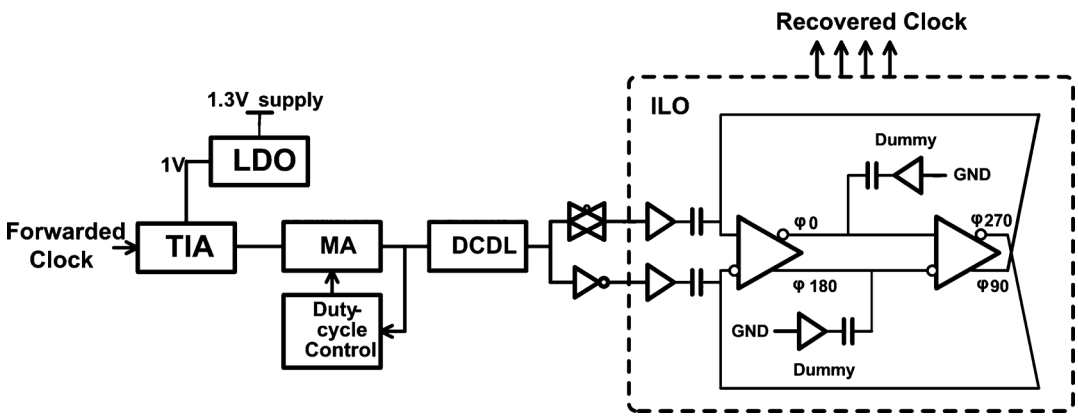
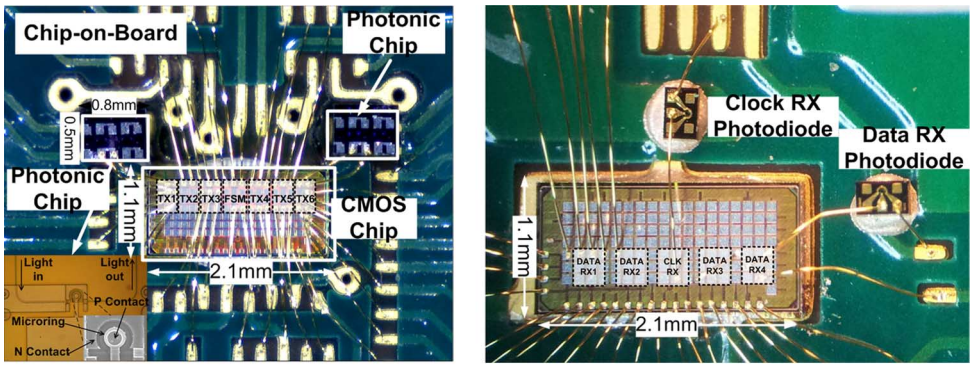


Fig. 18. Optical clock receiver.

A differential transconductance stage then amplifies the difference between this filtered node and half the adaptive supply to produce the offset correction current. This reduces the output common-mode disturbance with a 5 mV power supply step from 92 mV with a simple single-ended low-pass filter to 1.5 mV with the adaptive-supply referenced implementation.

The optical receiver sensitivity-power adaptation is done partially with a software-controlled outer loop that monitors the BER and adjusts the voltage margin with the eye-monitor comparator threshold through a serial test interface and an on-chip state machine that scales the front-end power supply level. Fig. 17 summarizes the eye monitor and supply scaling state machine. The adaptation algorithm captures two consecutive bits D1 and D2, and proceeds only with a "01" pattern for the worst case ISI condition. Next, the data comparator output (D2) is compared with eye monitor output (D2') on the same clock phase, and an error is recorded if there is a difference. After a certain amount of total bits, a decision is made to reduce the power supply if no error is observed, or increase the power supply if the error rate exceeds a preset threshold. In order to minimize dithering without the overhead of a large averaging counter, the power supply does not change if the error rate is below a certain threshold.

Fig. 18 shows a block diagram of the clock receiver, which utilizes the same inverter-based TIA front-end, but with a constant 1 V supply for minimal jitter. The TIA output is amplified to full CMOS levels by a multi-inverter stage main amplifier (MA) that also contains a duty-cycle control loop. Global skew adjustment between the clock and data channels is achieved by a subsequent digitally controlled delay line, which provides approximately 130 ps de-skew range. This single-ended clock is then converted from singled-ended to differential full-rail signals for injection by ac-coupling into a two-stage differential oscillator that generates the quadrature clocks that are distributed



(a) (b)

Fig. 19. Optical transceiver circuits prototype bonded for electrical characterization and optical testing. (a) Optical transmitter configuration with silicon ring resonator modulators. (b) Optical receiver configuration with commercial photodetectors.

to the four data receiver channels. The ILO has dummy injection buffers to reduce the quadrature mismatch caused by the differential injection, with post-ILO per-phase tunable delay buffers providing additional skew compensation. A relatively wide injection locking range of ∼100 MHz is achieved, with the free-running frequency set manually in this prototype via tuning of the tail current source. While not implemented in this prototype, a periodically activated control loop could set the ILO free-running frequency equal to the injection clock [36] to reduce quadrature phase errors and provide increased robustness to PVT variations.

VI. Experimental Results

The optical transceiver circuits prototype was fabricated in a 65 nm CMOS general purpose process. As shown in the photographs of Fig. 19, a chip-on-board test setup is utilized, with the CMOS die wire-bonded both to PCB traces for electrical characterization and to silicon ring resonator chips and commercial photodetectors for optical testing. Different bonding configurations are used for transmitter and receiver characterization.

In order to verify the functionality of the pre-emphasis transmitters, electrical characterization is performed with the $2V_{pp}$ and $4V_{pp}$ transmitters driving a single-ended 50 Ω and differential 100 Ω termination, respectively. Fig. 20 shows $2^7 - 1$ PRBS electrical eye diagrams with minimum and maximum pre-emphasis settings for the $2V_{pp}$ transmitter module, which operates error-free up to 9 Gb/s, and the $4V_{pp}$, which achieves 8 Gb/s operation. A clear over/undershoot is observed for both drivers with the maximum pre-emphasis settings enabled. Note, for these electrical eye diagrams, the lack of driver output impedance control and the relatively long bond wires introduces some additional reflection-induced ISI. In both cases the maximum electrical data rate is limited by attenuation in the on-chip global clock distribution path.

For high-speed optical testing, a continuous-wavelength laser is vertically coupled to a waveguide connected to a silicon ring resonator which is driven by a $4V_{pp}$ transmitter. The current version of the grating coupler used in this work exhibits 7 dB loss/port due to the simplified structure of the grating undergoing etching at the same time as the waveguide. In future work, further improvement can be achieved with more sophisticated two-mask gratings which have demonstrated loss down to 2–3 dB [37]. The waveguide loss is measured to be 3 dB/cm, which is negligible for the ∼500 μm waveguide. Overall, with 1 mW optical power from the CW laser source, around 40 μW is detected at the ring's through-port output when the ring is on off-resonance. After vertically coupling the modulated light out into a single-mode fiber, the light is observed with an optical oscilloscope to produce the 5 Gb/s eye diagrams of Fig. 21. The eye is completely closed with the minimum pre-emphasis settings, while optimizing the pre-emphasis settings allows for an open eye with a 12.7 dB extinction ratio. Here the maximum optical data rate is limited to 5 Gb/s due to the unanticipated excessive contact resistance (∼2 kΩ) of the ring resonator modulator. Improving the modulator device contact resistance to more reasonable values (∼200 Ω) is a point of emphasis for future planned prototypes.

The bias-based resonance wavelength tuning effectiveness is demonstrated with two different ring resonator modulators with 0 V-bias resonance wavelengths of 1287.01 and 1312.06 nm. Fig. 22(a) shows the effectiveness of this bias-based control, with the extinction ratio improving from 1.8 dB to 11.0 dB after activating the tuning loop to lock to a 1286.93 nm laser wavelength. A high extinction ratio is maintained as a given ring is tuned over different wavelengths, as shown by Fig. 22(b) where the bias-based tuning loop is able to lock to input wavelengths spaced by 0.1 nm and obtain extinction ratios in excess of 11 dB. The overall tuning range is 0.28 nm for a tuning power of 340 μW, which results in a tuning efficiency of 6.8 μW/GHz. Note, this tuning power includes the entire tuning feedback loop of Fig. 10. Here the speed is limited to 500–800 Mb/s due to the bias-based tuning being implemented with the $2V_{pp}$ driver. Improving the excessive 2k Ω contact resistance of the current ring resonator modulator to a more reasonable sub-100 Ω value should allow for simultaneous high-speed modulation and bias-based tuning capabilities. Given ring resonator devices display typical thermal time constants on the order of 100 μs [31], any data-induced deterministic thermal effects should be adequately filtered for PRBS patterns near $2^{17} - 1$. However, if a system is required to support longer run-length data patterns, this may impact the tuning performance. Techniques similar to the low-frequency equalizers [34] and baseline-wander correction circuits [35] used in electrical links offer potential

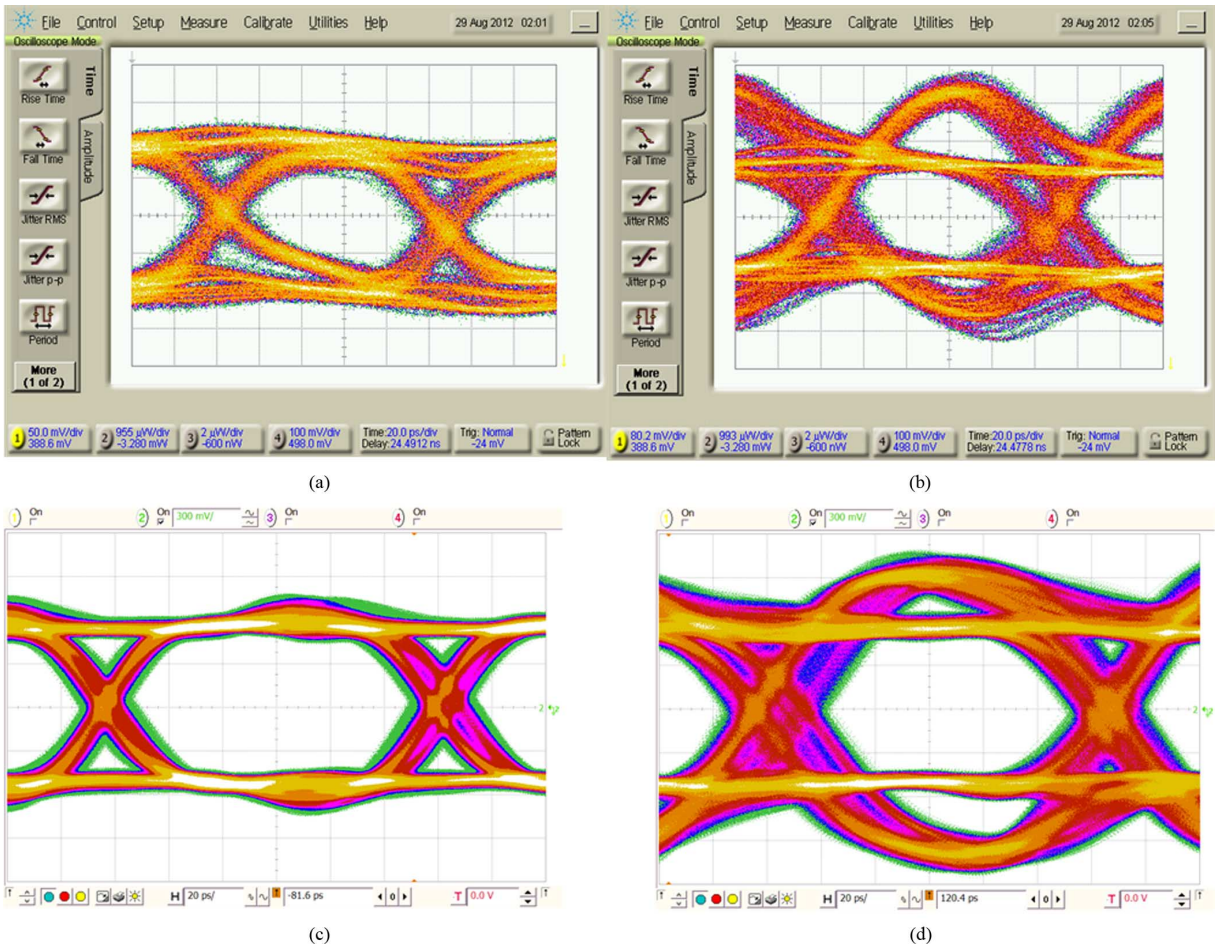


Fig. 20. Modulator drivers' electrical eye diagrams. 9 Gb/s operation with $2V_{pp}$ driver with (a) minimum pre-emphasis and (b) maximum pre-emphasis. 8 Gb/s operation with $4V_{pp}$ driver with (c) minimum pre-emphasis and (d) maximum pre-emphasis.

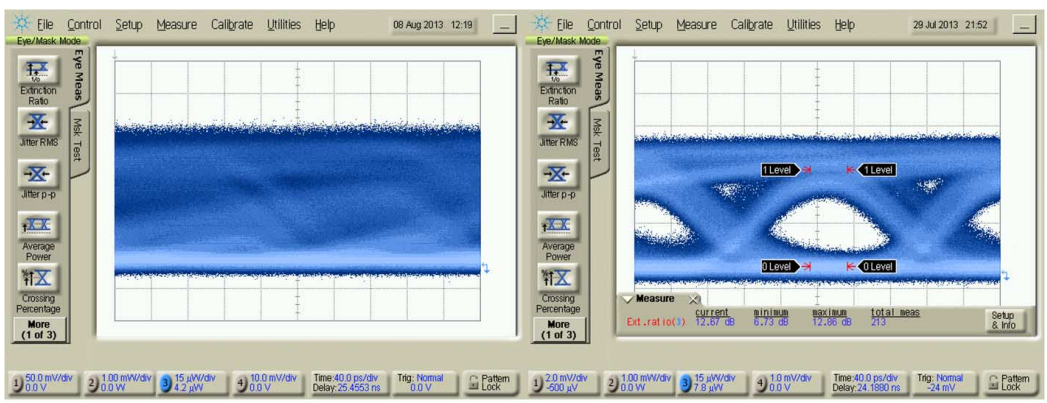


Fig. 21. 5 Gb/s optical eye diagrams with silicon carrier-injection ring resonator modulators driven by the $4V_{pp}$ transmitter. (a) Minimum pre-emphasis settings. (b) Optimized pre-emphasis settings.

solutions to compensate for any low-frequency data-induced thermal effects.

In order to characterize the optical performance of the data receiver, an externally-modulated laser source is vertically coupled to a 150 fF Cosemi LPD3012 photodiode which is wire-bonded to the receiver input. This photodiode displays 1.0 A/W responsivity at 1310 nm. The Fig. 23 BER measurements with an Anritsu MP1800A signal quality analyzer show that when the nominal 1 V front-end power supply is utilized, a sensitivity of -9 dBm is achieved at 8 Gb/s for a $\mathrm{BER} = 10^{-9}$ with a $2^7 - 1$ PRBS data pattern. Relaxing the input sensitivity by $\sim$2 dB with increased optical input power enables the adaptive TIA supply to decrease by 4%, resulting in a 14% reduction in TIA power. As the data rate and BER performance of the current

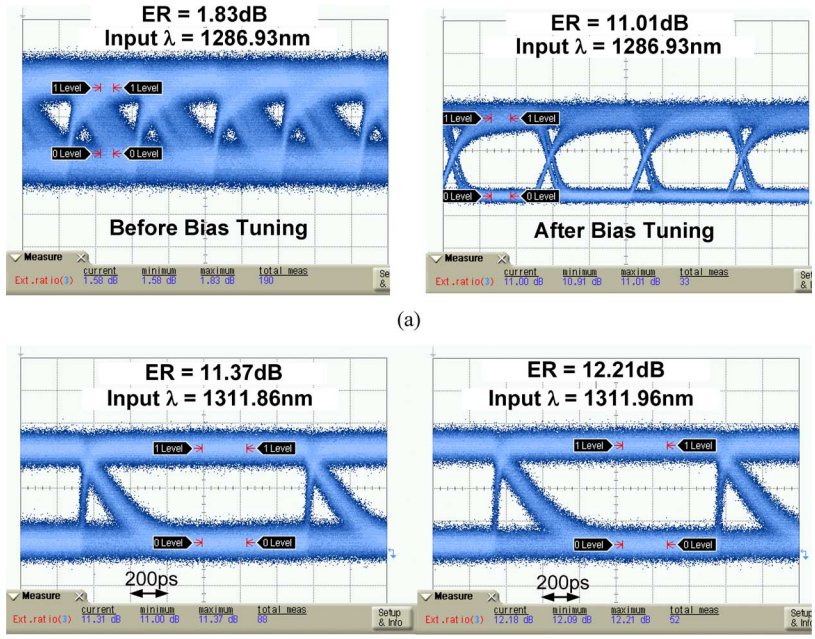


Fig. 22. Ring resonator bias-based wavelength stabilization measurements. (a) Ring #1's 500 Mb/s eye diagrams demonstrating the automatic bias tuning stabilizing to 1286.93 nm. (b) Ring #2's 800 Mb/s eye diagrams with input laser wavelengths of 1311.86 and 1311.96 nm.

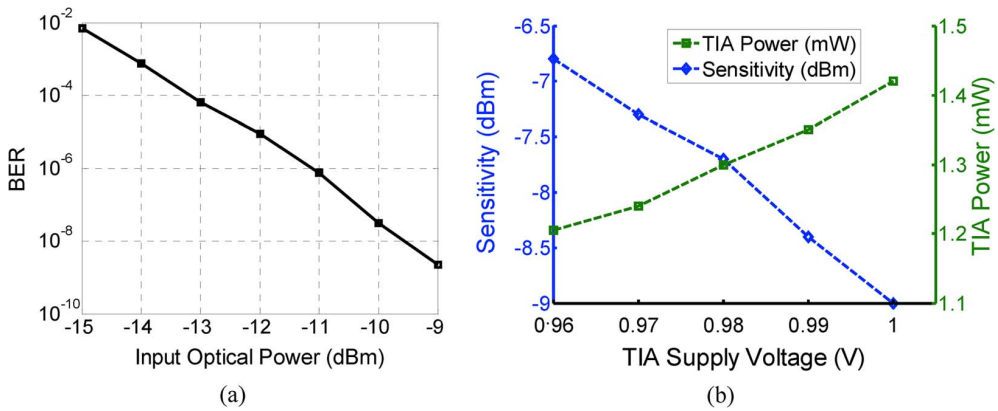


Fig. 23. 8 Gb/s receiver measurements. (a) BER versus input optical power with a 1 V power supply. (b) Sensitivity ($\mathrm{BER} = 10^{-9}$) and power versus TIA supply voltage.

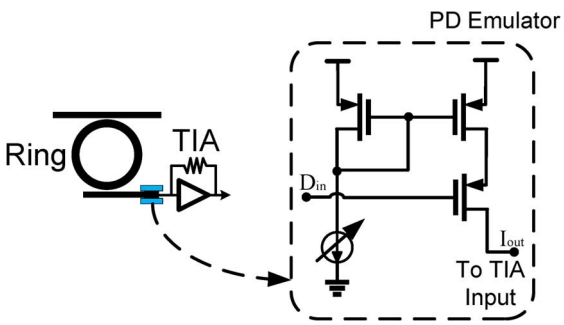


Fig. 24. Integrated photodetector emulator circuit.

optical characterization are limited by ∼1.5 mm bondwires and ∼200 fF total capacitance, an on-chip current source (Fig. 24) is used to emulate a high-speed waveguide photodetector capable of being tightly integrated with the optical receiver, either in a monolithic manner [15], [18] or with microsolder bonding [16]. This test structure allows for receiver benchmarking and motivates future planned prototypes with microbump integration and Ge waveguide photodetectors in the same 130 nm SOI photonics process as the ring modulators/filters. Note that an improved version of this photodetector emulator circuit would also include programmable input capacitance values to investigate the impact of different integration approaches. Fig. 25 shows that this enables operation at a higher data rate of 10 Gb/s with an improved sensitivity of -18 dBm at a $\mathrm{BER} = 10^{-12}$, assuming a unity responsivity. This on-chip test setup also enables a wider range of supply scaling, with the automated control loop reducing the TIA power ∼40% as the input current is scaled from 16 to 60 μA with a 50–100 mV eye monitor margin. Refining the control state machine and using a more aggressive margin level could potentially achieve even more power savings, as overriding the automated control loop yields ∼60%

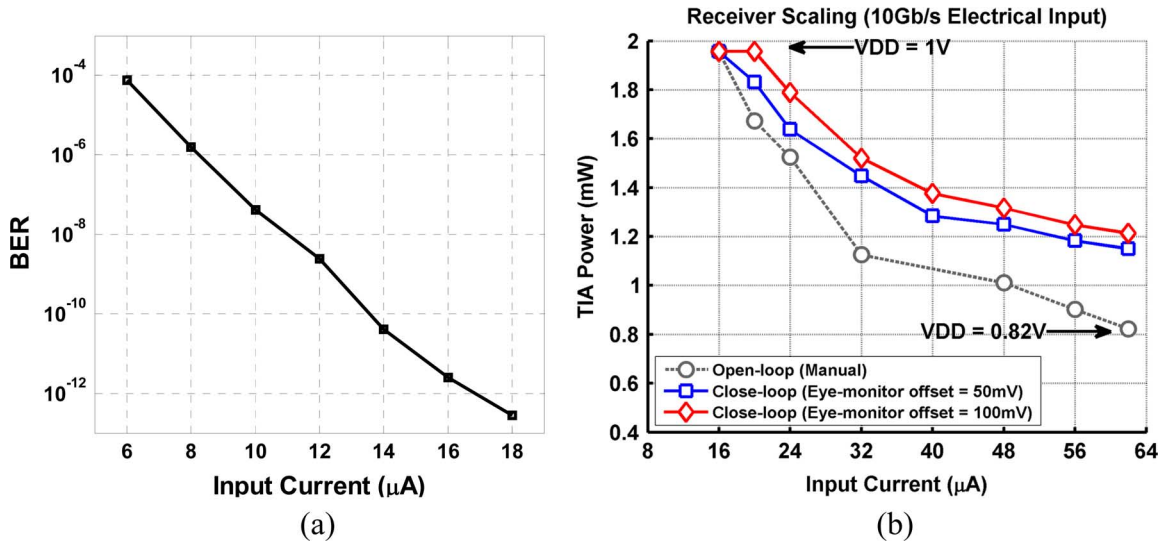


Fig. 25. 10 Gb/s receiver measurements with photodetector emulator circuit. (a) BER versus input current with a 1 V power supply. (b) TIA power scaling versus input current.

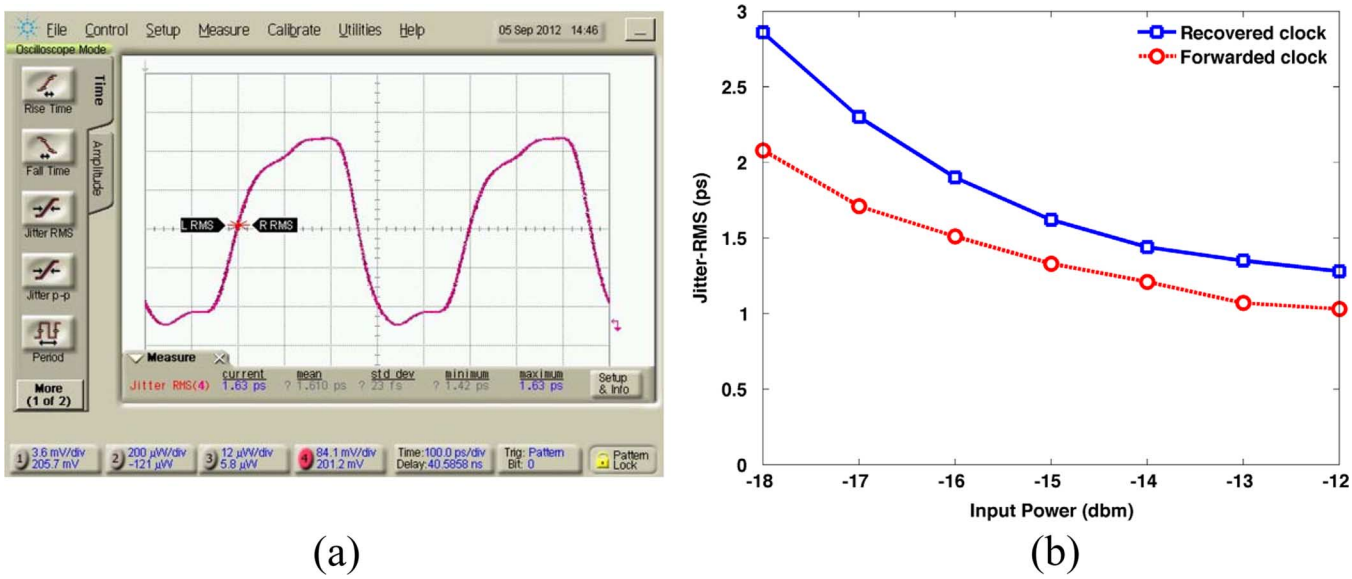


Fig. 26. Optically forwarded-clock receiver measurements: (a) 2 GHz recovered clock waveform and (b) jitter versus input optical power.

power reduction. The overhead of the eye monitor comparator and adaptation logic is estimated to be 160 μW at 8 Gb/s. This overhead can be further reduced be either stopping the operation of the eye monitor after adaptation or only activating it periodically.

A similar optical test setup is used to characterize the optical clock receiver. An optical clock signal in amplified by the clock receiver and quadrature clocks are generated by the ILO, with one of the 2 GHz quadrature clocks used for the 8 Gb/s data receiver clocking shown in Fig. 26. The recovered clock jitter performance is a function of the input clock jitter and power, with the clock path introducing an additional $0.25\text{ps}_{\text{rms}}$ jitter for -12 dBm input power and able to generate sub-2ps_{rms} total jitter down to -16 dBm.

Table I shows the transceiver circuits performance summary and compares this design with both recent ring resonator optical interconnect work utilizing hybrid integration via face-to-face microsolder bonding [16] and monolithic integration [18] and also electrical I/O designs optimized either for low-power at moderate data rates [36] or 40 Gb/s operation [38]. An extinction ratio of 12.7 dB is achieved with the injection-mode ring resonator modulators used in this work, which exceeds the $\sim$7 dB extinction ratios achieved with the depletion-mode devices of [16], [18]. The 4V_{pp} transmitter achieves 808 fJ/bit at 5 Gb/s, while the 2V_{pp} transmitter demonstrates bias-based resonator tuning with a 10% power overhead. While the optical receiver test configuration contributed to a dramatically higher input capacitance, a superior energy efficiency of 275 fJ/bit is achieved with the adaptive power-sensitivity receiver. Relative to a 32 nm electrical IO design optimized for moderate data rates and channel loss [36], the combined energy efficiency of the proposed 65 nm optical transceiver circuits is comparable at near 1 pJ/b. This provides strong motivation to leverage this photonic I/O archi-

TABLE I
PERFORMANCE SUMMARY AND COMPARISONS

	This Work	[16]	[18]	[36]	[38]
Technology (Photonics)	130nm SOI	130nm SOI	130nm CMOS SOI	Electrical I/O	Electrical I/O
Technology (CMOS)	65nm CMOS	40nm CMOS		32nm CMOS	40nm CMOS
Integration Type	Hybrid	Hybrid	Monolithic	50cm cable channel w/ 6dB loss at 4GHz	Nelco PCB channel w/ 21dB loss at 22GHz
Wavelength	1310nm	1550nm	1560nm		
Laser Power	0dBm	0dBm	6dBm		
Waveguide Loss	3dB/cm	9-15dBtotal	3dB/cm		
Coupler Loss	7dB		5.5dB		
Ring Insertion Loss	0.9dB		5dB		
Ring Radius	2.5μm	12μm	7.5μm		
Ring Mode	Carrier-injection	Depletion	Depletion		
Ring Q Factor	~8,000	~15,000	~13,000		
Supply Voltage	1V, 2V, 2.5V	1V, 1.3V, 2V	1.2V/-1.2V	0.6 - 1.08V	1V/1.5V
TX Opt.Data Rate	5Gb/s ($4V_{pp}$ TX)	10Gb/s	25Gb/s	N/A	N/A
TX Elec. Data Rate	9Gb/s	10Gb/s	25Gb/s	2 - 16Gb/s	39.8 – 44.6Gb/s
ER	12.7dB	7dB	6.9dB	N/A	N/A
Tuning Method	Voltage Bias	Thermal	N/R		
λ Tuning Range	0.28nm	1.6nm			
TX Area $4V_{pp}$ TX $2V_{pp}$ TX (w/ Tuning)	 $0.04mm^2$ $0.08mm^2$	$0.00012mm^2$	$0.48mm^2$	$0.014mm^2$	$2.21mm^2$
TX Power $4V_{pp}$ TX $2V_{pp}$ TX (w/ Tuning) Tuning	 4.04mW (0.81pJ/b) 3.48mW (0.70pJ/b) 0.34mW* (6.8μW/GHz)	 1.35mW (0.14pJ/b) 1.25mW (6.3μW/GHz)	207.6mW (8.30pJ/b)	4.72 mW @ 8Gb/s (0.59pJ/b)	870mW (19.5pJ/b)
RX Input Cap	>200fF	40~60fF	20fF	N/A	N/A
PD Responsivity	1A/W	0.7A/W	0.8A/W		
RX Sensitivity Optical input data Optical input clock Electrical input data Electrical Input clock	 -9dBm@8Gb/s -18dBm@2GHz <17uA@10Gb/s <8uA@2.5GHz	-15dBm@10Gb/s	-6dBm@25Gb/s	$20mV_{ppd}$	$20mV_{ppd}$
RX Power TIA Comparators/other	 1.42mW (0.18pJ/b) 0.78mW (0.10pJ/b)	3.95mW (0.40pJ/b)	48mW (1.92pJ/b)	4.40mW @ 8Gb/s (0.55pJ/b)	1050mW (23.5pJ/b)
RX Area Clock RX Data RX	 $0.032mm^2$ $0.036mm^2$	$0.008mm^2$	$0.48mm^2$	$0.02mm^2$	$3.9mm^2$

*Includes the total power of the tuning loop shown in Fig. 10, N/R = not reported, N/A = not applicable.

tecture in a WDM system with multiple ~10 Gb/s channels on a single waveguide, as state-of-the-art 40 Gb/s electrical transceivers consumer near 40 pJ/b [38].

VII. CONCLUSION

This paper presented silicon photonic transceiver circuits for a ring resonator-based optical interconnect architecture that addresses limited modulator bandwidth, variations in ring resonator resonance wavelength and system link budget, and efficient receiver clocking. The photonic transmitters incorporate high-swing nonlinear pre-emphasis drivers to overcome the limited bandwidth of carrier-injection ring resonator modulators and an automatic bias-based tuning loop for resonance wavelength stabilization. An adaptive receiver trades-off sensitivity versus power to accommodate variations in input capacitance, modulator/photodetector performance, and link budget. The receive-side data sampling clocks are produced from an optically-forwarded quarter-rate clock which is amplified before being passed to an injection-locked oscillator for efficient quadrature clock generation. Overall, these circuits provide the potential for silicon photonic links that can deliver distance-independent connectivity whose pin-bandwidth scales with the degree of wavelength-division multiplexing.

REFERENCES

[1] I. Young, E. Mohammed, J. Liao, A. Kern, S. Palermo, B. Block, M. Reshotko, and P. Chang, "Optical I/O technology for tera-scale computing," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 235–248, Jan. 2010.

[2] M. Lipson, "Compact electro-optic modulators on a silicon chip," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1520–1526, Nov./Dec. 2006.

[3] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, "12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators," *Opt. Exp.*, vol. 15, no. 2, pp. 430–436, Jan. 2007.

[4] Z. Peng, D. Fattal, M. Fiorentino, and R. Beausoleil, "CMOS-compatible microring modulators for nanophotonic interconnect," in *Proc. Integr. Photon. Res. Silicon Nanophoton.*, Jul. 2010, paper IWA2.

[5] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, "Silicon optical modulators," *Nature Photon.*, vol. 4, pp. 518–526, Jul. 2010.

[6] G. Li, X. Zheng, J. Yao, H. Thacker, I. Shubin, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "High-efficiency 25 Gb/s CMOS ring modulator with integrated thermal tuning," in *Proc. 8th IEEE Int. Conf. Group IV Photon.*, 2011, pp. 8–10.

[7] L. Liao, A. Liu, J. Basak, H. Nguyen, and M. Paniccia, "Silicon photonic modulator and integration for high-speed applications," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2008, pp. 1–8.

[8] B. G. Lee, A. V. Rylyakov, W. M. J. Green, S. Assefa, C. W. Baks, R. Rimolo-Donadio, D. M. Kuchta, M. H. Khater, T. Barwicz, C. Reinholm, E. Kiewra, S. M. Shank, C. L. Schow, and Y. A. Vlasov, "Four- and eight-port photonic switches monolithically integrated with digital CMOS logic and driver circuits," in *Proc. IEEE-OSA Optical Fiber Commun. Conf.*, Mar. 2013, pp. 1–3.

[9] J. E. Roth, S. Palermo, N. C. Helman, D. P. Bour, D. A. B. Miller, and M. Horowitz, "An optical interconnect transceiver at 1550 nm using low-voltage electroabsorption modulators directly integrated to CMOS," *J. Lightw. Technol.*, vol. 25, no. 12, pp. 3739–3747, Dec. 2007.

[10] A. V. Krishnamoorthy, X. Zheng, G. Li, J. Yao, T. Pinguet, A. Mekis, H. Thacker, I. Shubin, Y. Luo, K. Raj, and J. E. Cunningham, "Exploiting CMOS manufacturing to reduce tuning requirements for resonant optical devices," *IEEE Photon. J.*, vol. 3, no. 3, pp. 567–579, Jun. 2011.

[11] B. R. Moss, C. Sun, M. Georgas, J. Shainline, J. S. Orcutt, J. C. Leu, M. Wade, Y. Chen, K. Nammari, X. Wang, H. Li, R. Ram, M. A. Popovic, and V. Stojanovic, "A 1.23 pJ/b 2.5 Gb/s monolithically integrated optical carrier-injection ring modulator and all-digital driver circuit in commercial 45 nm SOI," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 126–127.

[12] G. Li, X. Zheng, J. Yao, H. Thacker, I. Shubin, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, "25 Gb/s 1 V-driving CMOS ring modulator with integrated thermal tuning," *Opt. Exp.*, vol. 19, no. 21, pp. 20435–20443, Oct. 2011.

[13] C. Li, R. Bai, A. Shafik, E. Z. Tabasy, G. Tang, C. Ma, C. Chen, Z. Peng, M. Fiorentino, P. Chiang, and S. Palermo, "A ring-resonator-based silicon photonics transceiver with bias-based wavelength stabilization and adaptive-power-sensitivity receiver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 124–125.

[14] C.-H. Chen, C. Li, R. Bai, A. Shafik, M. Fiorentino, Z. Peng, P. Chiang, S. Palermo, and R. Beausoleil, "Hybrid integrated DWDM silicon photonic transceiver with self-adaptive CMOS circuits," in *Proc. IEEE Opt. Interconnects Conf.*, May 2013, pp. 122–123.

[15] M. Georgas, J. Leu, B. Moss, C. Sun, and V. Stojanovic, "Addressing link-level design tradeoffs for integrated photonic interconnects," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2011, pp. 1–8.

[16] F. Y. Liu, D. Patil, J. Lexau, P. Amberg, M. Dayringer, J. Gainsley, H. F. Moghadam, X. Zheng, J. E. Cunningham, A. V. Krishnamoorthy, E. Alon, and R. Ho, "10-Gbps, 5.3-mW optical transmitter and receiver circuits in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2049–2067, Sep. 2012.

[17] C. Sun, E. Timurdogan, M. R. Watts, and V. Stojanovic, "Integrated microring tuning in deep-trench bulk CMOS," in *Proc. IEEE Opt. Interconnects Conf.*, May 2013, pp. 54–55.

[18] J. Buckwalter, X. Zheng, G. Li, K. Raj, and A. Krishnamoorthy, "A monolithic 25-Gb/s transceiver with photonic ring modulators and Ge detectors in a 130-nm CMOS SOI process," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1309–1322, Jun. 2012.

[19] A. Liu, L. Liao, D. Rubin, J. Basak, H. Nguyen, Y. Chetrit, R. Cohen, N. Izhaky, and M. Paniccia, "High-speed silicon modulator for future VLSI interconnect," in *OSA Tech. Dig. Integr. Photon. Nanophoton. Res. Applications*, 2007, paper IMD3.

[20] G. Wojcik, D. Yin, A. Kovsh, A. Gubenko, I. Krestnikov, S. Mikhrin, D. Livshits, D. Fattal, M. Fiorentino, and R. Beausoleil, "A single comb laser source for short reach WDM interconnects," in *Proc. SPIE Photon. West*, 2009, 7230-21.

[21] S. M. Park and H. Yoo, "1.25-Gb/s regulated cascade CMOS transimpedance amplifier for gigabit ethernet applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 112–121, Jan. 2004.

[22] C. Li and S. Palermo, "A low-power 26-GHz transformer-based regulated cascode SiGe BiCMOS transimpedance amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1264–1275, May 2013.

[23] J. Proesel, C. Schow, and A. Rylyakov, "25 Gb/s 3.6 pJ/b and 15 Gb/s 1.37 pJ/b VCSEL-based optical links in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 418–419.

[24] S. Palermo, A. Emami-Neyestanak, and M. Horowitz, "A 90 nm CMOS 16 Gb/s transceiver for optical interconnects," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1235–1246, May 2008.

[25] M. Georgas, J. Orcutt, R. J. Ram, and V. Stojanovic, "A monolithically-integrated optical receiver in standard 45-nm SOI," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1693–1702, July 2012.

[26] Y.-H. Song, R. Bai, K. Hu, H.-W. Yang, P. Chaing, and S. Palermo, "A 0.47–0.66 pJ/bit, 4.8–8 Gb/s I/O transceiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1276–1289, May 2013.

[27] A. Ragab, Y. Liu, K. Hu, P. Chiang, and S. Palermo, "Receiver jitter tracking characteristics in high-speed source synchronous links," *J. Electr. Comput. Eng.*, vol. 2011, 2011, Article ID 982314.

[28] J. Stonick, G.-Y. Wei, J. Sonntag, and D. Weinlader, "An adaptive PAM-4 5-Gb/s backplane transceiver in 0.25-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 436–443, Mar. 2003.

[29] S. Palermo and M. Horowitz, "High-speed transmitters in 90 nm CMOS for high-density optical interconnects," in *Proc. Eur. Solid-State Circuits Conf.*, Sep. 2006, pp. 508–511.

[30] J. S. Orcutt, B. Moss, C. Sun, J. Leu, M. Georgas, J. Shainline, E. Zgraggen, H. Li, J. Sun, M. Weaver, S. Urosevic, M. Popovic, R. J. Ram, and V. Stojanovic, "Open foundry platform for high-performance electronic-photonic integration," *Opt. Exp.*, vol. 20, no. 11, pp. 12222–12232, May 2012.

[31] P. Dong, W. Qian, H. Liang, R. Shafiiha, D. Feng, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Opt. Exp.*, vol. 18, no. 19, pp. 20298–20304, Sep. 2010.

[32] J. S. Orcutt, A. Khilo, C. W. Holzwarth, M. A. Popovic, H. Li, J. Sun, T. Bonifield, R. Hollingsworth, F. X. Kärtner, H. I. Smith, V. Stojanovic, and R. J. Ram, "Nanophotonic integration in state-of-the-art CMOS foundries," *Opt. Exp.*, vol. 19, no. 3, pp. 2335–2346, Jan. 2011.

[33] Q. Xu, D. Fattal, and R. G. Beausoleil, "Silicon microring resonators with 1.5-μm radius," *Opt. Exp.*, vol. 16, pp. 4309–4315, 2008.

[34] S. Parikh, T. Kao, Y. Hidaka, J. Jiang, A. Toda, S. Mcleod, W. Walker, Y. Koyanagi, T. Shibuya, and J. Yamada, "A 32 Gb/s wireline receiver with a low-frequency equalizer, CTLE and 2-Tap DFE in 28 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 28–29.

[35] F. Zhong, S. Quan, W. Liu, P. Aziz, T. Jing, J. Dong, C. Desai, H. Gao, M. Garcia, G. Hom, T. Huynh, H. Kimura, R. Kothari, L. Li, C. Liu, S. Lowrie, K. Ling, A. Malipatil, R. Narayan, T. Prokop, C. Palusa, A. Rajashekara, T. Prokop, C. Palusa, A. Rajashekara, A. Sinha, C. Zhong, and E. Zhang, "A 1.0625 14.025 Gb/s multi-media transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3126–3139, Dec. 2011.

[36] M. Mansuri, J. Jaussi, J. Kennedy, T.-C. Hsueh, S. Shekhar, G. Balamurugan, F. O'Mahony, C. Roberts, R. Mooney, and B. Casper, "A scalable 0.128–1 Tb/s, 0.8–2.6 pJ/bit, 64-lane parallel I/O in 32-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3229–3242, Dec. 2013.

[37] D. Taillaert, W. Bogaerts, P. Bienstman, T. F. Krauss, P. van Daele, I. Moerman, S. Verstuyft, K. De Mesel, and R. Baets, "An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers," *IEEE J. Quantum Electron.*, vol. 38, no. 7, pp. 949–955, Jul. 2002.

[38] B. Raghavan, D. Cui, U. Singh, H. Maarefi, D. Pi, A. Vasani, Z. Huang, B. Catli, A. Momtaz, and J. Cao, "A sub-2 W 39.8–44.6 Gb/s transmitter and receiver chipset with SFI-5.2 interface in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3219–3228, Dec. 2013.

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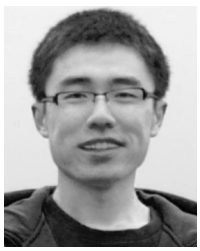

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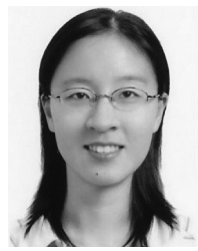

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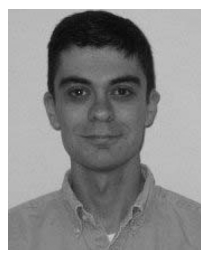

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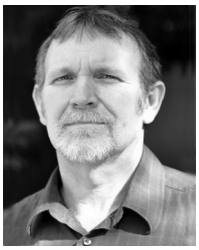

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