A Single Parity Check Forward Error Correction Method for High Speed I/O

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***Abstract*— Some proposed high speed wireline communications make use of an ADC front end to allow a feedforward equalizer (FFE) to compensate for the frequency dependent loss of the channel. High precision ADCs are expensive in terms of power. The FFE block performs multiplication and addition operations at high speed and further increases the power consumption. This paper proposes a simple forward error correction method by which the ADC resolution and the equalizer complexity can be reduced. A single parity check code implemented together with a threshold detector can provide single error correction capability. With this error correction capability, the number of taps required in the FFE block is shown to be reduced to 3 taps from 6 taps for a channel with 15dB insertion loss at 5GHz frequency with the data rate being 20Gb/s. The effective number of bits (ENOB) required from the ADC is also shown to reduce to about 3.5 bits from 6 bits. The high rate of the code and the very simple decoder architecture make this error correction mechanism well suited for the wireline application.**

I. INTRODUCTION

High speed serial links are typically limited by ISI and operate at high SNR values. This leads to a large power consumption at the transmitter side [1]. One way to reduce power consumption is by the use of forward error correction (FEC) coding. The philosophy of using forward error correction can be understood as under-designing the system, in the sense that the bit error rate (BER) achieved before the FEC block is higher than the targeted BER, but with a much lower power consumption. FEC is then used to lower the BER to the targeted value. With the use of FEC, the voltage swing generated at the transmitter can be reduced. On the receiver side, the main advantages of FEC are a relaxation in the equalizer complexity and the resolution of the ADC. In this paper we focus on the reduction in the power consumption at the receiver side. The downside to FEC that has so far hindered their adoption in these wireline communication systems is that, the increased rate of signaling due to FEC will exacerbate the ISI. There is also a power overhead in terms of the power consumption in the FEC encoder and decoder. Hence, the power consumption in several components of the transmitter and the receiver is reduced and some of it is redistributed in the encoder and decoder blocks used for implementing the forward error correction coding scheme. Therefore, for an FEC scheme to be effective its rate should be high and the encoding and decoding complexity should be low.

The single parity check code (SPC) is the simplest form of error correction coding. The single parity check code involves the addition of a single extra bit to a block of bits such that the total number of ones in the block is always either even or odd. It is called an even parity code if the number of ones is always even. It satisfies the two requirements of having a high rate and having a very simple encoding and decoding mechanism. Its effectiveness in high speed serial links is demonstrated in this paper.

II. SYSTEM DESCRIPTION

In order to implement the technique described here, the statistics of the signal at the receiver has to be known. A statistical model which provides the probability density function of the signal at the receiver has been utilized. This section briefly describes the statistical model used and the representative high speed wireline system being considered in this paper.

At the transmitter side, the bits to be transmitted are assumed to be generated in a memoryless fashion. These bits are grouped into blocks of k bits each. Each block is then provided with one additional bit which denotes the even parity of the k information bits in the block. Thus, each block of bits to be transmitted is k+1 bits long. This is called the block length of the code and is represented by n. This constitutes the encoding process. It can be seen that this encoding process simply involves the calculation of the modulo-2 sum of the k information bits and can be implemented very easily as an XOR function in the digital domain. The encoding scheme implies that to transmit k information bits, k+1 bits have to be transmitted on the channel. The rate of the code is thus k/k+1. It can be noted that this is the highest possible rate for a linear block code for a given block length of k+1.

The bits are then transmitted on the channel in the form of pulses using a modulation scheme such as PAM-2 or PAM-4. As the pulse propagates along the channel, the low pass nature of the channel smears the pulse into adjacent bit periods and produces ISI components.

At the receiver side the ADC digitizes the pulses and introduces quantization noise in doing so. The digital values are processed by the equalizer and the FEC block as shown in figure 1. The FEC block comprises of the decoder and the threshold detector. The role of the threshold detector is explained in the next section.

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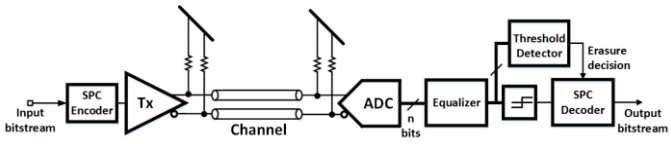

Figure 1. Block diagram of an ADC based serial link.

The pulse response of the channel can be combined with a feedforward equalizer to obtain an equalized pulse response. With this pulse response, the PDF of the signal received at the output of the equalizer can be calculated using the technique in [2]. The effect of the channel ISI, and the equalizer's role in combating this ISI, is captured in this PDF. The ADC quantization noise, receiver jitter and thermal noise are also added to obtain the final PDF. The effect of passing the ADC quantization noise through the FFE is also included in the statistical model. With the knowledge of this PDF, based on the value of the received signal, bits are either treated as having been received without any uncertainty or as having been erased. This is explained in detail in the following section.

III. SIGNAL MODELING

The details of the methodology used is illustrated in this section with an example.

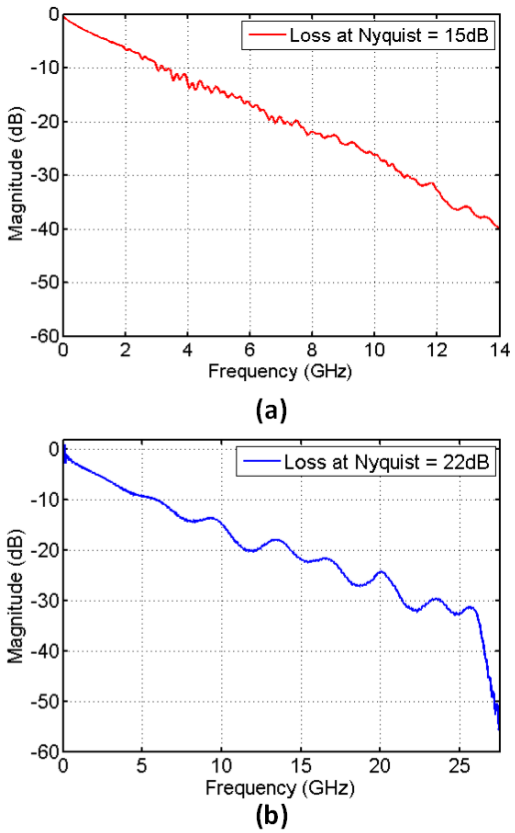

Figure 2. Frequency responses of the test channels.

The frequency responses of the channels used in this paper are shown in figure 2. Consider a PAM-4 system operating at a symbol rate of 10GS/s. The PDF of the received signal at the output of the equalizer will be of the form as shown in figure 3. The PDF has four lobes, each centered on one of the four possible values resulting from a PAM-4 modulation scheme. Let the four values of PAM-4 modulation scheme be represented as [b b/3 –b/3 –b]. Here, b represents the pulse amplitude. Figure 4 represents the PDF of the received signal when symbol b/3 is transmitted.

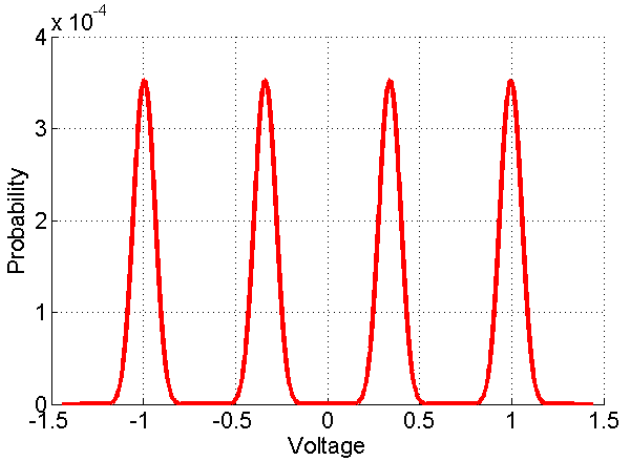

Figure 3. PDF of received signal at the output of the equalizer.

This PDF can be divided into 5 regions as shown in figure 4.

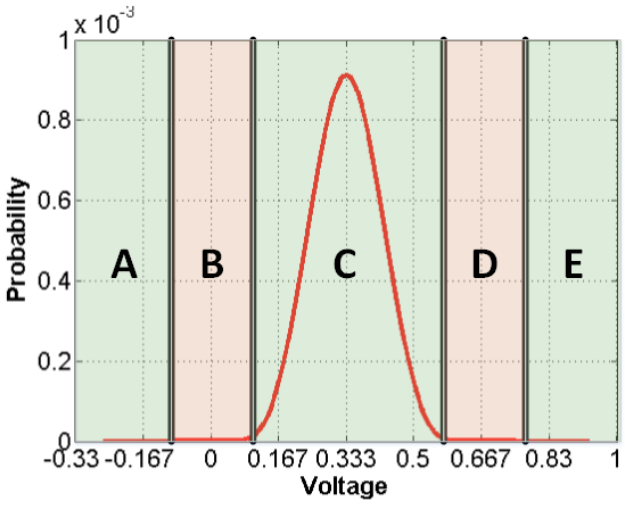

Figure 4. PDF showing different regions.

Region B of this PDF is where the PDF centered on the adjacent symbol (-b/3) has probability values above a certain threshold value. Beyond region B, in region C the probability curve centered around the symbol (-b/3) is below the threshold. This threshold value has to be chosen to be less than the target BER. Region D is where the PDF centered on the symbol b has finite probability values above the threshold. Any signal value in these regions has an ambiguity as to which symbol caused this value to occur. When the output of the equalizer falls within these regions, a bit decision is not immediately made. These bits are discarded i.e. treated as erasures and the single parity check condition is used to determine these bits. A, C and E represent the regions where

signal values which have no ambiguity (probability of error less than the threshold) associated with them fall. When a signal value falls in these regions the bit can be determined with certainty. A threshold detector is needed to determine which region a signal value belongs to. Thus, using this scheme all single bit erasures can be detected and filled correctly. The single parity check code cannot be used to determine the correct bits when two or more erasures occur within the same block. Assuming erasures occur independently of each other the probability of bit error P_{bit} with a single parity check code is given by,

$$P_{bit} = (1 - ((1 - P_{erase})^n + nP_{erase}(1 - P_{erase})^{n-1}))P + P_2 \quad (1)$$

Here, P_{erase} is the probability of bit erasure (probability of a signal value falling in regions B or D) and P is the probability of bit error before the SPC decoder is used. P_{bit} is the probability of bit error at the output of the SPC decoder and P_2 is the threshold probability value mentioned earlier. n, is the SPC block length.

In order to achieve a low P_{bit}, P_2 has to be very small. For making P_2 small, regions B and D have to be made wider. This will increase the probability of bit erasure, P_{erase}, which has the effect of increasing P_{bit}. Hence, the width of regions B and D has to be carefully chosen to get the optimum value for P_{bit}.

Here, an assumption has been made that each symbol is erased independently of all other symbols. In order to achieve this independence condition in practical systems, interleaving of bits at the transmitter and de-interleaving at the receiver becomes necessary [1]. This assumption has been justified in [4] with simulation results. The interleaving and de- interleaving process also protects the system against burst errors. With this assumption, the post FEC bit error rate P_{bit} can be calculated as a function of the pre FEC bit error rate P and the block length of the code as in [4].

The equalizer has to be designed to give a bit error rate of only P such that the target bit error rate of P_{bit} is achieved after the FEC block. To achieve this lower bit error rate P, the number of taps required in the equalizer and the required resolution of the ADC is smaller. This will directly translate to power savings.

The decoder required for a single parity check code is a modulo-2 running sum generator. In terms of digital hardware this can again be as simple as an XOR gate. This can be compared with the decoder complexity required for other linear block codes proposed for these high speed serial links such as the BCH codes. These codes require a syndrome calculation unit to detect the presence of errors. They would require the implementation of an algorithm such as the Berlekamp-Massey algorithm in digital hardware and are hence very expensive in terms of power.

IV. SIMULATION RESULTS

Using the method described in the preceding section the results are presented in this section.

For the first set of results presented in figures 5 and 6, the data rate is set at 20Gb/s. A PAM-4 modulation scheme is used. Hence, the Nyquist frequency is 5GHz. The channel used is shown in figure 2(a). Thermal noise with a standard deviation of 1 mV is added. Further, the simulation assumes the ADC has an ENOB of 4 bits. Recent high speed ADCs in [5] have reported a maximum ENOB around 4.75 and hence this is a valid assumption.

The reduction in the number of taps required in the equalizer is shown in figure 5. The figure shows the results for block lengths of 8, 32, 256 and 2048. From the figure it is clear that very small block lengths can actually degrade the overall performance. As the block length increases the rate of the code approaches 1. With the increase in the code rate, the signaling rate on the channel decreases and hence the amount of ISI seen also decreases. Therefore, a block length of 32 gives better results than a block length of 8 and a block length of 256 gives better results than a block length of 32. As the block length is increased further, there is a higher probability of having 2 or more erasures in a block and the code becomes less effective. Hence, block length of 256 is better than 2048. At these block lengths, the increase in code rate from a block length of 256 to 2048 is not significant enough to decrease the ISI. Therefore, there is an optimum block length and for this example system it is 256. Also, as the block length is increased the latency of the system increases. Hence, a block length of 32 may be the overall preferred block length. As can be seen from the figure, for a target BER of 10^{-12}, in the absence of coding, a 6 tap feedforward equalizer is necessary. With a single parity check code of block length 32 or higher, a 3 tap equalizer can achieve the target BER. This translates to a reduced number of multipliers and adders and hence a reduced power consumption.

The FFE block is also typically implemented in a parallel form to provide the high throughput that the application demands. This will further increase the number of multipliers and adders reduced in the overall receiver system.

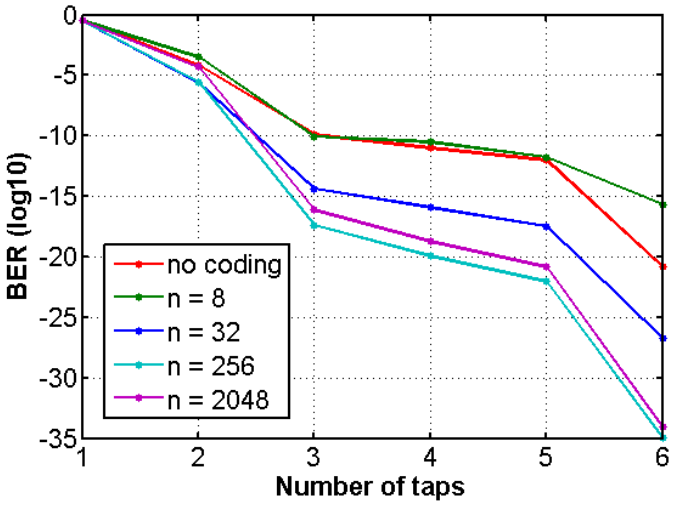

Figure 5. Equalizer complexity v/s BER.

The reduction in the ADC precision required is shown in figure 6. The results are for a data rate of 20Gb/s with the receiver having a 3 tap equalizer. In the case of no coding scheme being used, an ENOB of 6 bits is necessary to achieve the target BER of 10^{-12}. With coding, using a block length of 256, an ENOB of 3.5bits is sufficient to achieve the target BER. The second set of results are

presented in figures 7 and 8.

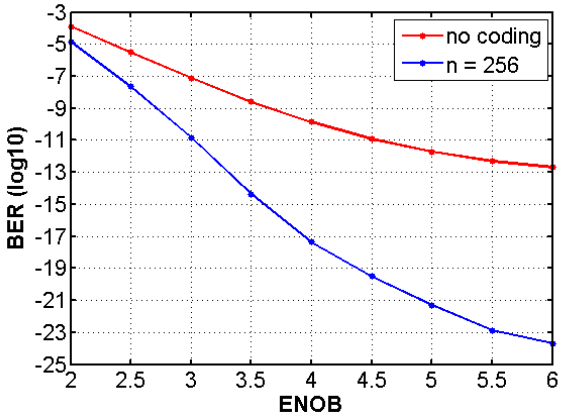

Figure 6. ADC resolution v/s BER.

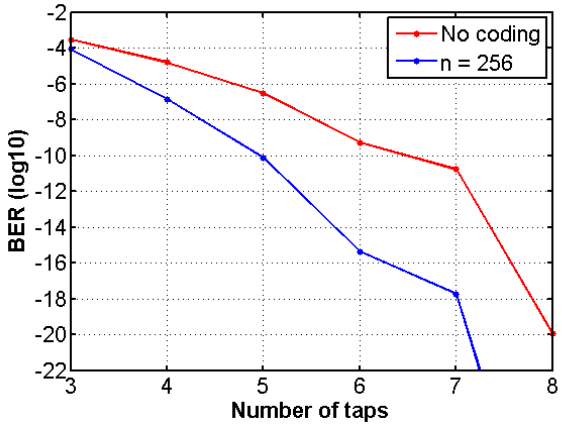

Figure 7. Equalizer complexity v/s BER.

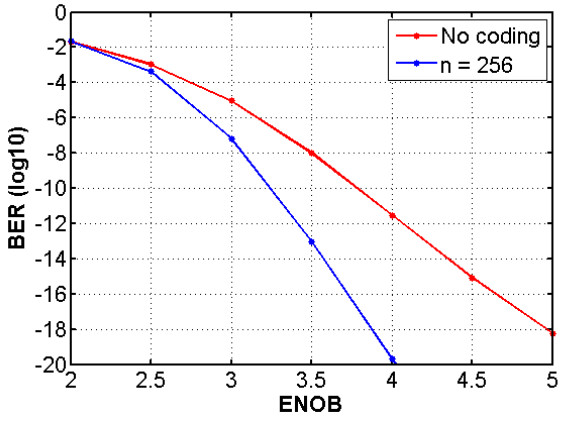

Figure 8. ADC resolution v/s BER.

Figure 7 shows the decrease in the equalizer complexity on using the SPC coding technique compared to a case with no coding. The channel used for this simulation is shown in figure 2(b). The data rate is 64Gb/s and the system employs a PAM- 4 modulation scheme. The number of FFE taps required is shown to reduce from 8 to 6. Figure 8 shows the decrease in the ADC ENOB requirement for the 64Gb/s system. Employing of the coding scheme helps relax the ADC ENOB by 0.7 bits.

V. CONCLUSION

By using the single parity check code the channel has been effectively converted to a binary erasure channel. Both the equalizer complexity and the ADC resolution can be relaxed by using the technique described here. Since, the hardware overhead involved in implementing the technique is minimal compared to the equalizer hardware complexity, there can be significant power savings. As the data rates continue to increase in these systems, techniques from the channel coding having to be adapted and adopted in order to meet the tight power constraints of the system.

ACKNOWLEDGMENT

This work was supported by the Semiconductor Research Corporation under Task 1836.111 through the Texas Analog Center of Excellence (TxACE).

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