2.5 A 0.25pJ/b 0.7V 16Gb/s 3-Tap Decision-Feedback Equalizer in 65nm CMOS

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Supply-voltage scaling has become one of the most effective methods to improve the energy efficiency of power-constrained systems, motivating its application towards high-performance I/O links [1]. Due to the accelerating need for more off-chip I/O bandwidth, it is desirable to provide both higher data rate and low-V_{DD} operation to achieve optimal energy efficiency. Unfortunately, efficient implementations of equalization circuits are one of the major challenges faced in >10Gb/s serial-link systems that attempt to incorporate reduced-supply operation. For example, a continuous-time linear equalizer (CTLE), due to its analog nature, exhibits a rapid degradation in gain/bandwidth and only linear power scaling when operating at low V_{DD}. Decision-feedback equalizers (DFEs) also have to make significant compromise of speed from longer delay in the critical feedback path. Consequently, previous >10Gb/s equalizers have not pursued extensive supply voltage scaling [2-5].

In this work, a DFE is presented that is designed specifically to operate at low V_{DD} and scale well in energy-efficiency. To achieve this goal, the following innovations are introduced: 1) fast and energy-efficient charge-based latch and sample-and-hold (S/H) topologies; 2) a CMOS-clocked quarter-rate DFE architecture with summer gain and power optimization; 3) an integrating summer with a compact common-mode restoration circuit. Leveraging these techniques, the DFE is capable of operating at or below 0.7V, with an energy efficiency of or better than 0.25pJ/bit.

Charge-based circuits have been previously shown to be effective in achieving high-speed operation and low-power consumption [6], but not at low supply voltages. Our low-V_{DD} DFE leverages a charge-based approach for the critical quantization latches and input sample-and-hold circuits, as shown in Fig. 2.5.1. First, consider the operation of the two-stage charge-based quantization latch. Both the 1st-stage output VXN/VXP and 2nd-stage output VON/VOP are reset to V_{DD} when the clock CK is low. When CK goes high, both stages start discharging toward GND. However, if the 1st-stage is designed with a faster discharge rate, the 2nd-stage discharging will stop and a differential output voltage is maintained that is proportional to the differential input. One potential problem for low-V_{DD} operation is that a large differential gain results in a significant common-mode voltage drop at the latch output. To mitigate this, MOS caps are added to dump positive charge into the output nodes to elevate the output common-mode voltage level. Fast settling and small aperture time are achieved due to the charge-based latch's tail nodes rapidly being pulled to GND, resulting in an effective one-stack circuit. The latch draws almost no static current and exhibits quadratic power savings with supply, resulting in significant power savings relative to conventional CML latches whose power scales linearly with supply. Furthermore, the latch is able to achieve a gain of more than 2, relaxing the gain and hence power requirements of the integrating summer. A similar topology is used by charge-based S/H circuits at the DFE input, with additional cascode devices added to the 2nd-stage that allow for near unity gain, preserving DFE input linearity. Compared to conventional transmission-gate based S/Hs, the designed S/H does not suffer from severe bandwidth reduction at 0.7V, and, if desired, has the added benefit of providing larger than unity gain.

A quarter-rate DFE architecture (Fig. 2.5.2) is employed to allow for CMOS clocking with a 0.7V supply. As shown in the timing diagram, because the sampling delay of the S/H and the CK-Q delay of the latch are nearly identical, timing margin is saved by aligning these two phases. Each summer output is followed by a successive chain of three charge-based latches, which then provide feedback to the three other summers. Note that return-to-zero (RZ) operation of these latches is not a problem because the feedback values only have to be valid during the first half of the summation period, i.e., one quarter of the cycle.

Because four integrating summers are used, it is critical to optimize the summer static current consumption by achieving only the minimum gain required to make a correct decision. Since the decision amplitude does not need to be full swing but just large enough to slew the differential pairs of the feedback taps [5], the over-drive voltage of the summer feedback differential pairs are designed to be less than 200mV. Thus, assuming a 100mV input cursor amplitude, only a total gain of 2 is needed in the S/H-summer-latch path. Since the gain of the latch itself is more than 2, the gain and therefore power of the summer can be minimized.

The integrating summer consists of a linearized input tap, three feedback taps, and one offset-cancellation tap, with 7b control for both the input and 1st-tap, and 6b control for the remaining taps and offset cancellation. To avoid gain and linearity degradation at 0.7V operation, we connect a pair of common-mode restoration circuits to the summation nodes. During the summer reset phase, the capacitor is charged to V_{DD} by the M1 PMOS transistor. When the summer integration starts, the initial voltage on the capacitor top plate is bootstrapped to ~$2V_{DD}$, thereby keeping M2 in saturation in order to pump current into the summation node. By maintaining a high impedance for the current sources, linearity and differential gain are preserved while introducing more than 200mV boost in the common-mode voltage. Using high-density MOS varactors, each pair of restoration circuits adds 34μm^2 of area overhead.

Figure 2.5.7 shows a die micrograph of the DFE, fabricated in a 65nm CMOS process. The compact size of the 60×60μm^2 DFE core area is critical, as the speed, gain, and power consumption of charge-based circuits are all heavily affected by parasitic capacitance. During BER testing, a 16Gb/s 2^7-1 PRBS pattern is applied to the DFE inputs through an RF probe to evaluate the DFE performance. One of the four integrating summers is on-chip buffered and driven off-chip through another RF probe to produce the eye diagrams seen in Fig. 2.5.4. The integrating summer's output eye is completely closed when all the equalization taps are disabled, and gradually opens as more feedback taps are enabled. Note that the buffer gain is less than 0.4 to reduce loading to the summer. Figure 2.5.5 shows the measured BER bathtub curves for two test channels with 13dB and 18dB loss at 8GHz. With the 13dB-loss channel, the DFE operates at 0.65V with 3.3mW power consumption and achieves a 0.53UI timing margin. As more equalization and signal gain is required for the 18dB loss channel, a 0.7V supply and 4mW of power are required to obtain a 0.46UI timing margin. Fig. 2.5.6 shows the measured DFE power breakdown for 0.7V operation with the 18dB loss channel. The reported power includes the DFE core, DACs, DC biasing, and clock buffers, excluding only the CML clock divider that down-converts an 8GHz differential input clock for quadrature phase generation. A comparison with recently published low-power DFE designs shows that this work achieves a 2× improvement in energy-efficiency for a 0.7V supply, and is further improved when the supply is reduced to 0.65V.

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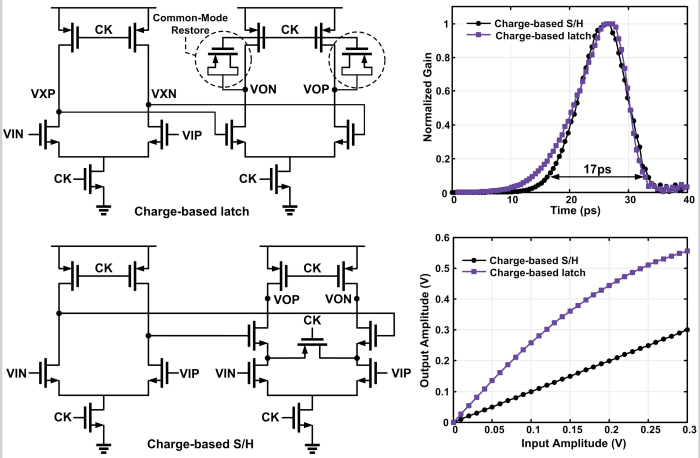


Figure 2.5.1: Charge-based latch and S/H with simulated Impulse Sensitivity Function (ISF) and gain at VDD=0.7V.

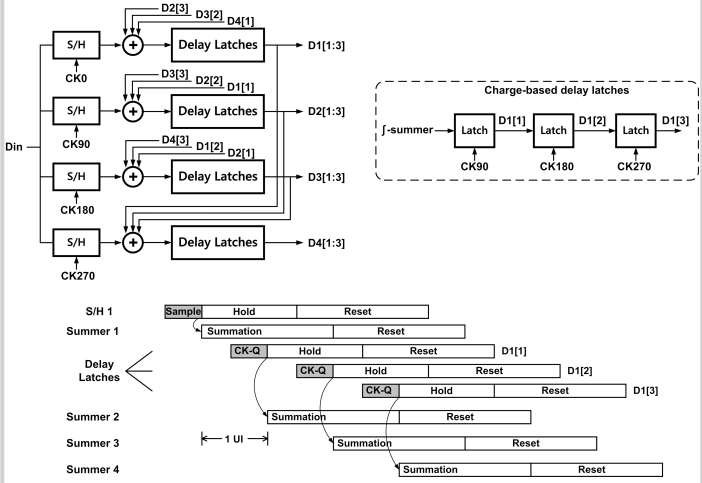


Figure 2.5.2: Block diagram and timing diagram of proposed DFE.

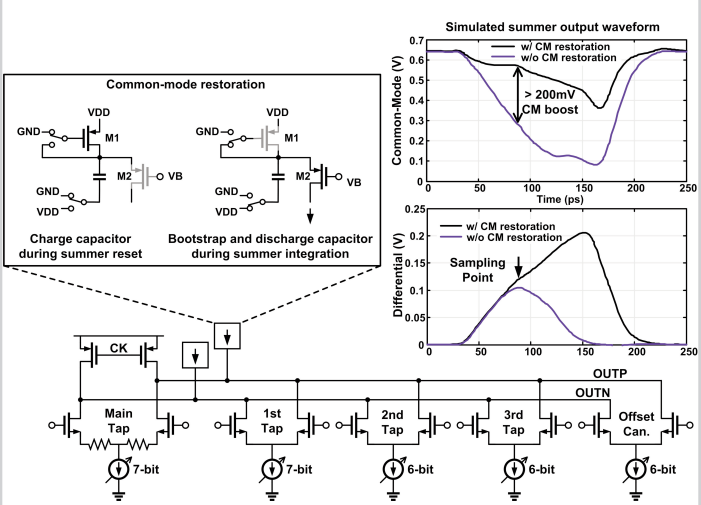


Figure 2.5.3: Integrating summer with common-mode restoration.

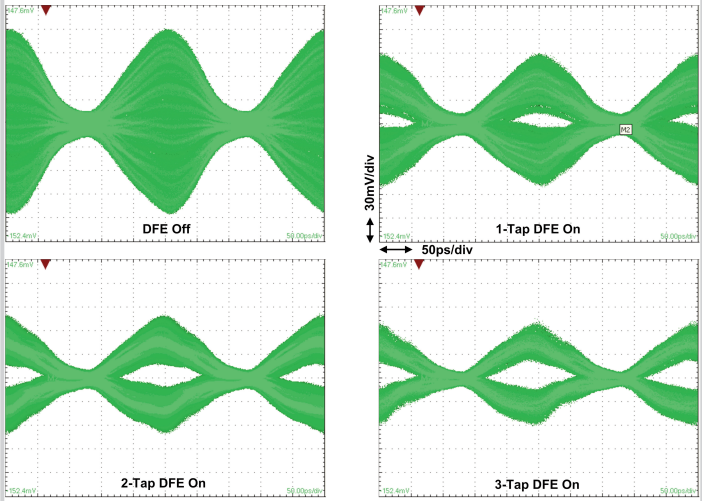


Figure 2.5.4: Internal eye diagrams of the integrating summer at the 4Gb/s quarter rate, measured from on-chip buffer with a high-speed probe.

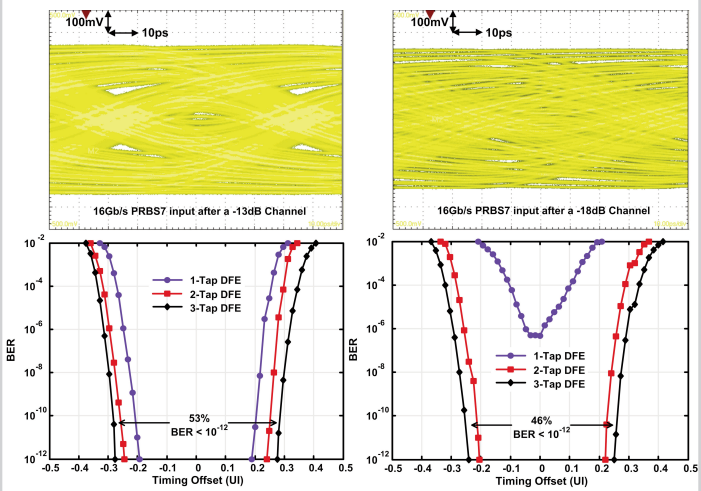
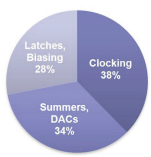


Figure 2.5.5: DFE input and BER bathtub curve with a 13dB loss channel, 0.65V supply and a 18dB loss channel, 0.7V supply.

Component	Power (mW)
Summers and DACs	1.4
Latches and biasing	1.1
Clocking	1.5
Total	4



References	[2]	[3]	[4]	[5]	This Work	
Data Rate (Gb/s)	15	20	16	66	16	
Process	45nm SOI	45nm SOI	40nm GP	65nm GP	65nm GP	
Equalization	2-tap DFE	CTLE + 1-tap DFE	Passive LE + 1-tap DFE	3-tap DFE	3-tap DFE	
Clocking	Half Rate	Half Rate	Half Rate	Half Rate	Quarter Rate	
Supply (V)	1.2	1.2	1.0	1.2	0.65	0.7
Channel Loss (dB)	14.5	26.3	15	N/A*	13	18
Timing Margin	34% BER < 10^{-8}	26% BER < 10^{-12}	>25% BER < 10^{-12}	60% BER < 10^{-12}	53% BER < 10^{-12}	46% BER < 10^{-12}
Power (mW) (Including Clocking)	7.5	13.2	9.25	55.1**	3.3	4
Energy Efficiency (pJ/b)	0.50	0.66	0.59	0.86**	0.21	0.25

* ISI emulated by a 3-tap transmitter FIR filter with a total post cursor 1.65x of main cursor.
** 9.1mW input from external clock source used for clocking power calculation

Figure 2.5.6: Power breakdown, performance summary and comparison.

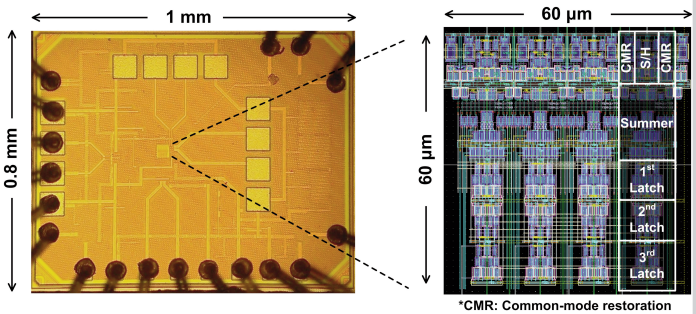


Figure 2.5.7: Die micrograph.

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