A CMOS Fractional-N PLL-Based Microwave Chemical Sensor With 1.5% Permittivity Accuracy

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***Abstract*—A highly sensitive CMOS-based sensing system is proposed for permittivity detection and mixture characterization of organic chemicals at microwave frequencies. The system determines permittivity by measuring the frequency difference between two voltage-controlled oscillators (VCOs); a sensor oscillator with an operating frequency that shifts with the change in tank capacitance due to exposure to the material under test (MUT) and a reference oscillator insensitive to the MUT. This relative measurement approach improves sensor accuracy by tracking frequency drifts due to environmental variations. Embedding the sensor and reference VCOs in a fractional-N phase-locked loop (PLL) frequency synthesizer enables material characterization at a precise frequency and provides an efficient material-induced frequency shift read-out mechanism with a low-complexity bang–bang control loop that adjusts a fractional frequency divider. The majority of the PLL-based sensor system, except for an external fractional frequency divider, is implemented with a 90-nm CMOS prototype that consumes 22 mW when characterizing material near 10 GHz. Material-induced frequency shifts are detected at an accuracy level of 15 ppm_{rms} and binary mixture characterization of organic chemicals yield maximum errors in permittivity of $<$1.5%.**

***Index Terms*—Chemical sensor, dielectric constant, frequency synthesizer, mixture characterization, oscillator, permittivity detection.**

I. Introduction

DETECTION of chemicals and biological materials is vital in an enormous number of applications, including pharmaceutical, medical, oil, gas, and food/drug safety fields. An effective material detection approach involves characterizing physical and electrical properties of materials under test (MUTs), such as electrical permittivity [1]. The development of efficient permittivity detection techniques will benefit systems used for medical diagnosis and imaging, DNA sensing, material characterization, agricultural development, forensics, and bio-threat detection. Since many chemicals/bio-materials show significant changes at RF/microwave frequencies [1]–[8], permittivity detection in this band is particularly useful for chemical detection [1], [5] and for medical applications, such as cell detection [6], [7] and blood-sugar monitoring [8].

Capacitance-based sensing, where a capacitor exposed to a MUT exhibits changes in electrical properties, is a common technique reported in the literature for permittivity detection. Low-frequency charge-based techniques to detect capacitance changes include embedding biomaterial-sensitive capacitors in a relaxation oscillator [9] and as load devices for charge integration with precisely controlled current sources [10]. Another example in the 10-MHz range is an impedance spectroscopy approach [11], where a sinusoidal voltage source is applied to a material-sensitive capacitor and the impedance magnitude and phase is extracted with a coherent detector.

However, the aforementioned techniques are not well suited for permittivity detection at microwave frequencies. For microwave permittivity sensing, one approach is to detect the sensor's reflection and or transmission properties to characterize the MUT [8], [12], [13]. A drawback of these approaches is that they require somewhat large transducer structures, especially if scaled to the 10-GHz range. Another microwave-based technique is to deposit the MUT on top of a microwave resonator and observe the permittivity change as a shift in the resonance frequency. While on-board sensors have been implemented using this resonant-based technique [14], [15], fully integrated permittivity sensors at microwave frequencies are necessary for compact size and low cost to be suitable for lab-on-chip and point-of-care applications.

In [1], a CMOS integrated microwave chemical sensor based on capacitive sensing is proposed with an LC voltage-controlled oscillator (VCO) that utilizes a sensing capacitor as a part of its tank. The real part of the permittivity of the MUT applied on the sensing capacitor changes the tank resonance frequency, and hence, the VCO free-running frequency. Embedding the material sensitive VCO in a phase-locked loop (PLL) allows the oscillator free-running frequency shift to be translated into a change in the control voltage, which is read by an analog to-digital converter (ADC). A multi-step detection procedure, with the ADC output bits controlling an external tunable reference oscillator to equalize the control voltage in both the presence and absence of the material, is then used to read-out the sensor oscillator frequency shift. While this system was able to measure the real part of the permittivity of organic chemicals and binary organic mixtures in the range of 7–9 GHz with a 3.5% error, defined as the absolute difference between the

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room temperature (20 °C) measured and theoretical values [16], [17], it suffers from several drawbacks, which are: 1) an expensive tunable reference frequency source is required; 2) the ADC resolution limits the accuracy of the frequency shift detection; and 3) utilizing a single VCO sensor necessitates a complicated multi-step measurement procedure and makes the system performance susceptible to low-frequency environmental variations.

This paper presents a CMOS fractional-N PLL-based chemical sensor based on detecting the real part of a MUT's permittivity. Detection of this real part of the permittivity is suitable for the characterization of mixing ratios in mixtures, which is beneficial in many applications, including: 1) medical applications such as the estimation of the glucose concentration in blood [8] and 2) the estimation of moisture content in grains [18]. The system utilizes both a sensor and reference VCO, which enables improved performance and lower complexity relative to the system in [1]. For the frequency-shift read-out, instead of controlling an expensive externally tunable reference oscillator, a low-complexity bang–bang control loop periodically compares the control voltage when the sensor and the reference oscillator are placed in the PLL loop and adjusts a fractional-N loop divider. Since the system determines permittivity by measuring the frequency difference between the sensor and reference VCO, common environmental variations are cancelled out and the measurement procedure is dramatically simplified to a single-step material application. Also, utilizing a high-resolution fractional divider allows the frequency shift resolution measurement to be limited by system noise, rather than the ADC quantization noise [1].

This paper is organized as follows. Section II discusses VCO-based sensing systems and provides an overview of the proposed fractional-N PLL-based chemical sensor system. Key design techniques for the capacitive sensor and the VCO, which is optimized to minimize the effect of the imaginary part of the permittivity on the oscillation frequency to ensure the real part is accurately detected, are discussed in Section III. Section IV provides more circuit implementation details of the shared-bias sensor and reference VCO, other PLL blocks, and the bang–bang comparator, which senses the VCO control voltage. The 90-nm CMOS prototype and the chemical sensing test setup are detailed in Section V. Section VI shows the experimental results, including characterization of key circuit blocks and organic chemical mixture detection measurements. Finally, Section VII concludes this paper.

II. VCO-Based Sensing Systems

This section first details key characteristics of VCO-based sensing systems. The proposed fractional-N PLL-based sensor system is then described.

A. VCO-Based Sensor Characteristics

A VCO-based sensor is composed of a sensing VCO and a frequency detector to detect a frequency shift, Δf, as shown in Fig. 1(a). The frequency resolution, defined as the minimum frequency shift that can be detected by the system, is primarily a function of the system's input referred noise and frequency

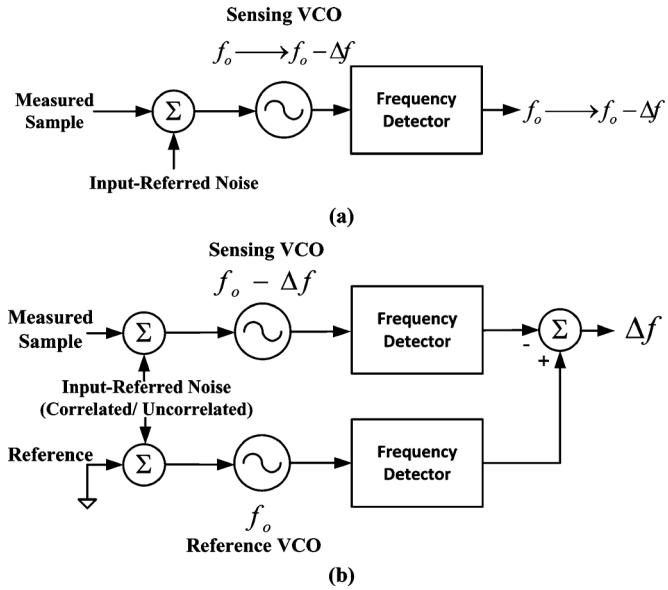

Fig. 1. VCO-based sensors incorporating: (a) a single VCO and (b) reference and sensing VCOs.

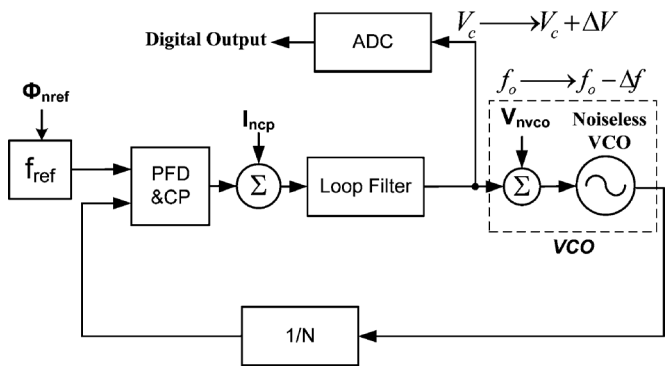

Fig. 2. VCO-based sensor using a PLL and an ADC as a frequency detector [1].

detector quantization noise. Note that both the VCO phase noise and the frequency detector circuitry can contribute to the system's input-referred noise. The performance of the sensing system in Fig. 1(a) is limited by VCO temperature sensitivity and low-frequency noise. This motivates the use of a reference oscillator [19], as shown in Fig. 1(b), and measuring the desired frequency shift as the difference between the sensing and the reference VCOs. One practical issue with this approach is that the two VCOs should be in close proximity to maximize noise correlation. However, this causes VCO frequency pulling when the VCOs are simultaneously operating. In order to avoid this, the two VCOs can be periodically activated such that only one operates at a time [19]. This results in a beneficial high-pass filtering of the correlated low-frequency noise between the sensor and reference VCO.

One common frequency detector implementation is a frequency counter [19]. While this method can achieve high resolution, it requires long measurement times, on the order of milliseconds. Also, since the VCOs are embedded in an open loop system, the absolute oscillator frequency drift makes it difficult to characterize the MUT properties at a precise frequency.

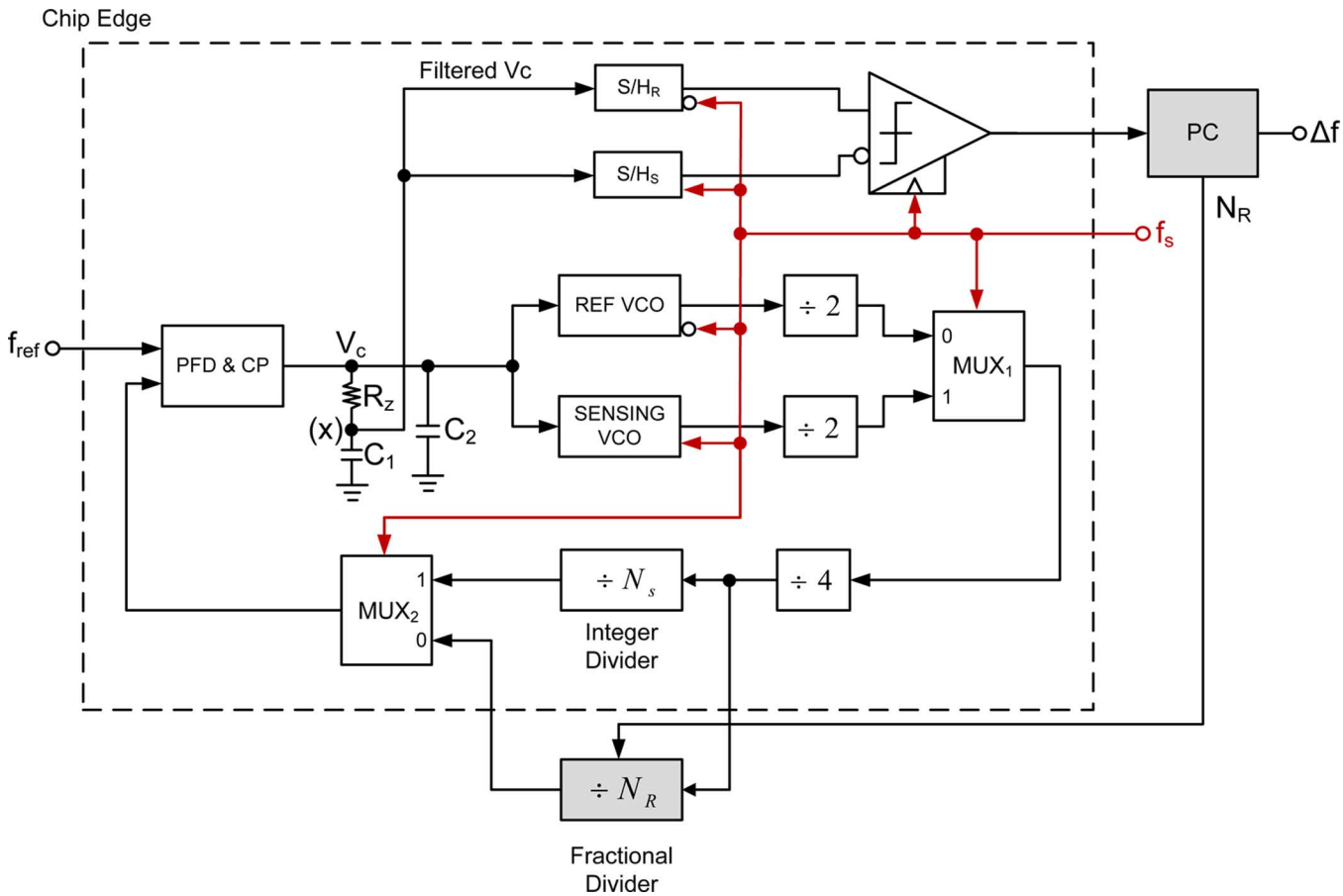

Fig. 3. Block diagram of the dielectric sensor based on a fractional-N frequency synthesizer with sensor and reference VCOs and dual-path loop dividers. A bang–bang control loop adjusts the fractional divider value to determine the frequency shift between the sensor and the reference VCO.

A PLL can serve as a closed-loop frequency detector circuit, as shown in Fig. 2 [1], to enable MUT characterization at a precise frequency. For a fixed division ratio, N, and reference frequency, $f_{\rm ref}$, the change in the VCO free-running frequency is translated into a change in the control voltage, V_c, and read out using an ADC. This method also offers a significantly faster measurement time set by PLL settling, typically on the order of microseconds, which is useful for high-throughput chemical characterization systems and emerging biosensor platforms for real-time monitoring of fast biological processes, such as protein-drug binding kinetics [20].

In addition to the VCO, the other blocks in the PLL-based system also contribute to system noise and should be analyzed by considering the transfer function from that particular block to the control voltage node. The PLL filters high-frequency content of the VCO input-referred noise, $V_{n,\rm vco}$, as the transfer function, $V_c/V_{n,\rm vco}$, is a low-pass response with a cutoff frequency equal to the loop bandwidth [1], while noises from the charge pump (CP), $I_{n,\rm cp}$, and input reference clock, $\phi_{n,\rm ref}$, are bandpass filtered by the loop. Also, in the locked condition, the CP noise is scaled due to it only appearing on the control voltage for a time equal to the reset path delay of the phase-frequency detector (PFD) [21], which is a fraction of a reference clock cycle. Assuming a low-noise input reference clock, the VCO noise and CP noise are generally dominant. However, care should also be used in choosing the loop filter resistor, as its noise on the control voltage is high-pass filtered by the loop. Note, an important tradeoff exists between the control voltage noise level and the PLL settling time, as reducing the PLL bandwidth filters more VCO input-referred noise and CP noise at the cost of increasing the system measurement time. Another important noise source, the system quantization noise, is set by the ADC resolution [1]. This implies a significant increase in ADC resolution requirements and overall complexity for improved frequency shift measurement capabilities.

B. Proposed System

As mentioned before, the use of a reference VCO enables filtering of correlated low-frequency noise between the sensor and reference VCO. This is achieved in a PLL-based system with the proposed sensor architecture shown in Fig. 3. Here, the PLL utilizes a single fixed reference clock and is controlled by the f_s clock, which alternates between having the sensor oscillator and fixed integer divider, N_S, in the loop and having the reference oscillator and adjustable fractional divider, N_R, present.

When f_s is in the low state, the reference VCO frequency, $f_{{\rm vco},R}$, is set to $8N_R f_{\rm ref}$ and the control voltage settles to $V_{c,R}$, while when f_s is in the high state, the sensor VCO frequency, $f_{{\rm vco},S}$, is set to $8N_S f_{\rm ref}$ and the control voltage settles to $V_{c,S}$. Assuming that the two division values are equal, $N_R = N_S$,

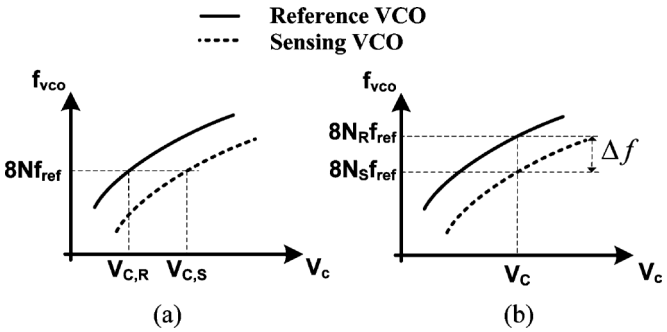

Fig. 4. VCO frequency versus control voltage. (a) $N_R = N_S = N$. (b) $V_{c,R} = V_{c,S} = V_c$.

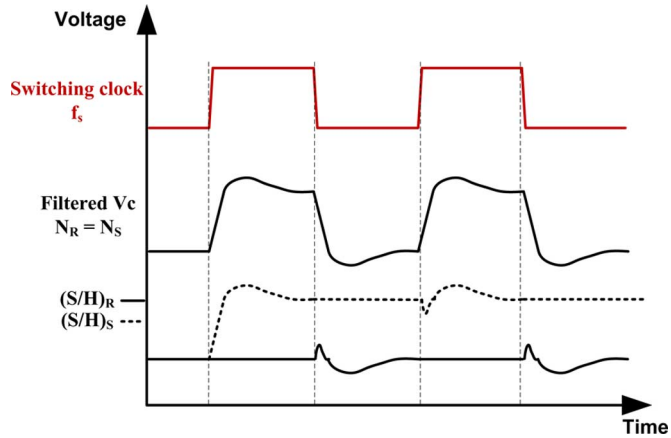

Fig. 5. System signals: sensor/reference control f_s, filtered control voltage V_c, and output of sample and hold circuits.

the difference between $V_{c,R}$ and $V_{c,S}$ is a function of the MUT-induced frequency shift between the two VCOs and

$$f_{\mathrm{vco},R} = f_o + K_{\mathrm{vco}} V_{c,R} \tag{1}$$
$$f_{\mathrm{vco},S} = (f_o - \Delta f) + K_{\mathrm{vco}} V_{c,S} \tag{2}$$

where K_{vco} is the VCO gain in Hz/V, f_o is the free-running frequency of the reference VCO, and Δf is the difference between the free-running frequencies of the reference and sensing VCOs, which is the subject of detection. Substituting $f_{\mathrm{vco},R} = 8N_R f_{\mathrm{ref}}$ and $f_{\mathrm{vco},S} = 8N_S f_{\mathrm{ref}}$ results in

$$8N_R f_{\mathrm{ref}} = f_o + K_{\mathrm{vco}} V_{c,R} \tag{3}$$
$$8N_S f_{\mathrm{ref}} = (f_o - \Delta f) + K_{\mathrm{vco}} V_{c,S}. \tag{4}$$

Thus, as shown in Fig. 4(a), the frequency shift can be approximated as

$$\Delta f = K_{\mathrm{vco}}(V_{c,S} - V_{c,R}). \tag{5}$$

However, measuring the frequency shift based on the difference between $V_{c,R}$ and $V_{c,S}$ suffers from two drawbacks, which are: 1) the accuracy is degraded due to the VCO gain nonlinearity and 2) ahigh-resolution ADC is required. Using (5), the relationship between the VCO frequency, frequency shift in ppm, the average VCO gain, supply voltage, V_{DD}, and the number of ADC bits, N_{ADC}, is

$$\Delta f(\mathrm{ppm}) = \frac{V_{DD} K_{\mathrm{VCO}}}{2^{N_{\mathrm{ADC}}}} \times \frac{10^6}{f_{\mathrm{vco}}}. \tag{6}$$

For example, if $V_{DD} = 1.2$ V, $K_{\mathrm{vco}} = 500$ MHz/V, and $f_{\mathrm{vco},S} = 10$ GHz, an ADC with a minimum 10-bit resolution is required to detect frequency shifts in the order of ~60 ppm. The following describes how these two drawbacks are mitigated by a different detection algorithm and a bang–bang control loop.

In order to eliminate the effect of VCO gain nonlinearity, a different detection algorithm is used that is based on changing the division value, N_R, until the control voltage $V_{c,R}$ becomes equal to the control voltage $V_{c,S}$, as shown in Fig. 4(b). Here, the difference between N_R and N_S represents the frequency shift between the two VCOs,

$$\Delta f = 8 f_{\mathrm{ref}}(N_R - N_S). \tag{7}$$

Here, the frequency shift measurement is independent of the VCO gain nonlinearity. However, the measurement accuracy is still limited by the reference frequency value and the resolution of the adjustable frequency fractional divider. As reducing the reference frequency mandates reducing the PLL bandwidth, which increases the PLL settling time, this system employs an off-chip fractional divider, N_R. While this fractional divider could easily be implemented in the CMOS chip, since designing high-resolution dividers is much easier than high-resolution ADCs, due to tape-out time constraints an external divider was used in this prototype, as shown in Fig. 3. A fractional divider with M-bit fractional resolution provides a minimum frequency shift of $\Delta f(\min, \mathrm{ppm}) = f_{\mathrm{ref}}(1/2^M)(10^6/f_{\mathrm{vco}})$. For example, utilizing a 25-MHz reference frequency, 10-GHz VCO frequency, and a 25-bit fractional divider results in a resolution of 7.7×10^{-5} ppm.

In order to alleviate the need for a high-resolution ADC, a bang–bang control loop is used to adjust the divider value. Here the term "bang–bang" indicates that the control loop's error detector, which is a comparator, generates only a quantized logical "−1" or "+1" depending only on the error sign, similar to the operation of a bang–bang phase detector used in clock-and-data recovery systems [22]. As illustrated in Fig. 5, the control voltage is sampled during each phase of the switching clock, f_s, using sample and hold circuits $(\mathrm{S/H})_R$ and $(\mathrm{S/H})_S$ and applied to a comparator. The comparator output is used to adjust the fractional divider value and determine the frequency shift. A cumulative density function (CDF) of the average comparator output, V_{comp}, versus the difference between $V_{c,R}$ and $V_{c,S}$ is shown in Fig. 6, assuming Gaussian system noise. If the average comparator output is near a logical "−1" or "+1," the difference between $V_{c,R}$ and $V_{c,S}$ is significantly larger than the total system noise and the system uses the averaged comparator output to adjust the reference divider. As the difference between $V_{c,R}$ and $V_{c,S}$ moves toward zero, the system noise causes the comparator to output a similar number of "−1" and "+1" outputs, and the averaged output approaches zero. Once the averaged comparator output is near zero to within a certain tolerance, the frequency shift is then calculated. As the sensor divider remains fixed, this approach ensures that the frequency shift is measured at a fixed frequency, regardless of the frequency shift.

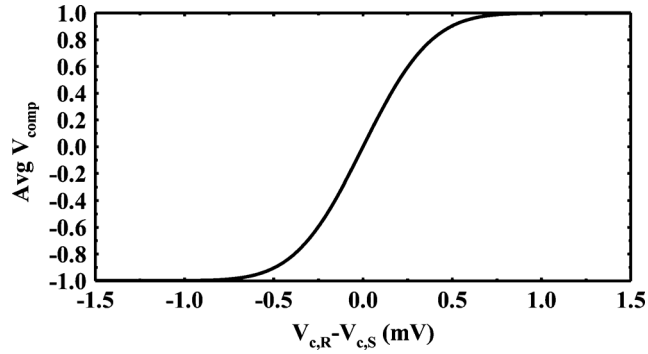

Fig. 6. CDF function that represents the averaged comparator output versus the difference between $V_{c,R}$ and $V_{c,S}$ with $\mathrm{sigma} = 0.25$ mV, which corresponds to 15 ppm at $k_{\mathrm{vco}} = 500$ MHz/V.

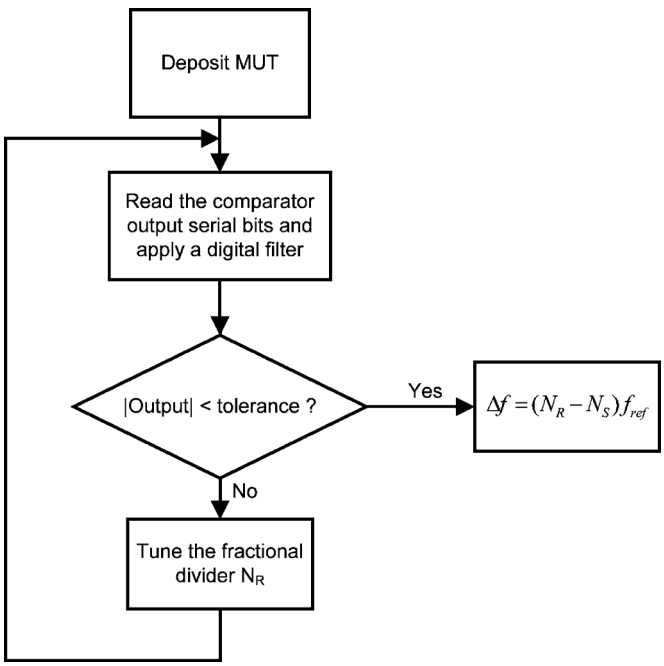

Fig. 7. Flowchart of the frequency shift measurement algorithm.

The flowchart of Fig. 7 summarizes the system operation as follows.

1) The MUT is deposited on top of the sensing VCO.
2) The comparator output bits are readout to a PC and digitally filtered.
3) The division ratio, N_R, is tuned until the average comparator output approaches zero.
4) At which, the frequency shift is measured as $f_{\mathrm{ref}}(N_R - N_S)$.

Note that this measurement procedure requires only a single MUT application, and is dramatically simpler than the multi-step MUT application and de-application procedure of [1]. Several techniques are utilized in order to improve the system noise performance and account for mismatches between the sensor and reference VCO. A filtered version of the PLL control voltage at node X (Fig. 3) is sampled in order to filter high-frequency noise. Additional low-frequency noise filtering is also possible by increasing the averaging time of the comparator outputs. As the mismatches between the two VCOs and the comparator input-referred offset introduces a systematic system offset, this is accounted for during sensor calibration by characterizing the system with the sensing VCO not loaded with any MUT. For this calibration case with the sensor only exposed to air, the difference between N_R and N_S is read out, recorded, and serves as the overall system offset. Note that this offset calibration should be performed at each material characterization frequency in order to account for the VCOs' K_{vco} variation with frequency. In addition, any K_{vco} mismatch between the VCOs can be calibrated by performing measurements with control materials of known permittivity; with system accuracy improving with the number of calibration materials employed. Additional sensor calibration details are provided in the experimental results of Section VI-B.

TABLE I
10-GHz PLL PARAMETERS

f_{ref}	25 MHz
Damping Factor, ζ	1
Bandwidth	1 MHz
k_{vco}	600 MHz/V
Charge Pump Current, I_{cp}	100 μA
R_z	49 kΩ
C_1	13 pF
C_2	800 fF

Table I summarizes the 10-GHz PLL system-level specification. The PLL utilizes a 25-MHz reference clock and is designed with a damping factor of 1 for robust operation and a 1-MHz bandwidth to enable fast switching between the sensor and reference VCOs. Tradeoffs between system noise and loop filter area are considered in selecting the CP current and loop filter parameters. While increasing the CP current decreases the contributed noise on the control voltage [21], for a given bandwidth and damping factor, it increases the required loop filter capacitor, which increases the area. Thus, a 100-μA CP current is selected to enable reasonable loop filter values. Also, as the control voltage is observed at the loop filter internal node X, the values of R_z and C_1 are selected to enable a fast switching frequency between the two VCOs, f_s.

III. Sensor Design

A. Sensing Element

Each MUT has a frequency-dependent complex relative permittivity $\varepsilon_r(\omega) = \varepsilon_r'(\omega) - j\varepsilon_r''(\omega)$ with both real and imaginary components. The real part represents the stored energy within the material and the imaginary part represents the material's loss with the loss tangent quantifying the ratio between $\varepsilon_r''(\omega)$ and $\varepsilon_r'(\omega)$ $(\tan\delta = \varepsilon_r''(\omega)/\varepsilon_r'(\omega))$. As the objective of the implemented sensor is to detect the real part of the MUT's complex permittivity, the MUT is placed on top of a capacitor-based sensor and the permittivity is measured with the change in the sensor's capacitance. This section explains the sensor's design and key characteristics. It also discusses the effect of the material's loss on the capacitance measurements and permittivity detection.

A capacitor implemented on the top metal layer of a CMOS process with an area of 0.0461 mm^2, shown in Fig. 8(a) and

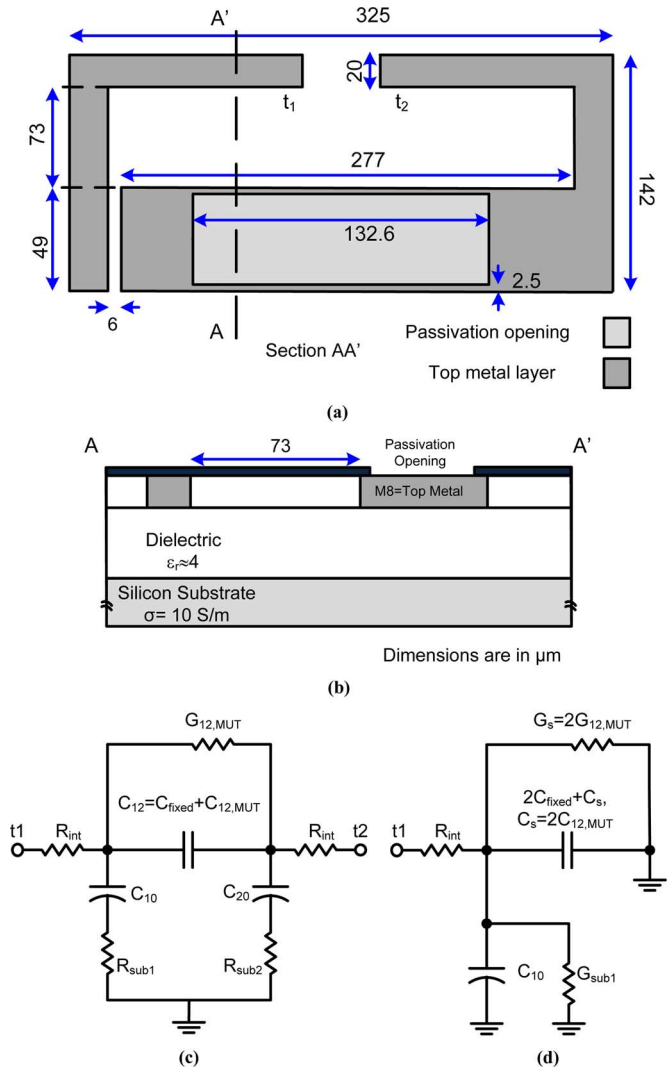

Fig. 8. Sensor capacitor. (a) Top view of the sensor. (b) Cross section (AA') view of the sensor. (c) Differential electrical model seen between t1 and t2. (d) Single-ended version of the capacitor model. All dimensions are in micrometers.

(b), forms the sensing element. The 325 μ m $\times$ 142 μm capacitor has the equivalent circuit model shown in Fig. 8(c). The MUT affects the electromagnetic (EM) fields between t1 and t2, with the admittance $Y_{12}(\omega)$ between t1 and t2 having a fixed capacitive component due to direct parallel-plate capacitance between the capacitor's metal, C_{fixed}, a parallel plate capacitance to substrate, C_{10}, C_{20}, and a fringing capacitance that changes according to the permittivity of the MUT, $C_{12,\text{MUT}}$. Loss components are present due to the substrate loss and MUT loss, which are modeled by R_{sub} and $G_{12,\text{MUT}}$, respectively. EM simulations show that the capacitor qualify factor in air is approximately 4.7 at 10 GHz and degrades to 1.7 when loaded with a MUT with permittivity of 10 and $\tan\delta = 1$. While this sensor capacitor Q is lower than anticipated due to an error in the substrate loss estimation in the initial design phase, it is only a minor contributor to the total oscillator tank Q and it does not have a major impact on the overall system performance.

When the sensor is exposed to air, the fringing component consists only of $C_{12,\text{air}}$ due to air being lossless. After depositing a MUT with permittivity of $\varepsilon_r(\omega) = \varepsilon_r'(\omega) - j\varepsilon''(\omega)$,

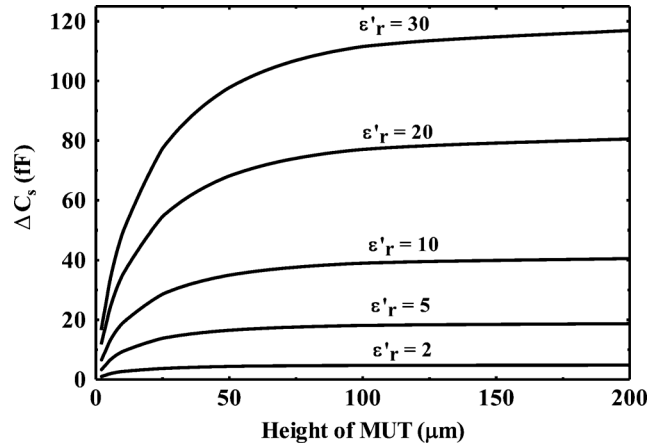

Fig. 9. Sensing capacitance variations versus the deposited height of the MUT for five ε_r' values.

the fringing component changes to the parallel combination of $C_{12,\text{MUT}}$ and a conductive part, $G_{12,\text{MUT}}$. Neglecting the sensor interconnect resistance, R_{int}, the equivalent parallel-plate capacitance and conductance of the sensing element are approximately given by

$$\begin{aligned} C_{12,\text{MUT}} &= \varepsilon_r'(\omega) C_{12,\text{air}} \\ G_{12,\text{MUT}} &= \omega \varepsilon_r''(\omega) C_{12,\text{air}}. \end{aligned} \tag{8}$$

Fig. 8(d) shows the equivalent half circuit model, where C_s is the effective capacitance proportional to the real part of the material's dielectric constant, $C_s = 2\varepsilon_r'(\omega)C_{12,\text{air}}$, and G_s is the effective parallel conductance modeling the effect of the material loss, $G_s = 2\omega\varepsilon_r''(\omega)C_{12,\text{air}}$.

The capacitance C_s changes with ε_r' and with the height of the MUT deposited on top of the sensing capacitor [1]. EM simulations for the sensing capacitor were performed using Sonnet,[1] with Fig. 9 showing the value of the sensing capacitance versus the MUT height for different values of ε_r' up to 30. The capacitance increases with MUT height until saturating for heights larger than 50 μm, which is considered to be the sensor EM field saturation height.

A more detailed expression for the sensor input capacitance is obtained from the total admittance at terminal t1, including the sensor interconnect resistance

$$Y_{t1} \cong j\omega C_o \frac{1 - R_{\text{int}} G_o}{1 + \omega^2 R_{\text{int}}^2 C_o^2} + G_o \frac{1 + \omega^2 C_o^2 R_{\text{int}}/G_o}{1 + \omega^2 R_{\text{int}}^2 C_o^2} \tag{9}$$

where

$$\begin{aligned} G_o &= G_{\text{sub}} + G_s \\ C_o &= 2C_{\text{fixed}} + C_s + C_{10}. \end{aligned}$$

Equation (9) shows that in addition to the sensor capacitance terms, the sensor conductance can impact the total equivalent capacitance at t1 due to the interconnect resistance term. R_{int} should be minimized in order to minimize the effect of the sensor conductance on its capacitance. As shown in Table II, the R_{int} value of 0.55 Ω is achieved by using wide top-level

[1]Sonnet Software Inc. [Online]. Available: www.sonnetsoftware.com

TABLE II
SENSOR CAPACITOR MODEL PARAMETERS IN AIR

C_{12}	7 fF
C_{10}	18 fF
C_{20}	55 fF
G_{sub1}	0.32 mS
G_{sub2}	1.15 mS
R_{int}	0.55 Ω

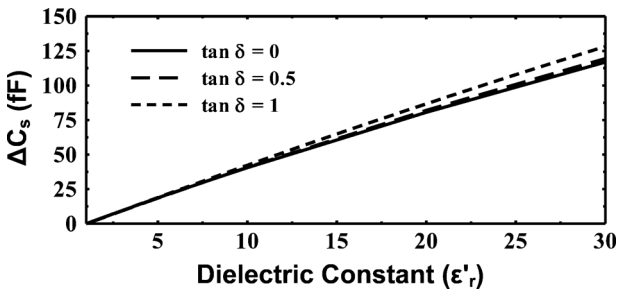

Fig. 10. Sensing capacitance variations versus ε'_r of MUT for height 200 μm (above saturation height) at 10 GHz.

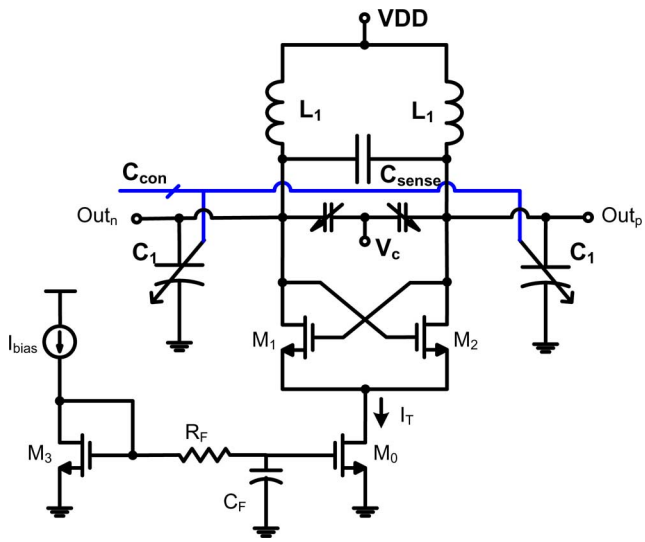

Fig. 11. Simplified schematic of the nMOS cross-coupled sensing VCO.

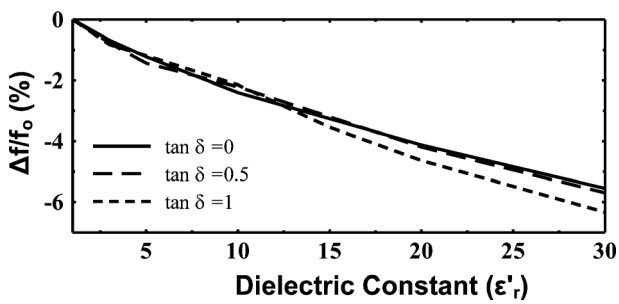

Fig. 12. Percentage variation of the resonance frequency versus ε'_r for different values of $\tan\ \delta$ at a MUT height of 200 μm.

metal connections. Fig. 10 shows that this allows for a nearly linear relationship between C_s and ε'_r, with the loss tangent $(\tan\ \delta)$ having only a small effect on the value of C_s for ε'_r less than 10.

B. Sensing VCO

Fig. 11 shows a simplified schematic of the sensing VCO used to measure the $C_s(\omega)$ capacitance change due to the MUT deposition. The large intrinsic transconductance, with relatively small parasitic capacitance, of the nMOS cross-coupled transistors allows for high-frequency operation at the nominal 1.2-V supply voltage. In addition to the sensing capacitor, inductor L_1 and capacitor C_1 make up the oscillator's resonance tank. By applying the MUT, $C_s(\omega)$ changes and the frequency of oscillation shifts by a value of Δf. Assuming C_1 is much larger than $C_s(\omega)$, there is a linear relationship between $\Delta f/f_o$ and the relative C_s capacitance change for small frequency shifts

$$\Delta f/f_o \approx -\frac{1}{2}\frac{\Delta C_s}{(C_1+C_s)} \approx -\frac{(\varepsilon'_r(\omega)-1)C_{12,\text{air}}}{(C_1+C_s)} \tag{10}$$

where f_o is the resonance frequency in air.

The simulation results of Fig. 12, which show the percentage variation of the VCO resonance frequency with ε'_r for different values of $\tan\delta$, verify this linear relationship and show only a small impact due to $\tan\delta$. Note that the material loss, or ε''_r, can affect the frequency shift due to two reasons, which are: 1) it can potentially change C_s (however, as shown in the previous section, ε''_r has a small effect on C_s) and 2) loss variations result in amplitude variations, which translate into frequency variations due to amplitude modulation to frequency modulation (AM–FM) conversion [23]. This is a nonlinear process, as shown in the VCO simulation results of Fig. 13. For small amplitudes up to around 0.45 V, the frequency is nearly constant versus the amplitude. However, as the amplitude further increases, the frequency decreases dramatically. Thus, to minimize the AM–FM conversion, the selected range for the VCO single-ended amplitude is designed below 0.45 V.

IV. CIRCUIT IMPLEMENTATION

A. Sensor and Reference VCOs

In order to track the frequency drift of the sensing VCO due to environmental conditions and low-frequency noise, a reference VCO is also employed, as shown in Fig. 14(a). Since the frequency shift is measured as the difference in the oscillating frequency of both the sensing and reference VCOs, any correlated noise is filtered [19]. While noise correlation is maximized with the sharing of as many elements as possible, with the best scenario involving the sharing of all VCO components, except the sensing and reference capacitors, the periodic enabling of the VCOs in this case necessitates a high-frequency switch, which degrades the tank quality factor considerably at 10 GHz. However, it is still possible to share the tail current source, which represents a main source of flicker noise, between the two VCOs with a low-frequency switch. Thus, the VCO noise contribution in the system frequency shift measurements is affected only by the noncommon elements, which include the cross coupled pair and the *LC* tank. It is worth mentioning that the applied MUT has negligible impact on both the sensor and reference VCO tank inductance due to the virtually unity relative permeability

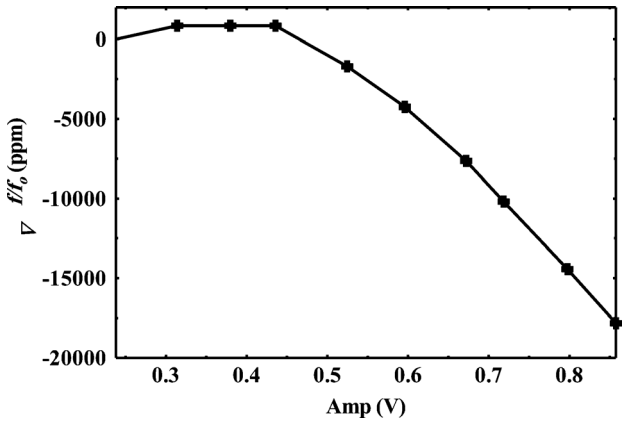

Fig. 13. Percentage variation of the VCO output frequency versus the single-ended amplitude level.

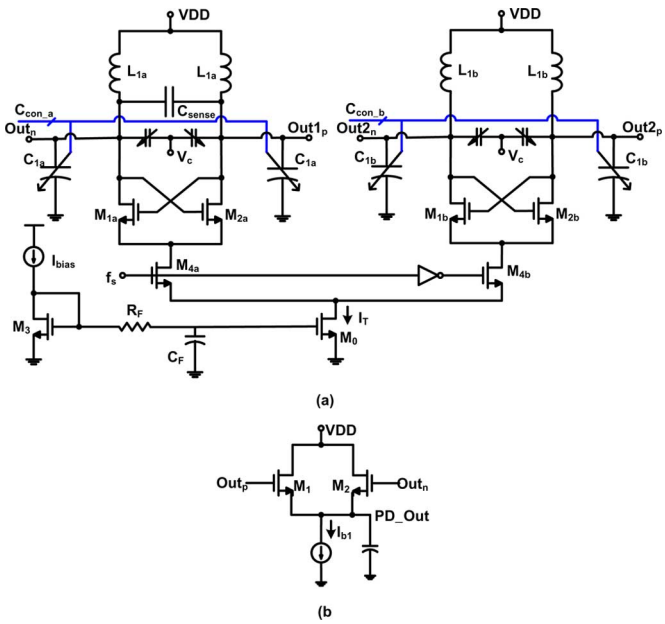

Fig. 14. (a) Schematic of the shared-bias VCO circuits (the sensing VCO and the reference VCO) with a common tail current source to increase correlated noise. (b) Peak detector schematic.

of the materials under study. Moreover, any changes in the inductor's parasitic capacitance due to MUT application is minimized due to the 1-μm passivation layer between the MUT and the inductors.

The VCO phase noise should be minimized to enhance the sensor sensitivity, particularly at low-frequency offsets where flicker noise dominates. In order to achieve this, the following design techniques are implemented.

1) The inductor quality factor is maximized at the operating frequency by employing a single-turn inductor using wide 4-μm-thick top metal (Al) tracks that are 5.75 μm from the substrate, resulting in an inductor factor (Q_{L1}) of around 18. When varactor and sensor capacitor losses are included, the total tank Q degrades to 10 in air and around 7 when loaded with a MUT with permittivity of 10 and $\tan\delta = 1$.
2) A low-pass filter formed with R_F and C_F reduces the noise contribution of the bias transistor M_3.

TABLE III
SIZES OF TRANSISTORS IN VCO

Transistor	$W(\mu)/L(\mu)$
M_0	480/0.8
M_1, M_2	22/0.1
M_3	80/0.8
M_4	768/0.1
L_1	220 pH
C_1	≈ 1 pF

In order to minimize the phase noise due to AM–FM conversion, the oscillator's bias current is adjusted to keep the single-ended oscillation amplitude around 0.45 V (Fig. 13). A peak detector, shown in Fig. 14(b), is connected to the VCO output to sense the amplitude level, which is used to control the amplitude.

Table III summarizes the VCO transistor sizes and tank component values. Post-layout simulations show that the VCO operating near 10 GHz has a 7% tuning range, phase noise of -107 dBc/Hz at a 1-MHz offset, and 9-mA current consumption.

B. Frequency Divider

Fig. 15 shows a detailed block diagram of the on-chip integer divider. In order to provide flexibility in reference clock selection, the integer divider has a programmable ratio from 256 to 504 with a step of 8. The divider is partitioned into current-mode logic (CML) stages, which offer high-frequency operation and superior supply noise rejection, for the initial divide-by-8, followed by CML-to-CMOS conversion and the use of static CMOS circuitry to implement the remaining division in a robust and low-power manner. Two independent CML divide-by-2 blocks are utilized for the initial 10-GHz frequency division in order to provide sufficient isolation between the sensor and reference VCOs and also reduce oscillator loading. These initial dividers are ac coupled to the VCO for proper biasing and consume 2 mA each with an effective 12-GHz bandwidth. A MUX unit then selects which divided clock is placed in the loop and also serves as a buffer to drive a second CML divide-by-4 stage. As this second divider stage works near 1.25 GHz, it only consumes 0.3 mA. The CML-to-CMOS converter stage [24] drives both a buffer to the external fractional divider and the on-chip five-stage dual-modulus 2/3 divider [25] that provides a programmable division ratio from 32 to 63 with a step of 1.

C. PFD and CP

The PFD is implemented using the common topology described in [26]. A relatively low 25-MHz reference frequency for the 90-nm CMOS technology allows for a static CMOS design for robustness and low-power consumption.

Fig. 16 shows the CP schematic [26], [27]. Here, current from the M5/M6 down/up current sources is steered between a path attached to the loop filter and an auxiliary path connected to a $V_{\rm ref}$ voltage. This approach allows the current sources to conduct current at all times, which reduces the charge sharing that can occur if the current source drain voltages completely discharge to the supply voltages and results in lower deterministic disturbances on the control voltage. Improved matching

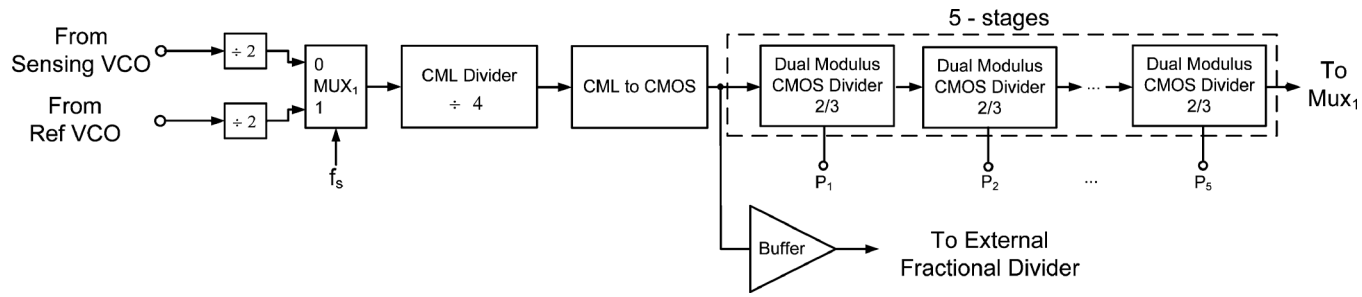

Fig. 15. Integer frequency divider block diagram.

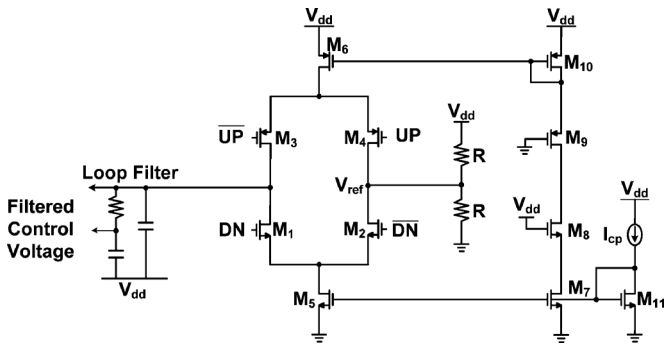

Fig. 16. CP schematic.

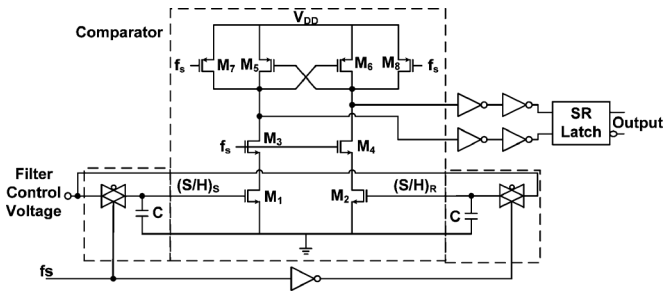

Fig. 17. Comparator and sample and hold circuits.

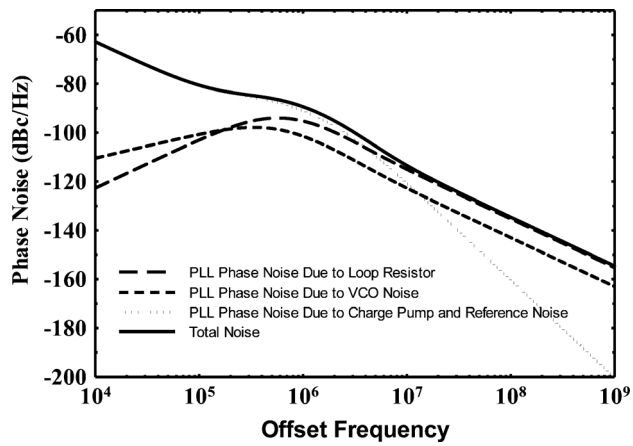

Fig. 18. Simulated closed-loop PLL 10-GHz output phase noise.

between the CP up/down currents is also achieved by using dummy switch transistors M8 and M9 in the bias current mirror path.

D. S/H and Comparator

The S/H and comparator circuits are shown in Fig. 17. As mentioned in Section II-B, the filtered VCO control voltage is sampled when both the sensor and reference oscillator are in the PLL loop. The f_s clock signal controls the transmission-gate switches to hold the control voltage on a 1-pF capacitor, C. These sampled control voltage signals are applied to a dynamic voltage-mode sense-amplifier comparator. This comparator's output is buffered through a series of inverters, stored with a set–reset (SR) latch, and driven off-chip for digital filtering to control the adjustable divider. While the kilohertz-range sample clock frequency relaxes the comparator design, it is important to reduce the comparator input-referred noise, as it appears directly on the critical VCO control voltage. Note that while the comparator offset also directly contributes to the system offset, this is less critical because it can be measured and canceled through the sensor calibration procedure described in Section VI-B.

E. System Sensitivity

As mentioned in Section II-B, amongst the core PLL circuits, the VCO, CP, and loop filter resistor contribute to the simulated closed-loop PLL output phase noise of Fig. 18. Here, a phase noise of -88 dBc/Hz is achieved at a 1-MHz offset. Using the simulated noise from each block and the transfer function from that block to the control voltage, an overall integrated noise is calculated and converted to a frequency noise using a $K_{\rm vco}$ of 600 MHz/V, resulting in a 2-ppm$_{\rm rms}$ frequency noise. However, as the comparator for the bang–bang control loop is directly attached to the control voltage, its noise must also be carefully considered. Utilizing the dynamic comparator noise simulation procedure described in [28] results in a comparator input-referred noise of 0.2 mV$_{\rm rms}$, which, using (5), is equivalent to 12 ppm$_{\rm rms}$ with a $K_{\rm vco}$ of 600 MHz/V. Combining the noise contributions statistically yields an overall system noise estimate of 12.2 ppm$_{\rm rms}$, indicating that the overall system noise is actually dominated by the comparator of the bang–bang control loop. This insight allows for further performance improvements in future implementations by locating the comparator after a low-noise pre-amplifier stage designed for reduced input-referred noise [29]. Note that the above analysis is for air loading, and the VCO performance will degrade when loaded with a lossy MUT. Simulations indicate that when loaded with a MUT of ε_r' of 10 and $\tan\delta$ of 1, the phase noise degrades by 5 dB. However, due to the noise of the comparator

used in the current design, this MUT-loading noise degradation has minimal impact on overall system sensitivity.

V. System Integration and Test Setup

A. System On-Board Integration

Fig. 19 shows the chip microphotograph of the PLL-based dielectric sensor, which was fabricated in a 90-nm CMOS process and occupies a total chip area of 2.15 mm^2. As detailed in Table IV, the overall chip power consumption is 22 mW, with the VCO and high-frequency dividers consuming the most power. An open-cavity micro lead frame (MLP) 7×7 mm^2 QFN 48 package is used for chip assembly[2] to allow for MUT deposition on top of the sensing capacitor. All electrical connections between the chip and the package lead frame are made via wire-bonding.

An off-chip commercial discrete fractional frequency divider (ADF4157) from Analog Devices[3] is utilized in order to achieve high resolution in the frequency shift measurements. The external divider has 25-bit resolution, which allows for potential frequency shift measurements down to 6×10^{-4} ppm, considering the divide-by-8 on-chip CML divider. This implies that the system is not limited by the divider quantization noise, but rather the system random noise discussed earlier.

Fig. 20 shows the photograph of the printed circuit board (PCB) with the mounted sensor chip and the external divider. The sensor chip interfaces with the external divider with a buffered version of the on-chip CML divide-by-8 output at 1.25 GHz (Fig. 15) driven to the external divider, and the divided output signal at 25 MHz fed back to the CMOS chip to MUX_2 (Fig. 3) that selects the PFD input based on the switching clock phase. Simple level-shifting interface ICs are used to condition the comparator's serial output bits to levels sufficient for the PC, which performs the digital filtering. The frequency shift measurement algorithm of Fig. 7 is performed automatically via a Labview[4] program such that the MUT is deposited on top of the sensor, the external reference divider is adjusted with a successive-approximation procedure, and the corresponding frequency shift is measured directly.

B. Chemical Sensing Test Setup

Organic chemical liquids, including methanol and ethanol and their mixtures, are applied to the sensor chip via a plastic tube fixed on top of the chip [1]. Due to the 1.2-mm tube diameter being comparable to the chip area and tube mechanical handling limitations, both the reference and sensing VCOs are covered by the MUT during testing. In order to avoid the effect of the MUT on the reference VCO, the metal capacitor in Fig. 19 is not attached to the reference oscillator. While this does result in a systematic offset between the VCOs, this is easily measured with the sensing capacitor exposed to air and later calibrated out.

In order to control the volume of the material applied on the sensor chip, a Finnpipette[5] single-channel micropipette is utilized to apply the liquid via the tube. After material application, the tube is capped to avoid evaporation. All measurements were performed with volumes less than 20 μL, which is sufficient to cover the sensor in excess of the saturation height due to the small sensor size.

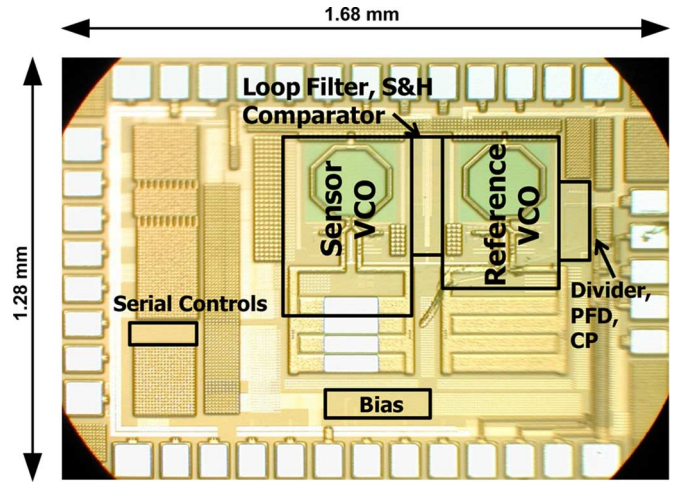

Fig. 19. Micrograph of the PLL-based dielectric sensor chip.

TABLE IV
Sensor Chip Power Consumption

Block	Power Consumption (mW)
VCO	10.8
High Frequency Dividers	7.2
PFD + CP	0.4
Output Buffer	3.6
Total	22

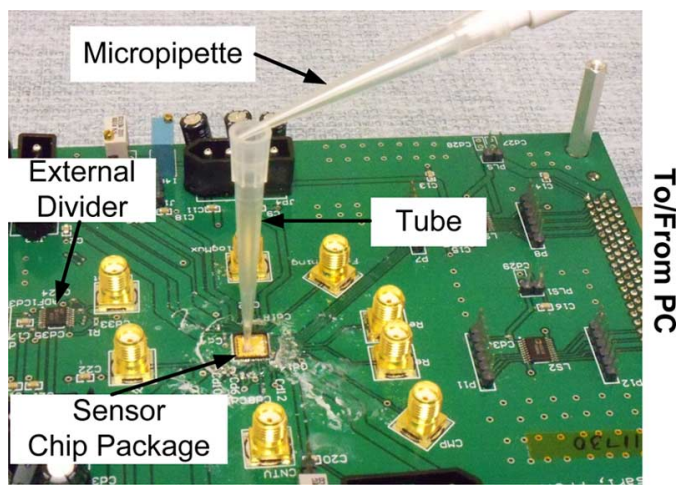

Fig. 20. Photograph of the PCB with the chip, external divider, micropipette, and the MUT application tube indicated.

VI. Experimental Results

This section discusses the fractional-N PLL-based chemical sensor experimental results. First, key measurements of the PLL and system sensitivity are presented. Next, data is shown with the system characterizing organic chemical mixtures.

[2]Majelac. [Online]. Available: www.majelac.com

[3]Analog Devices. [Online]. Available: www.analog.com

[4][Online]. Available: www.ni.com/labview

[5][Online]. Available: http://www.thermoscientific.com

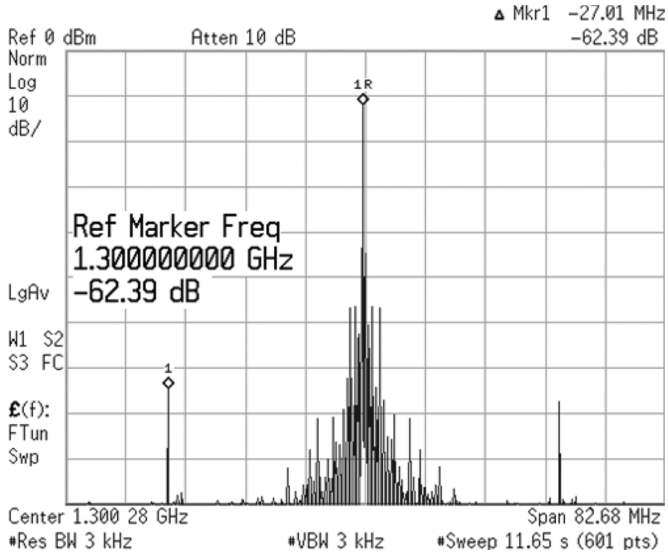

Fig. 21. PLL output spectrum after CML divide-by-8 divider.

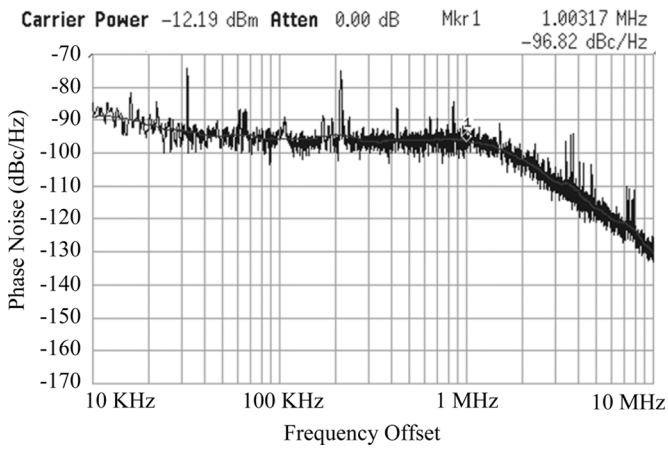

Fig. 22. Reference VCO phase noise measurements after CML divide-by-8 divider.

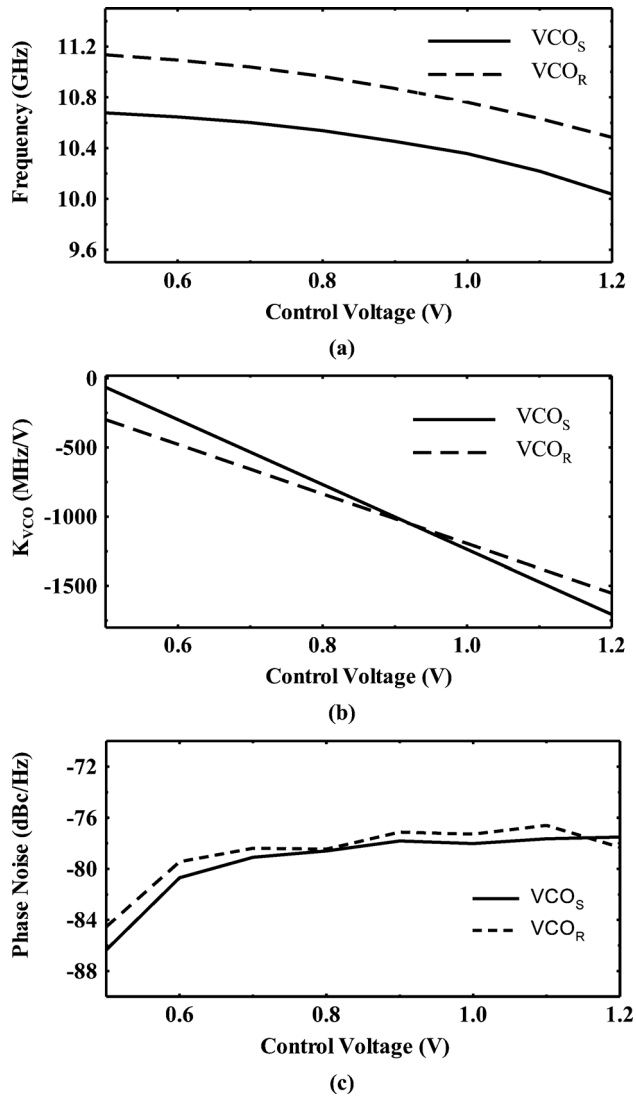

Fig. 23. PLL measurements versus the control voltage with both reference VCO and sensor VCO. (a) VCO frequency. (b) $K_{\rm VCO}$. (c) Phase noise at a 1-MHz offset.

A. PLL and Sensitivity Characterization

The output spectrum and phase noise of the closed-loop PLL with the sensor VCO in the loop is measured at the output of the divide-by-8 CML block, as shown in Figs. 21 and 22, respectively. For the 1.3-GHz signal, reference spurs less than -60 dBc and a phase noise of -97 dBc/Hz at a 1-MHz offset are achieved. This phase noise converts to -79 dBc/Hz at a 1-MHz offset for the on-chip 10.4-GHz signal. As shown in Fig. 23, the PLL achieves a 640-MHz locking range between 10.04–10.68 GHz and a 885-MHz/V $K_{\rm vco}$, at control voltage of 0.85 V, with the sensing VCO in the loop. Due to the absence of the sensor capacitor, the PLL achieves a 650-MHz locking range between 10.49–11.14 GHz and a 925-MHz/V $K_{\rm vco}$, at control voltage of 0.85 V, with the reference VCO in the loop. Similar phase noise is achieved for both VCOs operating inside the PLL versus the control voltage.

In order to characterize the system noise level, the bang–bang divider control is set in open-loop and a CDF of the average comparator output is produced by varying the external divider value, N_R. A switching frequency of $f_s = 1$ kHz is employed in order to allow enough time for the PLL to settle with high accuracy. The results in Fig. 24 are fitted to a Gaussian distribution and a system noise sigma of 15 ppm is extracted. This noise value is very close to the 13 ppm predicted by previously discussed system simulations, indicating that the comparator noise is most likely currently limiting the system performance.

B. Chemical Measurements

1) Dielectric Frequency Dispersion and Mixture Theories: For pure MUTs, the complex permittivity frequency dependency follows the Cole–Cole model [16] and the complex permittivity numbers in [17]. The model is as follows:

$$\varepsilon(\omega) = \varepsilon'(\omega) - j\varepsilon''(\omega) = \varepsilon_{r,\infty} + \frac{\varepsilon_{r,0} - \varepsilon_{r,\infty}}{1 + (j\omega\tau)^{1-\alpha}} \qquad (11)$$

where $\varepsilon_{r,0}$ is the static permittivity at zero frequency, $\varepsilon_{r,\infty}$ is the permittivity at ∞, τ is the characteristic relaxation time, and α is the relaxation time distribution parameter.

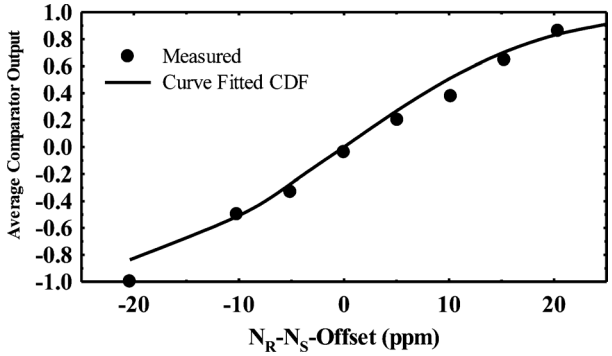

Fig. 24. Measured average comparator output versus the difference in the divider values.

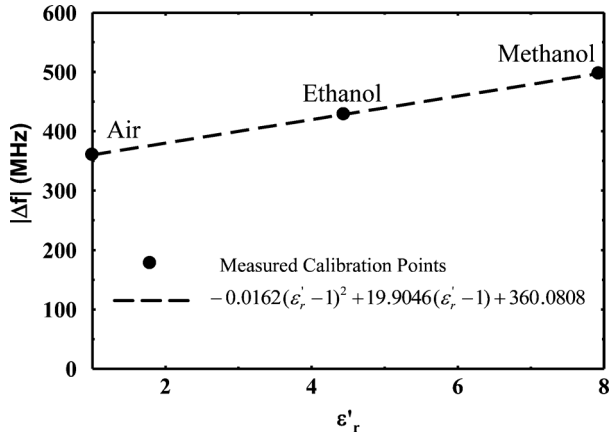

Fig. 25. Fitted absolute frequency shift $|\Delta f|$ versus ε_r' at the sensing frequency of 10.4 GHz with the calibration points indicated.

Binary mixtures are composed of two materials, which are: 1) the environment (host) and 2) the inclusion (guest) with ratios of $(1-q)$ and q, respectively. The complex permittivity of a binary mixture is a function of the complex permittivities of the two constituting materials and the fractional volume ratio q. This relationship is mathematically defined as follows [30], [31]:

$$\frac{\varepsilon_{\text{eff}}-\varepsilon_e}{\varepsilon_{\text{eff}}+2\varepsilon_e+\nu(\varepsilon_{\text{eff}}-\varepsilon_e)}=q\frac{\varepsilon_i-\varepsilon_e}{\varepsilon_i+2\varepsilon_e+\nu(\varepsilon_{\text{eff}}-\varepsilon_e)} \quad (12)$$

where ε_{eff} is the effective mixture permittivity, ε_e is the permittivity of the environment, ε_i is the inclusion permittivity, and ν is a parameter to define the employed model. ν has values of 0, 2, and 3 corresponding to Maxwell–Garnett, Polder-van Santen, and quasi-crystalline approximation rules, respectively.

2) Sensor Calibration: As previously described in the Fig. 7 flowchart, the MUT is deposited on the sensor and the corresponding frequency shift is measured to determine the permittivity. Due to process variations, system offset, and K_{vco} mismatches, the relationship between frequency shift and permittivity has to be calibrated for stable and accurate measurements. While (10) predicts an ideally linear shift in frequency with MUT ε_r', the use of a higher order polynomial function allows additional degrees of freedom to calibrate for items such as K_{vco} mismatches. A quadratic equation is used to describe the frequency shift in megaherz as a function of the permittivity [1]

$$\Delta f=a(\varepsilon_r'-1)^2+b(\varepsilon_r'-1)+c \quad (13)$$

where a, b, and c are the calibration constants. Note that the constant c represents the system offset mentioned in Section II-B. Three calibration materials are required to determine these constants. In this work, air, pure ethanol, and pure methanol are used as calibration materials whose ε_r' at the testing frequency (10.4 GHz) are 1, 4.44–j2.12 $(\tan\delta=0.48)$, and 7.93–j7.54 $(\tan\delta=0.95)$, respectively [17]. Depositing each of these calibration materials on the sensor independently and measuring the induced frequency shifts allows extraction of a, b, and c, which are found to be -0.0162, 19.9046, and 360.0808, respectively. During this calibration process, the comparator output is digitally filtered by averaging for 100–200 bits in order to ensure stable measurements. Fig. 25 shows how the measured frequency shift Δf versus permittivity ε_r' matches with the calibration curve.

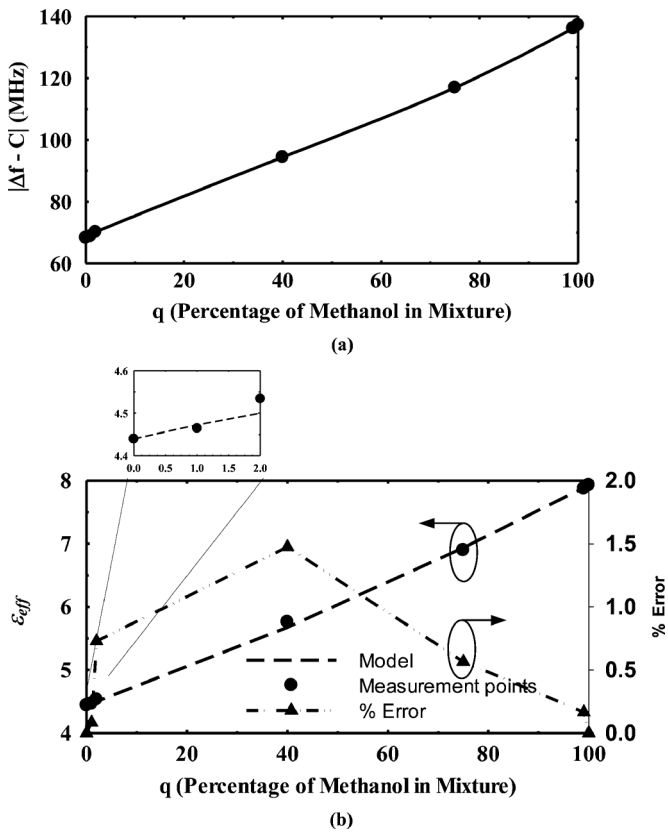

Fig. 26. Measurement results of an ethanol–methanol mixture. (a) Frequency shift versus the concentration of methanol in the mixture. (b) Effective dielectric constant derived from the measured frequency shifts and compared to the model with $\nu=2$ and permittivity percentage error.

3) Mixture Characterization and Permittivity Detection: As a proof of concept, the system is used to detect the permittivity of a mixture of ethanol and methanol with several ratios of q and $(1-q)$ respectively, $0\le q\le 1$. Mixture accuracy is ensured by preparation with high volumes using a micropipette with 1 μL accuracy. For example, with a q of 0.4 and a total volume of 500 μL, 200 μL of pure ethanol is mixed with 300 μL of pure methanol using the micropipette. 20 μL is then taken from the mixture and deposited on top of the sensor for detection. For

TABLE V
PERFORMANCE SUMMARY AND COMPARISON TO PREVIOUS WORK

	Operating Frequency	Sensor Read-Out Approach	Area	Power Consumption	Permittivity Error
[6]	0.4-35 GHz	S-parameter lab measurements	NA	NA	3%[a]
[15]	4.5 GHz	Discrete components [b]	NA	NA	2 %
[32]	500 - 800 MHz	Discrete components [c]	NA	NA	3 %
[33]	1, 2 and 3 GHz	Network Analyzer	112 × 2.4 mm^2 [d]	NA	0.7 % - 12 %
[34]	8 GHz	Network Analyzer	40 × 15 mm^2 [d]	NA	0.5%
[12]	120-130 GHz	Integrated reflectometer PLL in 250 nm SiGe BiCMOS	1.4 mm^2	247.5 mW	NA
[1]	7 - 9 GHz	Integrated PLL in 90 nm CMOS [e]	2.5 × 2.5 mm^2	16.5 mW	3.5%
This Work	10.4 GHz	Integrated PLL in 90 nm CMOS [f]	1.68 × 1.28 mm^2	22 mW	1.5%

[a] Error is reported at 25 GHz.
[b] The system uses fractional-N PLL, micro-controller and ADC.
[c] The system uses PLL, peak detector and micro-controller.
[d] Sensor area only.
[e] Tunable reference oscillator is required.
[f] Off-chip fractional divider is used.

this case, the absolute value of the frequency shift is then measured and found to be 454.45 MHz ($|\Delta f - c| = 94.37$ MHz). Using (13) and the values of a, b, and c, the permittivity is then estimated to be 5.76. Repeating this procedure for other q values, Fig. 26(a) shows the frequency shift values versus q, and Fig. 26(b) compares the measured ε' versus q with the theoretical Polder-van Santen mixture model ($\nu = 2$) (12). The maximum difference between the measured and theoretical permittivity is less than 1.5%, as shown in Fig. 26(b). Note that the maximum error values are achieved for mixtures with comparable host and guest levels. Higher accuracy levels are achieved for more extreme ratios, with the sensor able to differentiate mixture permittivities with fractional volume down to 1%. These measurements show that the detected permittivities fit quite well to the theoretical values and that the system can characterize mixtures at a high accuracy level.

Table V summarizes the performance and compares the results with prior work. This work achieves a higher level of integration and higher frequency measurement capabilities relative to the work of [15] and [32]–[34]. Compared to the system in [1], the presented fractional-N PLL-based sensor achieves a more than 2× improvement in permittivity error at comparable power consumption and CMOS integrated circuit (IC) area.

4) System Accuracy Limitations: Although the measured 15-ppm$_{\mathrm{rms}}$ system noise without material application (Fig. 24) converts to a 0.1%$_{\mathrm{rms}}$ permittivity value from (13), several error sources contribute to the 1.5% maximum error observed between the measured and theoretical permittivity values. A discussion of these error sources follows, along with proposed solutions.

- **Kvco mismatch:** While system performance is insensitive to K_{vco} nonlinearity, K_{vco} mismatch does impact the system error. The use of a higher order polynomial curve and additional calibration materials can reduce this error term.
- **Temperature dependency:** Since permittivity measurements are performed at room temperature without precise temperature control, while 20 °C permittivity values are used in the calibration procedure, any temperature variation will degrade sensor accuracy. A potential solution for future systems is to employ an accurate temperature sensor and integrated heater beside the sensing capacitor for temperature stabilization.
- **Mixing accuracy:** It is important to follow standard mixing procedures to ensure high measurement accuracy levels. Increasing the volumes mixed to obtain a given ratio can improve this.
- **Air/gas bubbles:** Any air or gas bubbles present in the material on top of the sensing capacitor will impact the measured permittivity. A more advance microfluidics structure for material dispensing is a potential solution to this issue.

VII. CONCLUSION

This paper presented a self-sustained fractional-N PLL-based CMOS sensing system for dielectric constant detection of organic chemicals and their mixtures at precise microwave frequencies. System sensitivity is improved by employing a reference VCO, in addition to the sensing VCO, that tracks correlated low-frequency drifts. A simple single-step material application measurement procedure is enabled with a low-complexity bang–bang control loop that samples the difference between the control voltage with the sensor and reference oscillator in the PLL loop and then adjusts a fractional frequency divider. Binary mixture characterization of organic chemicals show that the system was able to detect mixture permittivities with fractional volume down to 1%. Overall, the high-level of integration and compact size achieved in this work makes it suitable for lab-on-chip and point-of-care applications.

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REFERENCES

[1] A. A. Helmy, H.-J. Jeon, Y.-C. Lo, A. J. Larsson, R. Kulkarni, J. Kim, J. Silva-Martinez, and K. Entesari, "A self-sustained CMOS microwave chemical sensor using a frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2467–2483, Oct. 2012.

[2] A. Lonappan, G. Binda, and V. Thomas, "Analysis of human semen using microwaves," *Progr. Electromagn. Res.*, vol. 57, pp. 277–284, 2006.

[3] A. Lonappan, V. Thomas, and G. Binda, "Analysis of human cerebra spinal fluid at the ISM band of frequencies," *J. Electromagn., Waves, Appl.*, vol. 20, no. 6, pp. 773–779, 2006.

[4] V. J. Brown, "Development of computer modelling techniques for microwave thermography," Ph.D. dissertation, Dept. Phys. Astron., Univ. Glasgow, Glasgow, U.K., 1989.

[5] A. Helmy and K. Entesari, "A 1–8 GHz miniaturized spectroscopy system for chemical sensing," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 17–22, 2012, pp. 1–3.

[6] K. Grenier, D. Dubuc, P.-E. Poleni, M. Kumemura, H. Toshiyoshi, T. Fujii, and H. Fujita, "Integrated broadband microwave and microfluidic sensor dedicated to bioengineering," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3246–3253, Dec. 2009.

[7] T. Chen, D. Dubuc, M. Poupot, J. Fournie, and K. Grenier, "Accurate nanoliter liquid characterization up to 40 GHz for biomedical applications: Toward noninvasive living cells monitoring," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4171–4177, Dec. 2012.

[8] M. Hofmann, G. Fischer, R. Weigel, and D. Kissinger, "Microwave-based noninvasive concentration measurements for biomedical applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 21195–2204, May 2013.

[9] C. Stagni, C. Guiducci, L. Benini, B. Ricco, S. Carrara, B. Samori, C. Paulus, M. Schienle, M. Augustyniak, and R. Thewes, "CMOS DNA sensor array with integrated A/D conversion based on label-free capacitance measurement," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2956–2964, Dec. 2006.

[10] K.-H. Lee, S. Choi, J. O. Lee, J.-B. Yoon, and G.-H. Cho, "CMOS capacitive biosensor with enhanced sensitivity for label-free DNA detection," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 120–122.

[11] A. Manickam, A. Chevalier, M. McDermott, A. Ellington, and A. Hassibi, "A CMOS electrochemical impedance spectroscopy biosensor array for label-free biomolecular detection," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2010, pp. 130–131.

[12] B. Laemmle, K. Schmalz, J. C. Scheytt, R. Weigel, and D. Kissinger, "A 125-GHz permittivity sensor with read-out circuit in a 250-nm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 2185–2194, May 2013.

[13] K. Schmalz, J. Borngraber, M. Kaynak, W. Winkler, J. Wessel, M. Neshat, and S. Safavi-Naeini, "A 120 GHz dielectric sensor in SiGe BiCMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 1, pp. 46–48, Jan. 2013.

[14] G. M. H. W. Ho and R. M. Govan, "Microwave measurements of liquid water content of atmospheric aerosols," *J. Appl. Meteorol.*, vol. 13, no. 8, pp. 871–879, Dec. 1974.

[15] V. Sekar, W. Torke, S. Palermo, and K. Entesari, "A self-sustained microwave system for dielectric-constant measurement of lossy organic liquids," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1444–1455, May 2012.

[16] K. S. Cole and R. H. Cole, "Dispersion and absorption in dielectrics I: Alternating current characteristics," *J. Chem. Phys.*, vol. 9, no. 4, pp. 341–351, Apr. 1941.

[17] F. Buckley and A. A. Maryott, "Tables of dielectric dispersion data for pure liquids and dilute solutions," NIST, Boulder, CO, USA, NBS circular 589, 1958.

[18] K. Kim, L. Kim, S. Lee, and S. Noh, "Measurement of grain moisture content using microwave attenuation at 10.5 GHz and moisture density," *IEEE Trans. Instrum. Meas.*, vol. 51, no. 1, pp. 72–77, Feb. 2002.

[19] H. Wang, S. Kosai, C. Sideris, and A. Hajimiri, "An ultrasensitive CMOS magnetic biosensor array with correlated double counting noise suppression," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2010, pp. 616–619.

[20] R. Dror, R. Dirks, J. Grossman, H. Xu, and D. Shaw, "Biomolecular simulation: A computational microscope for molecular biology," *Annu. Rev. Biophys.*, vol. 41, pp. 479–452, 2012.

[21] S. E. Meninger, "Low phase noise, high bandwidth frequency synthesis techniques," Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., MIT, Cambridge, MA, USA, 2005.

[22] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York, NY, USA: McGraw-Hill, 2002.

[23] E. Hegazi and A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM–FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1033–1039, Jun. 2003.

[24] J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1723–1732, Nov. 1996.

[25] C. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35 μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, Jul. 2000.

[26] I. Young, J. Greason, and K. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, no. 11, pp. 1599–1607, Nov. 1992.

[27] M. Johnson and E. Hudson, "A variable delay line PLL for CPU-coprocessor synchronization," *IEEE J. Solid-State Circuits*, vol. 23, no. 5, pp. 1218–1223, Oct. 1988.

[28] B. Leibowitz, J. Kim, J. Ren, and C. Madden, "Characterization of random decision errors in clocked comparators," in *Proc. IEEE Custom Integr. Circuits Conf*, Sep. 2008, pp. 691–694.

[29] R. Rieger, J. Taylor, A. Demosthenous, N. Donaldson, and P. Langlois, "Design of a low-noise preamplifier for nerve cuff electrode recording," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1373–1379, Aug. 2003.

[30] A. Sihvola, "Mixing rules with complex dielectric coefficients," *J. Subsurface Sens. Technol. Appl.*, vol. 1, no. 4, pp. 393–415, 2000.

[31] A. Shivola, "Self-consistency aspects of dielectric mixing theories," *IEEE Trans. Geosci. Remote Sens.*, vol. 27, no. 4, pp. 403–415, Jul. 1989.

[32] E. Fratticcioli, M. Dionigi, and R. Sorrentino, "A simple and low-cost measurement system for the complex permittivity characterization of materials," *IEEE Trans. Instrum. Meas.*, vol. 53, no. 4, pp. 1071–1077, Aug. 2004.

[33] K. Saeed, A. Guyette, I. Hunter, and R. Pollard, "Microstrip resonator technique for measuring dielectric permittivity of liquid solvents and for solution sensing," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 1185–1188.

[34] K. Saeed, R. Pollard, and I. Hunter, "Substrate integrated waveguide cavity resonators for complex permittivity characterization of materials," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 10, pp. 2340–2347, Oct. 2008.

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