A 6-b 1.6-GS/s ADC With Redundant Cycle One-Tap Embedded DFE in 90-nm CMOS

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***Abstract*—ADC-BASED serial link receivers are emerging in order to scale data rates over high attenuation channels. Embedding partial equalization inside the front-end ADC can potentially result in lowering the complexity of back-end DSP and/or decreasing the ADC resolution requirement, which results in a more energy-efficient receiver. This paper presents a 6-b 1.6-GS/s ADC with a novel embedded DFE structure. A redundant cycle technique is proposed for a time-interleaved SAR ADC, which relaxes the DFE feedback critical path delay with low power/area overhead. The 6-b prototype ADC with embedded one-tap DFE is fabricated in an LP 90-nm CMOS process and achieves 4.75-bits peak ENOB and 0.46 pJ/conv.-step FOM at a 1.6-GS/s sampling rate. Enabling the embedded DFE while operating at 1.6 Gb/s over a 46-in FR4 channel with 14-dB loss at Nyquist bandwidth opens a previously closed eye and allows for a 0.2 UI timing margin at a BER $= 10^{-9}$. Total ADC power including front-end T/Hs and reference buffers is 20.1 mW, and the core time-interleaved ADC occupies 0.24 mm^2 area.**

***Index Terms*—Analog-to-digital converter (ADC), ADC-based receiver, decision feedback equalizer (DFE), embedded equalization, successive approximation register (SAR), time interleaving.**

I. Introduction

ADC-BASED serial link receivers are being proposed in order to enable operation at high data rates over high-loss channels [1]–[3]. In Fig. 1, a block diagram of an ADC-based high-speed link receiver is shown which employs an ADC as the receiver front-end followed by a digital signal processing (DSP) block. The use of an ADC-based receiver enables signal equalization to be performed in the digital domain, gaining advantages of area and power scaling with improved CMOS technology. This allows for the efficient implementation of complex equalization and the ability to support bandwidth-efficient modulation schemes, such as PAM4 and duobinary [4].

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Despite these advantages, ADC-based receivers are generally more complex and consume higher power than binary receivers. ADC resolutions in the range of 4–6 b are typically used, with flash or successive approximation register (SAR) architectures as the dominant choices. For many systems where link power efficiency is the key metric, multi-GS/s ADC implementations [3], [5], [6] often display prohibitive power.

The digital equalization that follows the ADC can also consume significant power as well, comparable to the power of the ADC. Embedding partial analog equalization in the front-end ADC allows for both a lower ADC resolution and reduced digital equalization complexity at a target bit error rate (BER) [7], which could translate into an overall lower power ADC-based receiver implementation. Previously, finite-impulse response (FIR) and infinite-impulse response (IIR) filtering has been embedded in the capacitive DAC of a SAR ADC, at the cost of increased DAC complexity and reduced ADC conversion rate [8]. Embedded multilevel decision-feedback equalization (DFE), which can be treated as embedded quantized IIR equalization, has also been previously proposed for pipeline ADCs [9].

DFE is a very powerful equalization technique, as it can selectively reduce post-cursor ISI without amplifying noise or cross-talk. However, one important issue in any DFE implementation involves the critical feedback timing path from the decision comparator to the summation circuit that subtracts the post-cursor ISI. Loop unrolling can be employed to resolve this issue, where speculative comparison with a redundant comparator is used [10]. This approach, however, can incur significant hardware overhead [9].

This paper presents a time-interleaved (TI) SAR ADC architecture with a novel low-overhead one-tap embedded DFE [11]. In Section II, statistical BER simulation results are discussed, showing performance advantages with embedded DFE, and comparing it against embedded IIR equalization, for three FR4 channels with differing loss profiles. The novel embedded DFE technique, which introduces an additional cycle in the time-interleaved SAR ADC in order to perform the DFE loop-unrolling with minimal hardware overhead, is proposed in Section III. Section IV details the ADC architecture and the main circuit blocks. Experimental results of the ADC with embedded one-tap DFE, fabricated in an LP 90-nm CMOS technology, are shown in Section V. Finally, Section VI concludes the paper.

II. Embedded Feedback Equalization Modeling

Here, the performance impact of embedding two types of feedback equalization, DFE and IIR, inside the ADC is

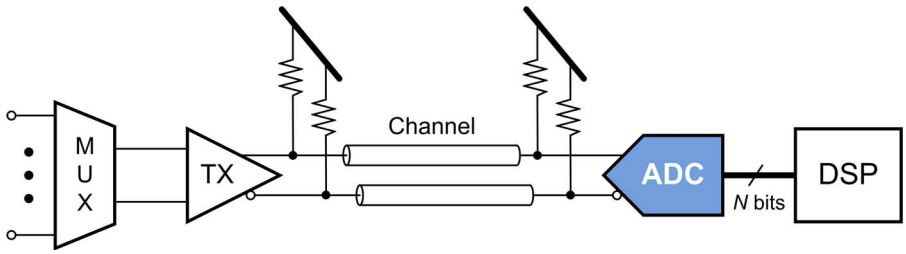


Fig. 1. High-speed link with an ADC-based receiver.

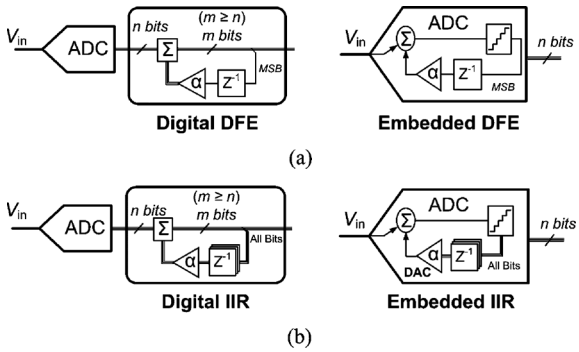


Fig. 2. Block diagrams of (a) digital versus embedded DFE and (b) digital versus embedded IIR.

analyzed. Utilizing a statistical simulation model, the embedded equalization approaches are compared for different operating conditions such as channel profile, transmitter equalization, and ADC resolution.

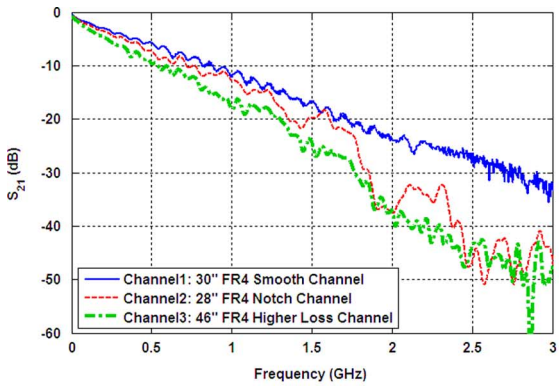
Fig. 2(a) shows a block diagram comparing post-ADC digital DFE and an ADC with an embedded DFE tap. In both cases, the output MSB, which is considered the decision in a conventional one-tap DFE with binary signaling is fed back, weighted by the DFE coefficient, and subtracted. The advantage of ADC embedded equalization is that, unlike digital equalization, where the resolution is limited by the ADC, embedded equalization applies the equalization taps to the unquantized analog input, allowing for both a lower ADC resolution and reduced digital equalization complexity at a target BER [7].

Similarly, Fig. 2(b) compares between digital and embedded IIR equalization realizations. In either case, the full ADC output word is scaled by the equalization coefficient and subtracted from the input, where the subtraction is performed with the analog input for the case of embedded equalization and with the quantized input in the case of digital IIR. The embedded IIR offers a potential advantage over embedded DFE, in that the IIR can be optimized to cancel multiple ISI terms, rather than a single post-cursor for the DFE case. However, while an analog value can still be used for the full-scale α value, the embedded IIR suffers from the ADC quantization in the feedback, which implies a minimum ADC resolution is necessary to avoid the quantization noise propagating in the feedback system.

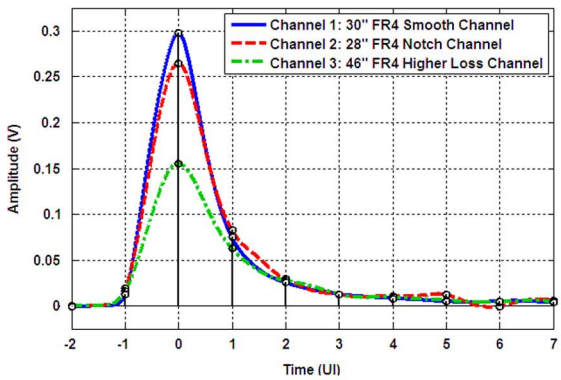
High-speed link simulation tools often use statistical modeling approaches to predict performance metrics such as BER without the need for lengthy bit-by-bit transient simulations [12], [13]. This work uses such a statistical framework for ADC-based receivers [7] in order to model the effect of embedded equalization on system performance, with 1.6-Gb/s operation assumed over the three FR4 channels shown in Fig. 3(a). While the first two channels display a similar $\sim$11-dB channel loss at the 0.8-GHz Nyquist frequency, the first channel has a smooth attenuation profile, in contrast to the second channel, which has a frequency notch near 2 GHz. In the time-domain 1.6-Gb/s pulse response, shown in Fig. 3(b), this translates to a reduced main cursor to first post-cursor ratio for the second channel and some noticeable reflections near the fifth and sixth post-cursors. The third channel has a higher attenuation of about 14 dB at Nyquist frequency. This again is reflected in the time-domain pulse response, where the main cursor for the third channel is almost half that for the other two channels. The presented results assume 1-$V_{\rm ppd}$ transmit swing, 2.5-$mV_{\rm rms}$ receiver input-referred thermal noise, and 10-mV uniform supply noise, and receiver sampling jitter with a 0.02 unit interval (UI) deterministic component (DJ) in the form of duty cycle distortion and a 0.02 $\rm UI_{rms}$ random component (RJ).

The impact of including one tap of embedded DFE for each of the channels is shown in Fig. 3(c), quantified in terms of receiver voltage margin at 1.6 Gb/s and a BER $< 10^{-12}$ for a given number of TX-FIR equalization taps. Without any TX equalization (one tap), the embedded DFE offers significant performance improvements in all three channels, with the voltage margin in channels 1 and 2 improving by 100 and 115 mV, respectively, and the higher loss channel 3 displaying a 50-mV margin from a previously closed eye. While the loss of channels 1 and 2 are similar, a higher percentage improvement with embedded DFE for the notch-shaped channel 2 is observed due to the cancellation of the first-post cursor that is a higher percentage of the main cursor value. The embedded DFE allows the optimization of the TX FIR taps to ignore the first post-cursor ISI term, which translates into more flexibility in FIR tap weighting to match a specific channel profile with additional taps. In order to have a fair comparison, the values of the TX-FIR taps are optimized separately with and without embedded DFE. Continued margin improvement is observed when TX equalization is introduced, with the embedded DFE offering a relatively constant additional 45 to 50 mV for channels 1 and 2 from two to four TX FIR taps, while for channel 3 this margin increases from 20 to 30 mV. Note that, for these channels the voltage margin roughly plateaus when TX equalization is introduced due to the majority of the residual ISI being cancelled and the 1-$V_{\rm pp}$ TX peak swing constraint.

These three channels are also utilized to compare the performance of embedded IIR with embedded DFE. Fig. 3(d) shows the achievable 1.6-Gb/s voltage margin as the ADC resolution is varied, assuming no transmit equalization. While the performance of the embedded DFE is independent of the ADC resolution, the embedded IIR equalization requires at least 4–5 b of resolution to approach the performance of the embedded DFE equalization for all three channels. As the hardware overhead of



(a)



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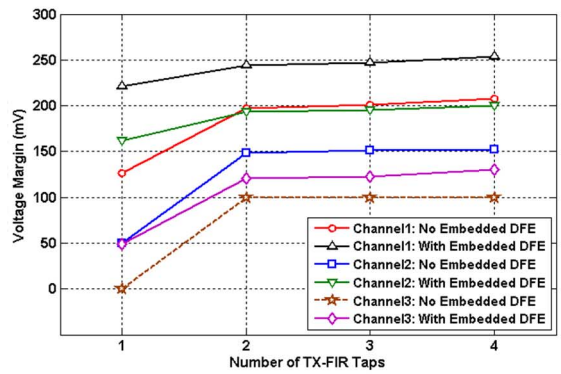
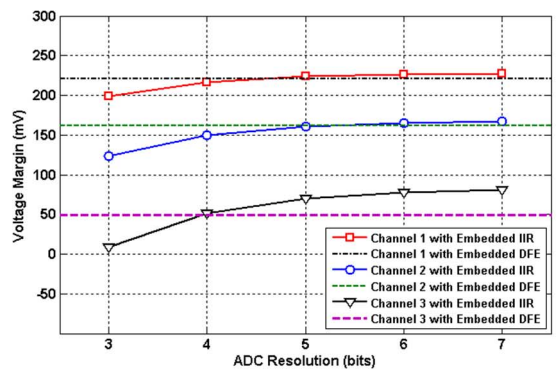


(c)



(d)

Fig. 3. (a) Magnitude and (b) 1.6-Gb/s pulse responses of three FR4 channels. (c) Impact of including one tap of embedded DFE equalization for different levels of TX-FIR equalization. (d) Impact of ADC resolution with embedded DFE and embedded IIR equalization with no TX FIR equalization over three FR4 channels.

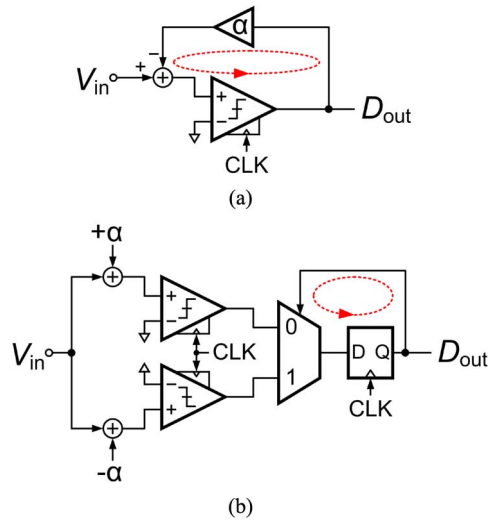


Fig. 4. DFE implementations. (a) Direct-feedback. (b) Loop-unrolled.

embedded IIR increases with ADC resolution, due to all of the output bits being used for ISI cancellation, these results suggest that, for the typical high-speed link ADC resolutions, embedded DFE offers potential performance and efficiency advantages.

III. Redundant-Cycle One-Tap Embedded DFE

While DFE is a very powerful equalization technique, as it can selectively reduce post-cursor ISI without amplifying noise or crosstalk, the feedback structure introduces some challenges in the implementation of this technique in high data rate systems. Here, we review a common loop-unrolling approach to improve the DFE speed and propose a novel redundant-cycle technique to efficiently embed a DFE tap in a multibit SAR ADC.

A. Loop-Unrolled One-Tap Embedded DFE

A receiver block diagram with a direct-feedback one-tap DFE is shown in Fig. 4(a). One of the main challenges in a DFE structure involves meeting the 1-UI critical feedback delay path

$$t_{\mathrm{clk}\rightarrow\mathrm{QSA}} + t_{\mathrm{sum}} < T_b = 1\ \mathrm{UI} \tag{1}$$

where $t_{\mathrm{clk}\rightarrow\mathrm{QSA}}$ is the clock-to-Q delay of the sense-amplifier comparator, t_{sum} is the summer delay which also includes the delay of DFE coefficient α generation [14], and T_b is the bit period equal to $1/f_{\mathrm{CLK}}$ in a full-rate architecture. The combination of the time required for the summer to settle to a required accuracy level and the comparator delay, which can have a long regeneration time with small input levels, makes this critical timing path often difficult to meet at high data rates.

In order to relax the critical delay path of the DFE feedback, loop unrolling or speculation with a redundant comparator may be used to calculate both positive and negative post-cursor cancellation coefficient possibilities simultaneously [10]. As shown in Fig. 4(b), a decision is made for both possible options of the DFE tap, $+\alpha$ and $-\alpha$, and the correct decision is chosen using

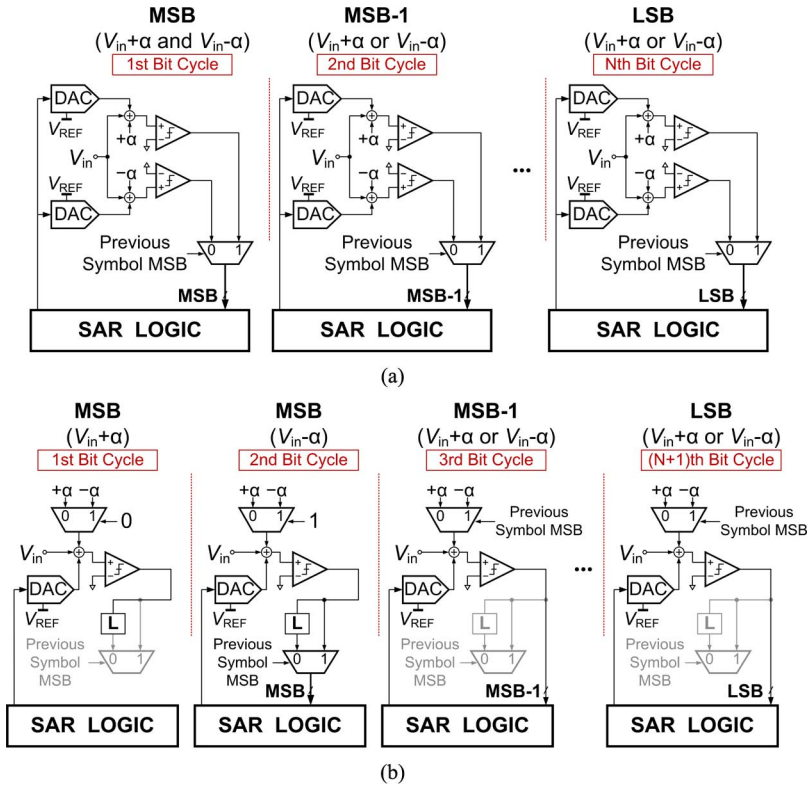


Fig. 5. Conceptual schematic of a unit SAR ADC with (a) loop-unrolled and (b) proposed redundant cycle one-tap embedded DFE.

a 2:1 multiplexer (MUX) controlled by the previous detected symbol decision. Now, the critical feedback delay path is

$$t_{\mathrm{clk}\rightarrow Q} + t_{\mathrm{mux}} < T_b = 1\ \mathrm{UI} \tag{2}$$

where $t_{\mathrm{clk}\rightarrow Q}$ is the flip-flop clock-to-Q delay and t_{mux} is the MUX delay. This is generally easier to meet, as all of the signals are operating at full logic levels. However, the primary disadvantage of this technique is that the number of comparators and summers is doubled.

Fig. 5(a) shows a sequential block diagram of this approach with a time-interleaved SAR ADC. After an initial track-and-hold (T/H) cycle, the MSB computation cycle computes both the positive and negative ISI combinations, $\mathrm{V_{in}} + \alpha$ and $\mathrm{V_{in}} - \alpha$, in parallel with the two comparators. The MSB of the previous symbol is then used to select the appropriate comparator output. This approach results in a significant circuit area penalty, as the number of comparators and digital-to-analog converters (DACs) present in the SAR ADC is doubled. Two significant power overheads are also incurred with this approach. The first is associated with clocking the extra comparator and DAC. However, this overhead can be minimized by disabling the incorrect DFE tap polarity comparator and DAC after the MSB computation. The second involves the increased capacitive loading from the additional capacitive DACs, assuming a conventional SAR architecture, that the ADC T/H circuit must drive and the reference voltage buffers must charge, resulting in increased T/H and reference buffer power. Moreover, doubling the comparators and DACs results in mismatch between the two paths which may necessitate additional calibration.

B. Redundant-Cycle One-Tap Embedded DFE

A new technique to more efficiently embed the DFE tap in a time-interleaved SAR ADC is shown in Fig. 5(b). Here, instead of a redundant comparator and DAC, a redundant ADC conversion cycle is added to the normal SAR operation. During the first cycle after the T/H cycle, the MSB value is computed with a $+\alpha$ value and latched, followed by the MSB computation with a $-\alpha$ value in the next cycle. This allows the use of only one comparator and DAC, as in a conventional SAR ADC. Both of the MSB computations are stored, and the previous symbol MSB is used to select the correct computation. For a 6-b ADC, including the sampling cycle and the redundant cycle, eight equal cycles are used for each sample conversion. The decrease in the ADC sampling rate due to the additional cycle can be compensated by increasing the ADC time-interleaving factor. In this work, the proposed redundant cycle method results in an $(8/7)\times$ increase in the time-interleaving factor and the conversion latency, and almost the same increase in the core ADC area of the 6-b prototype ADC. However, the increase in the total power is even smaller, since only the power of the time-interleaved SAR ADCs has increased, while the power consumption of the front-end T/Hs and the reference voltage buffers remains approximately the same.

Although this implementation requires eight equal cycles similar to a typical 7-b SAR ADC, the power and area overhead is less. A 7-b SAR ADC requires 1-b higher resolution front-end T/Hs, capacitive DACs, and lower offset, gain and

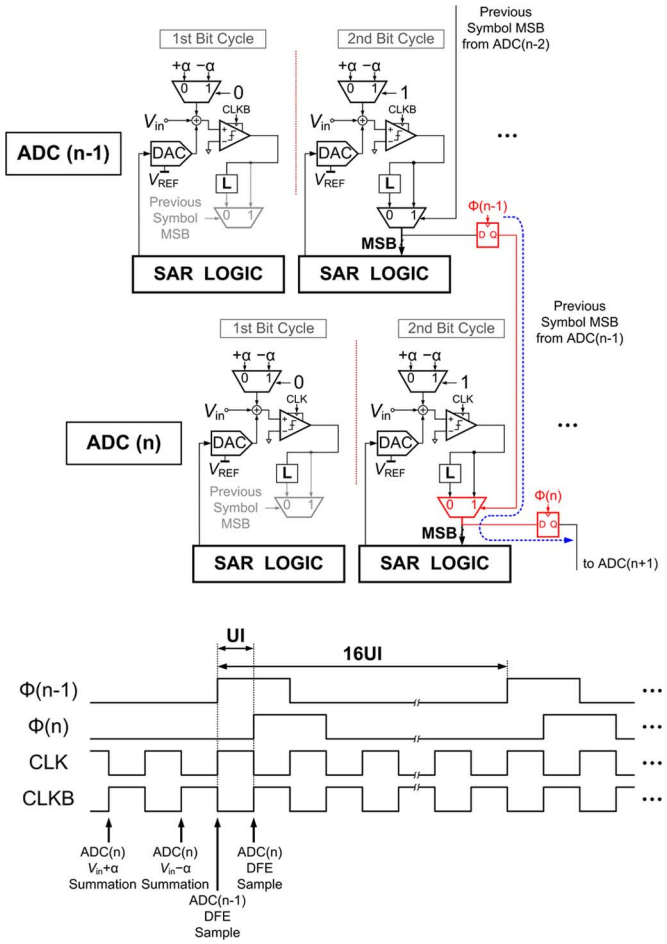


Fig. 6. Critical delay path for the redundant cycle one-tap embedded DFE. The instants when the summation and sampling in the one-tap embedded DFE occur are shown.

phase mismatches among the time-interleaved channels which increases its overhead more than $(8/7)\times$ compared with a 6-b ADC without embedded equalization. It should also be noted that the overhead due to the redundant cycle one-tap DFE decreases with increases in the ADC resolution, as one extra cycle is always required for this method independent of the resolution.

It is worth mentioning that the redundant cycle technique can be expanded to allow for a multitap DFE by adding additional cycles for extra taps. For example, a redundant cycle two-tap embedded DFE requires three extra cycles relative to a normal SAR ADC in order to relax the critical path delay for both DFE taps. This implies a $(10/7)\times$ increase in the time-interleaving factor, latency, and area. However, this overhead is much less than a SAR ADC with fully loop-unrolled two-tap embedded DFE realization, where the number of comparators and DACs should be quadrupled.

C. Critical Delay Path

While the redundant cycle one-tap embedded DFE adds some latency to the data conversion process, the critical delay path is similar to a loop-unrolled one-tap DFE. Fig. 6 details the critical delay path for two consecutive ADC channels, $\mathrm{ADC}(n-1)$ and $\mathrm{ADC}(n)$. Here, the critical timing path is governed by $\Phi(n)$ clocks operating at the sample frequency f_s divided by the time-interleaving factor $f_s/16$ for the prototype discussed in Section IV, which are spaced by one unit interval. At the end of the second bit cycle, the MSB from $\mathrm{ADC}(n-1)$ is resolved and sampled by a flip-flop clocked by $\Phi(\mathrm{n}-1)$ to produce the select MUX signal for the correct MSB of $\mathrm{ADC}(n)$. This ADC(n) MUX output must resolve before being sampled by a flip-flop clocked by $\Phi(n)$ to produce the select MUX signal for the $\mathrm{ADC}(n+1)$. Thus, the critical delay is

$$t_{\mathrm{clk}\to Q} + t_{\mathrm{mux}} < t_{\Phi(n)} - t_{\Phi(n-1)} = T_b = 1\ \mathrm{UI} \qquad (3)$$

which is the same as the conventional loop-unrolled approach.

A second critical timing path exists for the $\pm\alpha$ MUX, summer, and comparator in the DFE operation, which should finish before the sampling instant. As shown in Fig. 6, this delay should be less than the duration of one bit cycle, which is equal to 2 UI. However, this criteria is generally always satisfied because the normal SAR ADC operation requires that the delay of the SAR logic and capacitive DAC settling, whose delay path is similar to the DFE MUX plus summer, and comparator be less than the duration of one bit cycle.

D. Switched-Capacitor Implementation

A switched-capacitor topology has previously been shown as an efficient DFE approach for binary receivers [15]. This work modifies this structure to allow for embedding a one-tap DFE in a conventional SAR ADC. A switched-capacitor network, shown in Fig. 7(a), provides an efficient implementation of the MUX for choosing between $+\alpha$ and $-\alpha$ and the summer connected to V_{in} for performing the redundant cycle one-tap embedded DFE. Here, a simplified single-ended schematic is utilized to illustrate operation during the first three phases of the SAR conversion cycle, the first sampling phase and the two redundant-cycle MSB computations. During the first cycle, the input voltage is sampled on the C_{S} capacitor, and the differential voltage at the input of comparator, V_{X}, is zero, as shown in Fig. 7(b). In the next cycle, the Φ_{S} switches are OFF and the left side of C_{S} is connected to $-\alpha$, as shown in Fig. 7(c). Hence, the differential voltage at the input of the comparator is $V_{\mathrm{in}}+\alpha$, and the MSB is resolved for this tap polarity. In the next phase shown in Fig. 7(d) the MSB is reevaluated for the opposite tap polarity, as the left terminal of C_{S} is now connected to $+\alpha$, resulting in a differential voltage at the comparator input of $V_{\mathrm{in}}-\alpha$. The correct MSB decision is then made based on the MSB of the previous ADC channel. For the remaining ADC bit cycles, the correct DFE coefficient is known *a priori*, and the required switch for selecting $+\alpha$ or $-\alpha$ is fixed till the end of this SAR conversion period.

IV. ADC Design

A. Time-Interleaved Architecture

The redundant cycle embedded DFE is implemented in a 1.6-GS/s 6-b ADC, shown in Fig. 8, consisting of two time-interleaved sub-ADCs which operate at 0.8 GS/s. Each sub-ADC is formed by eight parallel unit ADCs which have eight operation cycles: one for input sampling, six for bit conversion, and

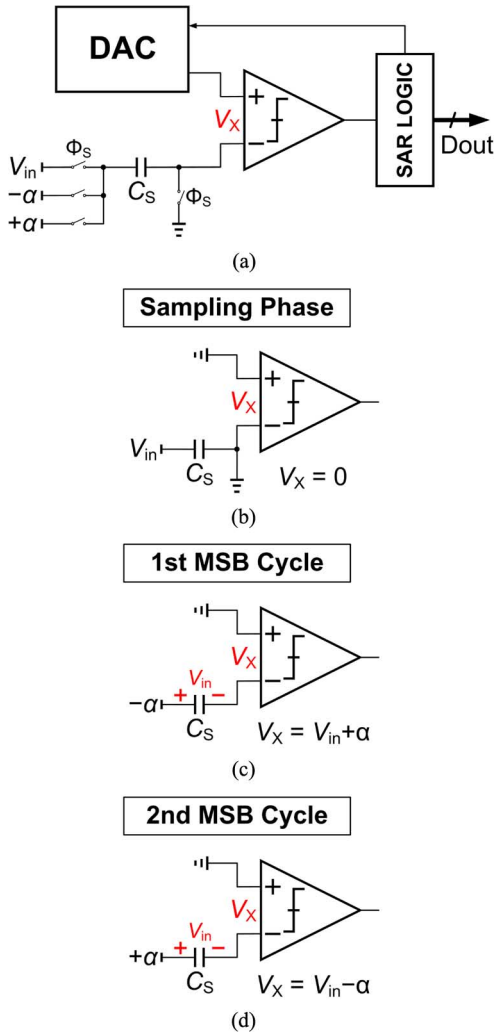


Fig. 7. SAR ADC with embedded one-tap DFE. (a) Simplified block diagram, operation during the (b) sampling phase, (c) first MSB evaluation, and (d) second MSB evaluation.

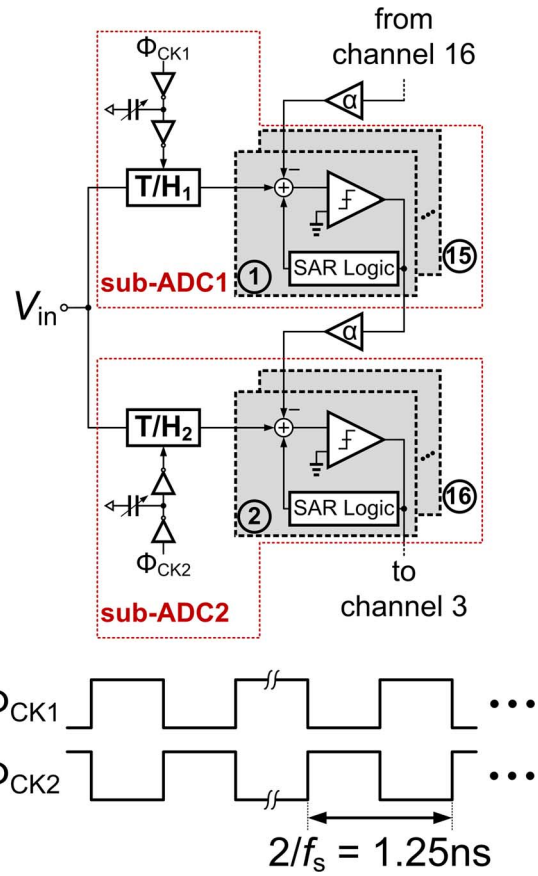


Fig. 8. Block diagram of the 16-way time-interleaved SAR ADC with embedded one-tap DFE.

one extra cycle for the equalization. While the total time-interleaving factor is 16, two front-end track-and-holds are used for each sub-ADC, allowing for the use of only two critical sampling phases at 0.8 GHz. The ADC includes calibration DACs for comparator offset and sampling clock skew cancellation.

B. Unit ADC With Embedded One-Tap DFE

Fig. 9 shows the fully differential schematic of the 6-b unit SAR ADC with embedded redundant cycle one-tap DFE. A four-input comparator with two differential input pairs allows separation of the input sampling and ISI cancellation path from the successive approximated value at the output of the reference DAC. One input pair is connected to the DAC output, while the other pair forms the input sampling network which also implements the embedded DFE tap. This allows the main DAC to remain similar to a conventional ADC without embedded DFE.

The DAC employs a merged capacitor switching (MCS) scheme [16] which allows for very low switching energy compared with the conventional capacitor DAC switching proposed in [17] and saves 50% of the DAC area through removing the MSB capacitor. In this fully differential structure, the MSB calculation is performed by comparing the sign of the input while all DAC capacitors are connected to common-mode voltage. Hence, there is no need for MSB capacitors, and a 5-b capacitive DAC can be used for the 6-b SAR ADC. A 4-fF unit capacitor, which is the default minimum metal–oxide–metal (MOM) capacitor in the 90-nm CMOS technology, is employed. In selecting this unit capacitor, both matching and noise performance is considered. Based on Monte Carlo simulations, this value provides <0.05 LSB maximum DNL error at a 6-b resolution. Also, assuming a 1-V_{pp} maximum swing, it is much larger than the 34-aF capacitor size required for an additive noise power less than 0.5 LSB.

Fig. 10 shows the four-input two-stage dynamic comparator [18] with current-based offset calibration. This comparator has a shorter regeneration time constant compared with a conventional StrongArm dynamic comparator, which results in superior metastability performance. The comparator size is scaled to satisfy a target metastability error better than 10^{-12}. Two 5-b current-steering DACs are used to calibrate comparator offsets at 3-mV resolution by sinking a current from the comparator internal nodes. This calibration scheme adds small loading to the comparator nodes which is relatively code-independent and results in negligible speed impact.

The differential DFE tap coefficients $V_{\rm cmi}+\alpha/2$ and $V_{\rm cmi}-\alpha/2$ in Fig. 9 are generated using off-chip tunable voltage regulators, and buffered on-chip before driving the unit ADCs. During the normal ADC operation, where α is set to zero, any

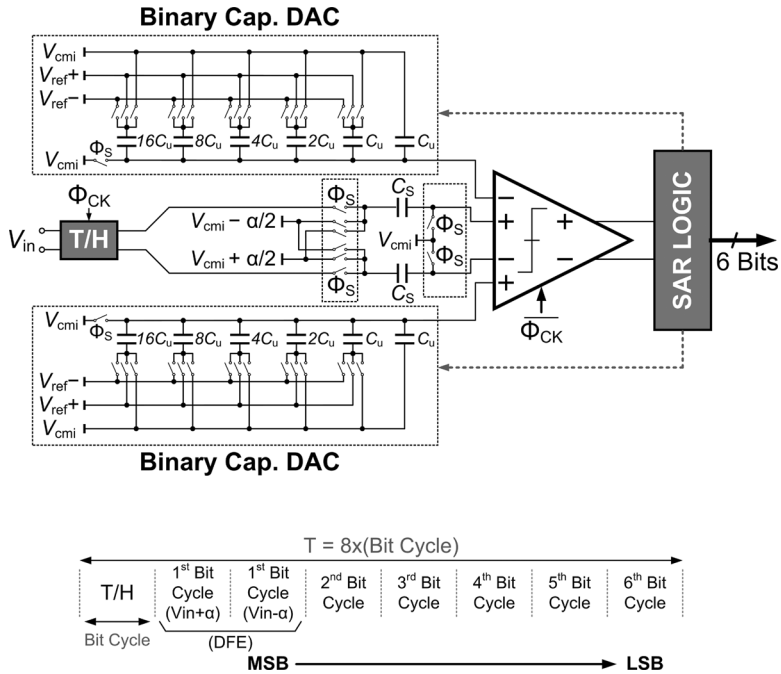


Fig. 9. Unit SAR ADC schematic with redundant cycle embedded one-tap DFE.

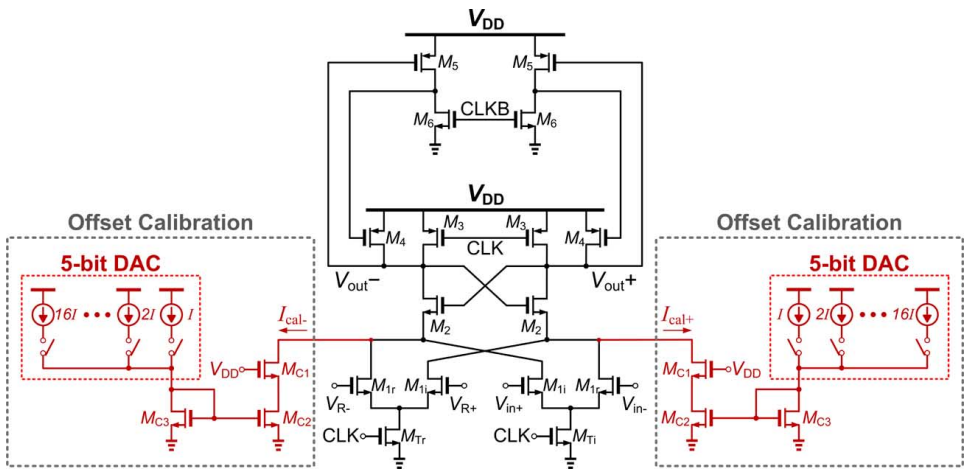


Fig. 10. Schematic of the four-input comparator with offset calibration current DACs.

offset mismatch equal to β volts between the two DFE tap coefficient buffers outputs results in $+\beta$ volts and $-\beta$ volts offset error during the current A/D conversion, for a positive and negative previous input sample, respectively. This error translates to a nonlinear harmonic distortion in the ADC performance. However, this mismatch can be simply calibrated out during measurement. After the offset calibration of all unit ADCs is performed, a positive dc input voltage $+V_1$, larger than $|\beta|$, is applied to the ADC. Since, the input is always positive, the ADC output code D_{OUT1} will be the 6-b representation of $V_1+\beta$. Then, the same procedure is repeated for a $+2V_1$ dc input voltage. In this case, the ADC output code D_{OUT2} is the 6-b representation of $+2V_1+\beta$. If β is zero, $2D_{\mathrm{OUT1}}-D_{\mathrm{OUT2}}=0$, assuming the ADC digital output is shown in a signed format. In practice, $2D_{\mathrm{OUT1}}-D_{\mathrm{OUT2}}$ is nonzero and equal to the 6-b representation of β. In this implementation one of the off-chip regulators is tuned to make the term $2D_{\mathrm{OUT1}}-D_{\mathrm{OUT2}}$ equal to zero. This procedure can be repeated for multiple voltage pairs to make sure the offset mismatch between the DFE tap coefficients is cancelled out completely.

C. Front-End T/H

A switched capacitor sampling network using a bootstrapped switch followed by an active buffer is used as the front-end T/H in each sub-ADC, as shown in Fig. 11 [19]. Bootstrapping improves the bandwidth and high-swing linearity of the sampling network, especially for the low-power CMOS technology with high MOSFET threshold voltages used in this work, and makes the charge-injection error input independent. A simple pseudo-differential PMOS source-follower is employed as the buffer to isolate the input sampling network from the unit ADCs. These buffers have a low frequency gain of -2.3 dB and an 8-GHz bandwidth. Similar PMOS source follower stages with equal attenuation are also used for on-chip buffering of the reference

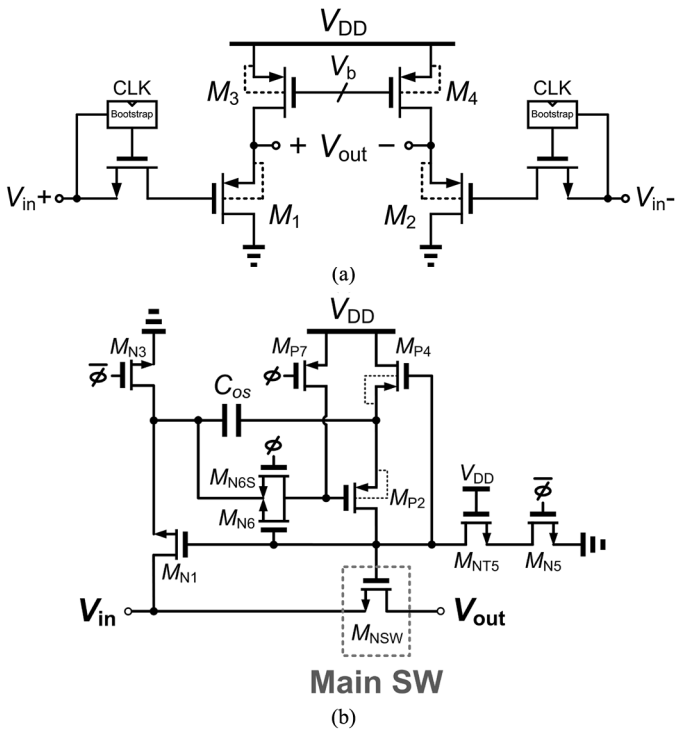


Fig. 11. Front-end T/H. (a) Schematic. (b) Bootstrapped switch structure.

and common-mode voltages which are generated off-chip. Simulation results show that with a 300-mV input common-mode voltage and a 1-V_{pp} input swing, a linearity better than 6 b is achieved up to a 4-GHz input bandwidth with a 0.8-GHz sub-ADC sample clock. This front-end T/H architecture allows a very large input sampling bandwidth, as the sampling capacitor is the ~30-fF parasitic capacitance at the source-follower input, which is significantly smaller than the 120-fF C_S in the unit ADC and the added loading due to the routing to all of the time-interleaved unit ADCs in each sub-ADC. Here, the 370-μV_{rms} kT/C noise from the 30-fF input sampling network is not a limiting factor for the 6-b ADC with 1-V_{pp} input range.

D. On-Die Offset and Clock-Skew Calibration

In this work, on-die offset and sampling clock skew calibration schemes are implemented to alleviate the mismatches among the parallel unit ADCs and improve overall performance.

1) Foreground Offset Calibration: As the proposed ADC employs 16 parallel-unit SAR ADCs any offset mismatch among them can limit the performance of the overall time-interleaved architecture. The offset voltage in each unit ADC has two main sources: the front-end T/H and the unit SAR ADC's comparator. Monte Carlo simulations show that the total output-referred offset of the front-end T/H is $\sigma = 8.2$ mV and the four input comparator input-referred offset is $\sigma = 11.2$ mV, yielding a total offset at the comparator input in each unit ADC of $\sigma \approx 13.9$ mV. Using the differential offset calibration current-steering DAC shown in Fig. 10, a correction resolution of 3 mV and maximum range of ±90 mV is achieved which covers more than $\pm 5\sigma$ range of the total offset voltage.

Fig. 12(a) shows the setup for foreground offset calibration. The ADC differential input is set to zero by connecting both positive and negative inputs to the 300-mV input common-mode voltage. A 16-to-1 MUX is then used to choose the MSB of the unit ADC under calibration and two 5-b calibration codes set the correct current in the comparator calibration DAC (Fig. 10). The optimum calibration code is determined when the MSB of the unit ADC under test toggles between 0 and 1 with near 50% probability. This procedure is then repeated for all unit ADCs.

2) Foreground Clock Skew Calibration: The phase mismatch calibration of the proposed 16-way time-interleaved ADC is relaxed by utilizing the two front-end T/Hs sampling at $f_s/2$. Since the T/H outputs are ideally held constant during the hold phase, any small phase mismatch in the unit ADC sampling clock following the T/H will not result in any overall ADC performance degradation. Thus, it is only necessary to calibrate these two critical T/H sampling phases.

Monte Carlo simulations show that the clock buffer and distribution network adds a phase mismatch with σ ~3.5 ps between the two front-end T/H complementary sampling phases. The digitally controlled delay lines in the clock distribution path allow any phase mismatch to be calibrated to less than 1 ps with ±11.5-ps tuning range, which covers about $\pm 3\sigma$ variation.

A foreground calibration procedure is used for cancelling the phase mismatch, as shown in Fig. 12(b). The ADC output FFT is measured with a sinewave input with frequency f_{in} and the main spur in the frequency response due to the phase mismatch between the two T/H sampling phases which occurs at $f_s/2 - f_{in}$, is observed. By tuning the digitally controlled MOS capacitor arrays in the clock distribution network, the optimum calibration code results in minimizing this spur amplitude and the best ADC output THD.

V. Measurement Results

Fig. 13 shows the chip micrograph of the prototype 6-b ADC, which was fabricated in an LP 90-nm CMOS process and occupies a total active area of 0.24 mm^2. The core time-interleaved ADC consists of two sub-ADCs, where each sub-ADC is constructed from eight parallel unit SAR ADCs. In order to optimize the critical MSB delay path for DFE operation, the unit ADCs are placed in a way that balances the distance between every two consecutive ADCs. Emphasis is placed on maintaining symmetry between the two sub-ADCs by placing both the reference and common-mode voltage buffers and the start generator in the middle. Also, the two front-end T/Hs are distributed symmetrically with the sampling phases routed from the central phase generation and distribution block. The characterization of the core ADC and the embedded redundant cycle one-tap DFE is discussed next.

A. Core ADC Characterization

The DFE coefficient α is set to zero to characterize the general performance of the 6-b ADC. For ADC testing the gain and offset errors are calibrated among the 16 time-interleaved unit ADCs, while the two complementary sampling clocks at $f_s/2$ are calibrated for phase mismatch. The dynamic performance of the full time-interleaved ADC at 1.6-GHz sampling frequency is shown in Fig. 14 as a function of the input frequency, with a maximum effective number of bits (ENOB) of 4.75 b. By using

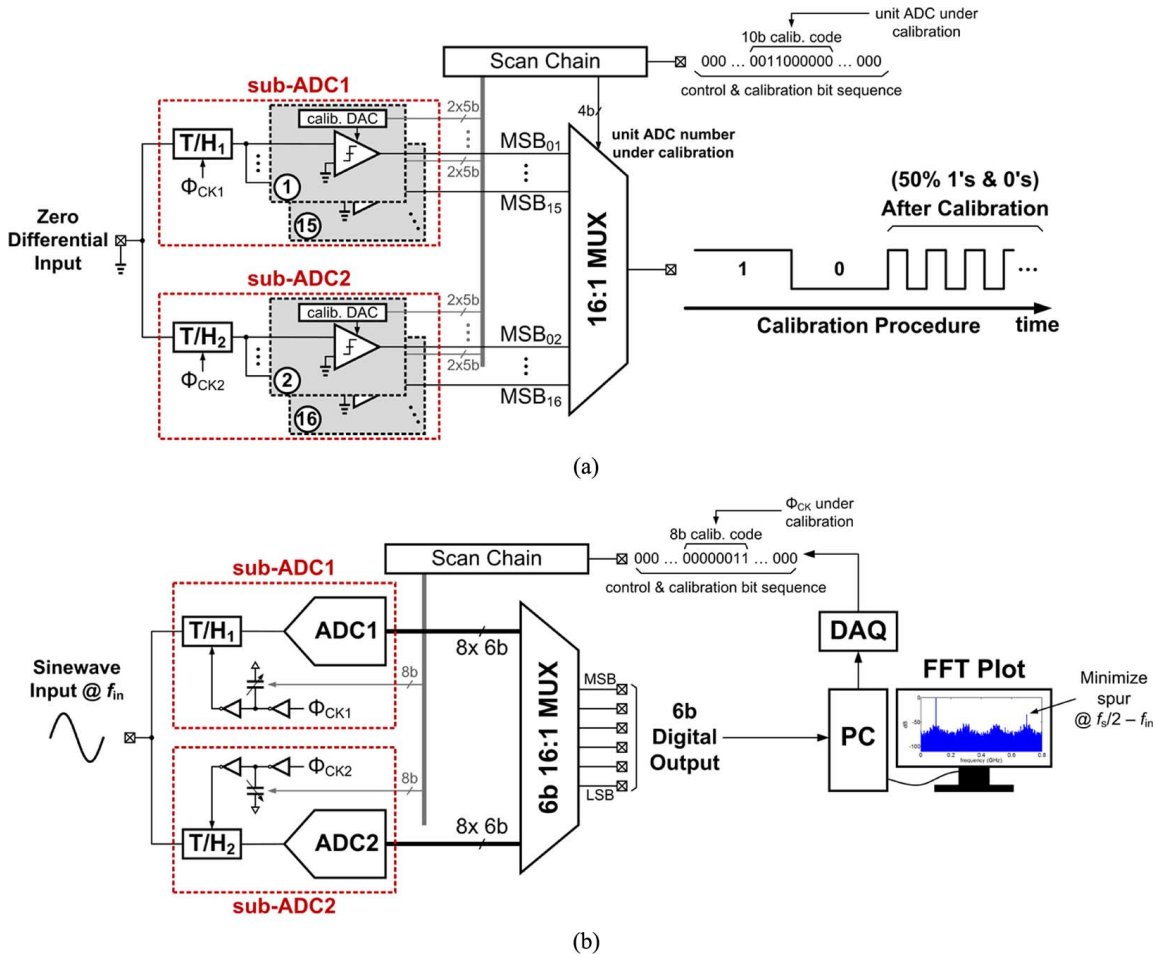
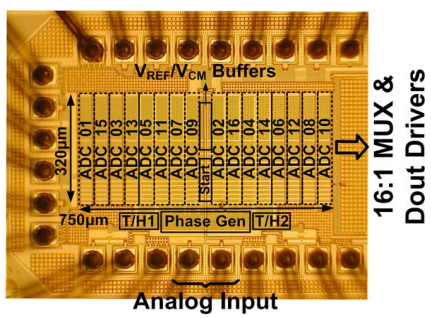


Fig. 12. Simplified diagrams of the foreground (a) offset calibration and (b) clock skew calibration setups.



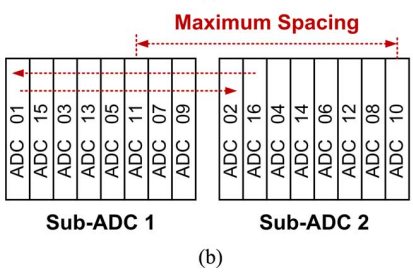


Fig. 13. Prototype ADC implemented in an LP 90-nm CMOS process. (a) Chip micrograph. (b) Optimized order of unit ADCs with respect to spacing between each two consecutive ADCs.

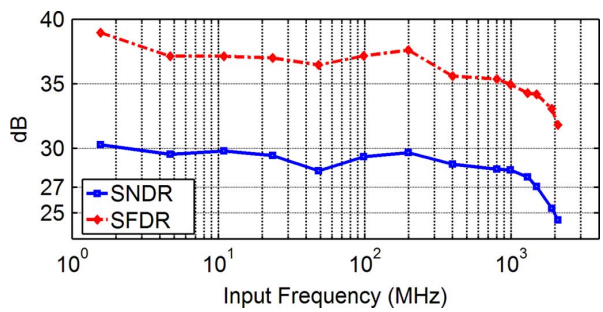


Fig. 14. ADC SNDR/SFDR versus input frequency at $f_s = 1.6$ GHz.

the front-end active T/Hs an ADC effective resolution bandwidth (ERBW) of 1.5 GHz is achieved, which is almost twice the Nyquist bandwidth of the 1.6-GS/s ADC, i.e., 800 MHz. Note that the SNDR/SFDR curves have a local minimum at around 50-MHz input frequency, as this is the Nyquist bandwidth of each unit ADC in the time-interleaved structure. At this frequency, each unit SAR ADC will experience maximum low-frequency nonlinearity. The frequency spectrum of the 1.6-GS/s ADC at 48.437-MHz input frequency after calibration is shown in Fig. 15. Here, the second and third harmonics are dominant, while the distortion due to the phase mismatch between the two T/H sampling phases, located at $f_s/2 - f_{in}$, is non-dominant. Although the entire ADC is differential, the large second-order harmonic distortion arises from the phase unbalance in the balun used for single-ended to differential transla-

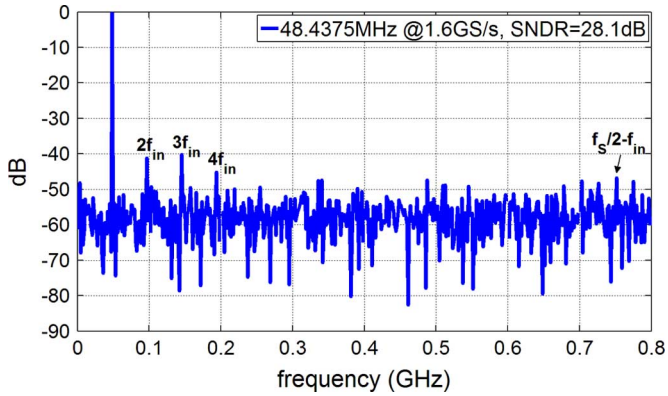


Fig. 15. The 1.6-GS/s ADC normalized output spectrum for $f_{\rm in} = 48.437$ MHz.

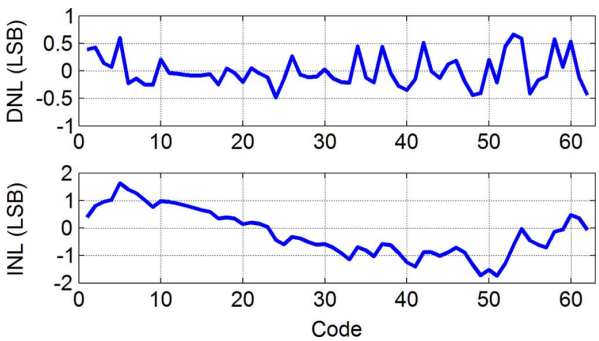


Fig. 16. DNL/INL plots with $f_{\rm in} = 2.7$ MHz at $f_{\rm s} = 1.6$ GHz.

tion of the input signal in test setup and the pseudodifferential topology of the front-end T/Hs. At high input frequencies, the sampling clock jitter limits the overall ADC performance, and the SNDR in Fig. 14 drops quickly with increasing input frequency.

Static characterization of the ADC is performed using a sinewave histogram technique [20] and a 2.7-MHz input at 1.6 GS/s. Maximum DNL and INL values for the 6-b ADC are $+0.67/-0.48$ LSB and $+1.6/-1.7$ LSB, respectively, as shown in Fig. 16.

B. Embedded DFE Functionality

In order to extract the range and resolution of the embedded DFE, Fig. 17 shows the average time-interleaved ADC output as a function of DFE tap coefficient voltage for two dc input cases of $V_{\rm in} = 0.5$ V and $V_{\rm in} = -0.5$ V, i.e., the extremes of the 1-$V_{\rm pp}$ input range. For $V_{\rm in} = 0.5$ V, the MSB should resolve to one, and the DFE coefficient should subtract from the input voltage. As shown in the right-hand side of Fig. 17, as the DFE coefficient is increased the averaged ADC output code linearly decreases. A similar process occurs for $V_{\rm in} = -0.5$ V, where the DFE coefficient should effectively add to the input voltage, and in the left-hand side of Fig. 17 the averaged ADC output code linearly increases as the absolute value of the DFE coefficient is increased. This linear transfer characteristic confirms that the embedded DFE coefficient achieves a resolution better than the 6-b ADC, and has a range as large as the ADC maximum input range.

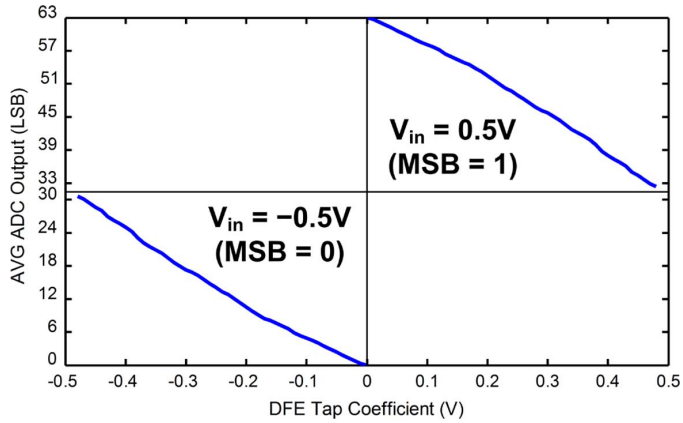


Fig. 17. Measured DFE tap coefficient range and resolution using a dc input voltage.

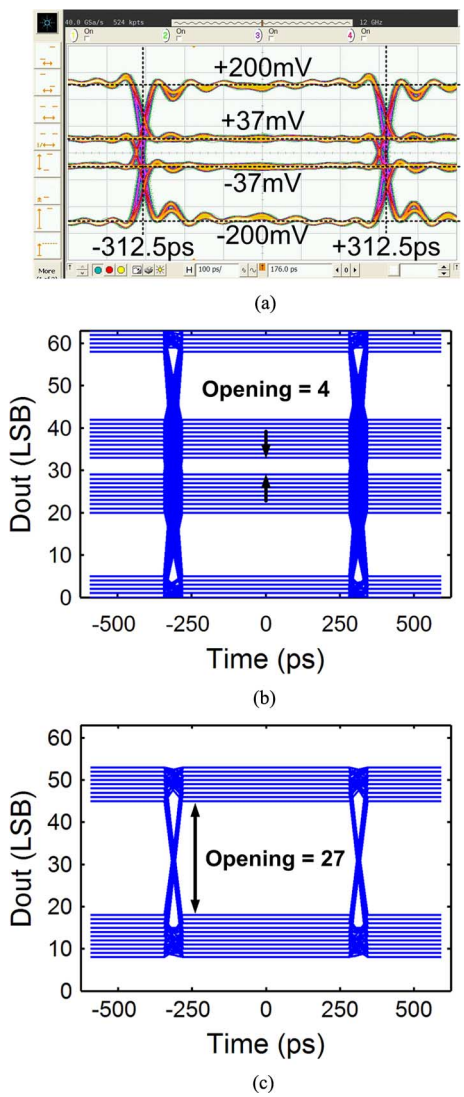


Fig. 18. 1.6-Gb/s ADC input generated by $2^{23} - 1$ PRBS after a two-tap FIR with 15-dB de-emphasis, and measured digitized 6-b ADC output (b) without and (c) with one-tap DFE enabled.

In order to verify the functionality of the embedded one-tap DFE, a 1.6-Gb/s $2^{23} - 1$ PRBS input is passed through a two-tap FIR filter $(1 - \alpha Z^{-1})$ from a Centellax PCB12500 transmit

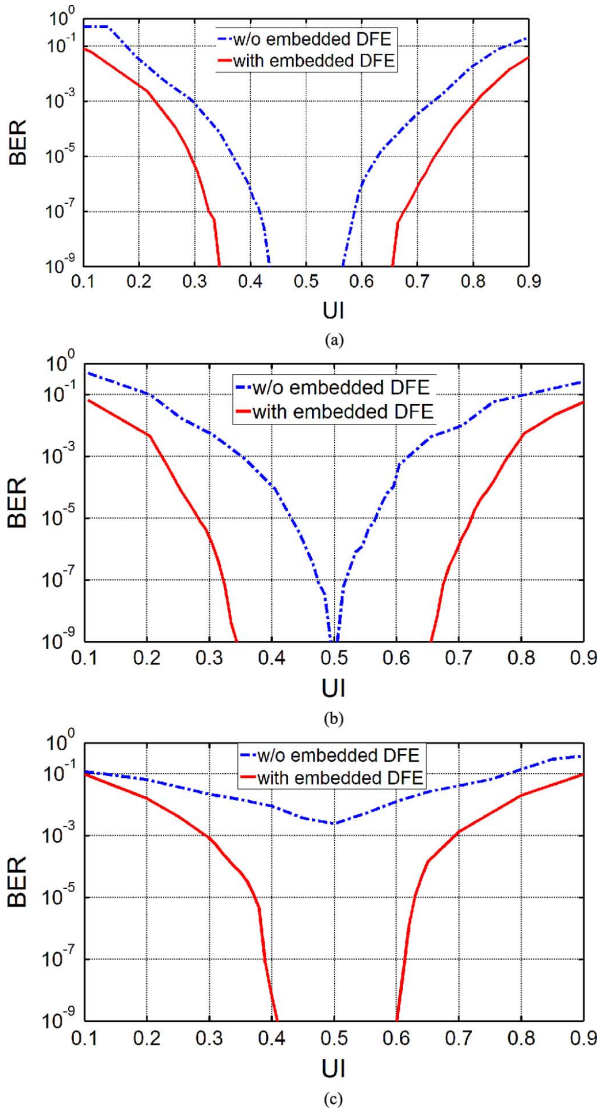


Fig. 19. Measured bathtub curves for the (a) 30-in smooth, (b) 28-in notch, and (c) 46-in higher loss FR4 channels shown in Fig. 3, with and without one-tap embedded DFE for a $2^{10} - 1$ PRBS input with 1-V_{pp} TX swing and no TX equalization.

module to emulate a controlled ISI amount. The ADC input eye diagram with 15-dB de-emphasis is shown in Fig. 18(a). Using a one-tap DFE with the same coefficient, this de-emphasis ISI can ideally be completely removed. The mid-point eye opening at the ADC output after reconstruction of the digital output word is shown in Fig. 18 with and without embedded DFE enabled. Activating the DFE, ISI subtraction improves the eye opening from 4 to 27 LSB.

The embedded DFE operation is also verified by measuring the BER on the three FR4 channels shown in Fig. 3, a 30-in channel with a smooth attenuation profile, a 28-in channel with a notch-shaped frequency response, and a 46-in channel with higher loss profile compared with the other two channels. Here, the MSB output of the ADC is fed back to the Centellax PCB12500 in order to produce BER bathtub curves with a 1-V_{ppd} $2^{10} - 1$ PRBS input without any transmit equalization, as shown in Fig. 19. While the eye is already open without embedded equalization at a BER $= 10^{-9}$ for the first two

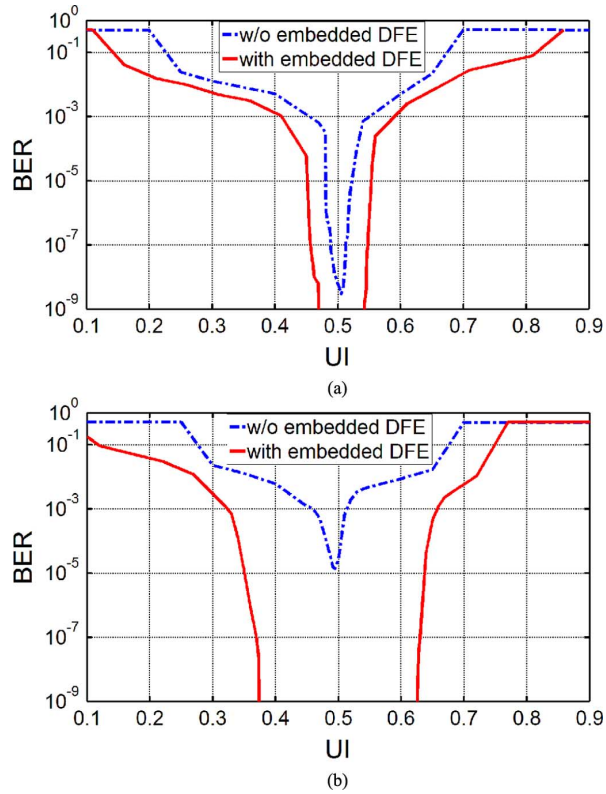


Fig. 20. Measured bathtub curves for the (a) 30-in smooth and (b) 28-in notch FR4 channels shown in Fig. 3, with and without one-tap embedded DFE for a $2^{10} - 1$ PRBS input with 300-mV_{pp} TX swing and no TX equalization.

channels, the horizontal eye opening improves after applying the one-tap embedded DFE, with the improvement being more significant for the notch channel. For channel 3 with ~14 dB loss at the Nyquist bandwidth, the embedded DFE opens the previously closed eye, and results in 0.2-UI timing margin at a BER $= 10^{-9}$. To further investigate the effectiveness of the proposed embedded DFE, the BER performance of the two lower-loss channels are measured for a 300-mV_{ppd} swing at the transmitter as shown in Fig. 20, which forces the notch channel to have a very poor BER performance without any equalization. In the smooth-loss channel, the horizontal opening is improved by more than 0.1 UI at a BER $= 10^{-9}$ relative to without any DFE, while for the notch channel enabling the embedded DFE allows a dramatic increase in horizontal eye opening to near 0.25 UI.

The main specifications of the designed ADC are summarized in Table I. The figure of merit (FOM) for the prototype ADC is calculated as

$$\text{FOM} = \frac{\text{Power}}{\min\{f_s, 2\text{ERBW}\} \cdot 2^{\text{ENOB}}} \quad \text{(pJ/conv.–step)} \qquad (4)$$

where f_s is the sampling frequency, and ERBW is the input frequency that SNDR degrades 3 dB compared with its low-frequency value. This equation results in a FOM of 0.46 and 0.58 pJ/conv.-step considering the ENOB at low-frequency and Nyquist bandwidth (800 MHz), respectively. The ADC performance is also compared with the previously reported similar works. Note that the traditional DFE implementation of this paper's design, which utilizes a symbol decision, differs from the multilevel embedded DFE implementation of [9], which

TABLE I
ADC PERFORMANCE COMPARISON

Specification	[9]	[21]	[22]	[23]	[24]	This Work
CMOS Technology	130nm	130nm	45nm	65nm	40nm	90nm
Supply Voltage (V)	1.2	1.2	1.1	1.2	1.0	1.3
ADC Architecture	TI Pipeline	TI SAR	TI SAR	Asynch. TI-SAR	Asynch. SAR	TI SAR
Input Capacitance (fF)	104	<100	N/A	84	N/A	60
Input Range (V_{pp})	N/A	1.2	1.0	N/A	2	1.0
Resolution (bit)	5	6	7	6	6	6
Sampling Rate (GS/s)	4.8	1.25	2.5	1.0	1.25	1.6
ERBW (GHz)	4	0.45	1.25	0.5	0.6	1.5
Max ENOB (bit)	4.76	5.5	5.9	4.94	4.77	4.75
Power (mW)	300	32	50	6.27	6.08**	20.1
FoM (pJ/Conv.-Step)	2.3	0.78	0.33	0.21	0.18	0.46
Embedded Equalization	DFE*	No	No	No	No	DFE
Active Area (mm^2)	1.69	2.32	1.0	0.11	0.014	0.24

* The embedded equalization is referred as multi-level DFE in [9], which differs from normal 1-tap DFE.
** There is no front-end active T/H in [24], and this structure does not need reference or common-mode voltage buffers.

does not make a hard symbol decision. To the best of our knowledge, this is the first ADC with a true embedded DFE implementation. The proposed design has significantly better FOM relative to the pipeline design with embedded DFE of [9]. Although the sampling frequency of this work is lower than [9] and [22], this can be improved by increasing the time-interleaving factor further without compromising the overall ADC FOM. This work also shows comparable performance as the designs of [21]–[24], which do not include any equalization functionality.

VI. CONCLUSION

A 1.6-GS/s 16-way time-interleaved SAR ADC with embedded one-tap DFE suitable for high-speed link applications is presented in this paper. The proposed redundant cycle technique allows embedding DFE with low power and area overheads. Embedding this partial equalization inside the front-end ADC can result in lowering the complexity of back-end DSP and/or decreasing the ADC resolution requirement. The 1.6-GS/s 6-b prototype ADC with redundant cycle one-tap embedded DFE is fabricated in an LP 90-nm CMOS process in 0.24-mm^2 area and consumes 20.1 mW of total power while achieving a FOM $=$ 0.46 pJ/conv.-step.

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