Continuous-Time Filters from 0.1Hz to 2.0GHz

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XVII Conference on Design of Circuits and Integrated Systems -- Santander, Spain

November 2002

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Abstract.-The bipolar transconductance amplifier (OTA) was commercially introduced in 1969 by RCA. Designers began using OTAs in the middle 80's, since then the CMOS-OTA has becoming a vital component in a number of electronic circuits, both in open loop and in closed loop applications. Here, we will focus on open loop applications. Continuous-time filters implemented with transconductance amplifiers and capacitors known as Gm-C or OTA-C are very popular for a host of applications. These applications involve frequency of operation from a few tents of a hertz up to several gigahertz. Several of those applications are in medical electronics and seismic area where the frequency range is between 0.1Hz up to 20Hz. Other applications in the audio range do not commonly use OTA-C filters because switched-capacitor techniques excel in this range. But for frequency range of a few MHz like in Intermediate Frequency (IF) filters in RF receivers OTA-C implementations are very attractive. For a few GHz range applications where the OTA becomes a simple differential pair there is number of researchers investigating LC-oscillators and filters. In this tutorial we discuss practical implementations of transconductance amplifiers oriented for wide range of applications for example in medical, IF filters, hard disk drive linear phase filters, LC-oscillators and RF filters. Furthermore the unavoidable tuning scheme to compensate the Gm/C deviations due to process technology variations is discussed. OTA single ended, fully differential and pseudo differential versions are introduced together with the common-mode feedback circuits needed for proper operation of differential architectures.

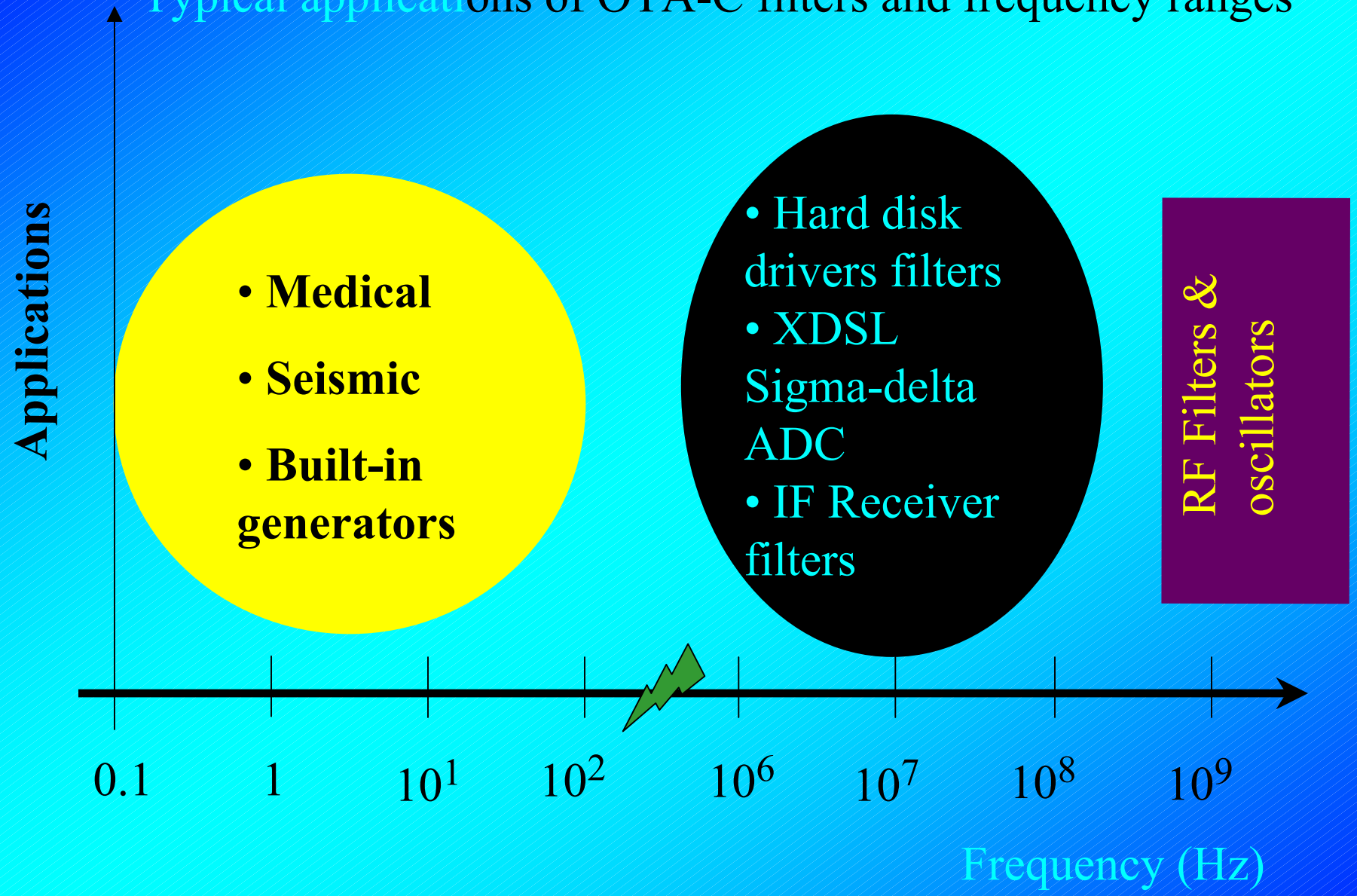
Continuous-Time Filters from 0.1Hz to 2.0GHz

Outline.-

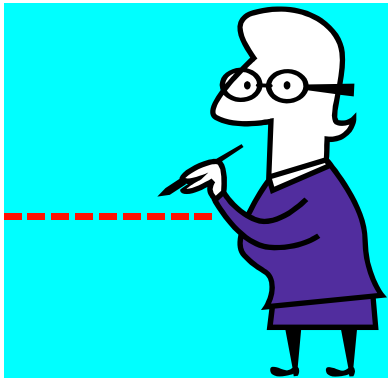
- **Introduction and Motivation**
- **A family of Transconductance for different frequency ranges (applications).**
- **Common-mode feedforward and feedback strategies needed for differential output filters.**
- **Frequency- and Q-tuning techniques for OTA-C filters**

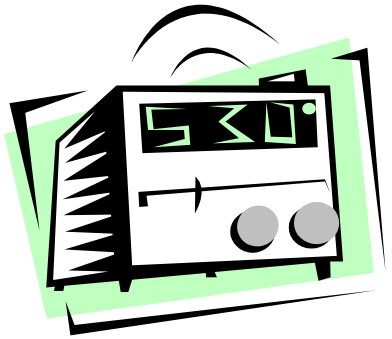
Evolution of the OTA

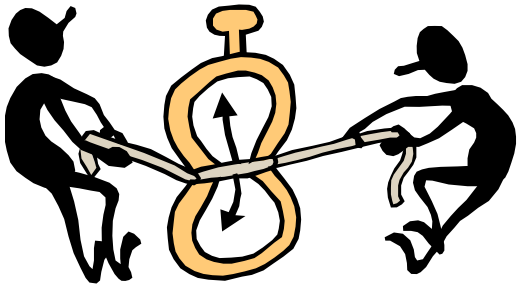
Typical applications of OTA-C filters and frequency ranges



A few examples of continuous-time filters in a host of applications





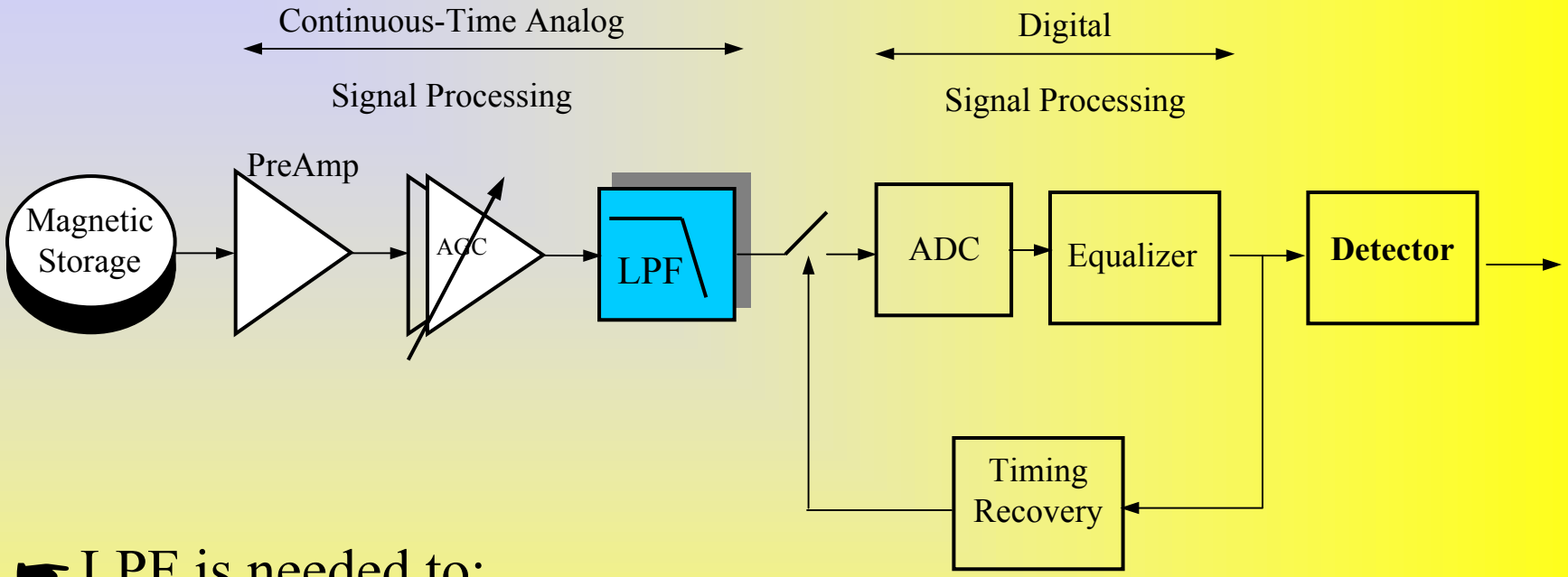


Applications for continuous time filters

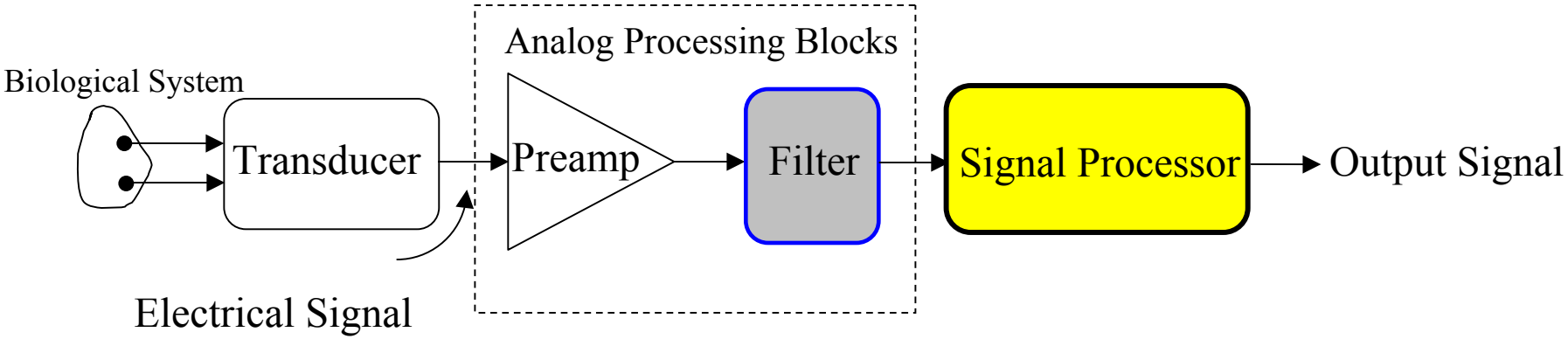
Top view of a 36 GB, 10,000 RPM, IBM SCSI server hard disk, with its top cover removed.

Read channel of disk drives -- for phase equalization and smoothing the wave form

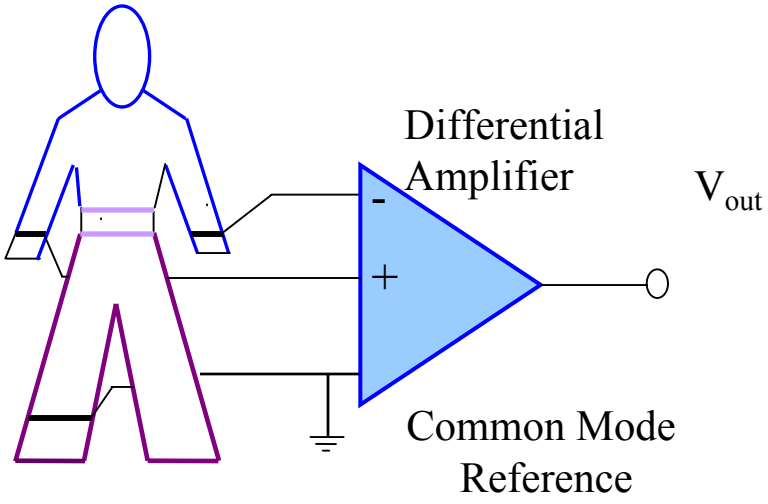
Hard Disk Driver Read Channel



- LPF is needed to:
  - Limit signal and noise bandwidth;
  - Provide anti-aliasing prior to sampling;
  - Provide significant contribution to overall equalization.



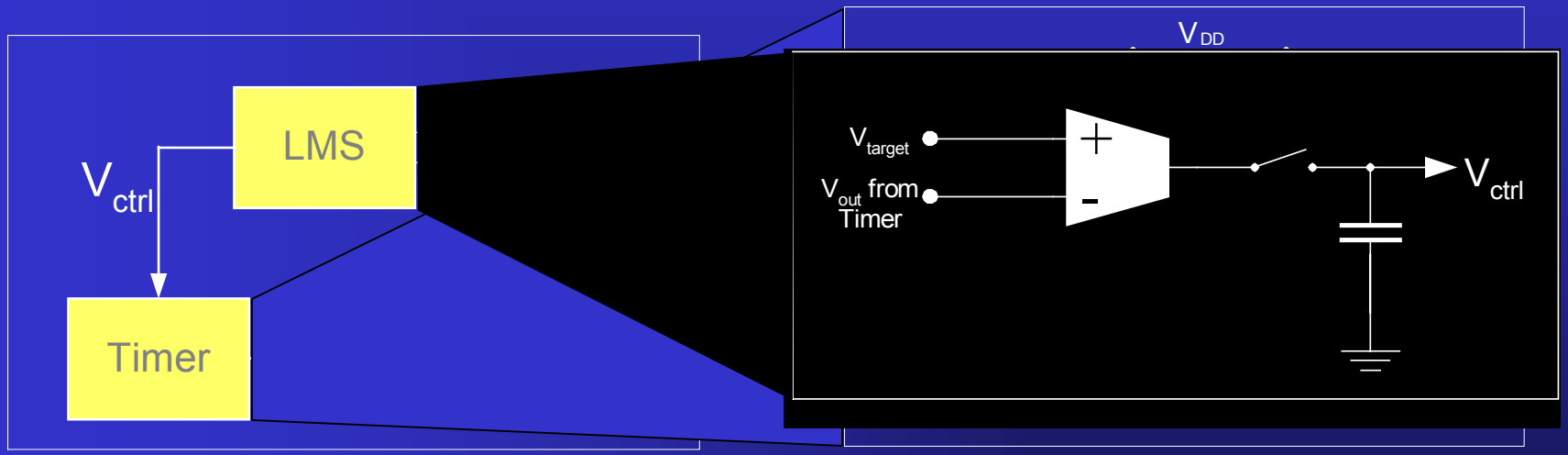
Block Diagram of a general purpose bioelectric signal acquisition system.



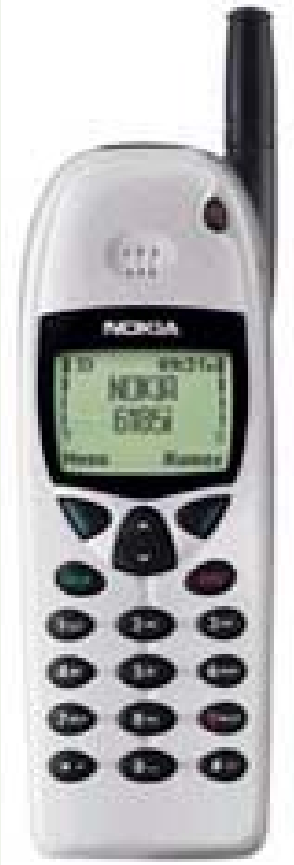
Typical configuration for the measurement of bio-potentials

Parameter	Typical range
Gain	1-1000
Bandwidth	0.1 Hz-10KHz
Dynamic Range (DR)	60dB-100dB
CMRR	80-140dB
Zinput	10MΩ-1GΩ at 60Hz
Vnoise	$<10nV/\sqrt{Hz}$
Inoise	$<1[A/\sqrt{Hz}$

Continuous-Time Linear Ramp Implementation
LMS Integrator



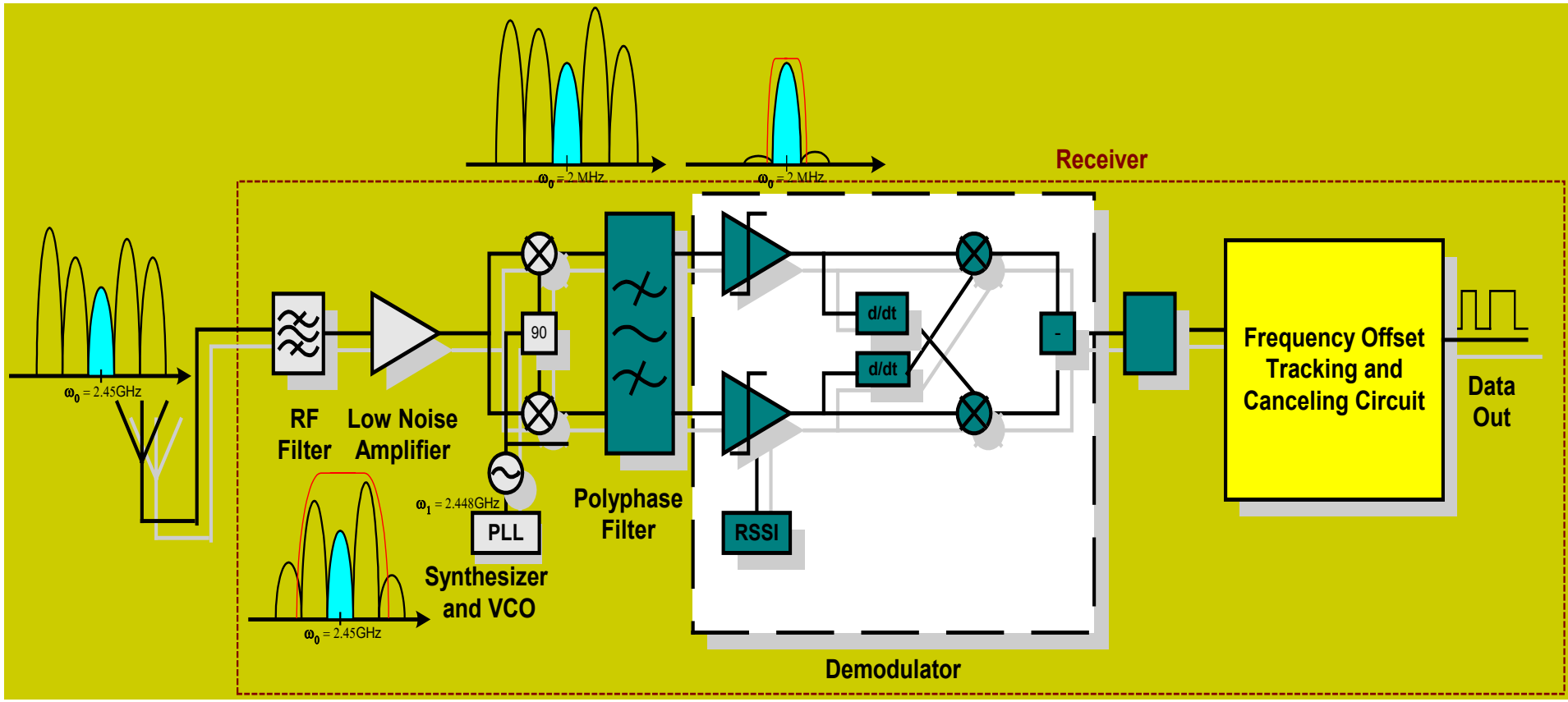
- The Timer is a cascode current source with V_{ctrl} controlling the gate voltage of the current source transistor
- The LMS block is an OTA-C integrator with a switch to control the charging of the capacitor



6185i digital cell phone from Nokia.

Receivers and Transmitters in wireless applications -- used in PLL and for image rejection

Low-IF Bluetooth Receiver

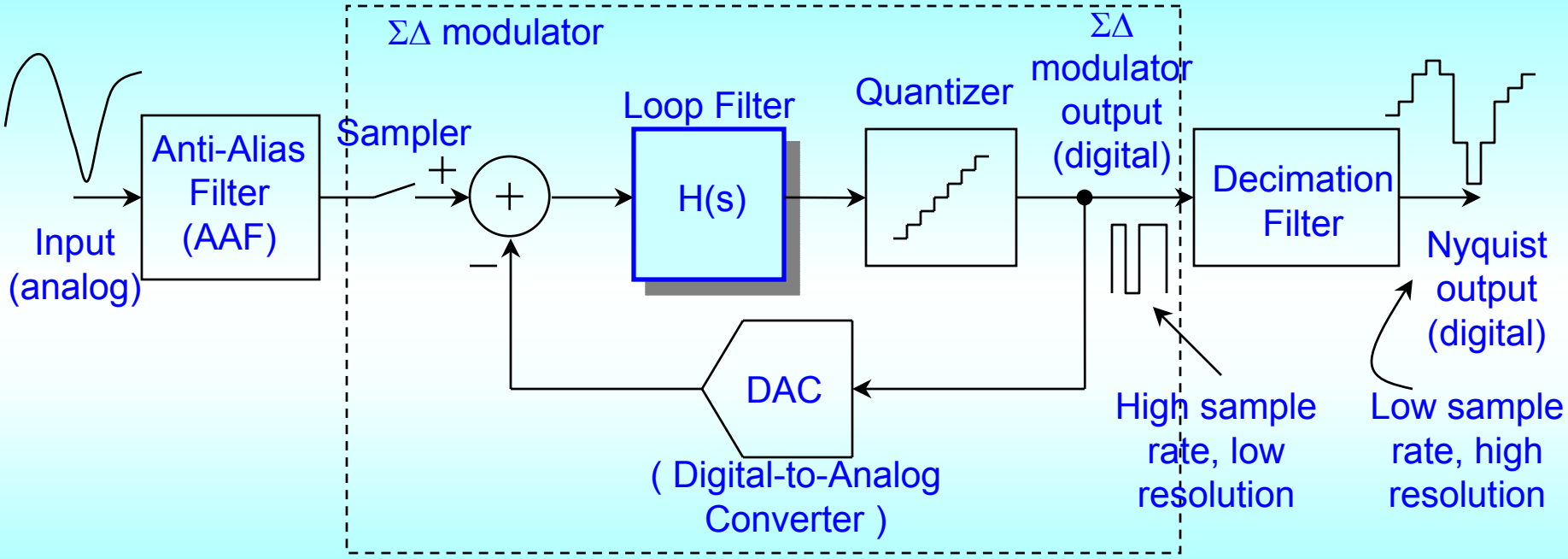


- Active polyphase filter is used to reject image and select channel.

CMP-35 portable MP3 player

All multi media applications --Anti aliasing before ADC and smoothing after DAC. Filters in the Sigma-Delta Converters

Sigma-Delta Oversampled A/D Conversion

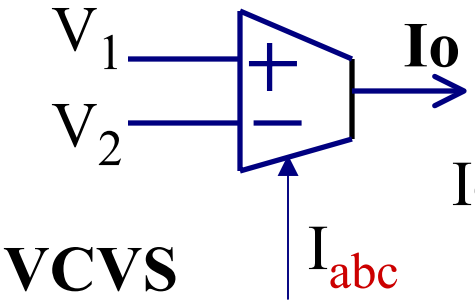


Functional level diagram of a general continuous-time sigma-delta oversampled analog-to-digital converter

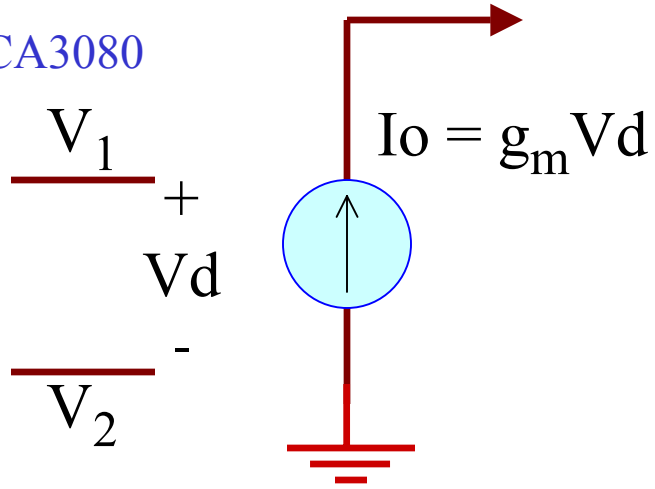
A family of Transconductances for different frequency ranges applications.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

First commercial OTA produced by RCA in 1969, i.e., CA3080



$$Io = g_m(I_{abc})(V_1 - V_2)$$



The transconductance gain " g_m" is a function of the I_{abc} .

$\mathbf{g_m} = h_1 I_{abc}$ for bipolar and weak inversion MOSFETs

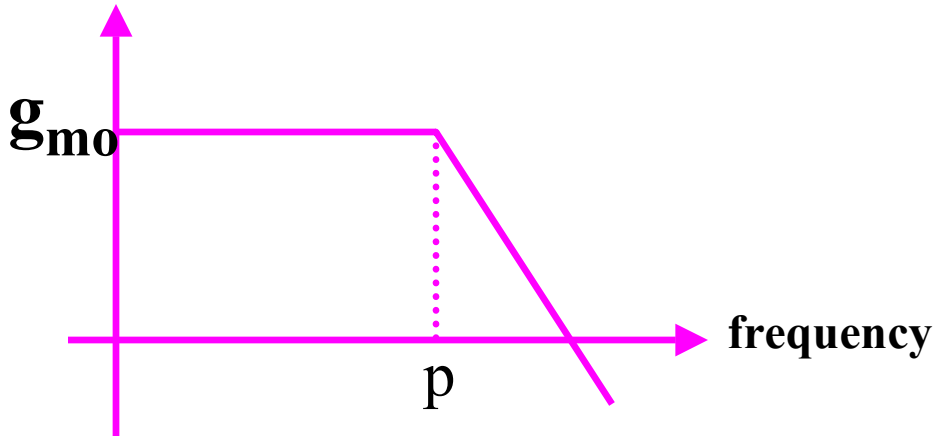
$\mathbf{g_m} = h_2 [I_{abc}]^{1/2}$ for MOSFETs in saturation

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) Frequency Dependence

$$G_m = g_{mo} / (1 + s/p)$$

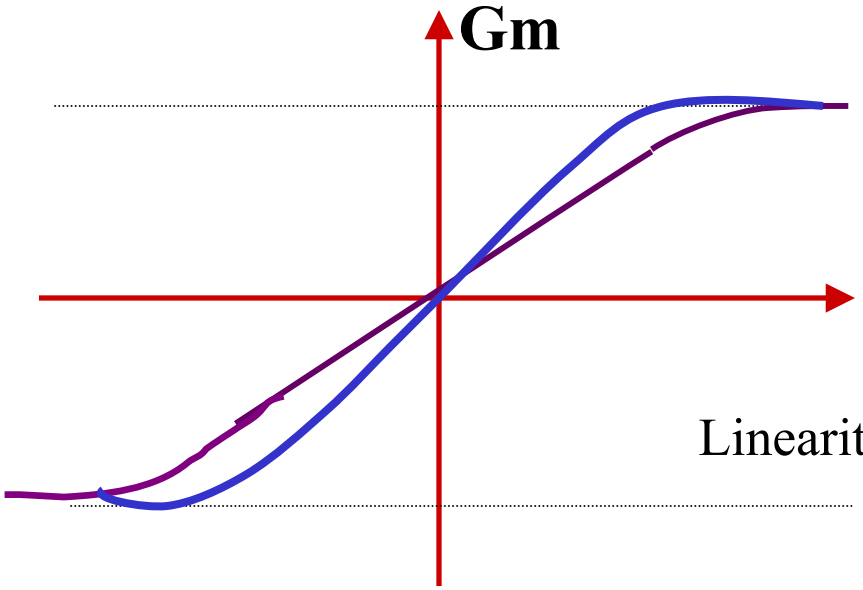
Where g_{mo} is the DC transconductance gain

p is the dominant pole which is around 10MHz to 100Mhz



Issues about the OTA:

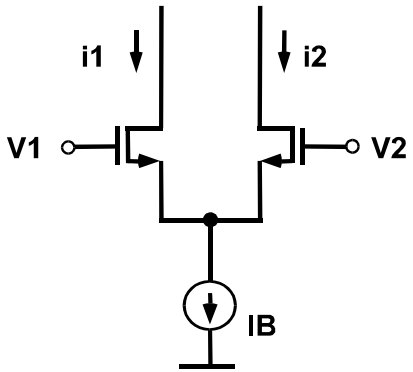
- Operated in open loop conditions
- High-Frequency Operation
- Poor Linearity Range

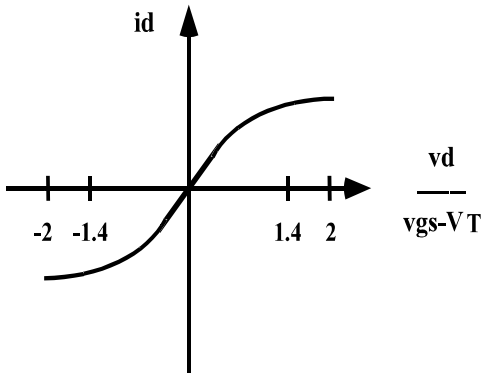


Linearity Range from 50mV to 200 mV

Linearity Issues:

Differential Pair as a V-I converter





$$i_d = \left(\frac{\sqrt{2\beta_1 I_B}}{2}\right) v_d \sqrt{1 - \left(\frac{v_{in}}{2(v_{GS} - v_T)}\right)^2}$$

$$g_m = \sqrt{2\beta_1 I_B}$$

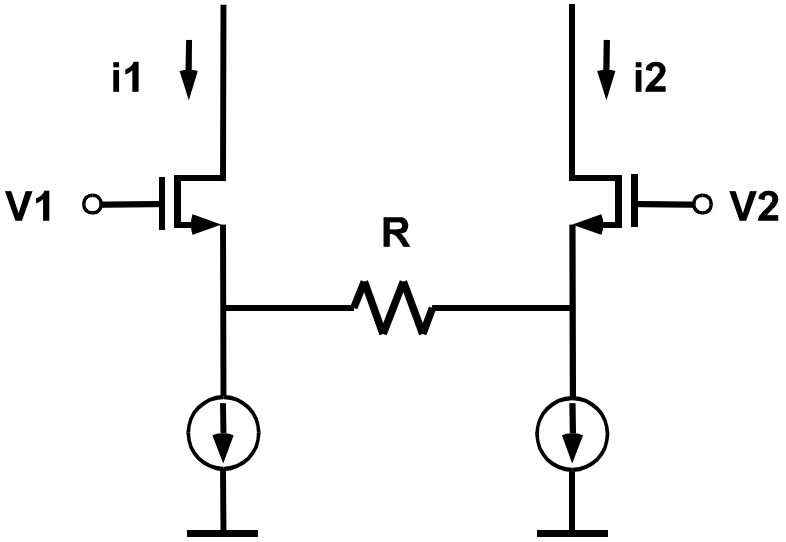
$$HD2 = 0$$

$$HD3 = \frac{1}{32}\left(\frac{v_d}{2(v_{GS} - v_T)}\right)^2$$

How to improve the linearity ?

Differential Pair with Source Degeneration

Improved linearity



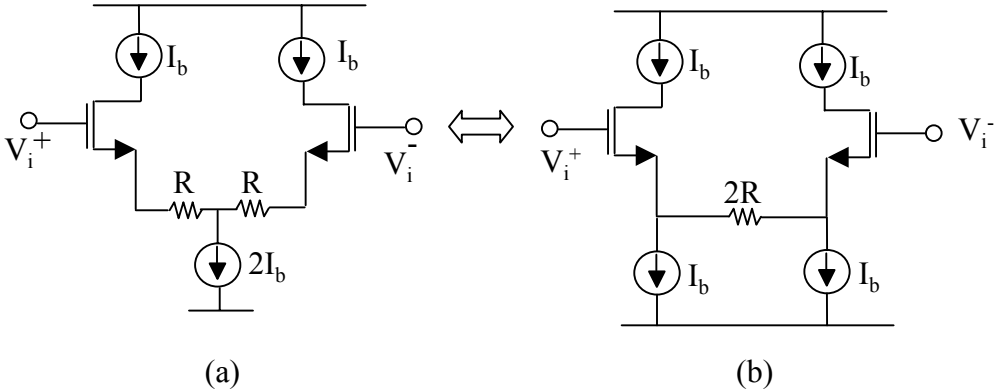
$$1/n = \frac{1}{1 + g_m R}$$

$$i_d = \left(\frac{\sqrt{2\beta_1 I_B}}{2}\right)\frac{v_d}{n}\sqrt{1 - \left(\frac{v_{in}}{2n(v_{GS} - v_T)}\right)^2}$$

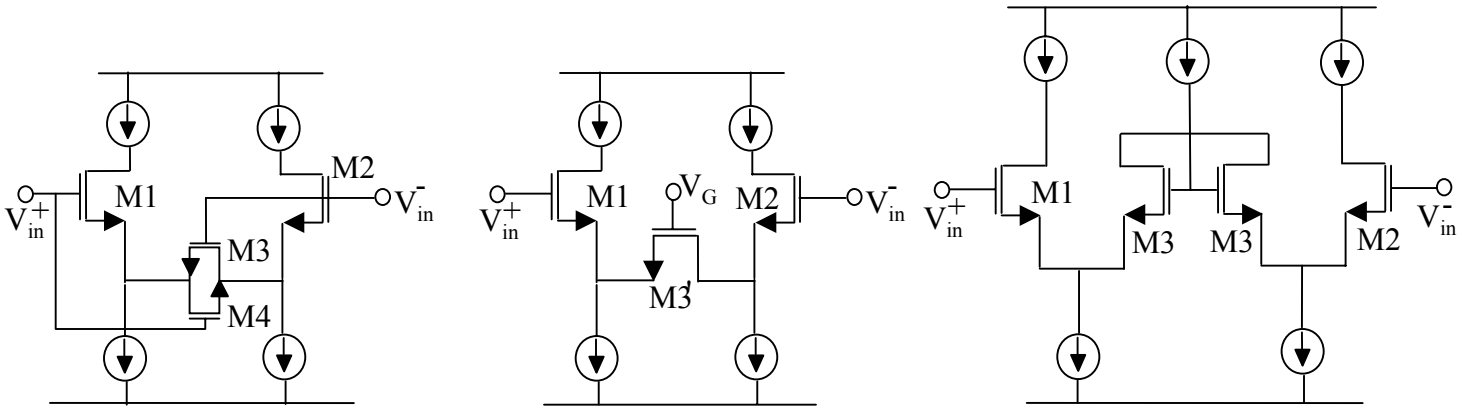
$HD2 = 0$ Ideally

$$HD3 = \frac{1}{32n^2}\frac{v_{in}^2}{(v_{GS} - v_T)^2}$$

g_m linearization schemes via source degeneration.



(a) (b)



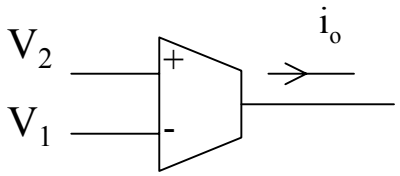
(a) (b) (c)

Active Source Degeneration topologies; (a) and (b) transistors biased on triode region and (c) with saturated transistors.

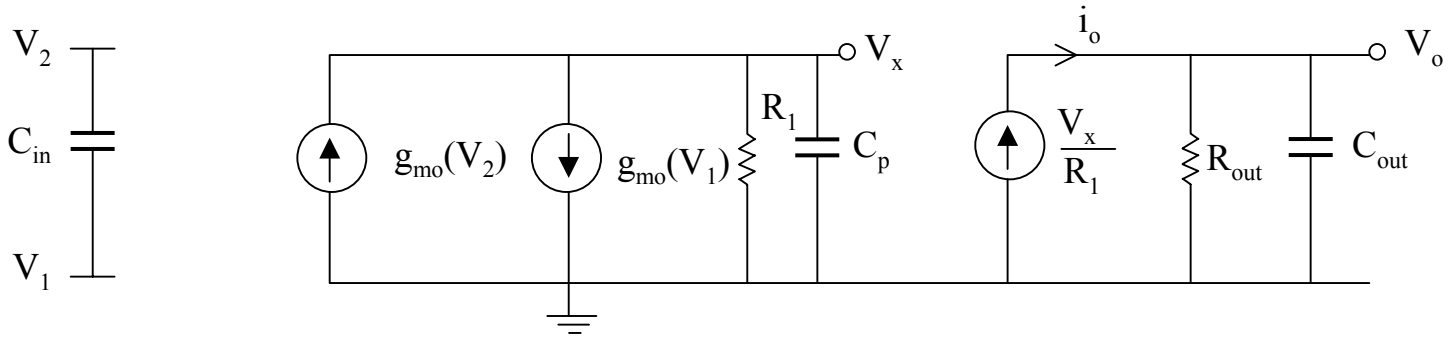
Table 3. Properties of OTAs using source degeneration

Reference/Figure	Transconductance	Properties
Fig. (a)	$\frac{g_{m1}}{1+\frac{\beta_1}{4\beta_3}}$	Low sensitive to common-mode input signals. The linear range is limited to $V_{in}<V_{DSAT}$, and THD=-50 dB. M1=M2, M3=M4
Fig. (b)	$\frac{g_{m1}}{1+g_{m1}R}$ $R=1/\mu_o C_{ox}\left(V_{gs}-V_T\right)$	Highly sensitive to common-mode input signals. For better linearity large V_{GS3} voltages are required. Large tuning range if V_G is used.
Fig. (c)	$\frac{g_{m1}}{1+g_{m1}/g_{m3}}$ M1=M2	Low sensitive to common-mode input signals. Limited linearity improvement, HD3 reduces by -12 dB. More silicon area is required.

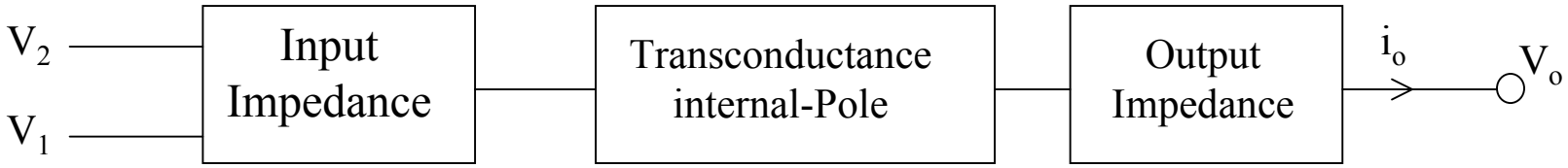
A Linear CMOS OTA Macromodel



$$g_m = \frac{g_{mo}}{1 + \frac{s}{\omega_p}} \quad ; \quad \omega_p = \frac{1}{R_1 C_p}$$

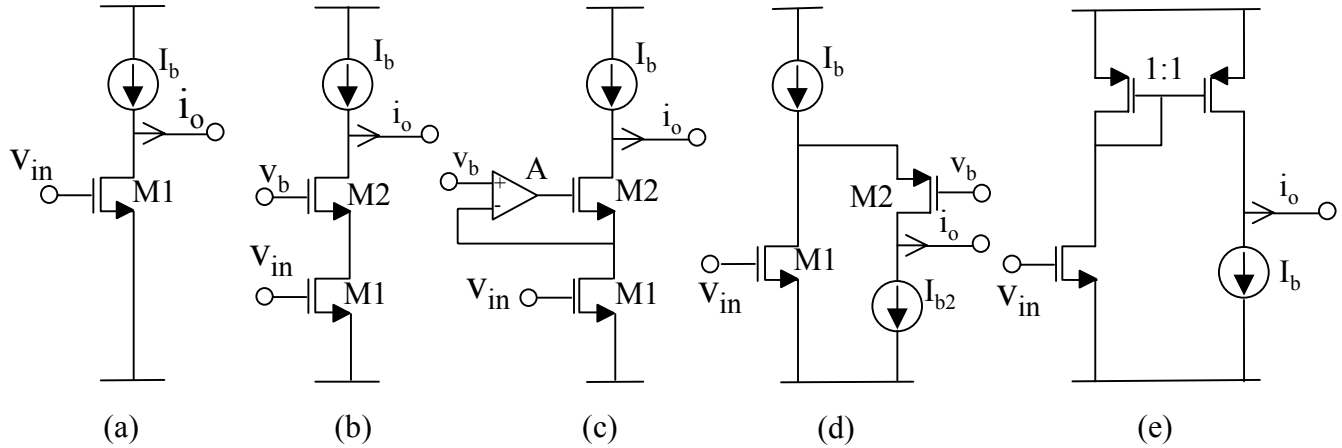


Real OTA Macromodel



OTA Macromodel Representation

Single-input Transconductor (ST) Implementations



Single Input (a) Negative Simple Transconductor, (b) Cascode Transconductor, (c) Enhanced Transconductor, (d) Folded-Cascode Transconductor, (e) Positive Simple Transconductor.

- Observe that:

  $g_m = f(I_b)$, the exact relation is a function of the transistor region of operation.

- Note that output impedance of (a) and (e) are only $1/g_{ds}$ and (b),(c) and (d) implementations have larger output impedances.

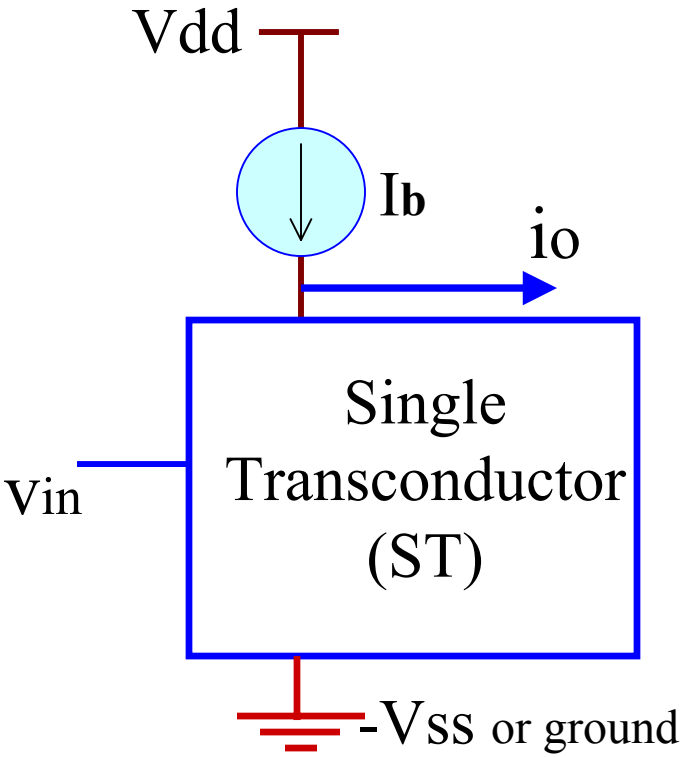
Properties of Simple (single input/ single output) Transconductors

Structure/ Figure	R_{out}	Min V_{DD} *
Simple/1(a)	$\frac{1}{g_{ds1}}$	$\sqrt{\frac{2I_B}{k}} + V_{sat,I_B}$
Cascode/l(b)	$\frac{g_{m2}}{g_{ds1}\ g_{ds2}}$	$(1+m)\sqrt{\frac{2I_B}{k}} + V_{sat,I_B}$
Enhanced/1(c)	$\frac{A\,g_{m2}}{g_{ds1}\ g_{ds2}}$	$(1+m)\sqrt{\frac{2I_B}{k}} + V_{sat,I_B}$
Folded/1(d)	$\frac{g_{m2}}{g_{ds1}\ g_{ds2}}$	$\sqrt{\frac{2I_B}{k}} + V_{Tp} + V_{sat,I_B}$

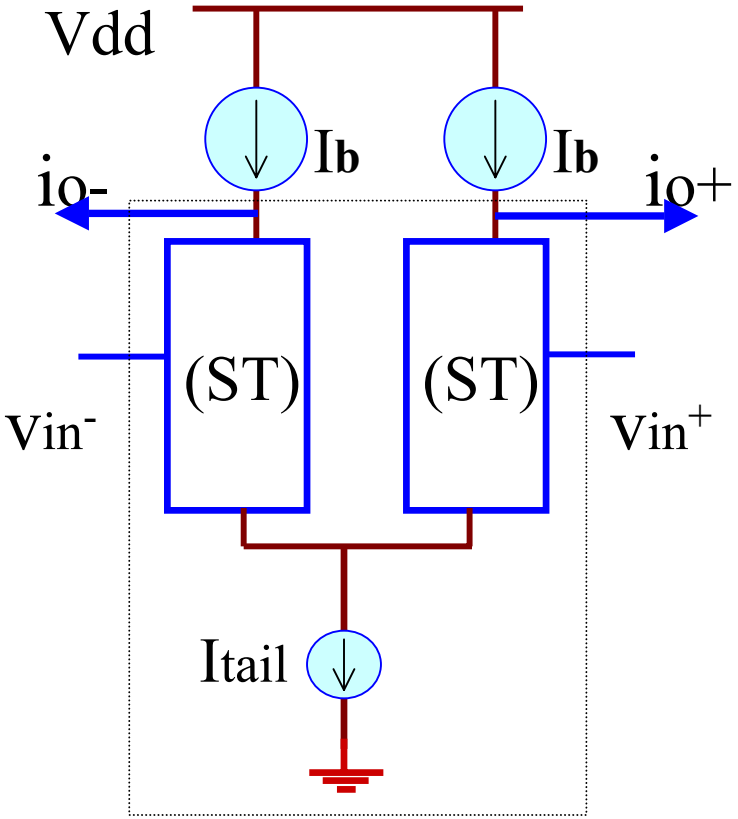
* The bottom devices of the cascode pairs have an aspect ratio of $(W/L)_1/(W/L)_2=m^2$. k is a technological parameter determined by the mobility, and the gate oxide; $V_{sat,IB}$ is the saturation voltage for the I_B current source.

Based on the simple (single input) transconductance how can one generate differential input/single output and fully differential transconductances?

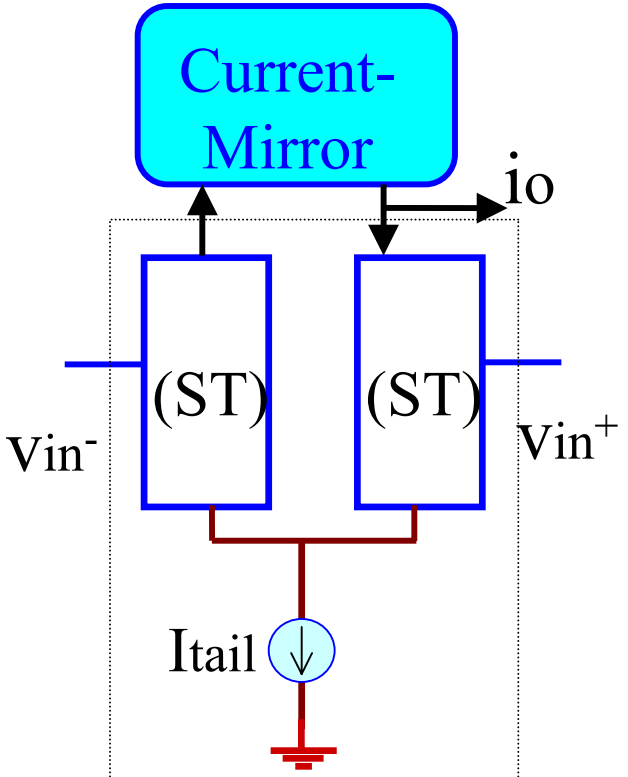
Basic Building Block



Two possible implementations of OTAs

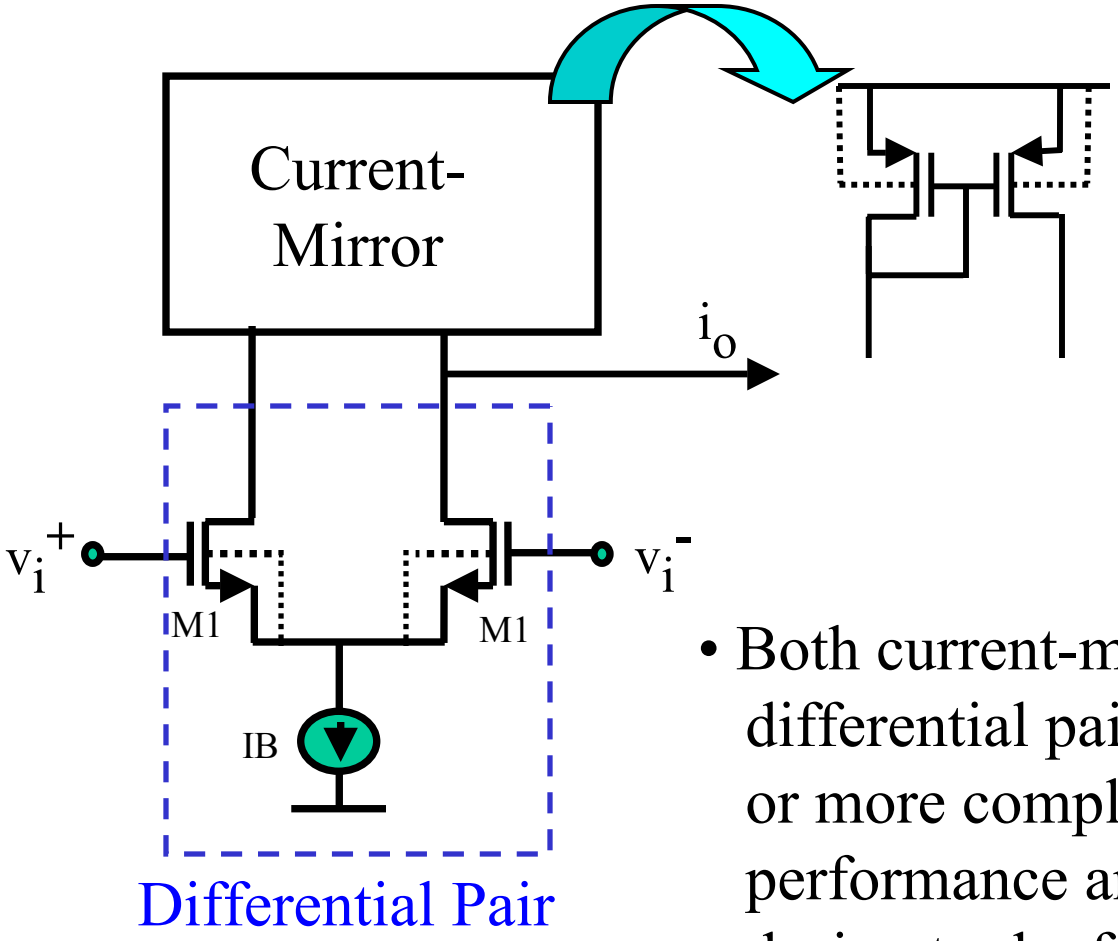


Differential Input -
Differential Output



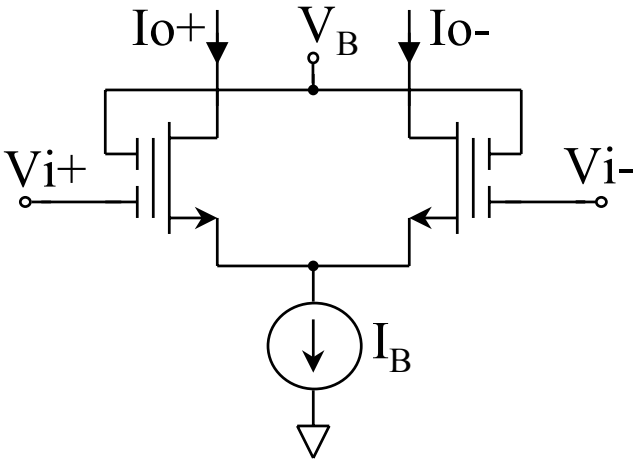
Differential Input -
Single-ended Output

Basic Differential Transconductance (Single-ended)

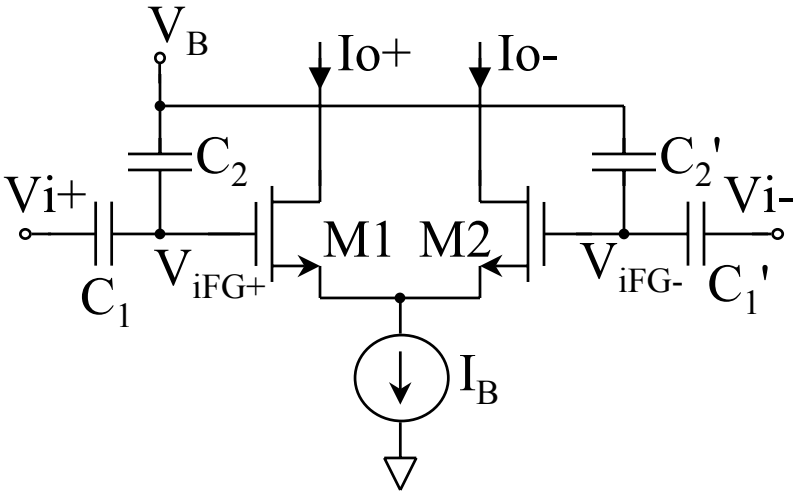


- Both current-mirror and/or differential pair can be simple or more complex to improve performance and/or to increase design tradeoffs

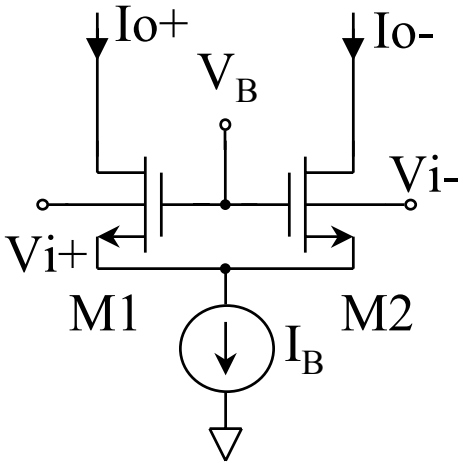
Potential Solutions for Rail-to-Rail Amplifiers: OTAs suitable for Low Frequency Applications



FG DP Implementation

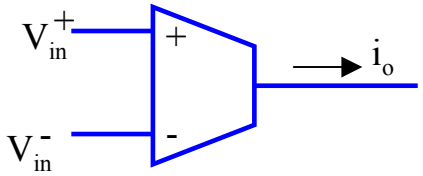


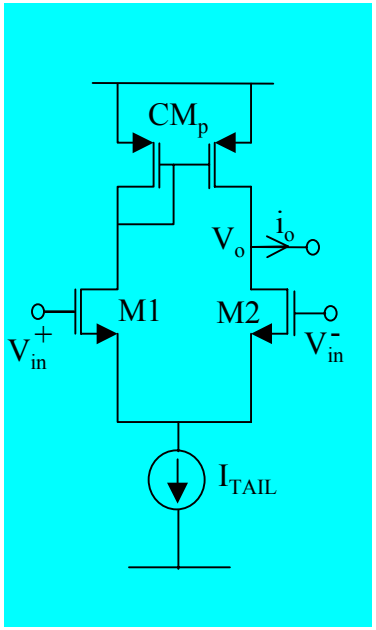
FG DP Equivalent circuit

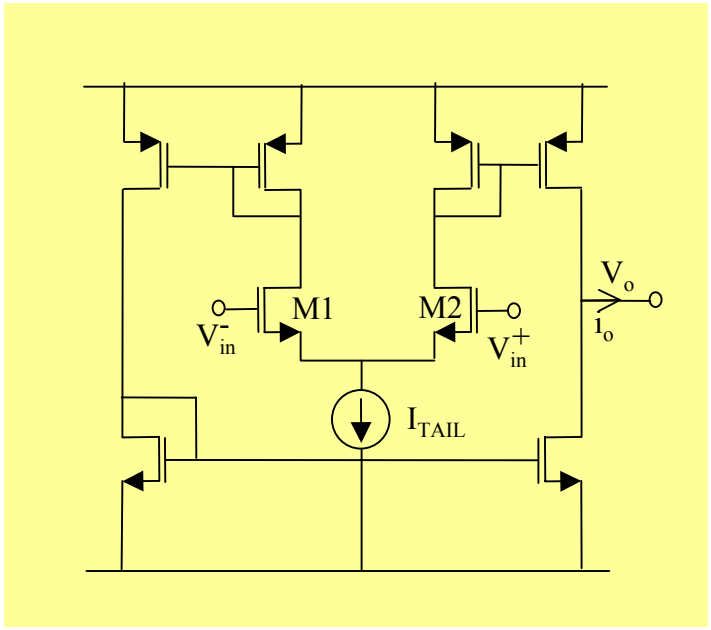


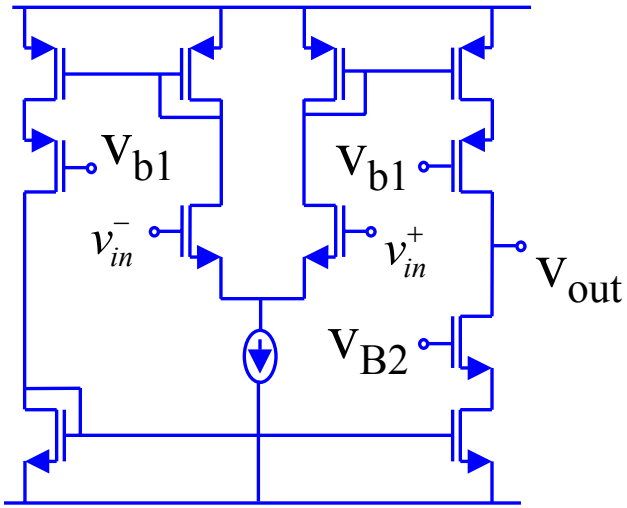
Bulk Driven DP

Three Conventional Differential Input –Single Ended OTAs



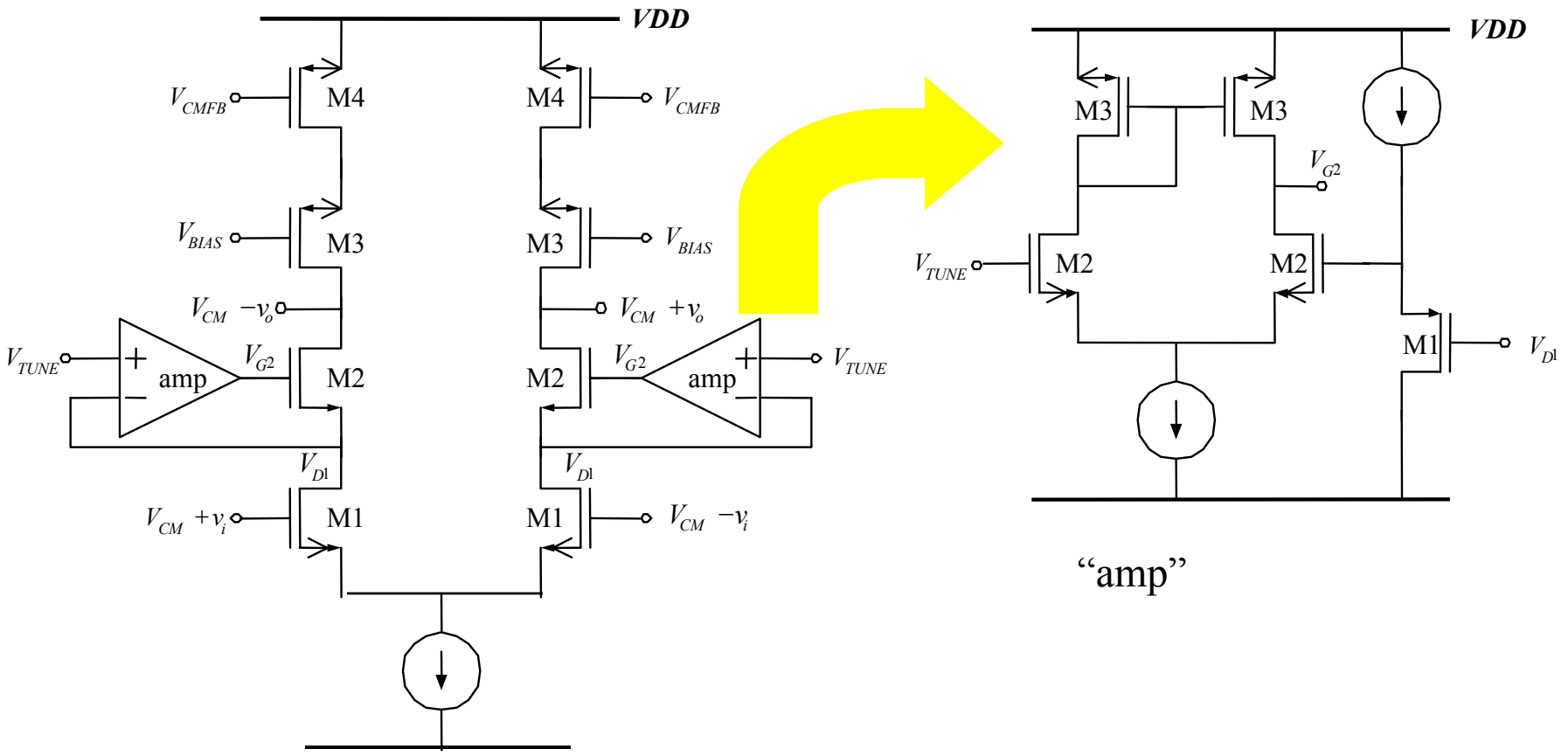






(a) Simple differential input OTA. (b) Balanced OTA (c) Cascode

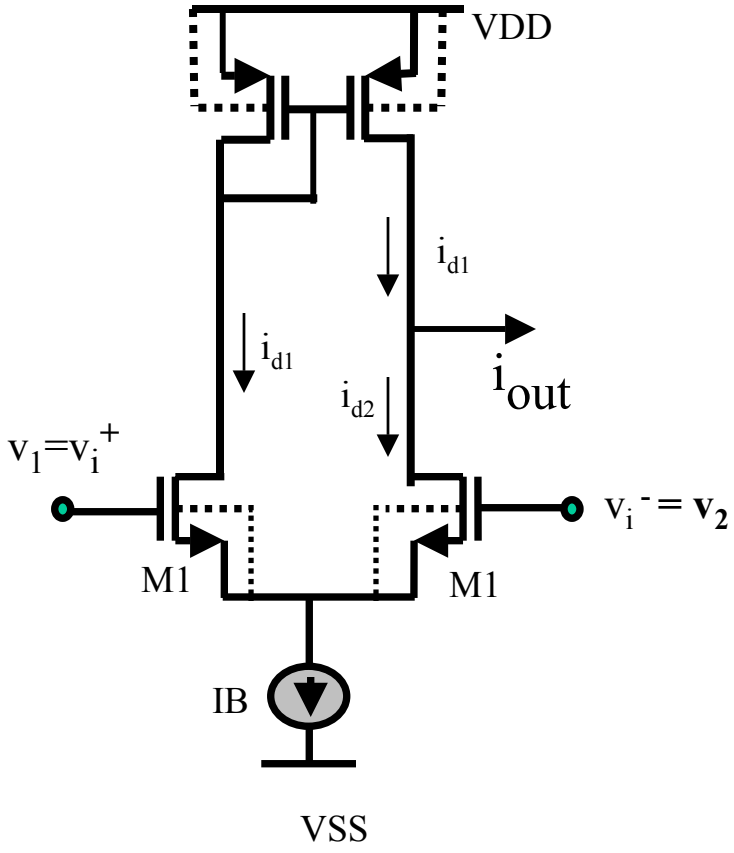
High DC Gain Differential OTA



☛ Transistors M1 operate in Linear region: Wide linear range; Large tuning range;

☛ RGC loop: Fix V_{DS1} ➡ better linearity.

Basic Operational Transconductance Amplifier Characteristics



DESIGN CONSIDERATIONS:

➪$v_d = v1-v2 < V_{DSAT}$

➪$V1,2 - VSS > V_{GS1}+V_{DSATB}$

$$i_{out} = \sqrt{\mu_n C_{OX} \frac{W}{L} I_B}\left(v_1 - v_2\right)$$

or

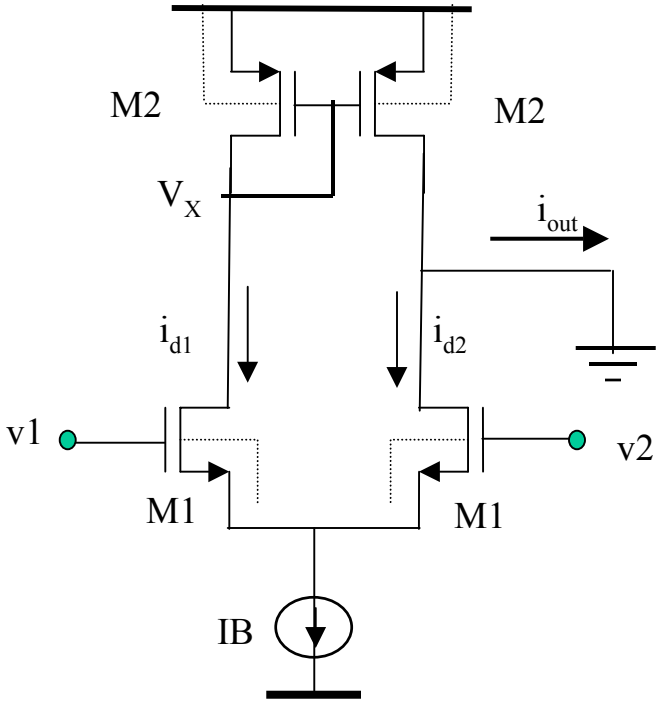
$$i_{out} = g_m\left(v_1 - v_2\right)$$ Sensitive to differential signals

$$v_{out} = g_m r_{out}\left(v_1 - v_2\right)$$

$$r_{out} = \left(g_{o1} + g_{op}\right)^{-1}$$

i_{out}=0 for v_1=v_2 ==> rejection to common-mode signals

Simple OTA Design Equations



$$g_m = \mu_n C_{OX}\left(\frac{W}{L}\right)V_{DSAT}$$

$$\text{Noise} \Rightarrow g_m > g_{m,min}$$

$$GBW = \frac{g_m}{C_L}$$

$$\omega_p = \frac{g_{mp}}{C_p} \cong \mu_p \frac{V_{DSAT}}{2L_p{}^2}$$

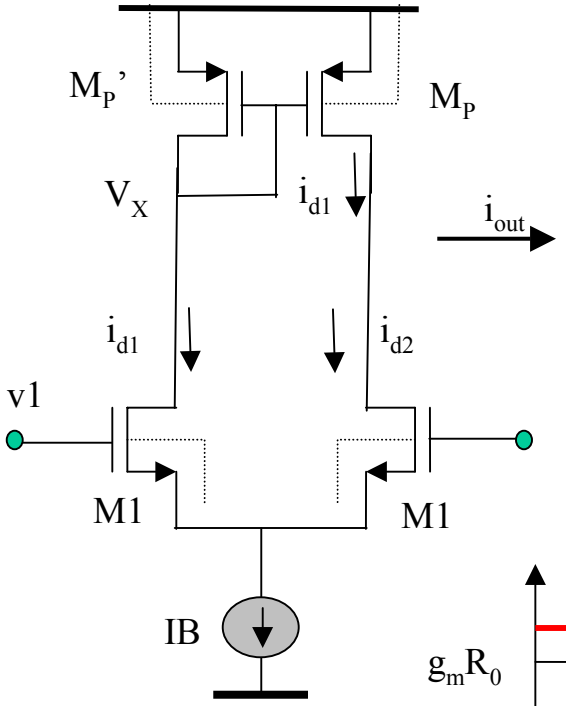
$$\text{Rout} \cong r_p \| r_n$$

V_{DSAT} is limited!!

$$\text{Noise}(V_{RMS}) = \sqrt{\frac{16kT}{3}}\sqrt{\frac{1}{g_{m1}}}\sqrt{1+\frac{g_{m2}}{g_{m1}}}\left(\sqrt{BW}\right)$$

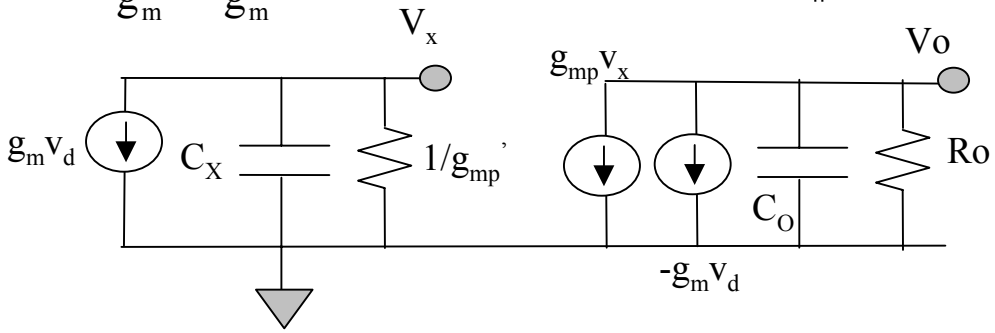
$$\text{Rout} \cong \frac{V_{early}L_P}{I_D}, \qquad \omega_P \cong \frac{g_{mp}}{2C_{GSP}} \cong \frac{\mu_P V_{DSATP}}{2L_P{}^2}$$

Simple OTA Frequency Response

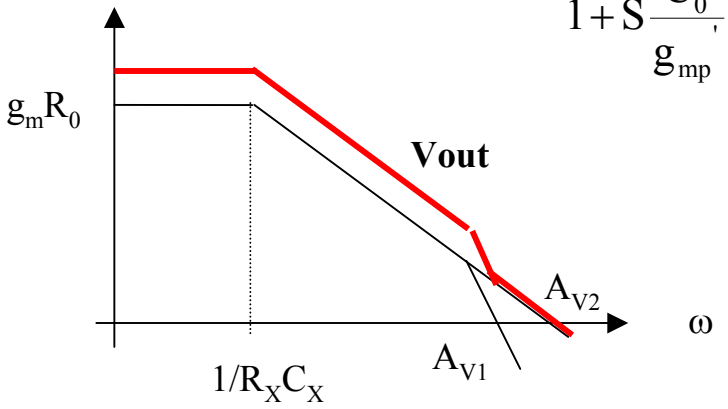


$$\frac{1}{g_m'} = \frac{1}{g_m'} \| R_{OL}$$

$$R_O = R_{ON} \| R_{OP}$$



$$V_0 = -\frac{g_m\left(\frac{g_{mp}}{g_{mp}'}\right)}{1+S\frac{C_0}{g_{mp}'}}\frac{R_0}{1+SR_0C_0}V_d - \frac{g_mR_0}{1+SR_0C_0}V_d$$

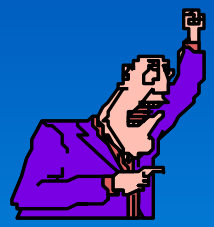


VERY LOW FREQUENCY FILTERS

The Design of Analog Circuits below 100 Hz

is not trivial

- **RC > 0.001 sec**
  - if C = 10 pF then R > 100 MOHMS
  - for a 1 Hz filter (pace makers and other applications)
  - C = 10 pF, R = 628 GOHMS (Gm = 2 pA/V)
  - C = 1000 pF, R = 6.28 GOHMS (Gm = 2 nA/V)



WE NEED SMALL G_M

For the basic OTA-C integrator,

$$\tau = \frac{C_L}{g_m} \Leftrightarrow f = \frac{g_m}{2\pi C_L}$$

- We need very small g_m for very low frequency applications
- As an example, for τ = 1s and g_m = 16nA/V, C_L = 1.6 nF !!
- For a POLY-I POLY-II Capacitor (C/A ~ 600 aF/μm^2) in the AMI 1.2μ process, this means a Si area of 2.7 mm^2 !! => Impractical for IC's (Tiny chip area ~ 4 mm^2)

How can we tackle this low frequency (large time constant) design problem ?

Possible Solutions for high-performanceVery small transconductance

OTA's circuits involve operating transistor in their transistion region and:

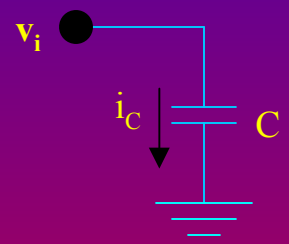
- Current division techniques
- Floating Gate Techmiques
- Bulk- Driven transistors

•Impedance scalers

- •Z==> NZ or Z/N (C ==> NC)
- •low-noise impedance scalers
- •small silicon area

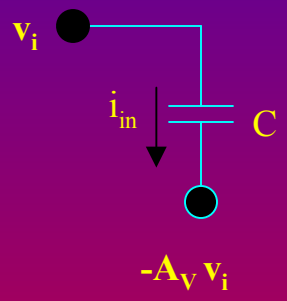
IMPEDANCE SCALERS

Single capacitor



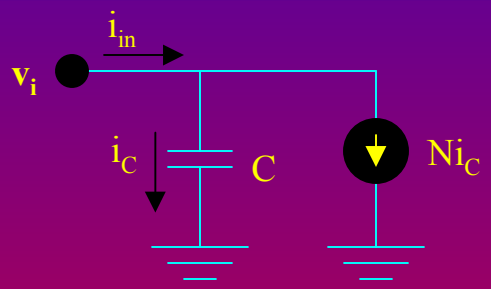
$$i_C = (sC)v_i$$

Voltage amplifier



$$i_{in} = \left(sC\left(1 + A_V\right)\right)v_i$$

Current amplifier



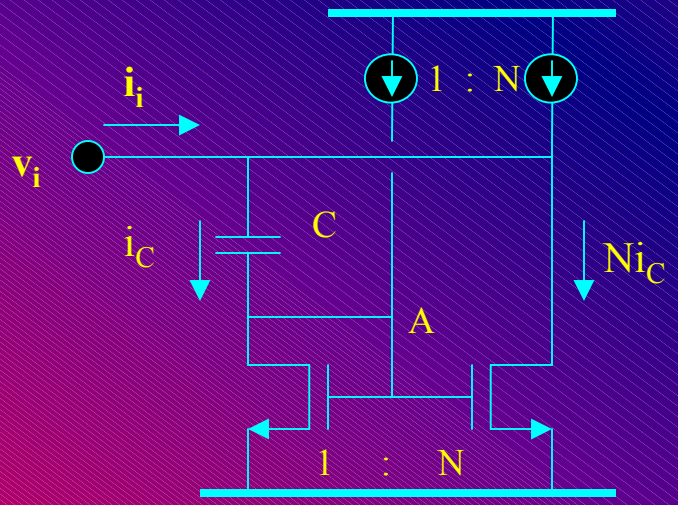
$$i_{in} = \left(sC\left(1 + N\right)\right)v_i$$

Remarks:

➪**Voltage amplification is useless for low-voltage continuous-time filters.**

➪**Impedance scaler based on currrent amplification is precise for moderated N.**

CAPACITOR MULTIPLIER CIRCUIT IMPLEMENTATION



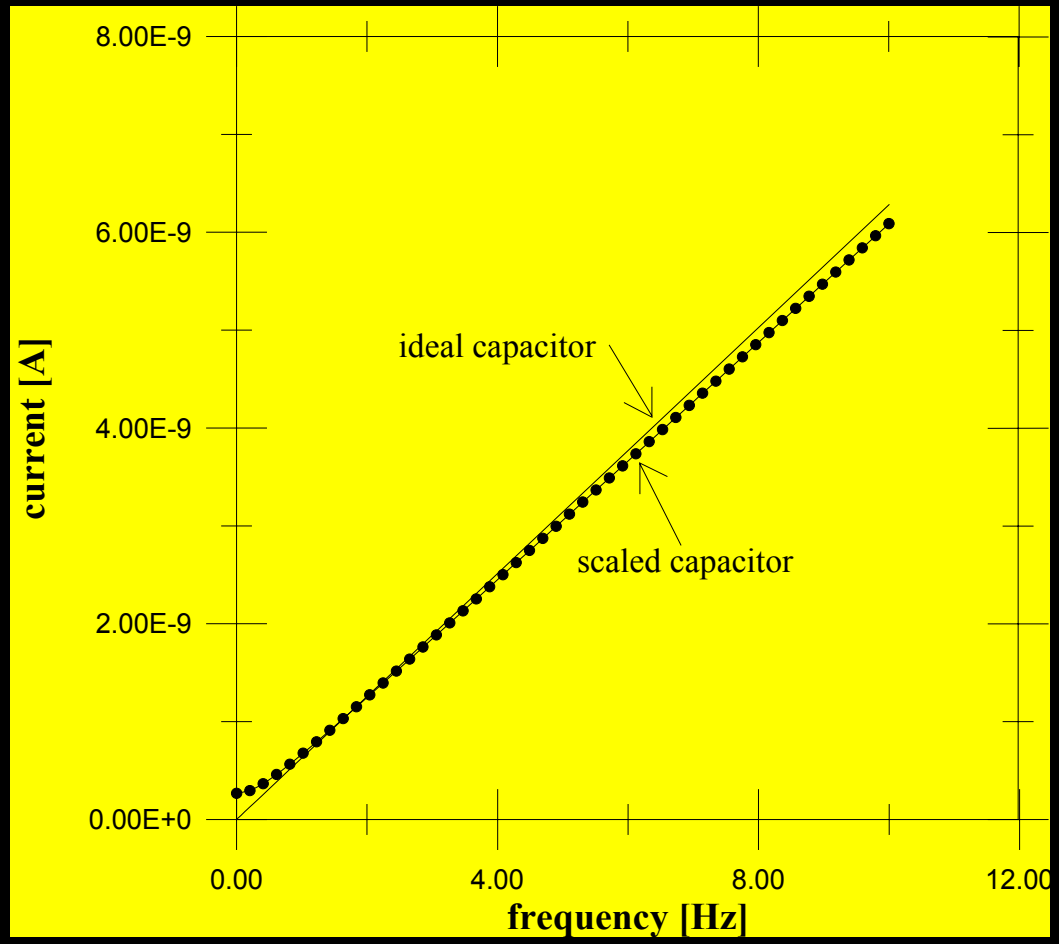
$$\frac{v_i}{i_i} = \frac{vi}{(N+1)i_C}$$

$$Z_{eq} = \frac{1}{s[(N+1)C]}$$

The following conditions must be satisfied:

- Low impedance at node A
- Transistor output resistance can be neglected
- Current gain is precise

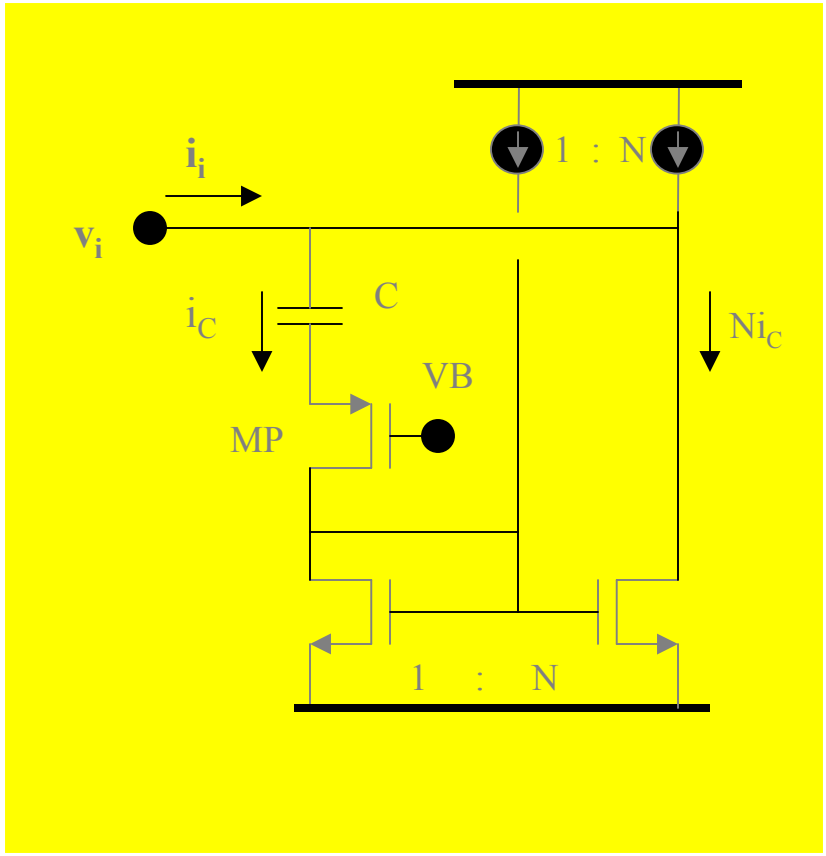
DESIGN EXAMPLE: Capacitor Multiplier



100 pF capacitor.

Scaled capacitor uses a 5 pF capacitor and N=19.

IMPROVING ITS FREQUENCY RESPONSE



Cascode transistor improves frequency response

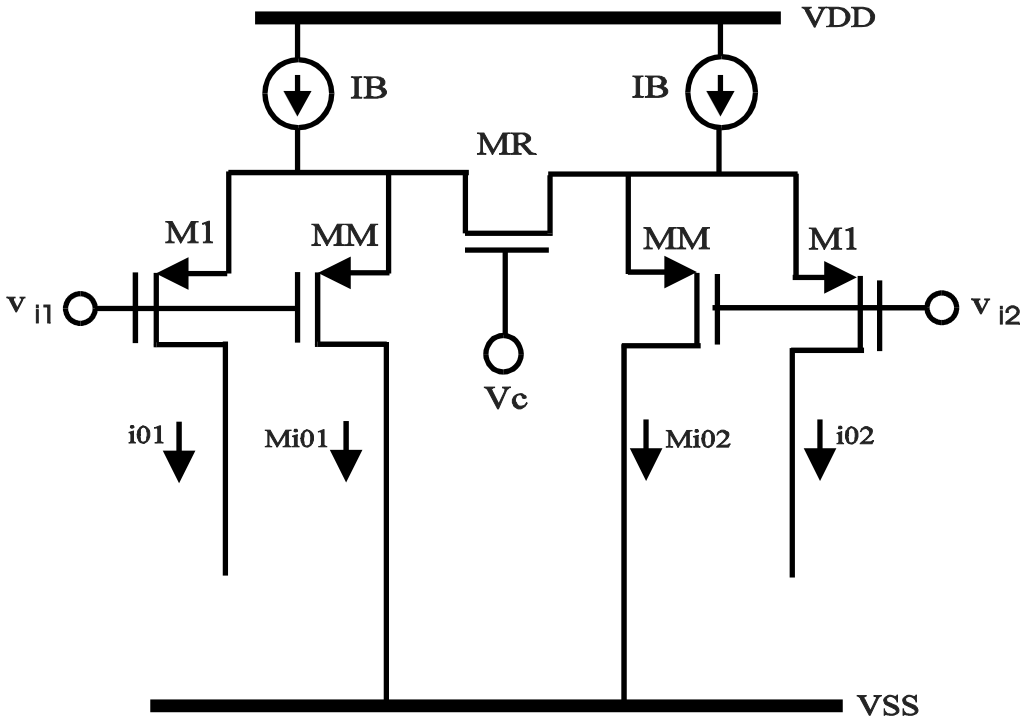
Design procedure:

MP is optimized for frequency.

N-type transistors are optimized for precision.

The loop must be stable

CURRENT DIVISION PRINCIPLE PLUS SOURCE DEGENERATION TRANSCONDUCTANCE

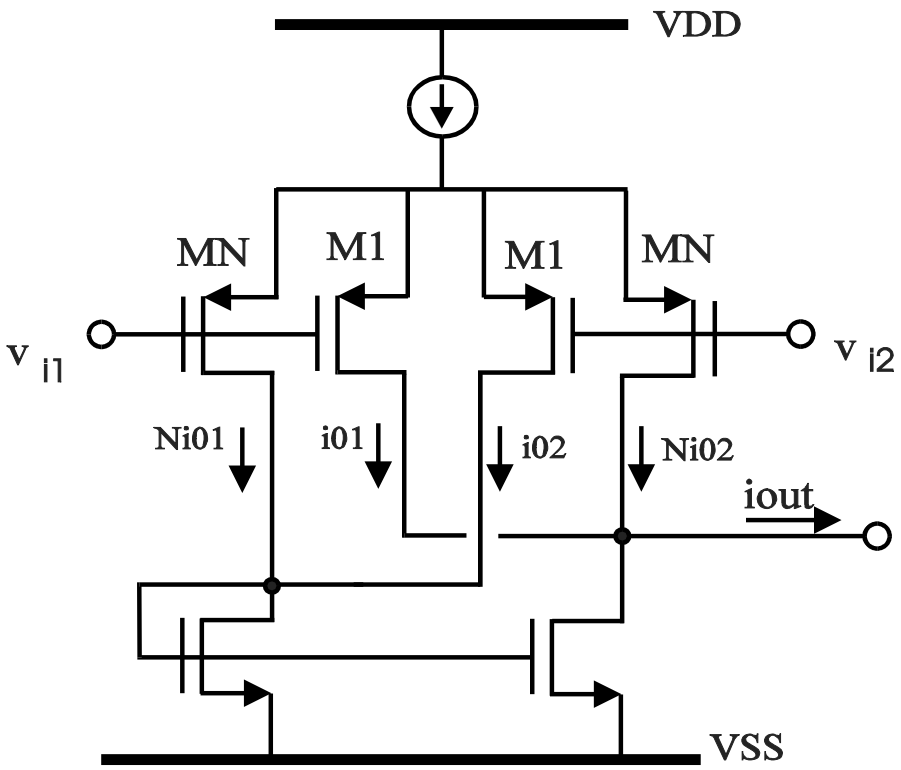


$$HD \propto \frac{v_{i1} - v_{i2}}{V_{GS} - V_T}$$

$$\frac{i_{01} - i_{02}}{v_{i1} - v_{i2}} = \frac{2\mu C_{OX}}{M+1}\frac{W_R}{L_R}(V_{GS} - V_T)$$

$$M = \frac{g_{mm}}{g_{m1}}$$

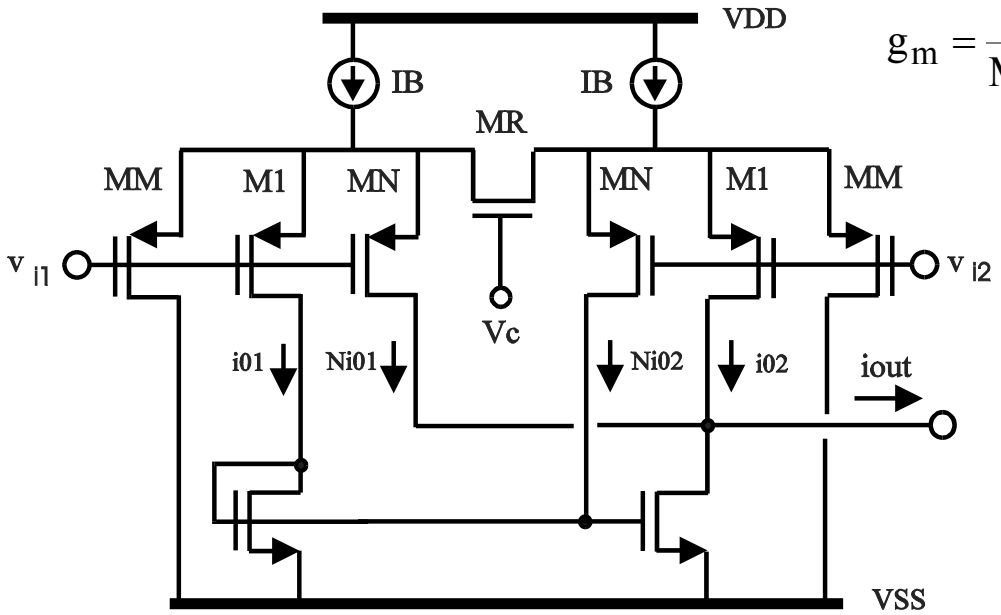
CURRENT CANCELLATION PRINCIPLE



$$G_m = \frac{N-1}{N+1} g_{ml}$$

PARTIAL POSITIVE FEEDBACK !!!

OTA FOR VERY LOW-FREQUENCY APPLICATIONS

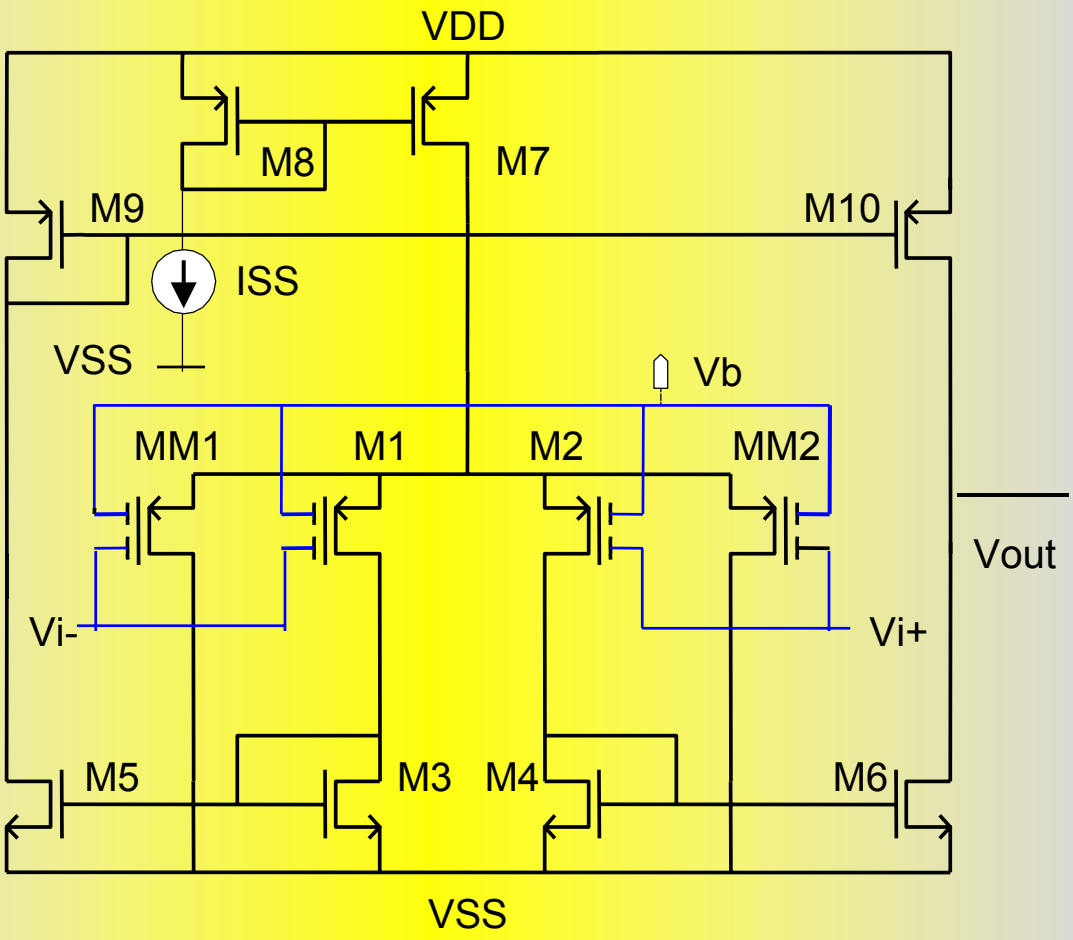


$$g_m = \frac{2(N-1)}{M+N+1}\left(\mu C_{OX}\frac{W_R}{L_R}(V_{GS}-V_T)\right)$$

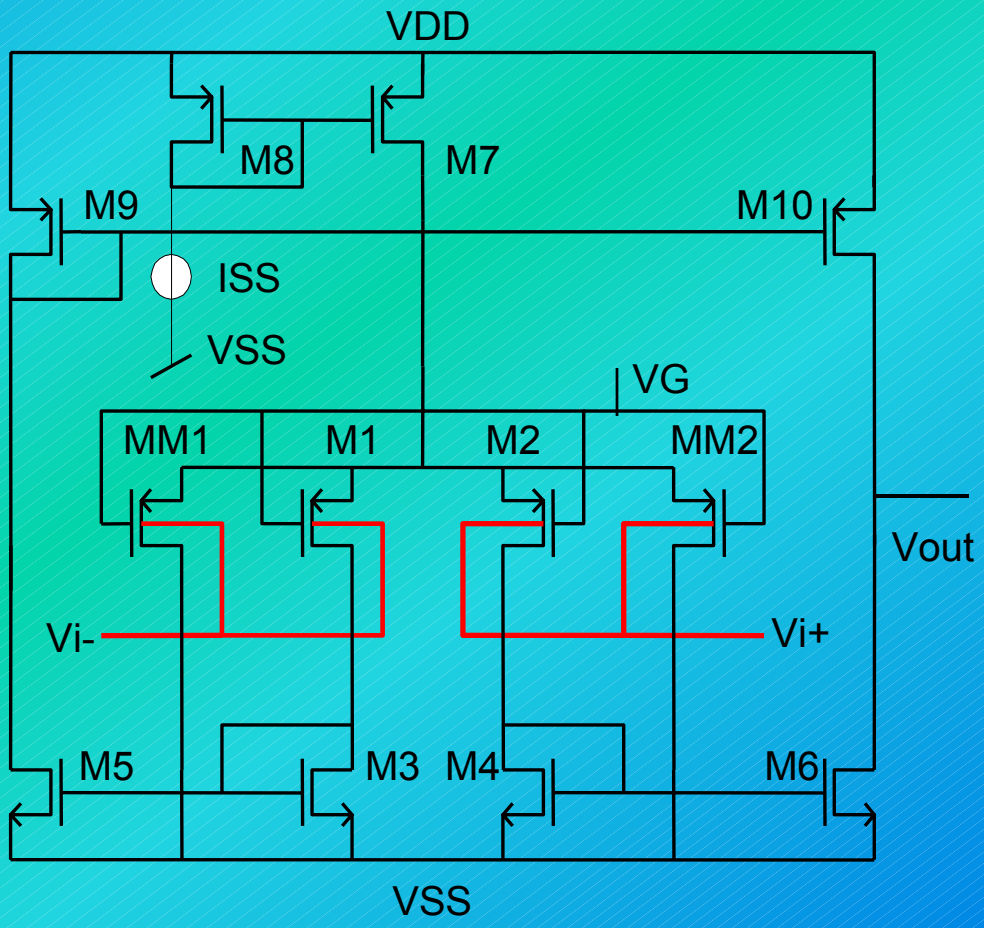
$$M = \frac{\left(\frac{W}{L}\right)_{MM}}{\left(\frac{W}{L}\right)_{M1}}$$

$$N = \frac{\left(\frac{W}{L}\right)_{MN}}{\left(\frac{W}{L}\right)_{M1}}$$

Floating Gate plus Current Division OTA

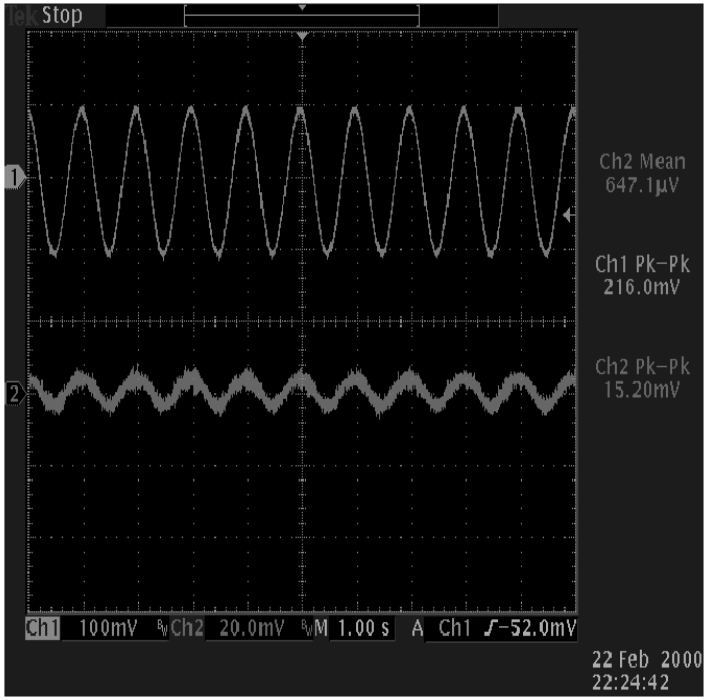


Bulk Driven plus Current Deviation OTA

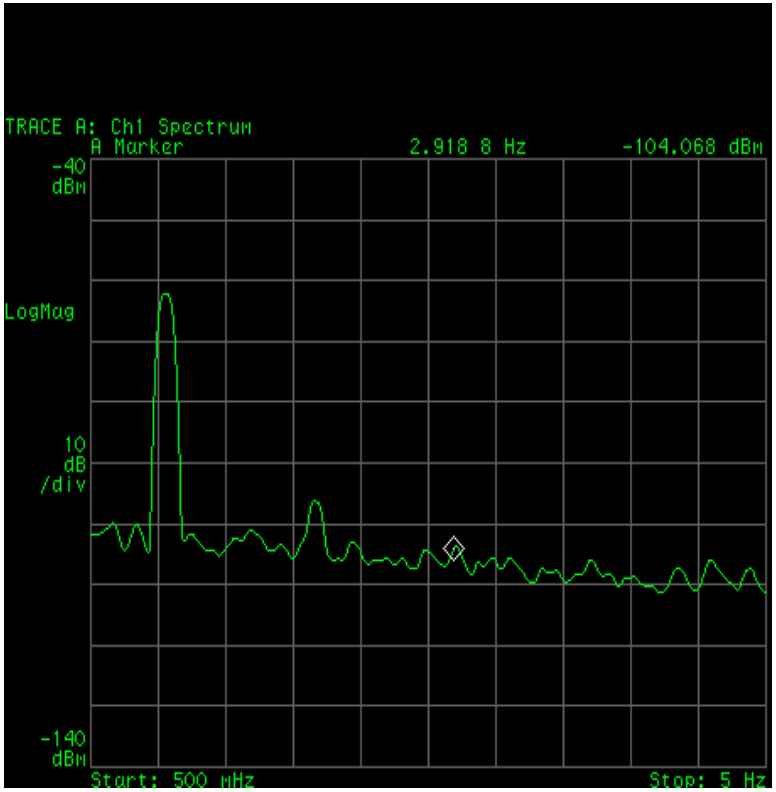


BULK DRIVEN OTA

EXPERIMENTAL RESULTS (0.5 um)



Input Ch1 214mVpp @ 1 Hz
Output Ch2 15.2mVpp



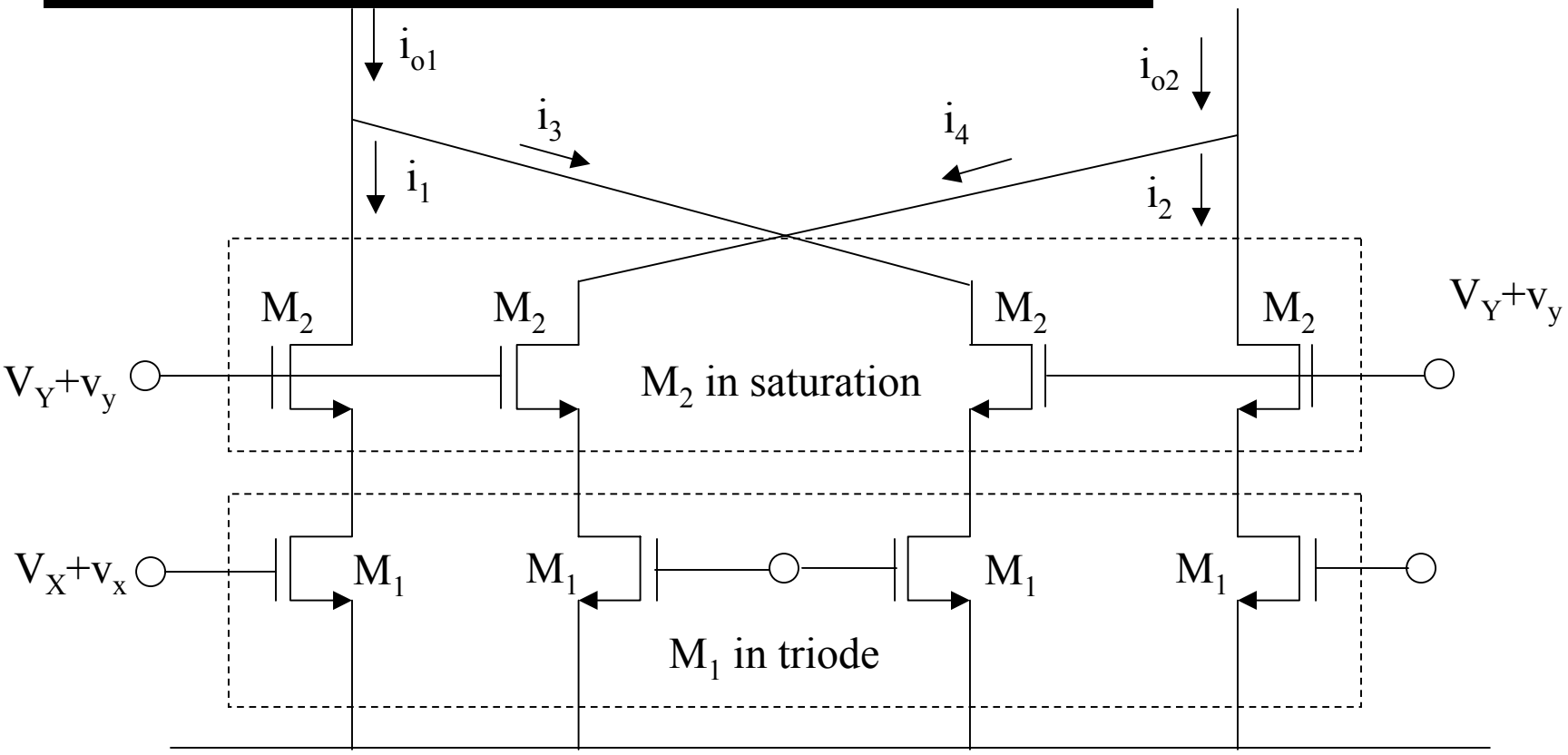
THD ~ -39dBm ~ 1.1% @214mVpp, 1Hz

EXPERIMENTAL RESULTS FOR THE DIFFERENT OTA DESIGNS

PARAMETER	REFERENCE	SD+CD	FG+CD	BD+CD
G_M (nA/V)	9.4	9.3	9.2	9.4
HD_3(%)	0.9@162mV+pp	1.0@242mV_{pp}	1.1@330mV_{pp}	0.9@900mV_{pp}
Input noise (μVrms)	18.1	26.1	39.1	104.7
SNR@1%HD_3(dB)	69.9	70.3	69.5	69.6
I_{BIAS}(nA)	2.6	120	232	560

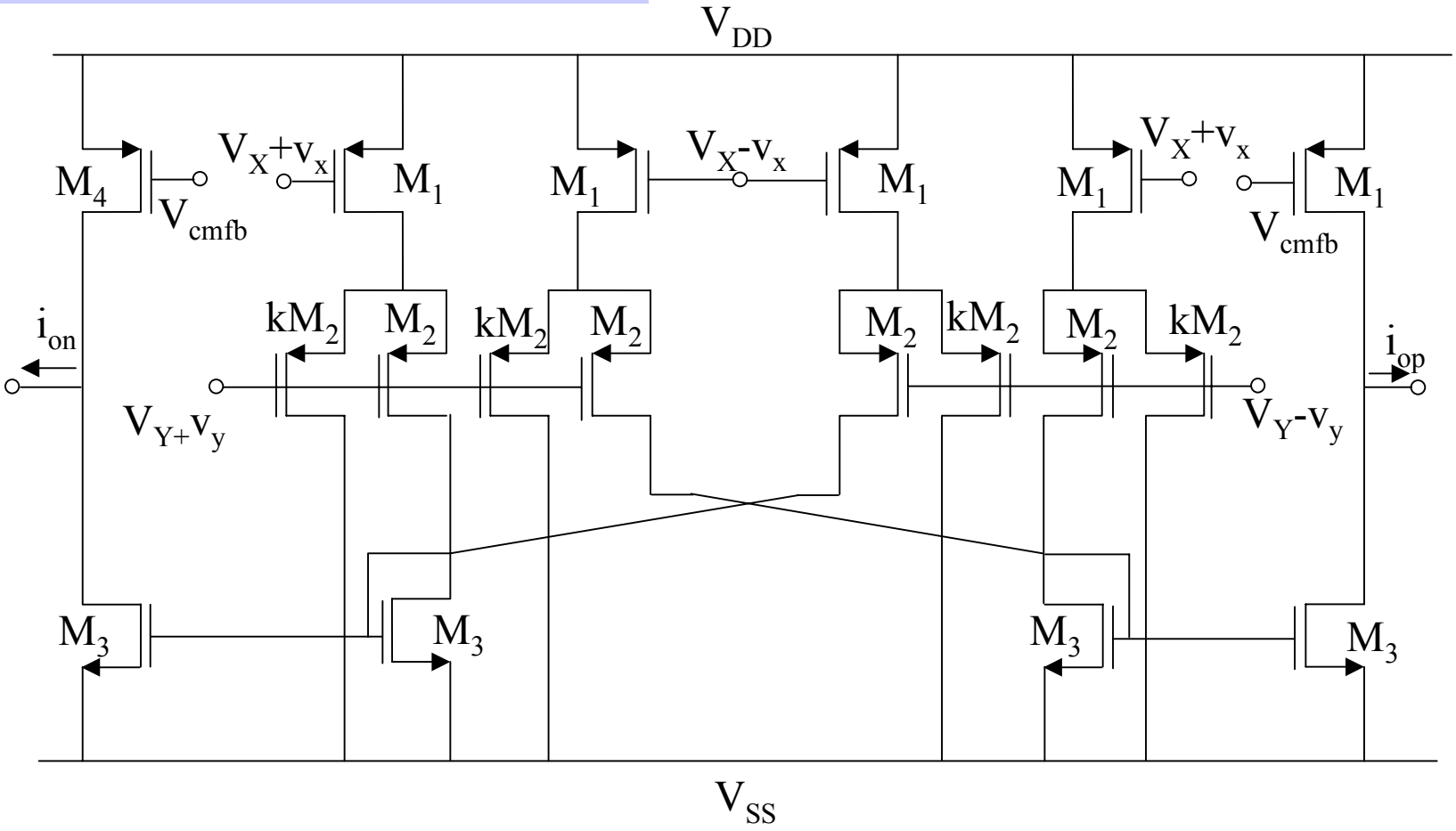
Key:
SD source degeneration
CD current division
FG floating gate
BD bulk driven

How to make a transconductor with a wide Gm tuning range?



Basic topology of the four-quadrant multiplier

Multiplier-based OTA with CD



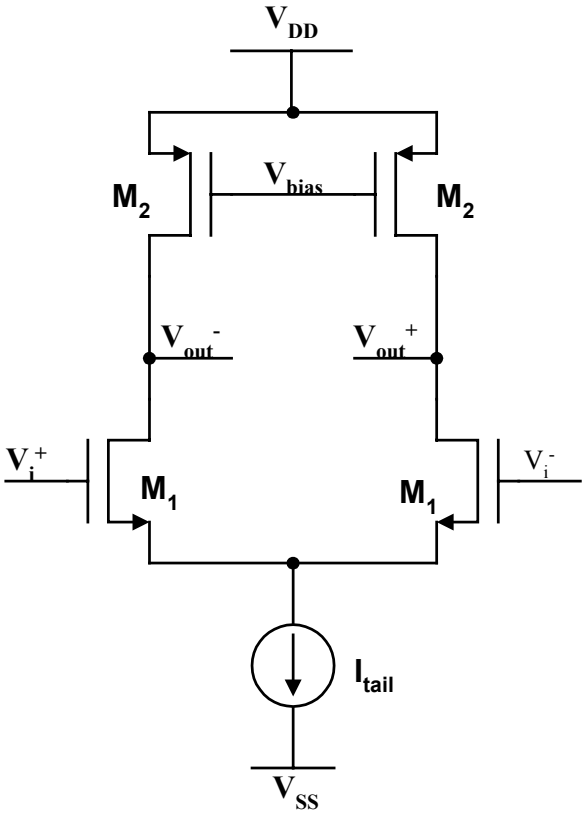
$$G_{Md}(v_x) \equiv \frac{i_{od}}{2v_y} = \left[\left(\frac{4\mu C_{ox} W}{L} \right)_{M_1} \left(\frac{1}{k+1} \right) \right] v_x$$

Fully Differential and Pseudo Differential OTAs

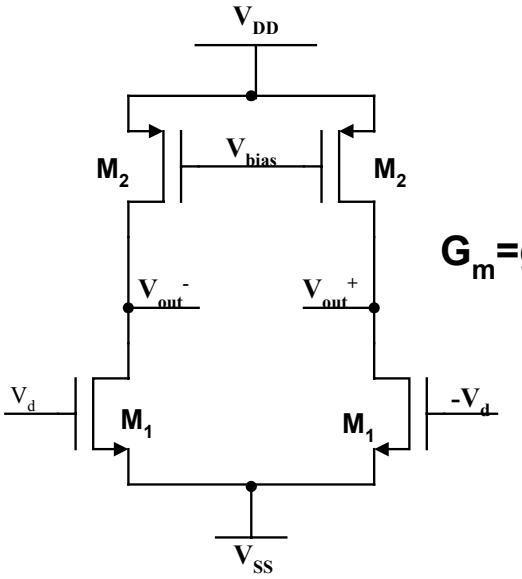
Common - Mode Feedforward and
Feedback strategies needed for
differential output filters

Fully Differential OTA Characteristics

Simple Differential OTA
With tail Current Source

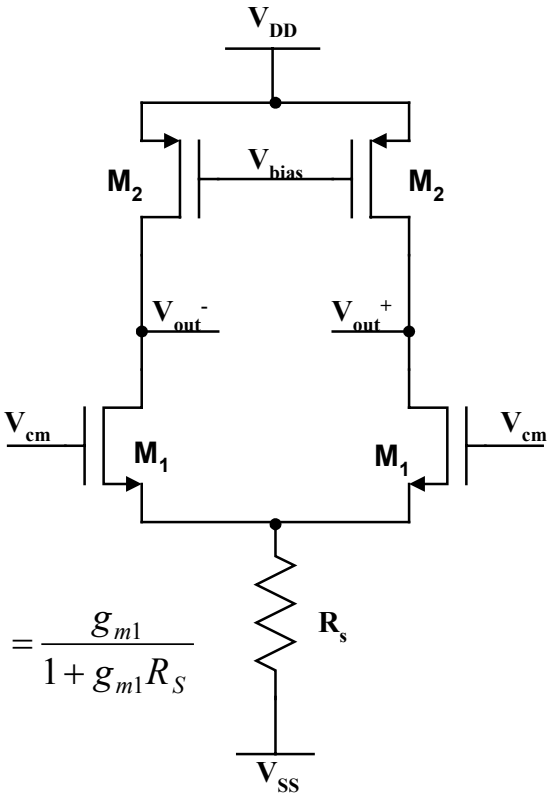


Differential-Mode



$G_m = g_{m1}$

Common-Mode

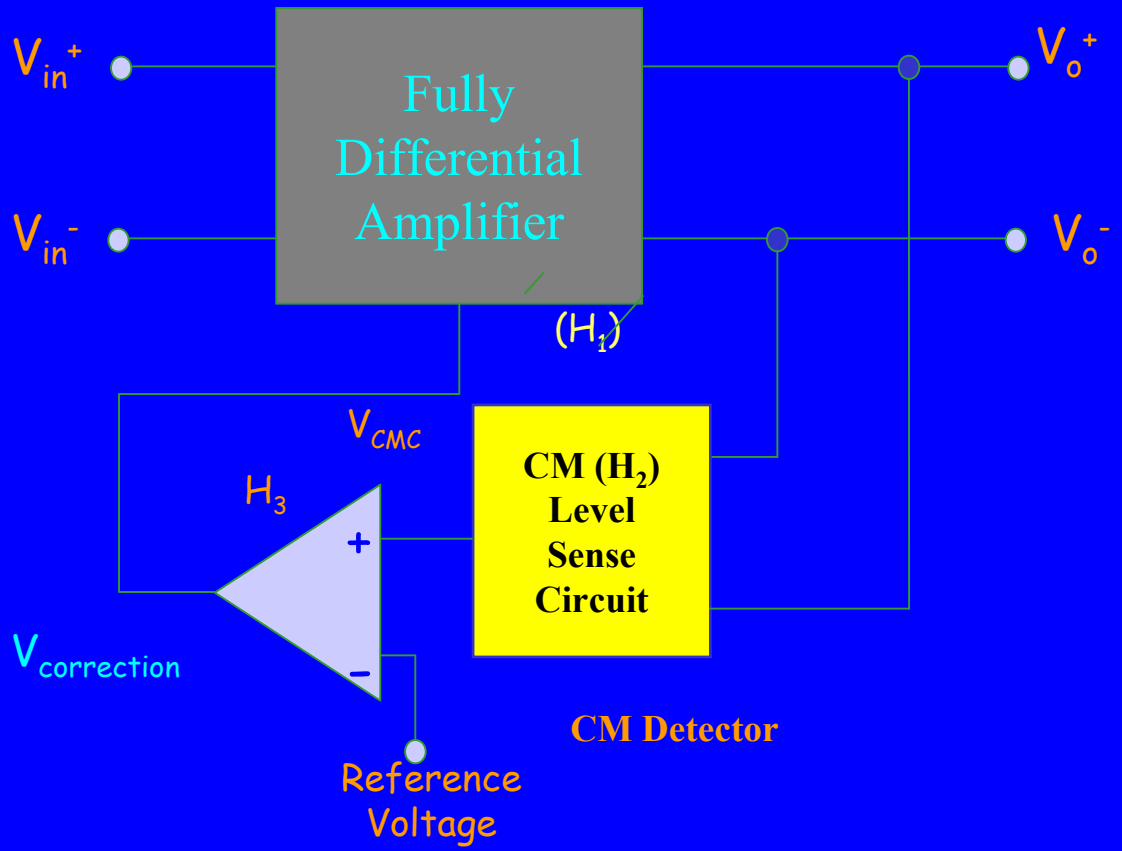


$$G_m = \frac{g_{m1}}{1 + g_{m1} R_S}$$

✗ Limited linear input range
✗ Limited tuning range

✓ Reasonable Common-mode gain
✓ Reasonable PSRR

Conceptual Architecture of Common-Mode Feedback Loop



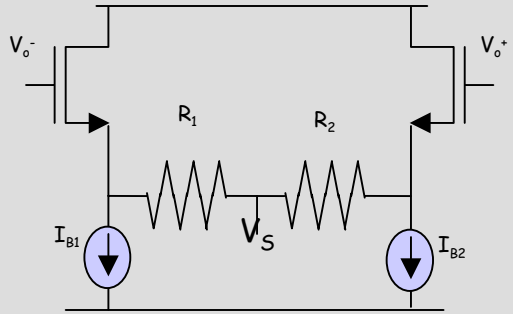
CM signal detectors : two conventional cases

$$V_S = \alpha_1 v_{o,cm} + \alpha_2 v_{o,dm} + \alpha_3 v^2_{o,dm}$$

Performance

Observations

CM Detector



$$\alpha_1 = 1$$

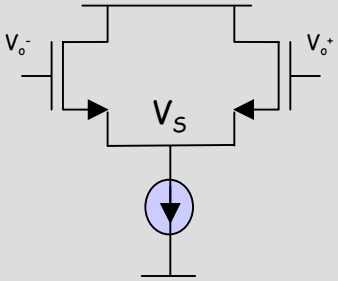
$$\alpha_2 = \frac{\Delta R}{4R} + \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\frac{\Delta R}{2R} + \frac{\Delta I_B}{4I_B} + \frac{\Delta\beta}{4\beta}}{2R + \sqrt{\frac{2}{\beta I_B}}}$$

$$+ \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\Delta V_T + \frac{\Delta I_B}{2I_B}\sqrt{\frac{2I_B}{\beta}}}{I_B\left(2R + \sqrt{\frac{2}{\beta I_B}}\right)^2}$$

$$\alpha_3 = \frac{1}{2I_B} \cdot \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{1}{\left(2R + \sqrt{\frac{2}{\beta I_B}}\right)^2}$$

- High DC offset due to source followers
- Other buffers can be used to reduce the DC offset
- Mismatching between the passive resistors is the dominant error in α_2
- Highly non-linear CM signal detector

CM Detector



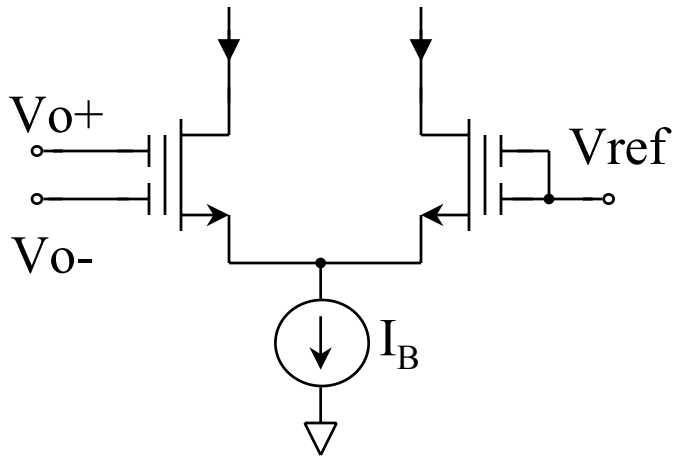
$$\alpha_1 = 1$$

$$\alpha_2 = \frac{\Delta\beta}{4\beta} + \frac{\Delta V_T}{4} \cdot \sqrt{\frac{\beta}{I_B}}$$

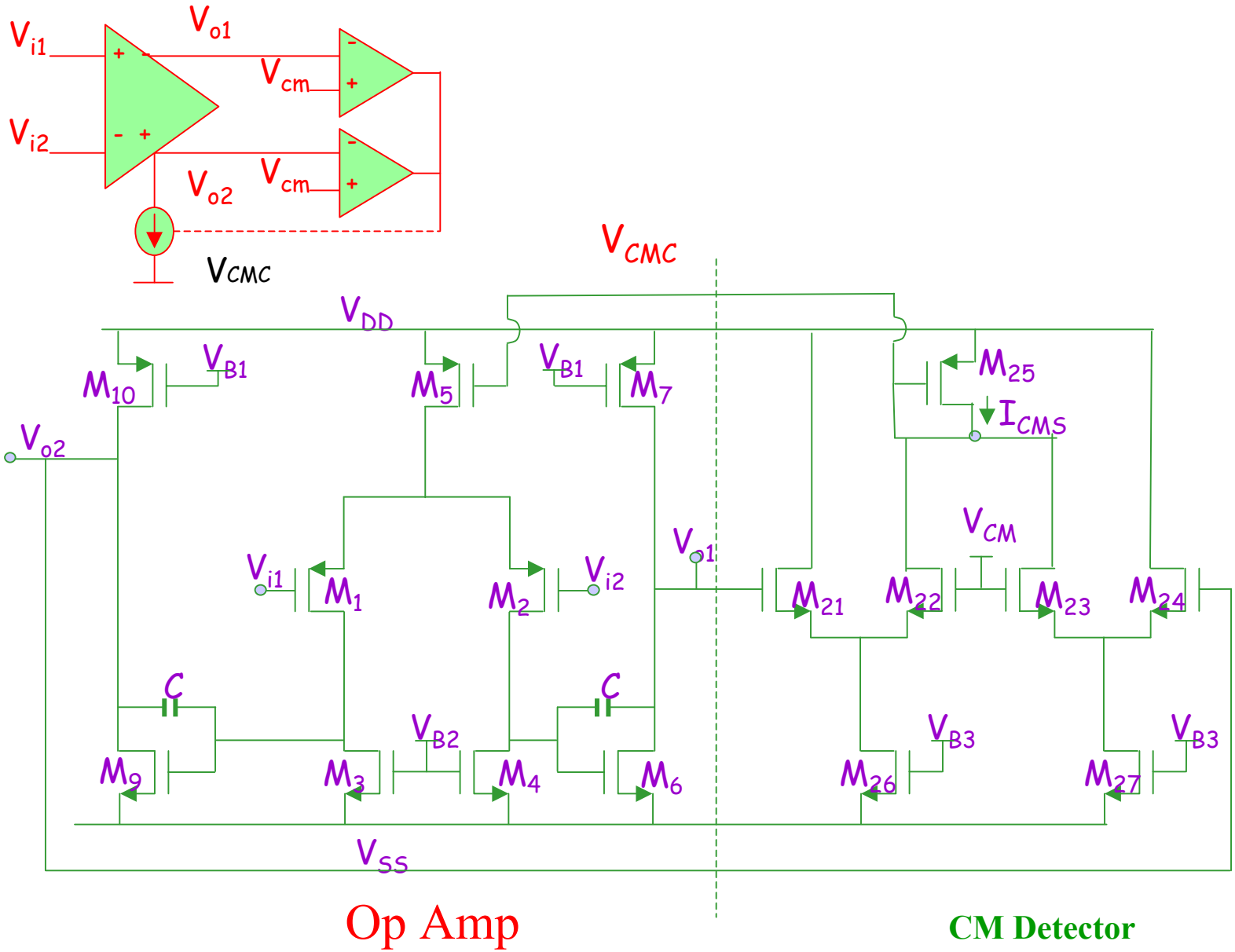
$$\alpha_3 = \frac{1}{8}\sqrt{\frac{\beta}{I_B}}$$

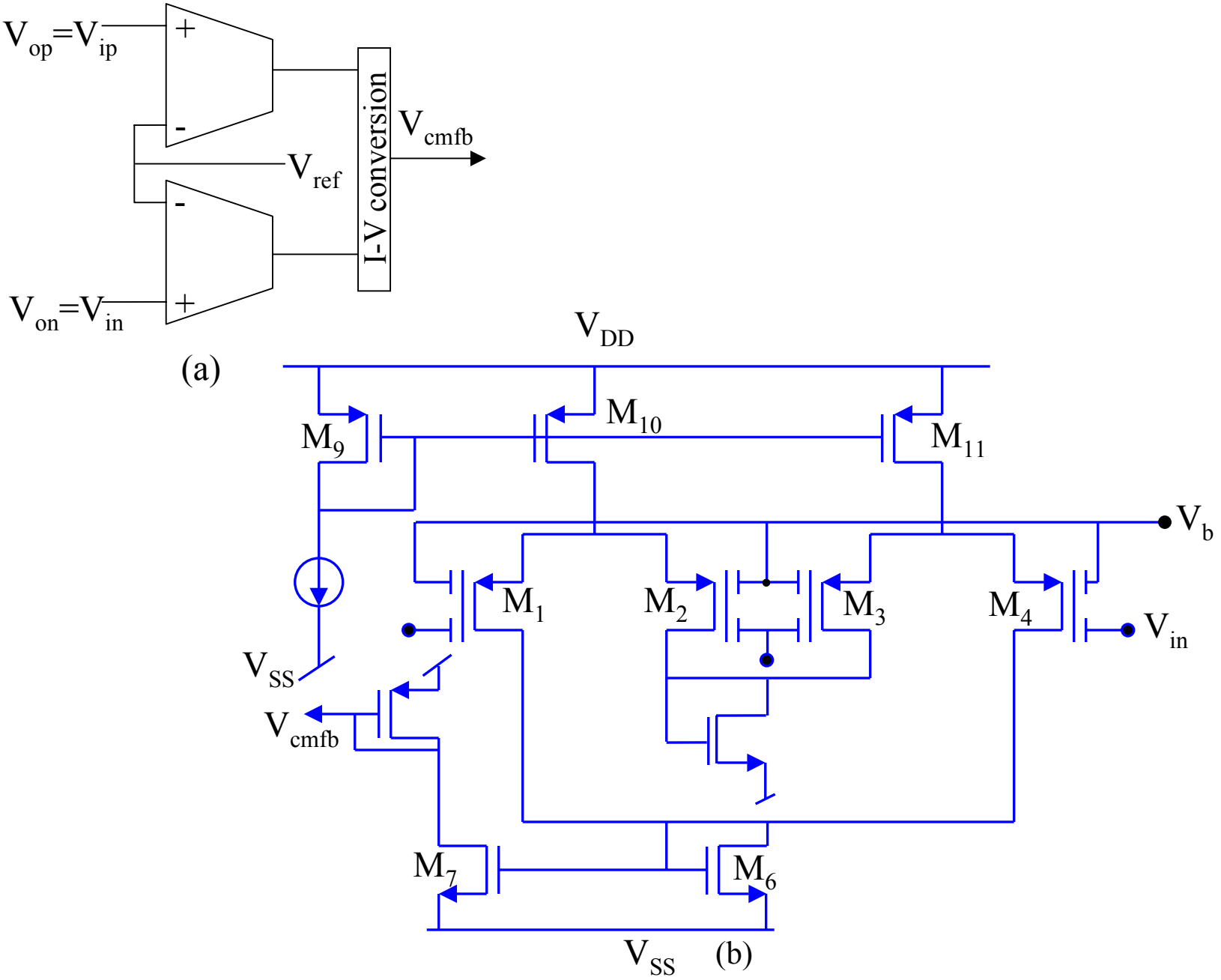
J.F. Duque-Carrillo, " Control of the Common-Mode Component in CMOS Continuous-Time Fully Differential Signal Processing, Analog Integrated and Signal Processing,Vol. 4, No.2, pp131-140, Sept. 1993

Floating Gate Non-conventional Differential Pair for common mode detection



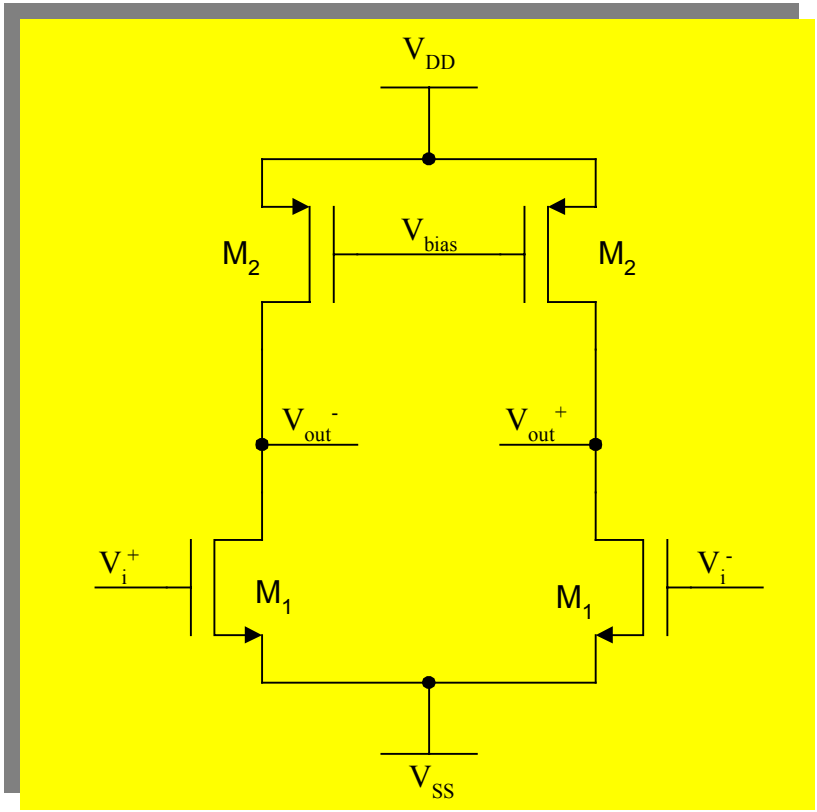
Example of a compensated Op Amp and a CM sense circuit





Common-mode feedback circuit. (a) Block diagram. (b) Circuit using floating gates.

Pseudo Differential Transconductance



Simple Pseudo Differential OTA

❑ Advantages

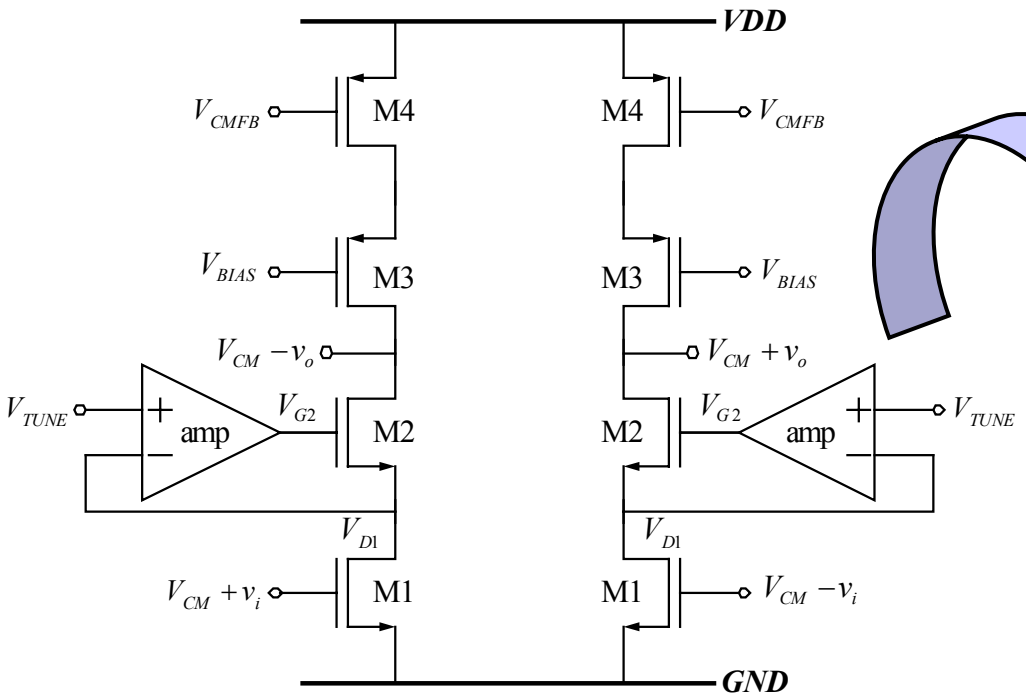
- ✓ Suitability for low voltage
- ✓ Wider common-mode input range

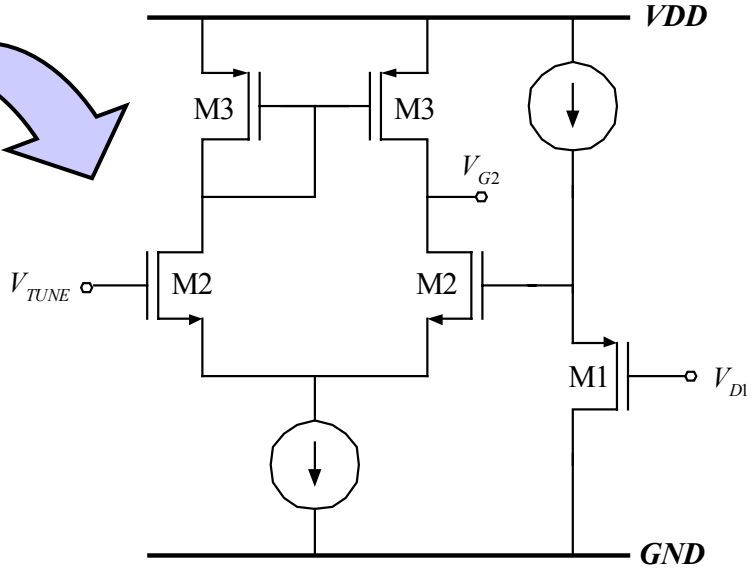
❑ Disadvantages

- ✗ Poor common-mode gain

  $A_{CM}=A_{DM}>>1$
- ✗ Poor PSRR
- ✗ Low output impedance
- ✗ Need for fast and strong Extra CMFB Circuit to
  (1) Fix output common-mode voltage
  (2) Suppress common-mode signals

Pseudo-Differential OTA with large output impedance



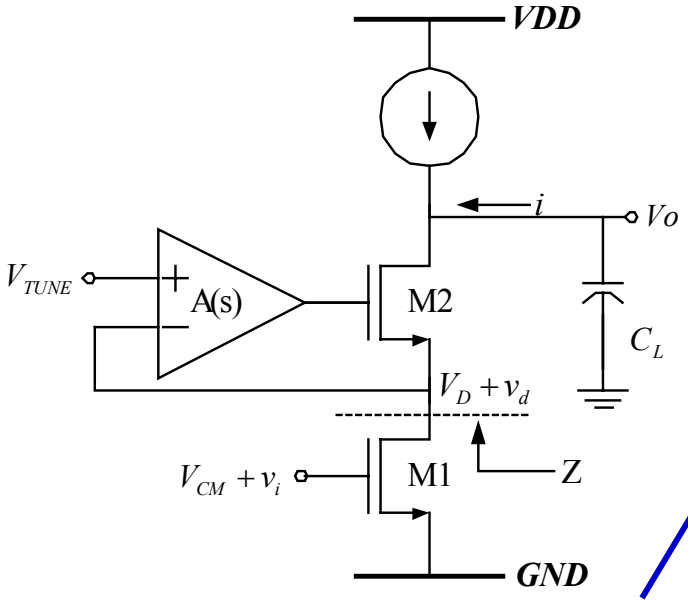


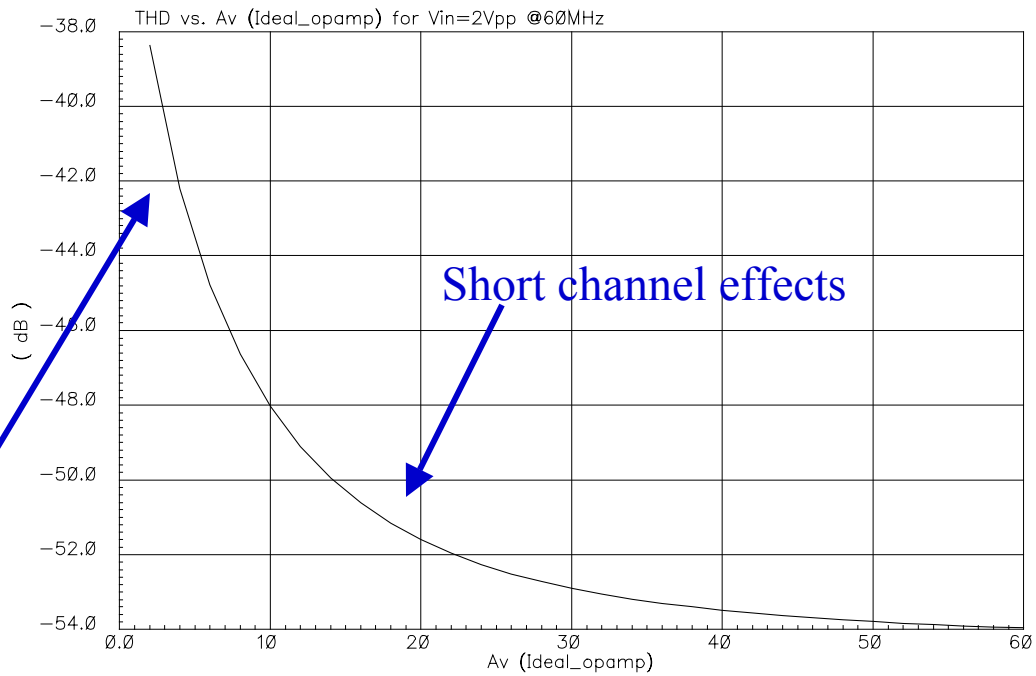
Pseudo-differential OTA

RGC amplifier "amp"

- Transistors M1 operate in Linear region: Wide linear range; Large tuning range;
- RGC loop: Fix V_{DS1} ➡ provides better linearity.

OTA Design Issues: RGC Loop



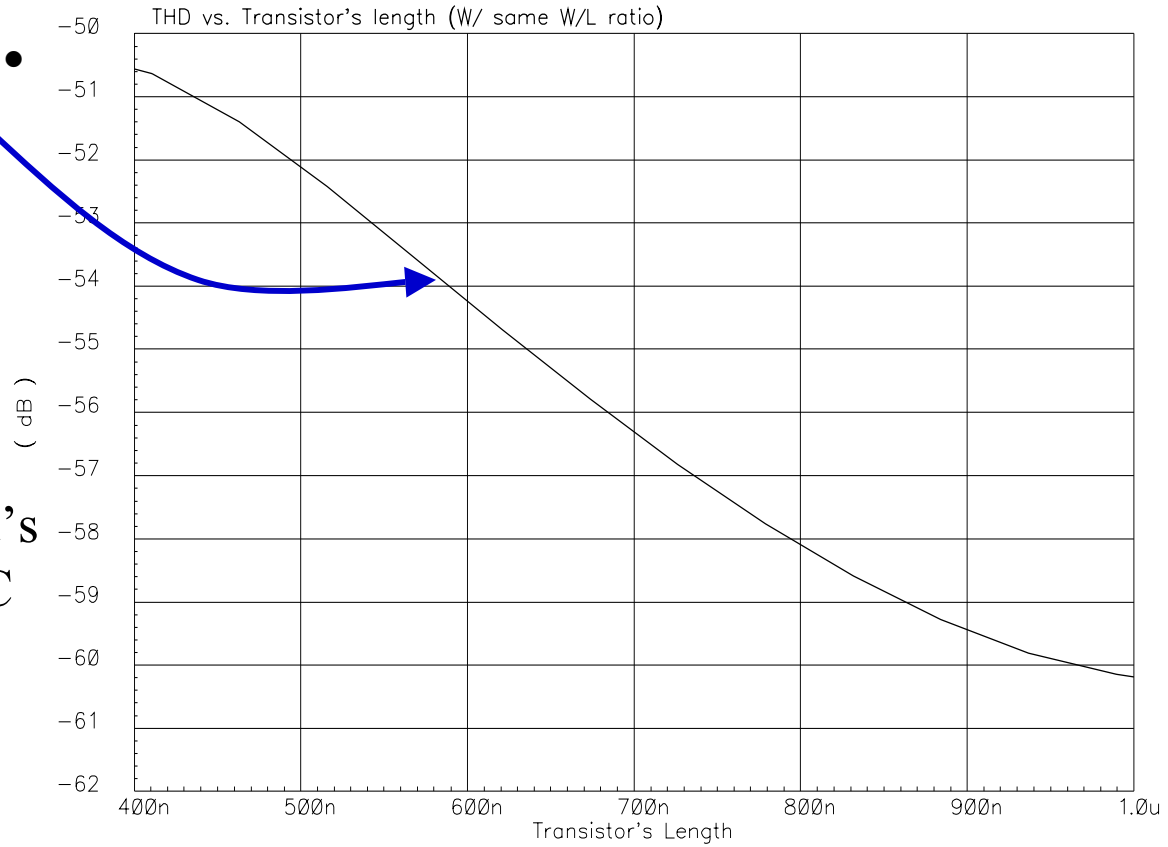


$$HD3 \approx \frac{V_i^2}{4} \cdot \frac{\beta^2}{[A(s)g_{m2} + \beta(V_{CM} - V_{TN} - V_D)]^2}$$

☛ OTA Gm's Linearity: Limited by how well the drain voltage of the input transistor is fixed.

Design Issues: Short-Channel Effects

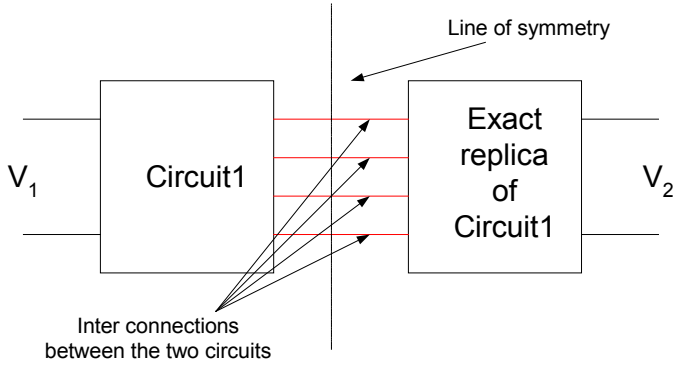
$$\mu_{eff} = \mu_0 \left(\frac{1}{1+\theta(V_{GS}+v_{gs}-V_T)} \right) \bullet \left(\frac{1}{1+\frac{1}{L\varepsilon_c}\cdot(V_{DS}+v_{ds})} \right)$$



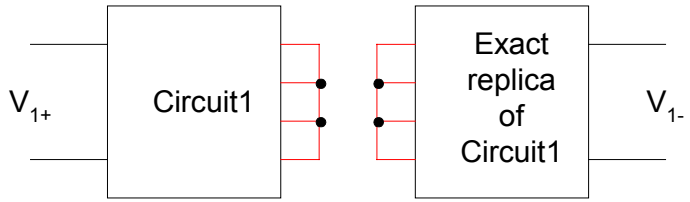
- Transversal electric field's effect is reduced by RGC loop;
- Trade-off:

THD vs. Frequency response

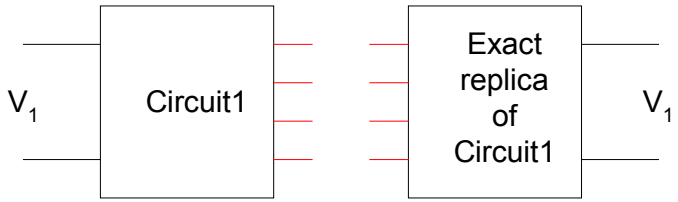
Behavior of symmetric circuits



An example of fully symmetric circuit

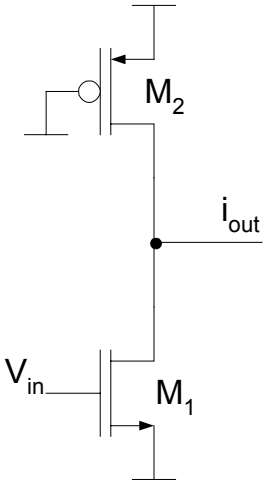


Equivalent circuit for fully differential input

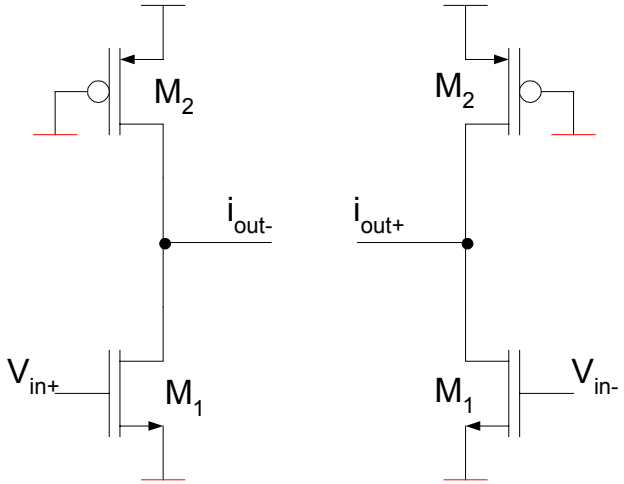


Equivalent circuit for common mode input

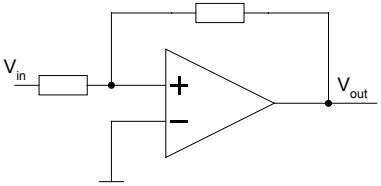
Derivation of CMFF Pseudo-differential **OTA**

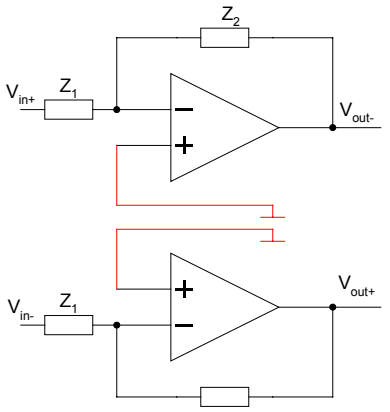


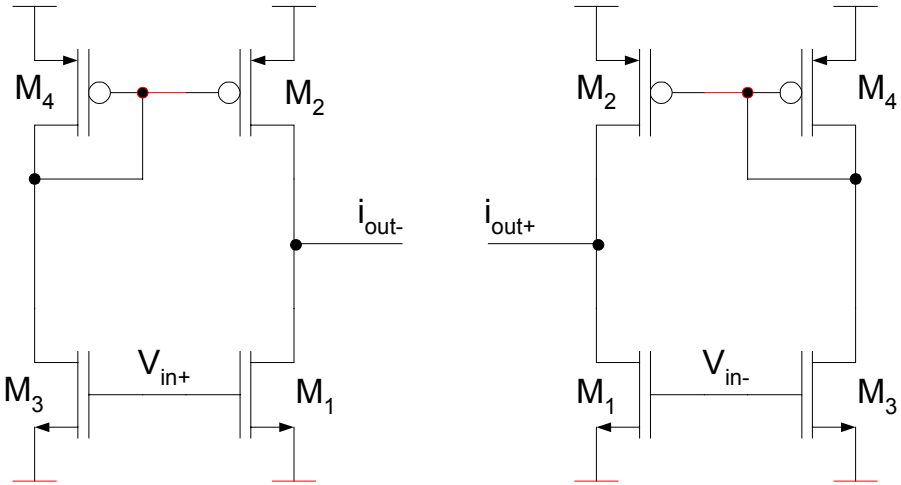
Single ended OTA circuit



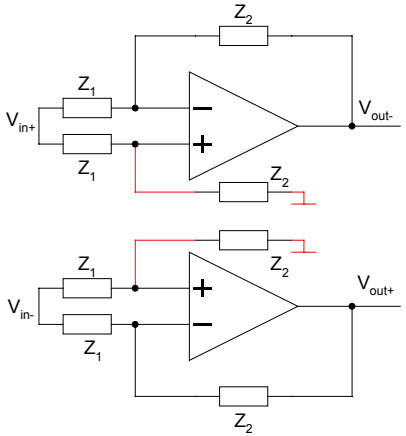
Circuit of OTA for differential input



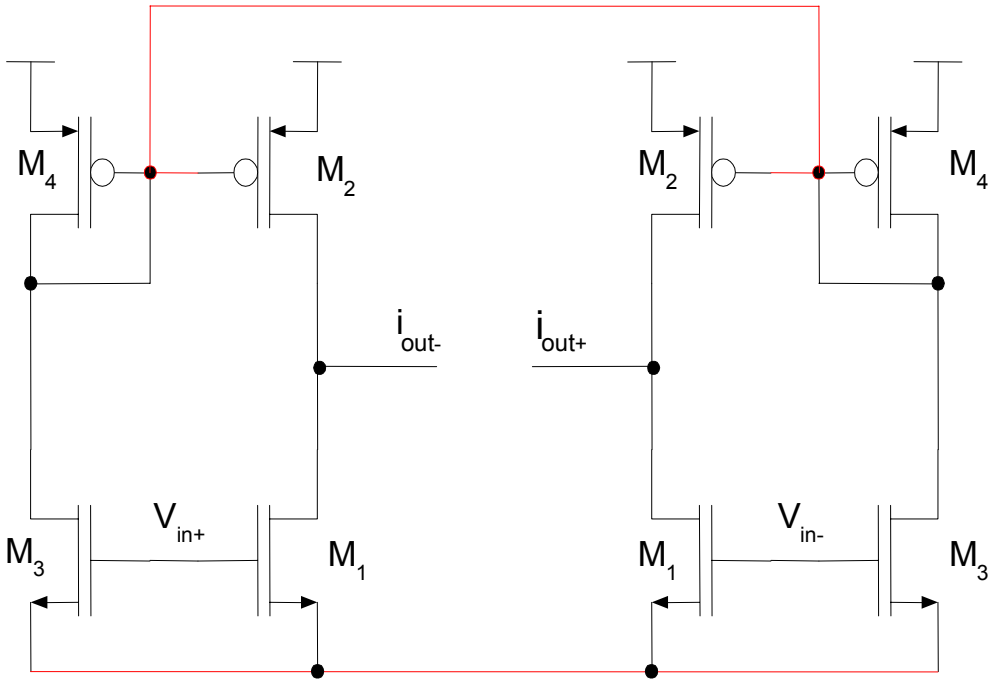


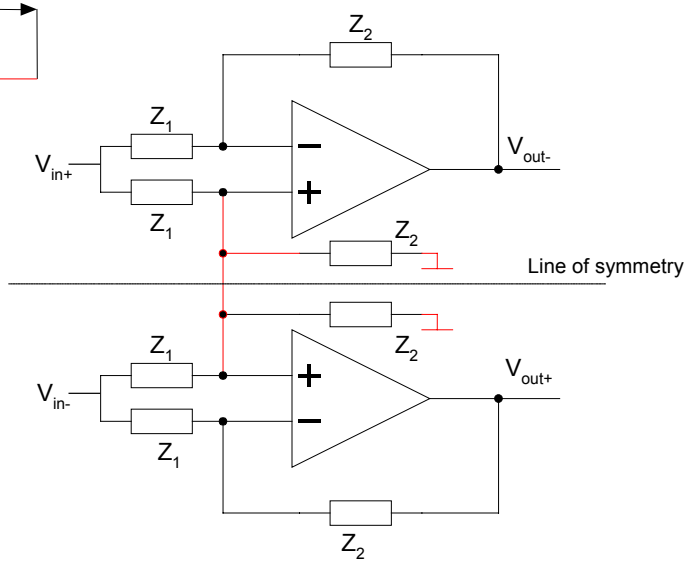


Circuit of OTA for common mode signals

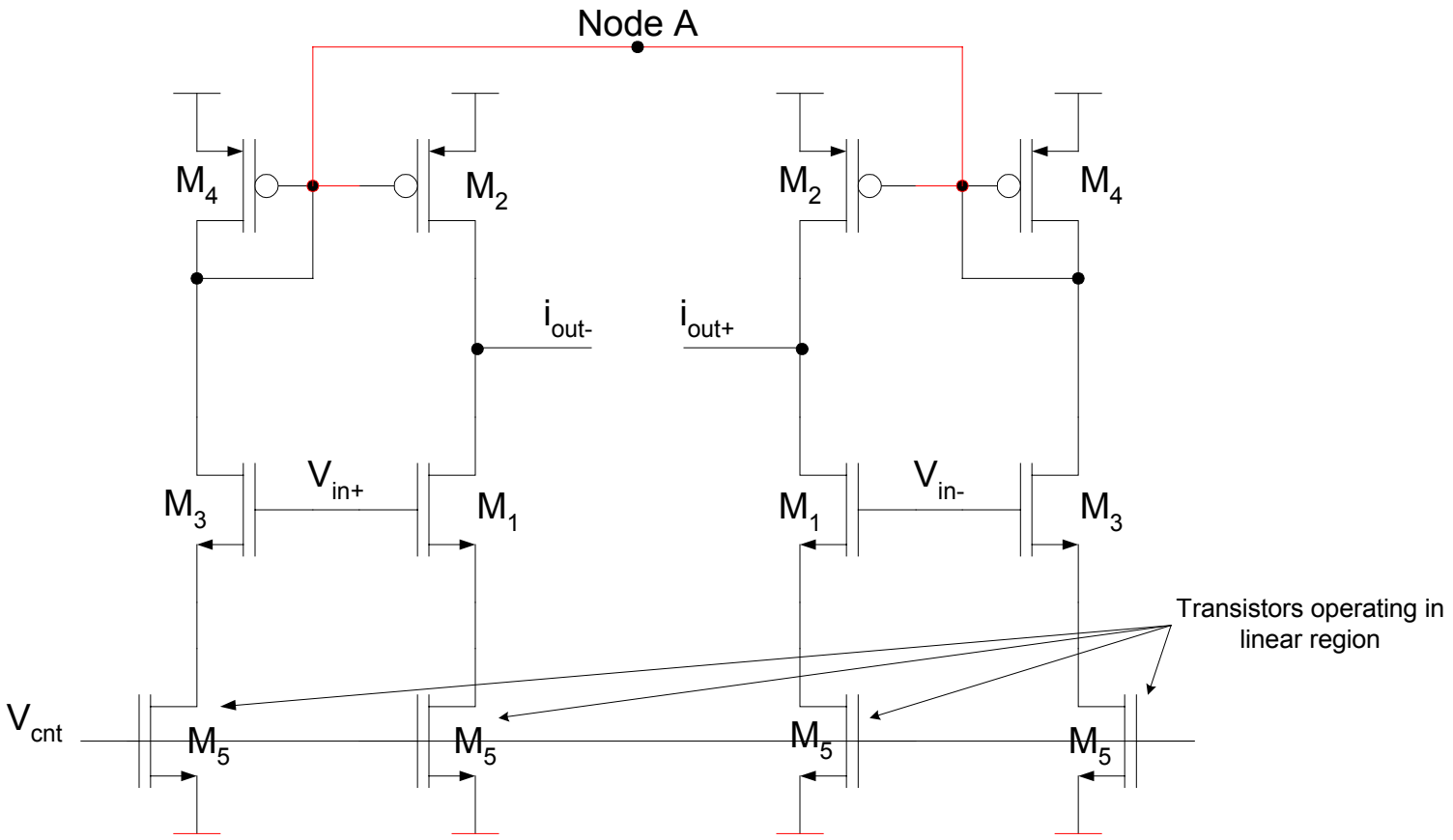


Fully-balanced, fully-symmetric **CMFF** OTA





OTA with improved performance



Fully-balanced, fully-symmetric, pseudo differential CMFF OTA

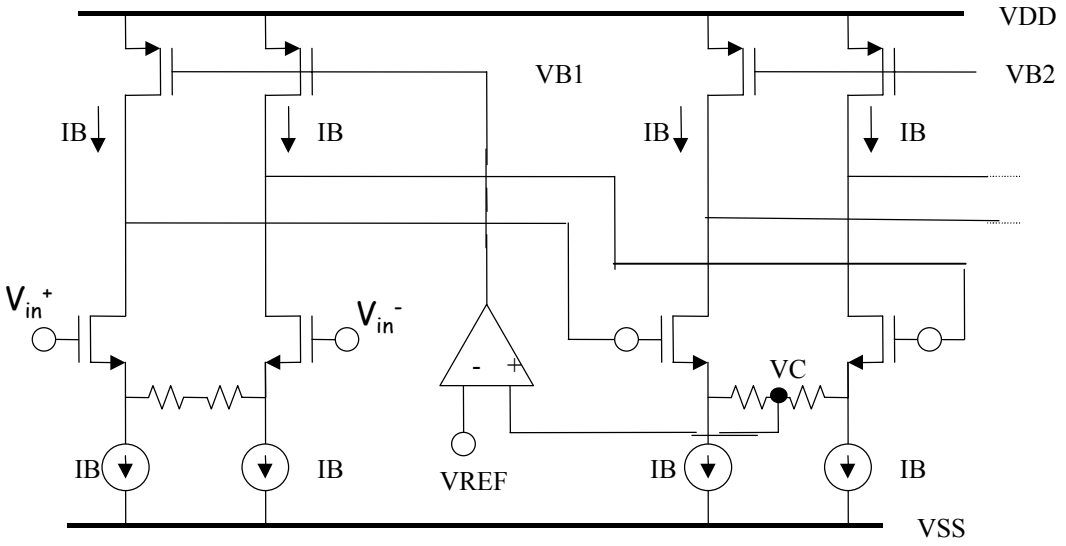
What are the Solutions to

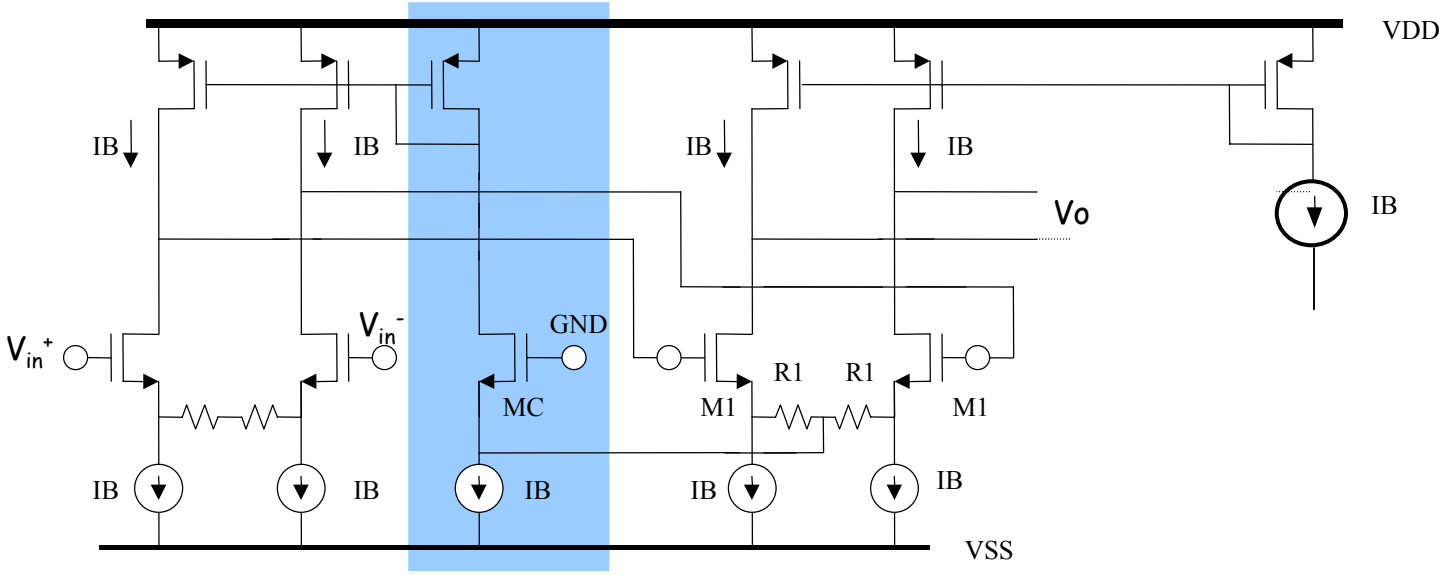
Overcome those Limitations?

CMFB FOR OTAS: Solution 1

Typical OTA connection in pseudo- differential OTA-C based circuits.

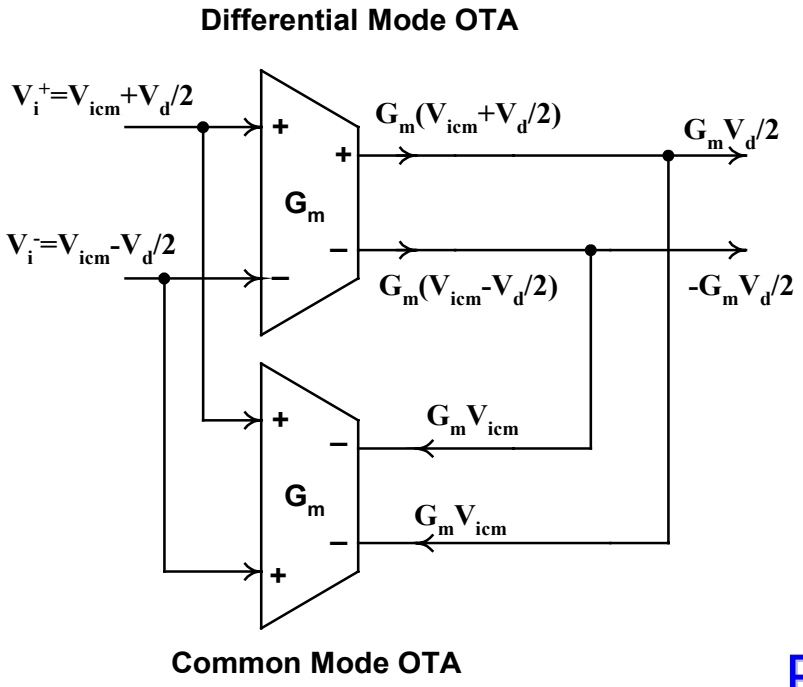
The common-mode voltage is obtained from the input of the following stage. Poor PSRR

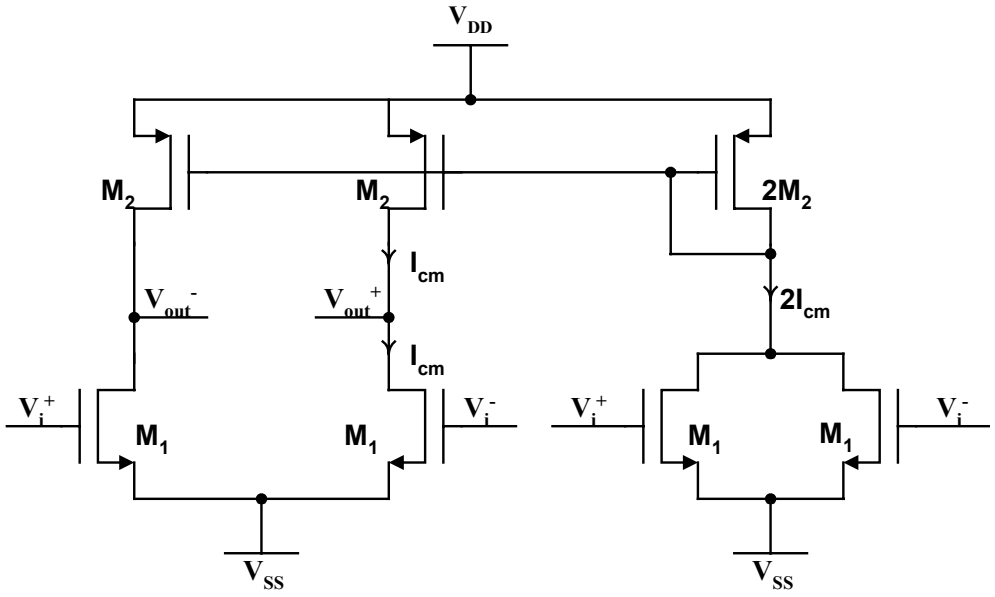




Pseudo-differential OTAs including the CMFB for the first one with good PSRR

A PD Solution 2 In the Literature

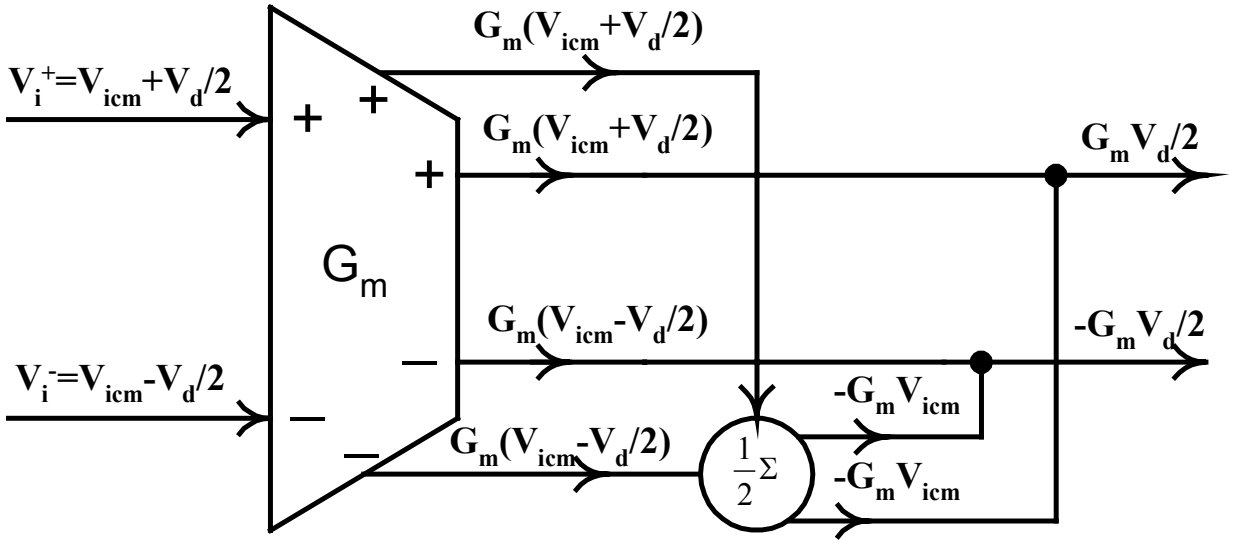




Pseudo differential OTA With CMFF

- ✓ CMFF is applied to cancel the common mode input signal
- ✗ Add load to the driving stage, input capacitance doubles
- ✗ CMFB is still needed

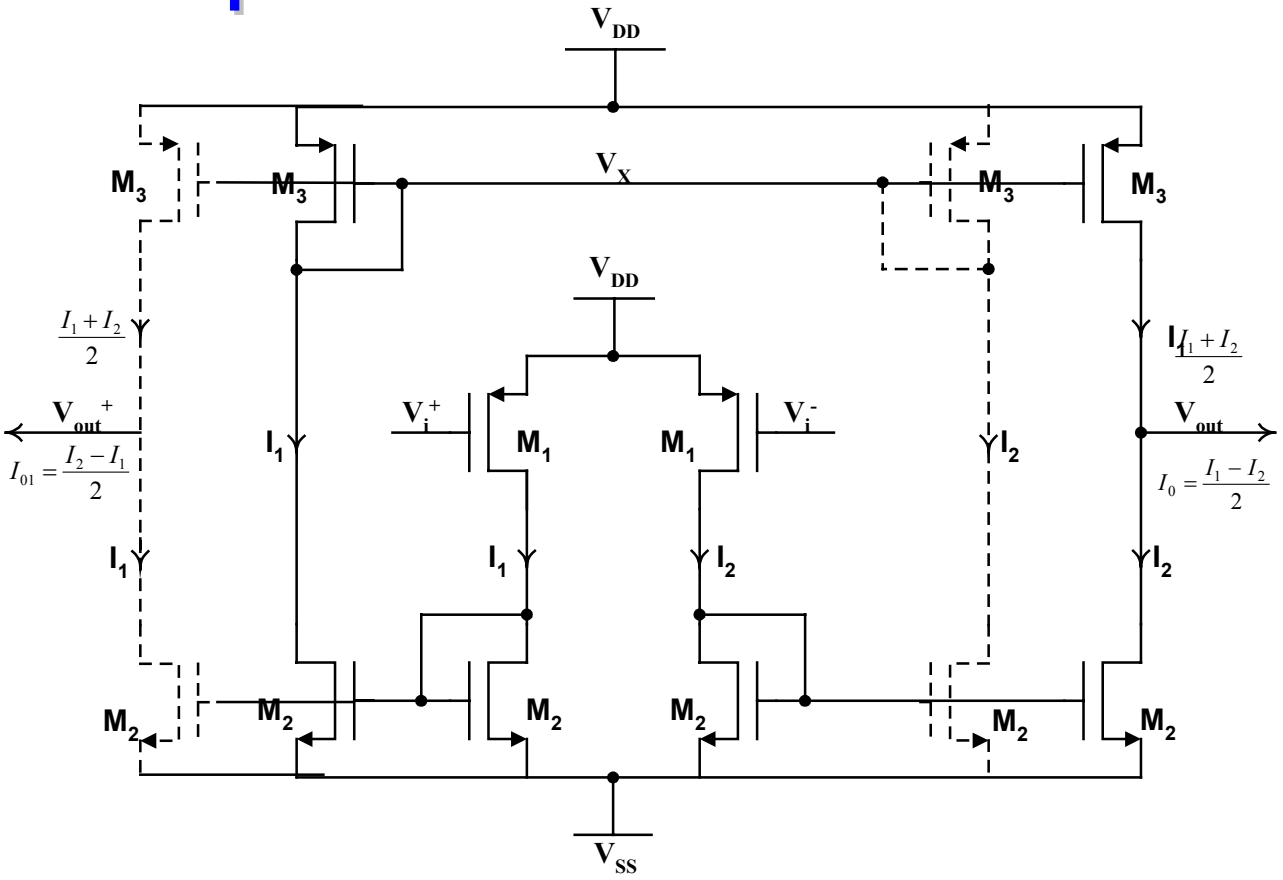
Proposed OTA Block Diagram (solution 3)



- Common-mode detection using the same differential transconductance by making copies of the current
- ✓ Input capacitance is not increased
- ✓ CMFF is inherently achieved
- ✓ CMFB can be easily arranged

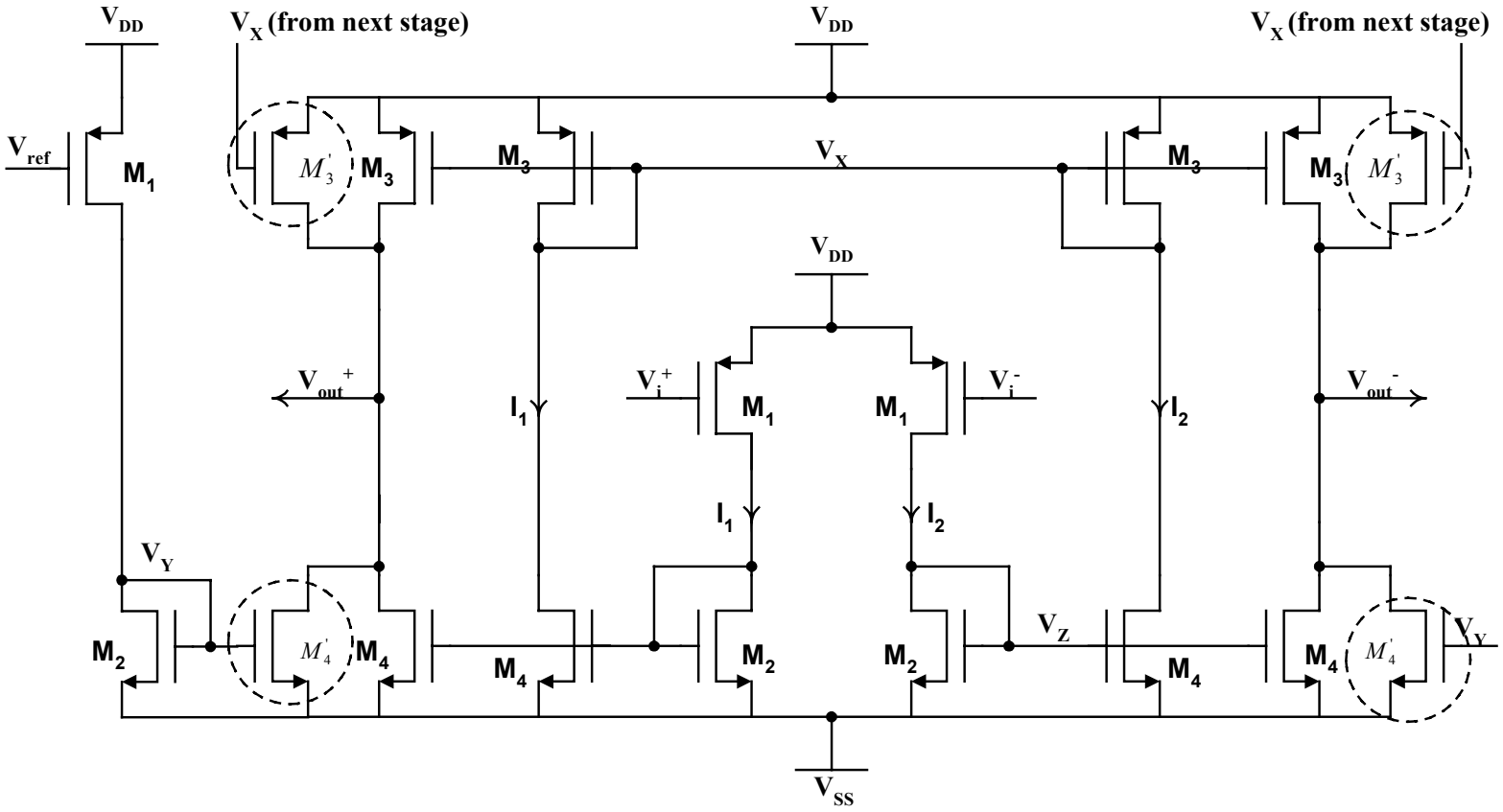
How to Implement the Proposed OTA?

Proposed OTA Architecture



- Inherent common-mode detection
- Inherent common-mode Feedforward

Combine CMFB and CMFF



- CMFB is arranged exploiting the direct connection of the OTAs
- Avoid using a separate common-mode detector
- Differential-mode signals and common-mode signals share basically the same loop

Small Signal Analysis

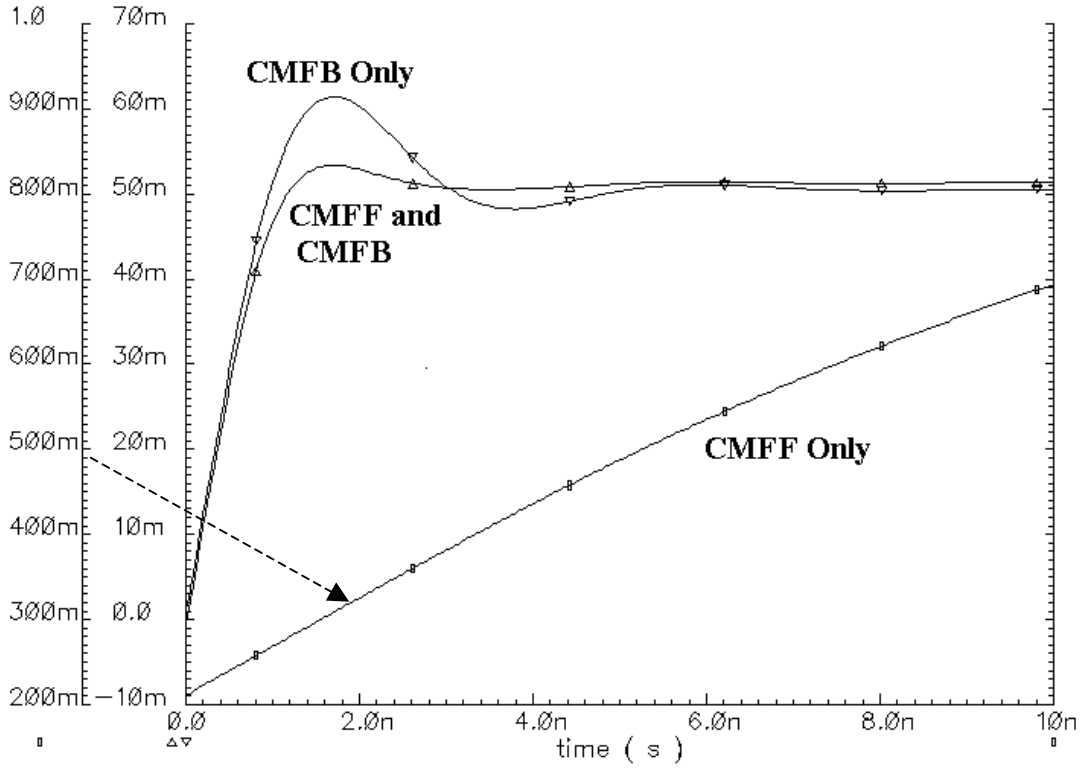
- The path from the differential signal to the ouput encounters one pole
- The other path is a common-mode path

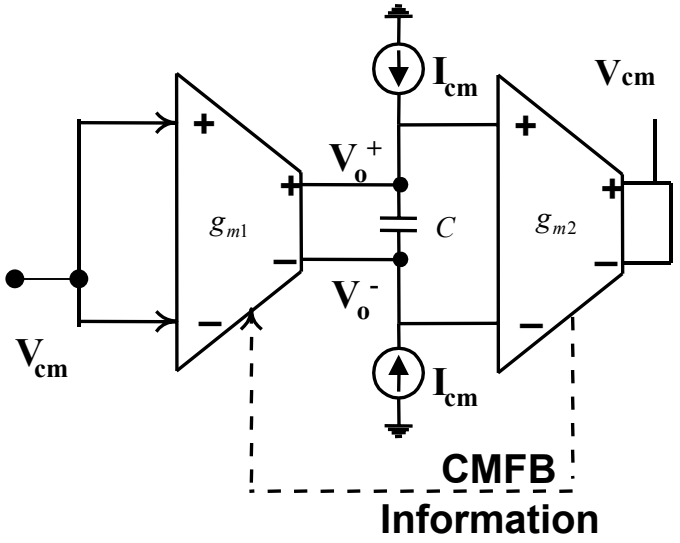
$$g_m(s) = \frac{i_{od}}{v_d} \cong g_{m1} \frac{g_{m2}}{g_{m2} + sC_Z} = \frac{g_{m1}}{1 + s/\omega_{nd}} \qquad \omega_{nd} = \frac{g_{m2}}{C_Z}$$

$$\Delta\phi \cong -\tan^{-1}\left(\omega/\omega_{nd1}\right)$$

$$\min V_{DD} = \max\left\{\left(V_{TN} + V_{ov1} + V_{ov2} + V_{peak}\right), \left(\left|V_{TP}\right| + V_{ov3} + V_{ov4}\right)\right\}$$

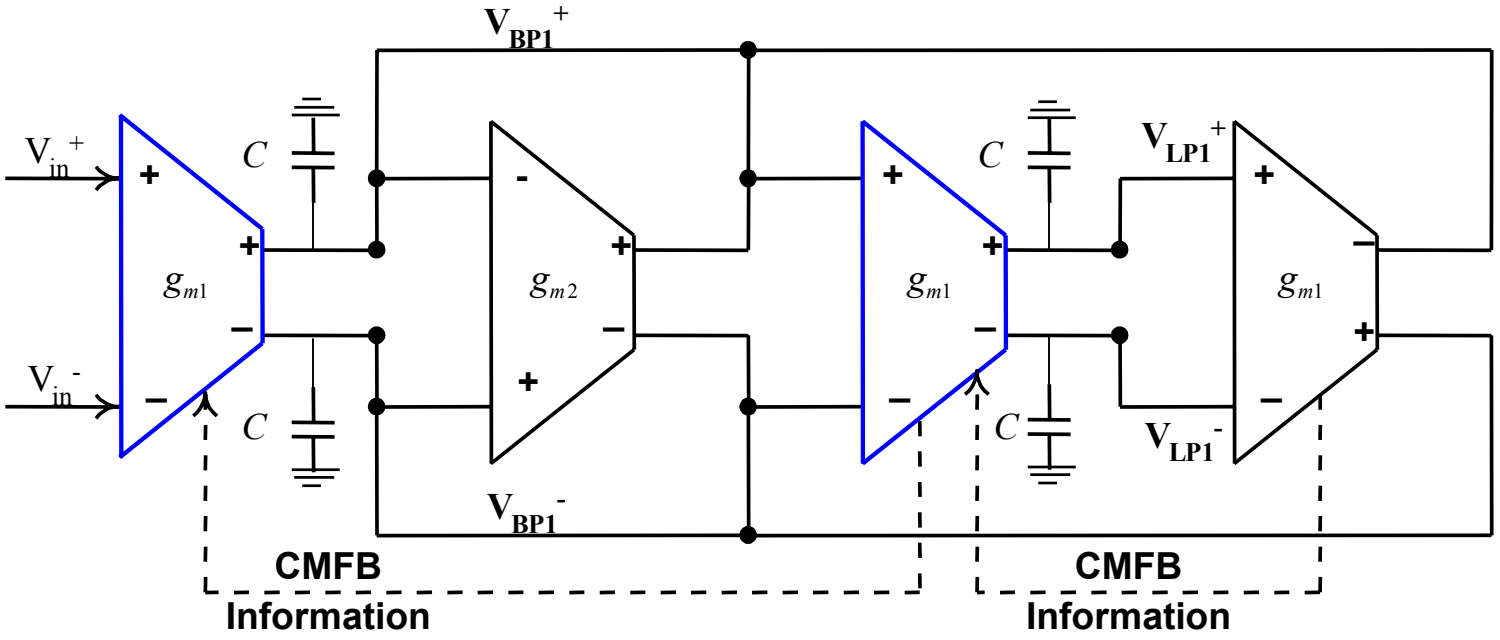
Simulation Results





Output voltage applying common-mode current step (I_{cm})

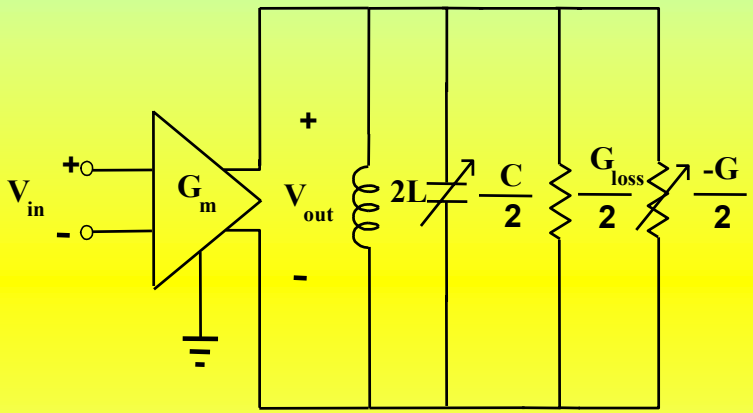
How to use OTAs as CM Detector?



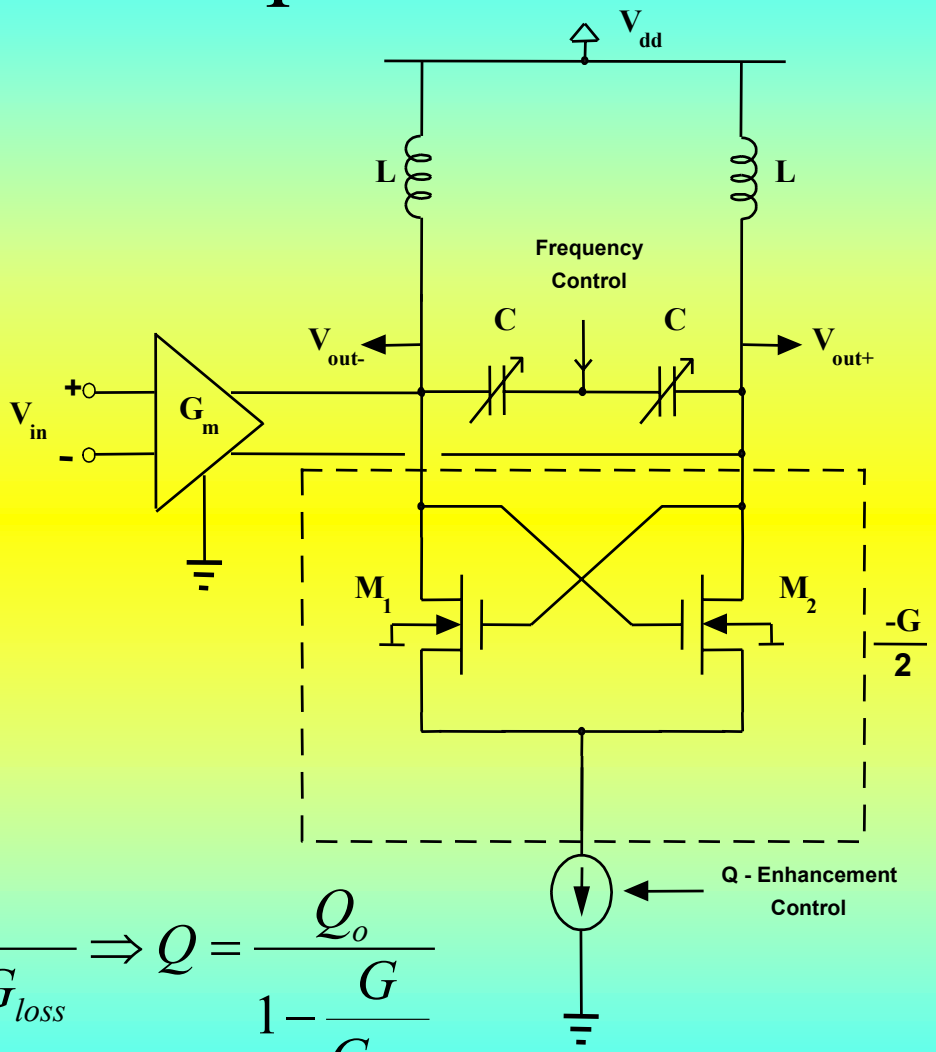
- A 2nd Order Filter is used as an example
- Exploit direct connection of the cascaded OTAs in the filter
- Differential OTA used as CM detector also

How to design filters operating in microwave frequencies ?

Q-Enhancement Bandpass Filters



(a)



(b)

$$Q_o \equiv \frac{1}{\omega_o L G_{loss}} \Rightarrow Q = \frac{Q_o}{1 - \frac{G}{G_{loss}}}$$

$$(G_{loss} > G \quad for\ stability)$$

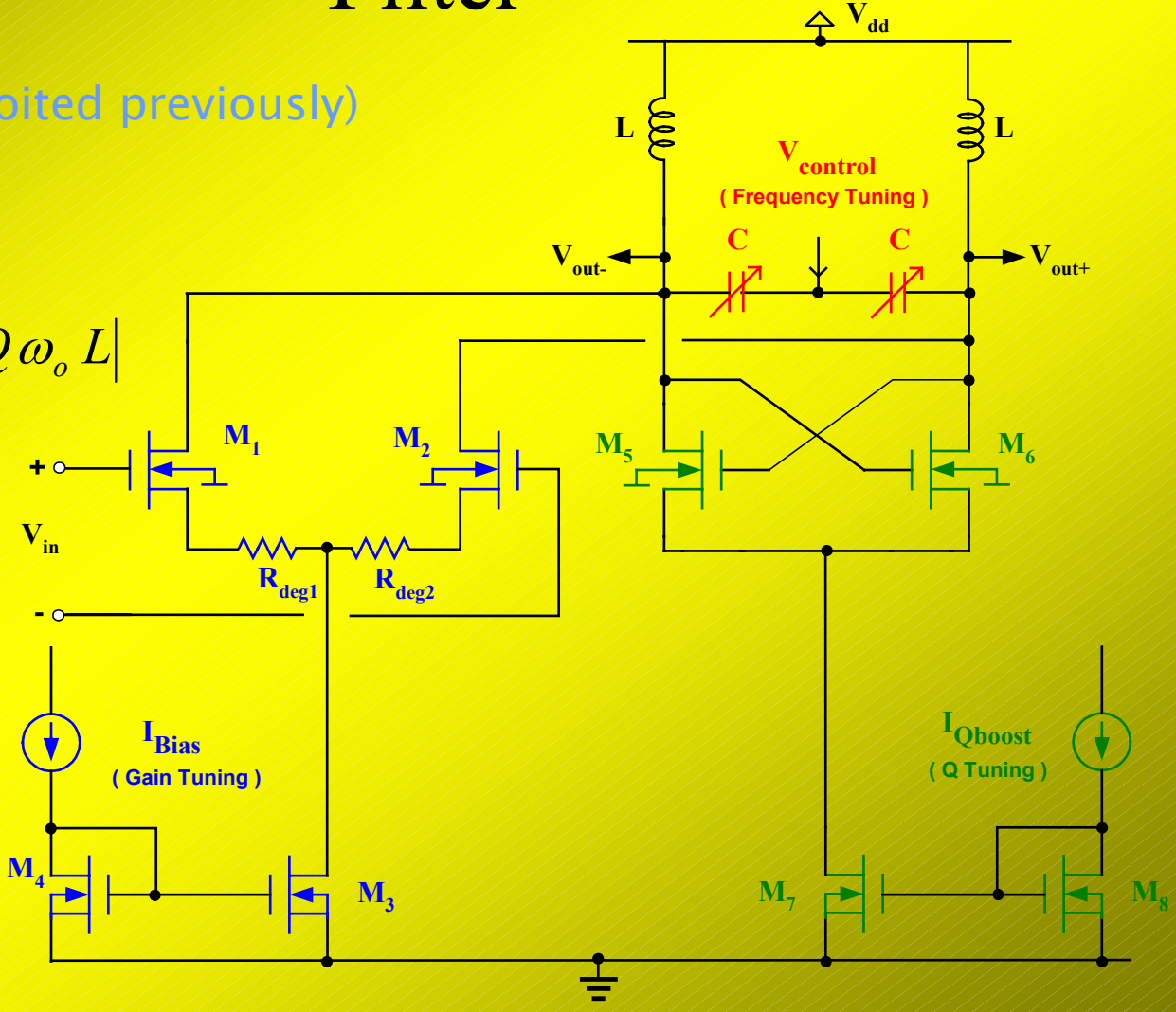
A CMOS Programmable RF Bandpass Filter

Programmable in:

- Peak Gain (not exploited previously)
- Filter Q
- Center Frequency

$$\left|H(j\omega_o)\right| \cong \left|G_m(j\omega_o) Q \omega_o L\right|$$

$$\omega_o \cong \frac{1}{\sqrt{LC}}$$



A CMOS Programmable Bandpass Filter

- The peak gain programmability through the input G_m stage.

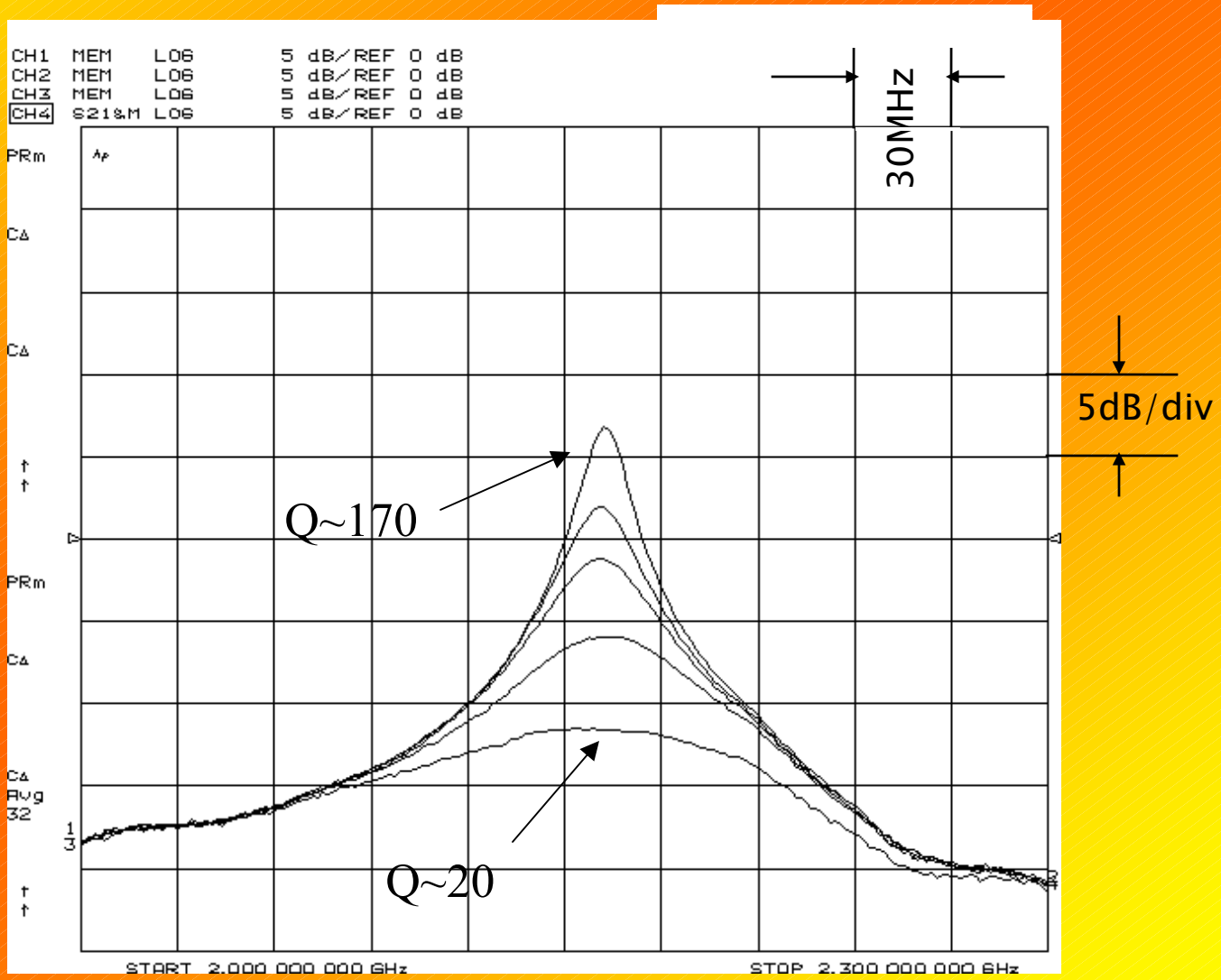
$$\left|H(j\omega_o)\right| \cong \left|\frac{G_m(j\omega_o)}{G_{loss}-G}\right| = \left|G_m(j\omega_o)\,Q\,\omega_o\,L\right|$$

- Increasing Q also increases the peak gain.

- If ω_o and Q are fixed, the peak gain can be modified through G_m.

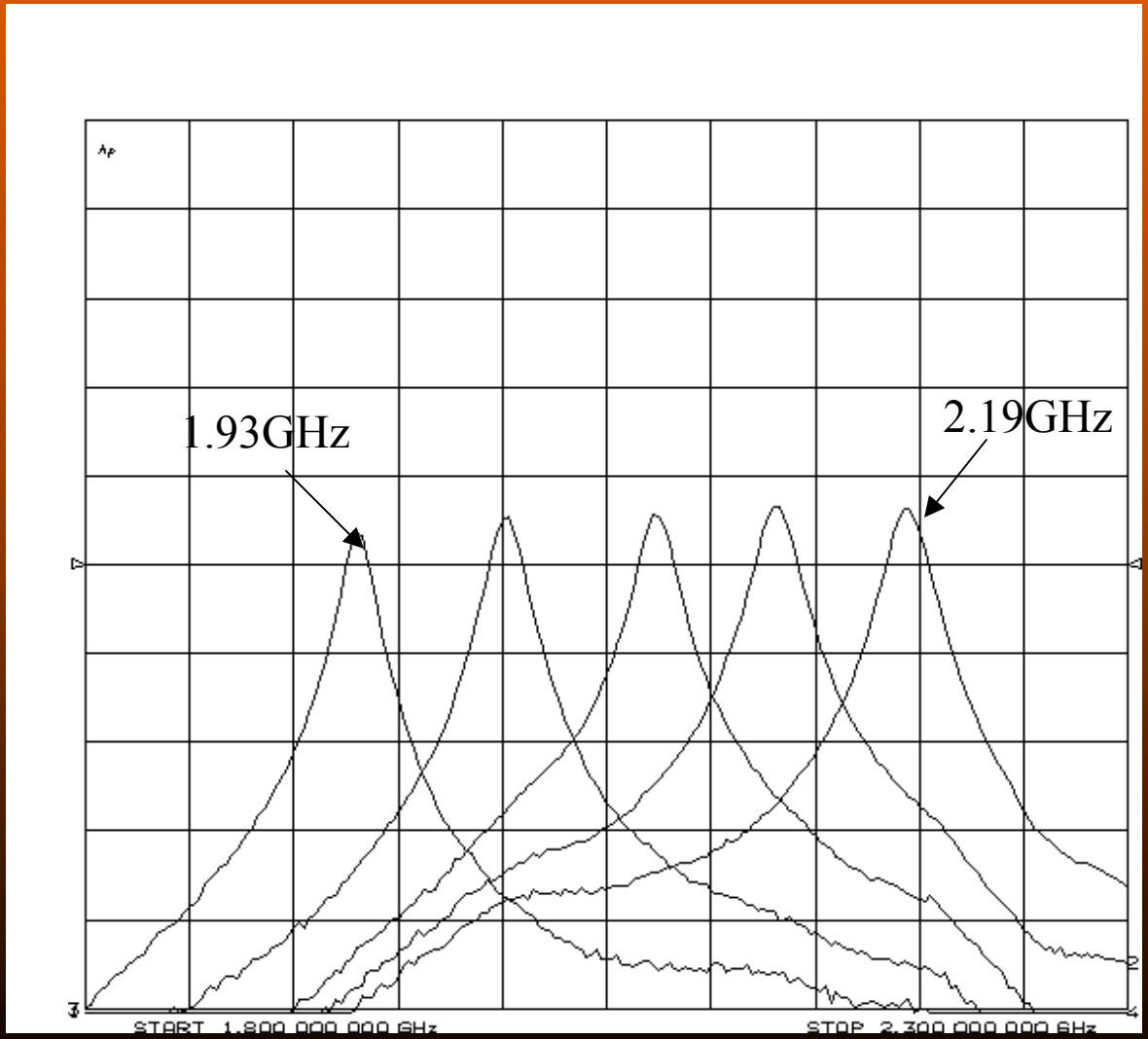
Measured Q-Tuning

More than 3 octaves at f_o=2.16GHz



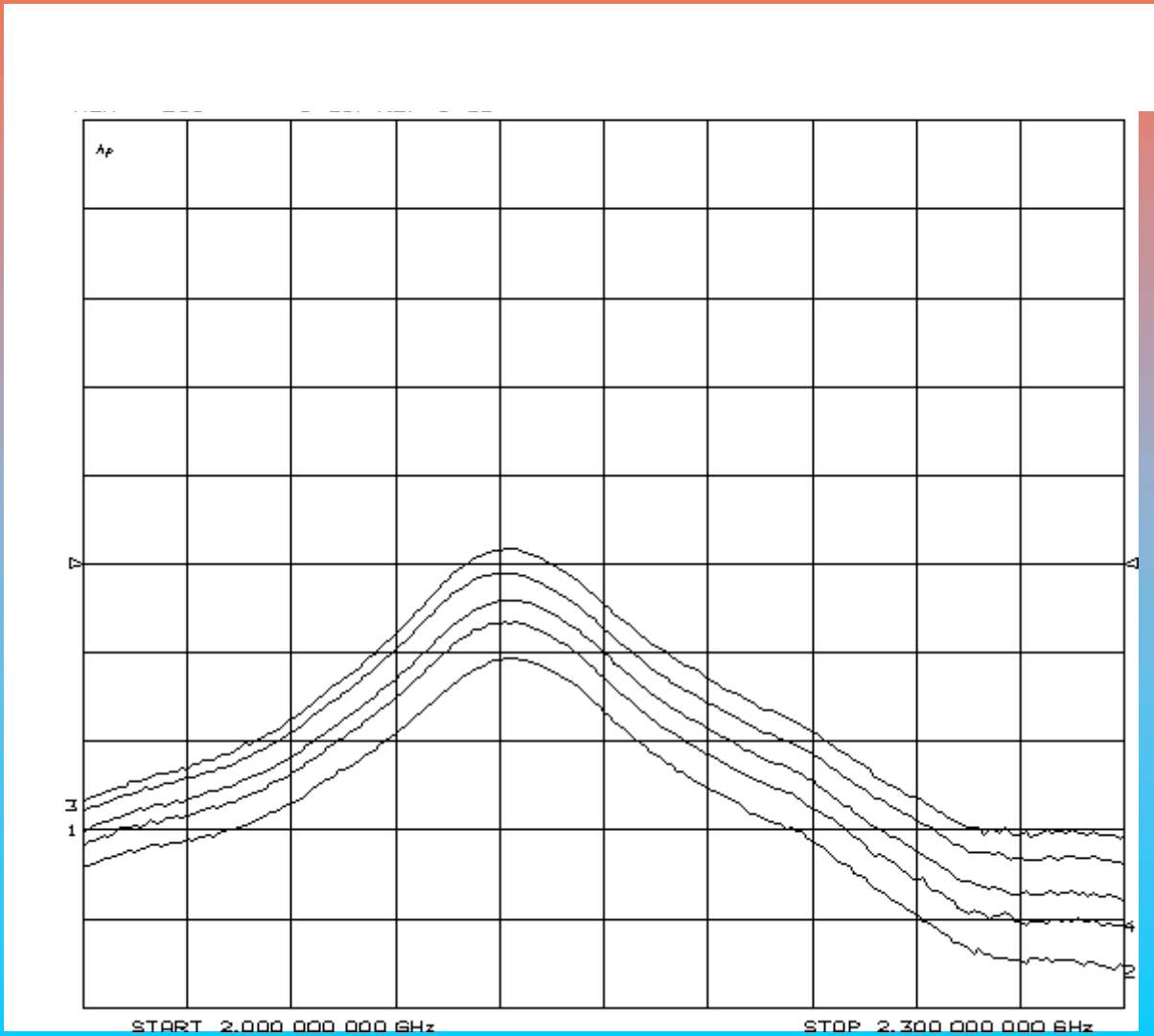
Measured Frequency Tuning

13% around 2.1GHz with Q~100



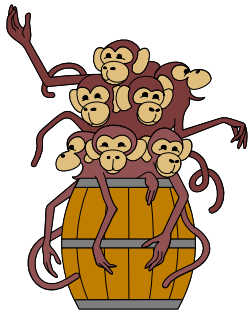
Measured Peak Gain Tuning

Around
2 octaves with
f_o=2.12GHz
and Q=40



Providing gain at the ω_o of an image-reject filter is useful in a receiver front-end after the LNA, to relax the NF spec of the mixer.

Frequency- and Q-tuning techniques for OTA-C filters



Need for Automatic Tuning

- Process variations can change f_o and Q by at least 20%
- Parameters also change with temperature and time(aging)

- Automatic tunining is a critical issue for the optimal performance of continuous-time circuits.

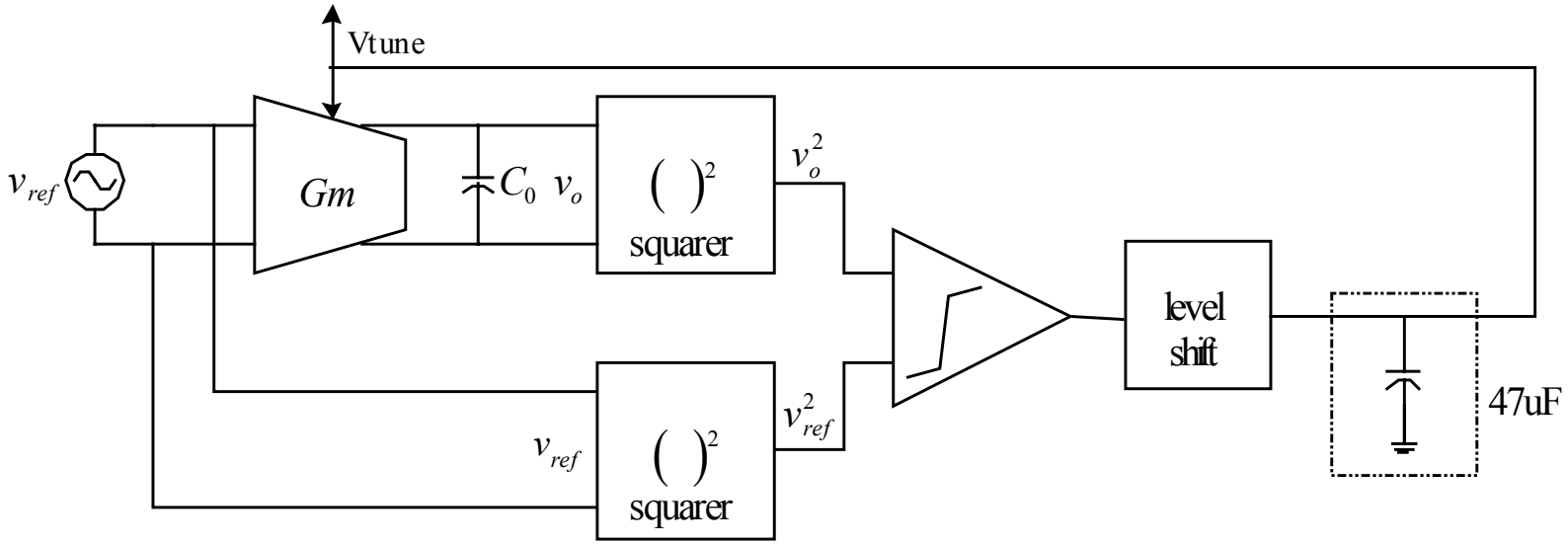
Methods of tuning

- Master-Slave
- Based on trigonometric properties
- Based on filter phase information
- Pre-tuning
- Burst tuning
- Switching between two filters

Automatic Frequency Tuning Scheme

BASED ON TRIGONOMETRIC FUNCTION PROPERTIES

$$\sin^2 x + \cos^2 x = 1$$

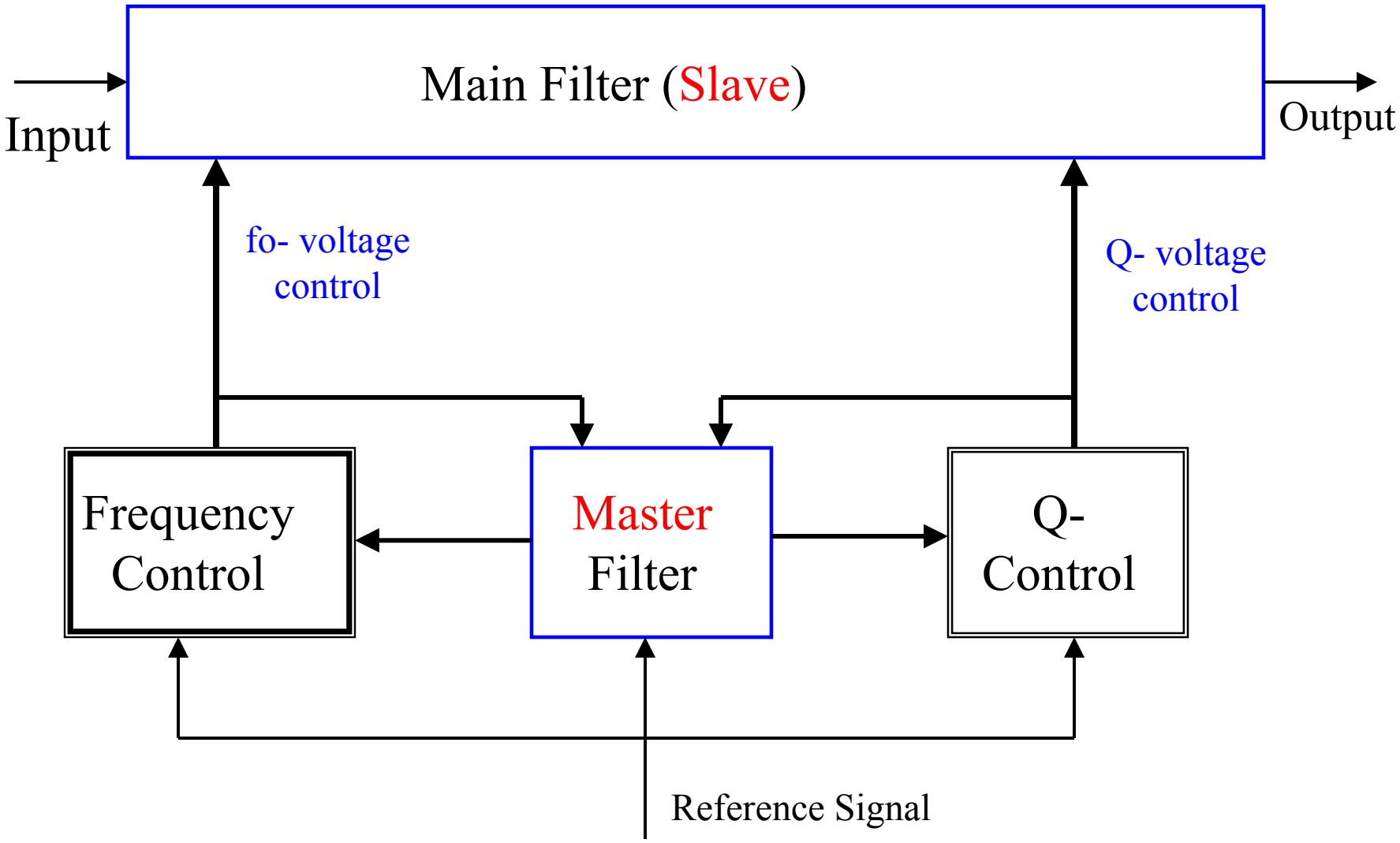


☛ Integrator--Gm & C: $$v_o^2 = \frac{1}{2}\left(\frac{f_u}{f_r}\right)^2 A^2 + \frac{1}{2}\left(\frac{f_u}{f_r}\right)^2 A^2 \cos(4\pi f_r t)$$

☛ Level shifter--Maximize the linear range of the automatic tuning system.

Master-Slave Tuning Concept

Master-Slave Tuning Concept



Frequency Tuning

Phased-Locked Loop (PLL)

- Most widely used scheme
- Accurate (less than 1% error is reported)
- **Square wave input reference**
- Only Phase - Frequency Detector, and LPF are the additional components
- It may take a large area overhead

VCF, VCO, Single OTA, Peak detect, adaptive….

Q Tuning Schemes

Based on an envelope detector and a switched-capacitor integrator. It yields an accuracy of about 30%

Modified LMS

- Q-accurate of about 1%
- It does not use envelope detector
- **Square wave input, any periodic function is sufficient**
- Independent of frequency tuning

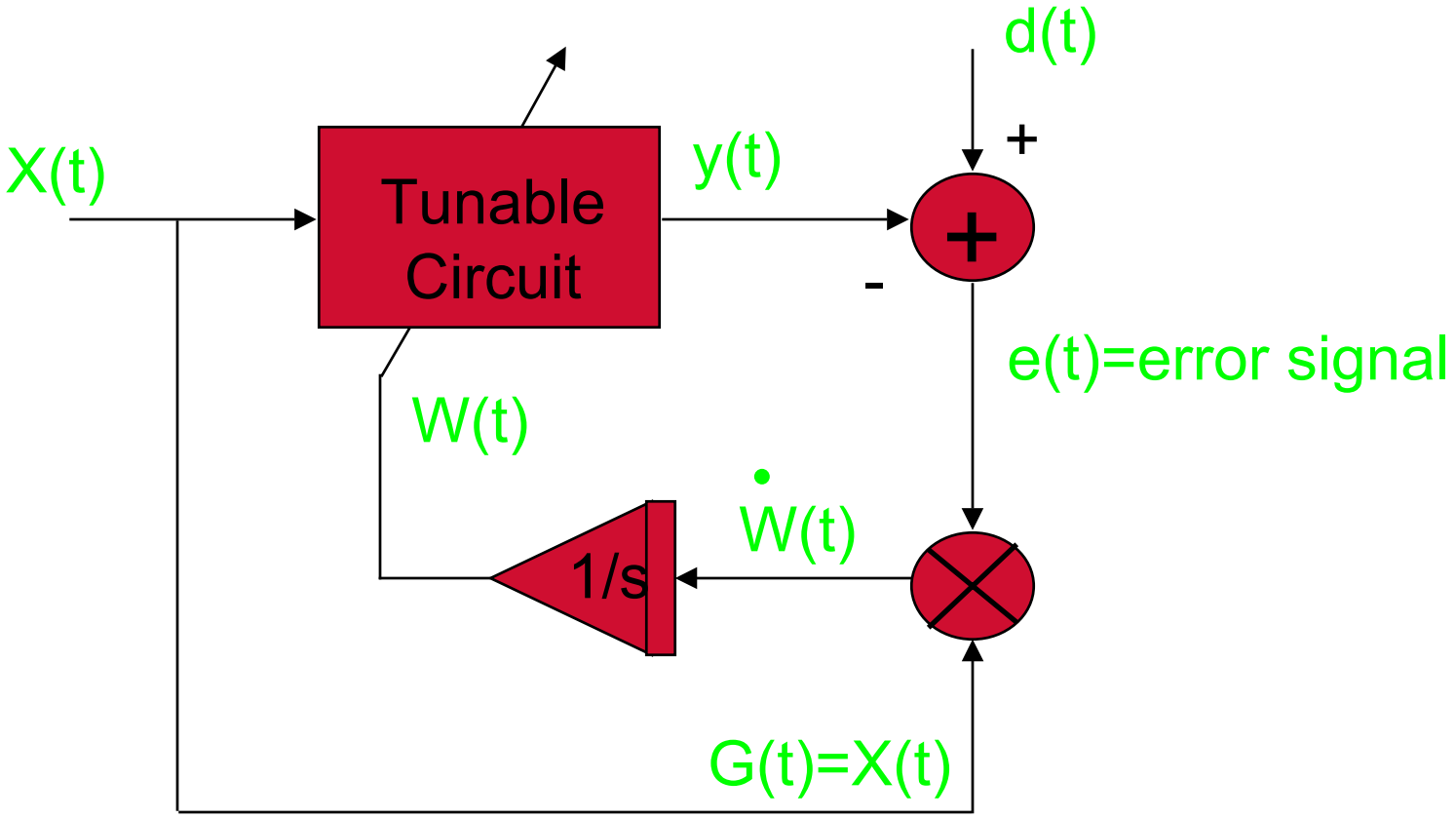
Adaptive LMS Algorithm: Introduction

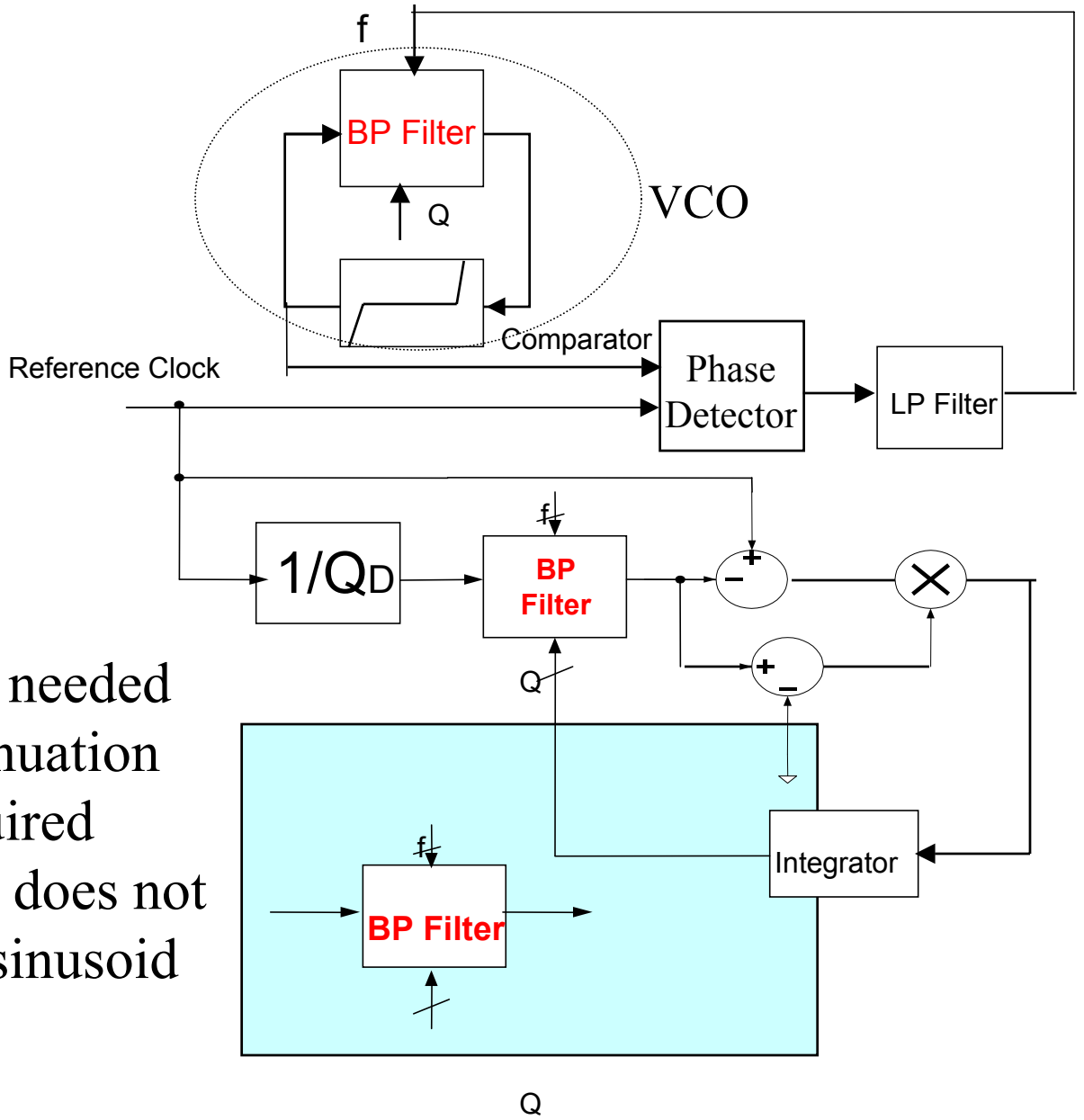
- Called Adaptive "Least-Mean-Squares" Algorithm because it learns by minimizing the *mean-square error (MSE)* between a desired response and the actual response of a system
- Minimizes error by updating system coefficients through a feedback loop

Adaptive LMS Algorithm: Theory

- Using the steepest descent algorithm to minimize the MSE we obtain:
- $\dot{\mathbf{W}}(t) = k[d(t) - y(t)]G(t) = k[e(t)]G(t)$
  - W(t) = tuning signal
  - d(t) = desired system output
  - y(t) = actual system output
  - G(t) = tuning gradient (partial derivative of y(t) with respect to W(t))
  - k = adaptation constant

LMS Algorithm: Block Diagram (Linear System)

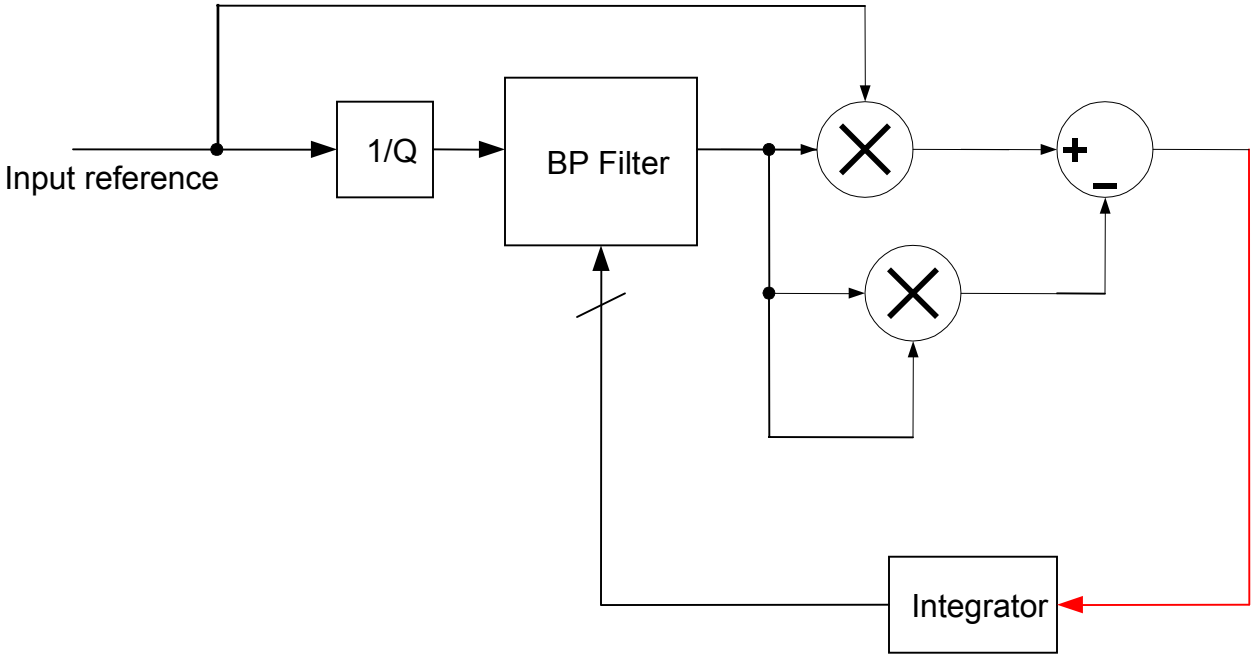




- Three Filters are needed
- An accurate attenuation 1/Q_D block is required
- Reference signal does not need to be a pure sinusoid

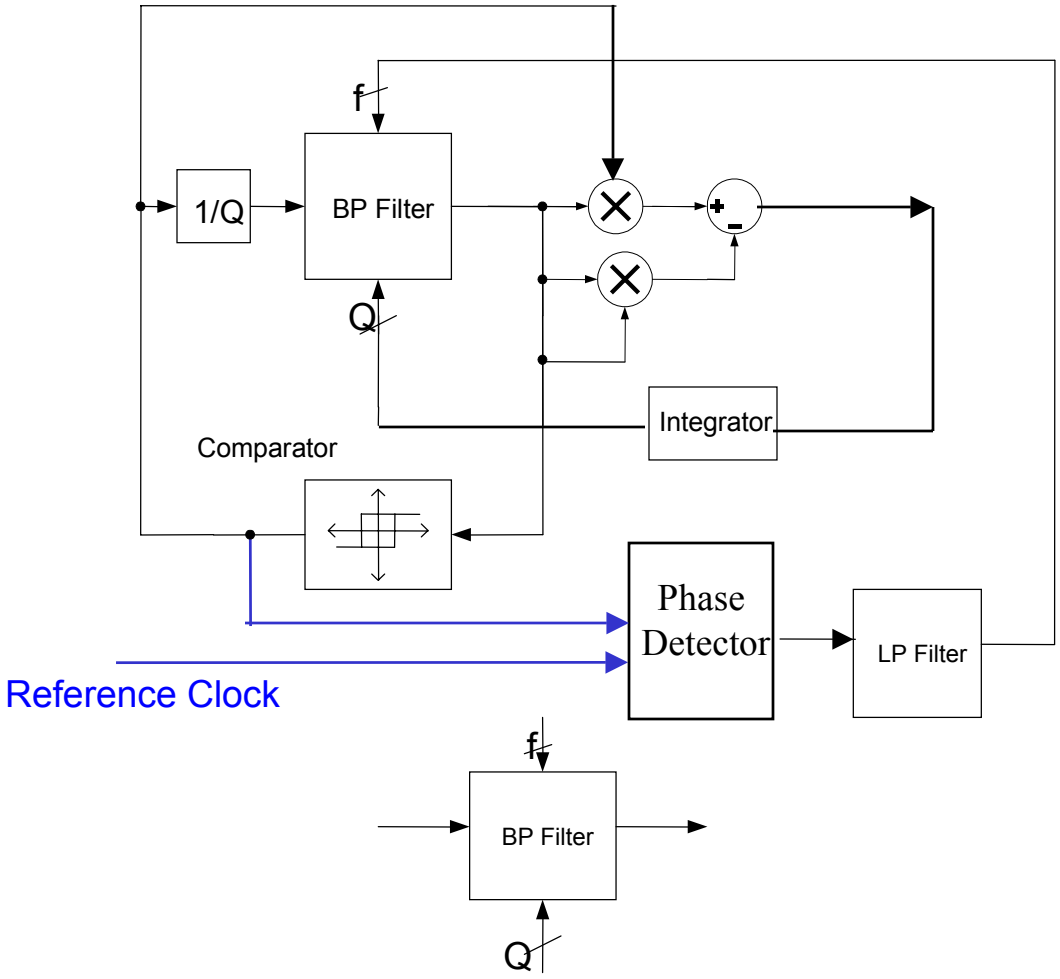
Stevenson, J.M.; Sanchez-Sinencio, E "An accurate quality factor tuning scheme for IF and high-Q continuous-time filters". IEEE Journal of Solid-State Circuits, Volume: 33 No.12 , Dec. 1998 , Page(s): 1970 -1978

An enhanced Q-tuning scheme



New implementation of modified-LMS Q-tuning scheme. Note that the LMS has been implemented in a different way yielding a structure with less offset voltages. See reference for more details.

The enhanced tuning scheme

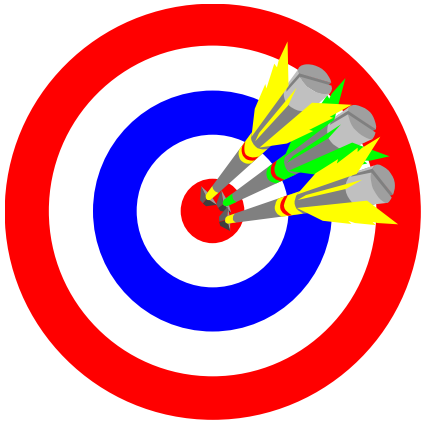


Improvements over the previous Tuning scheme comparison

- Area overhead decreased

  (Previous scheme => 2 extra filters

  New scheme => 1 extra filter)



- Eases the matching restrictions

  (Previous tuning scheme => match 3 filters

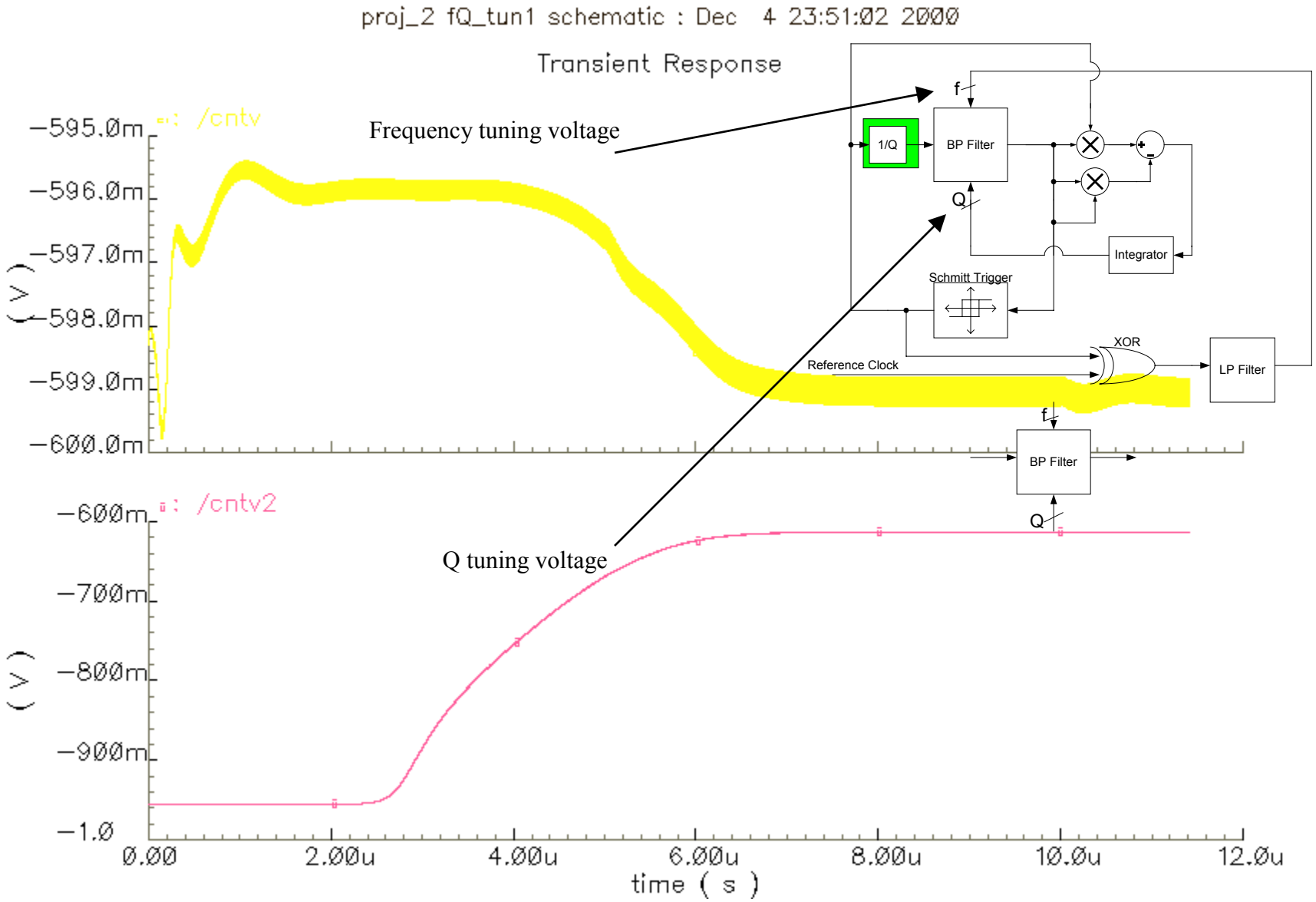
  New tuning scheme => match 2 filters)

- Improves accuracy of tuning

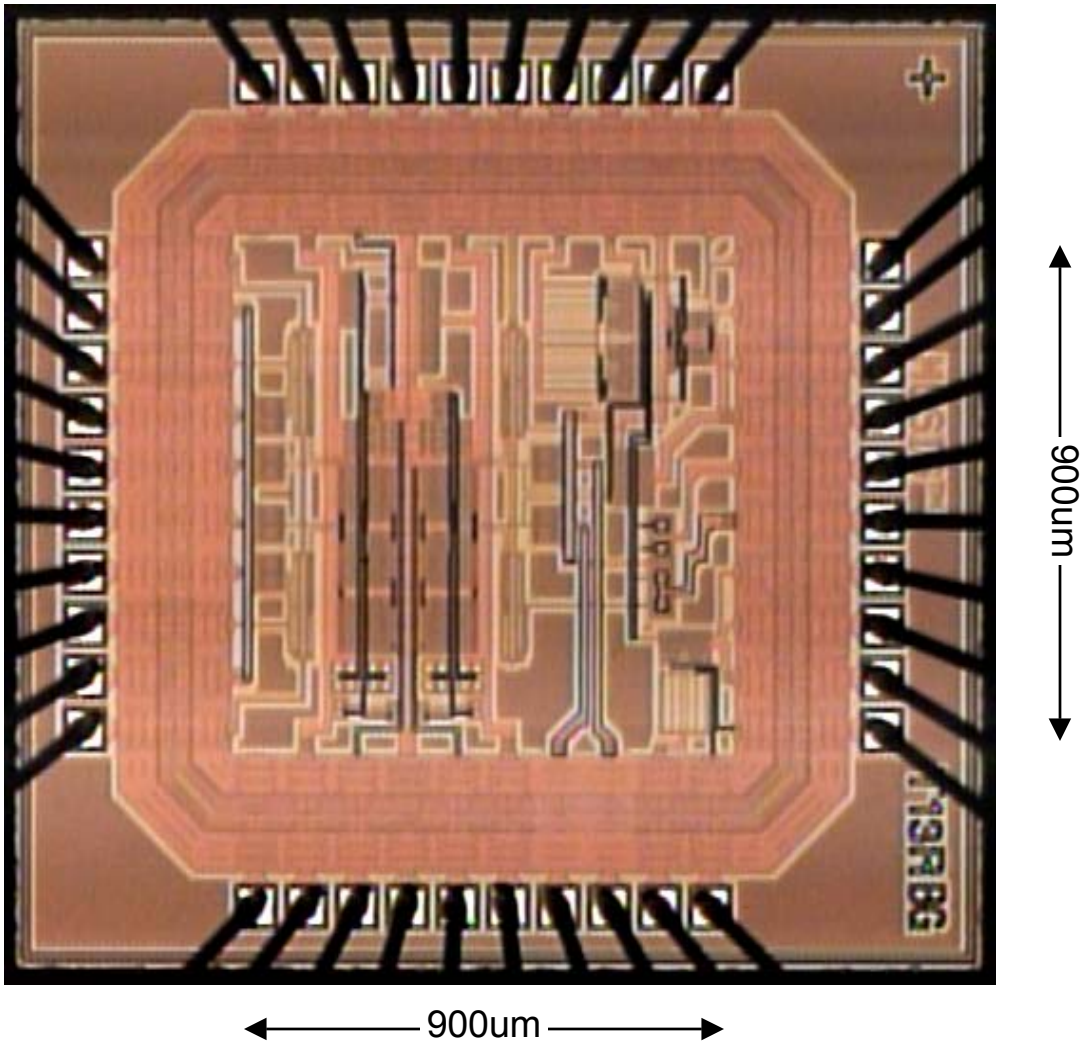
  (New tuning scheme is more tolerant to offsets than the previous one)

  The Q-tuning loop speed can be equal to the f_0-tuning loop for optimal performance

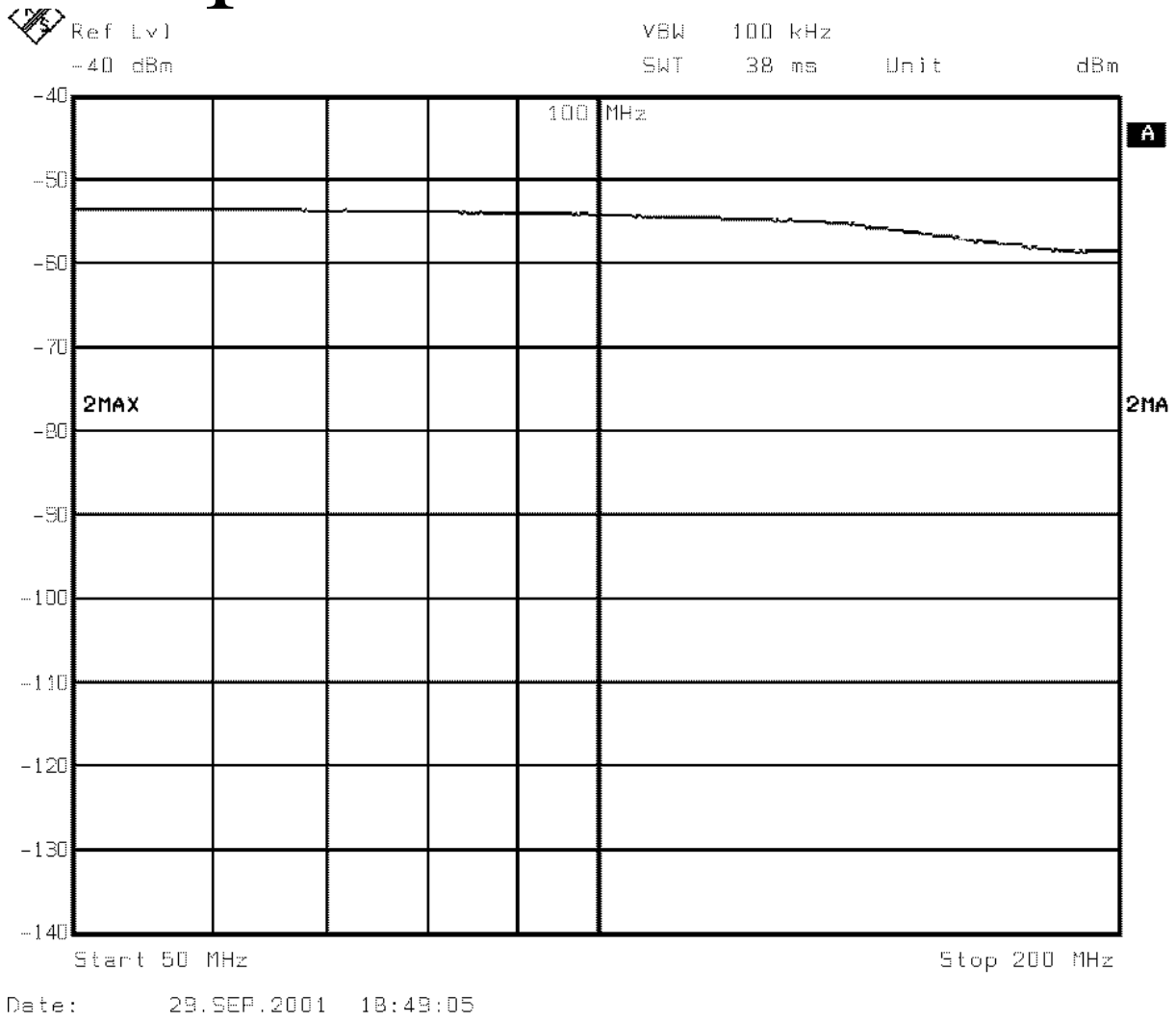
Simulated results for tuning scheme



Die Photograph

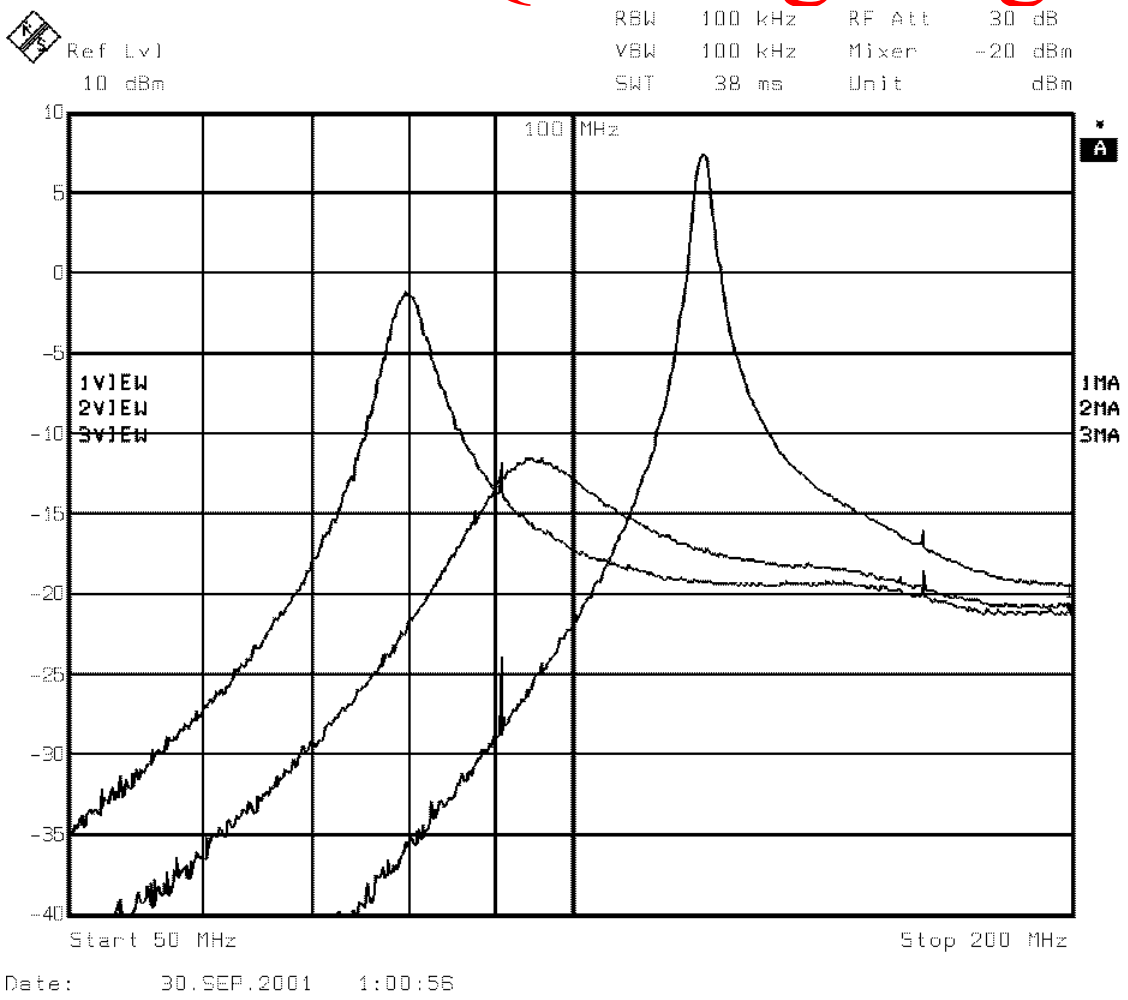


Experimental results on



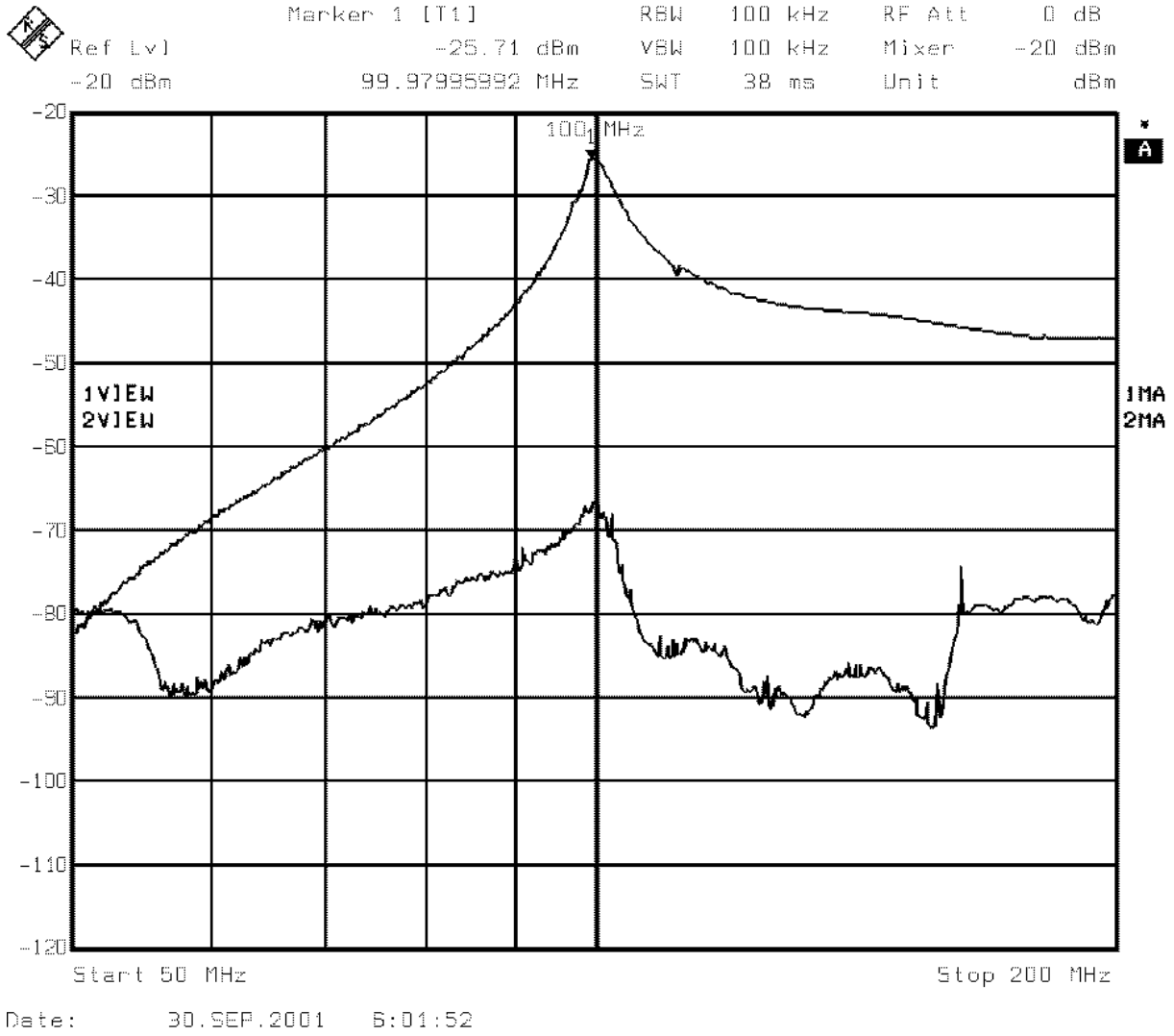
This response should be subtracted from other plots to get actual response

Experimental Q tuning range results



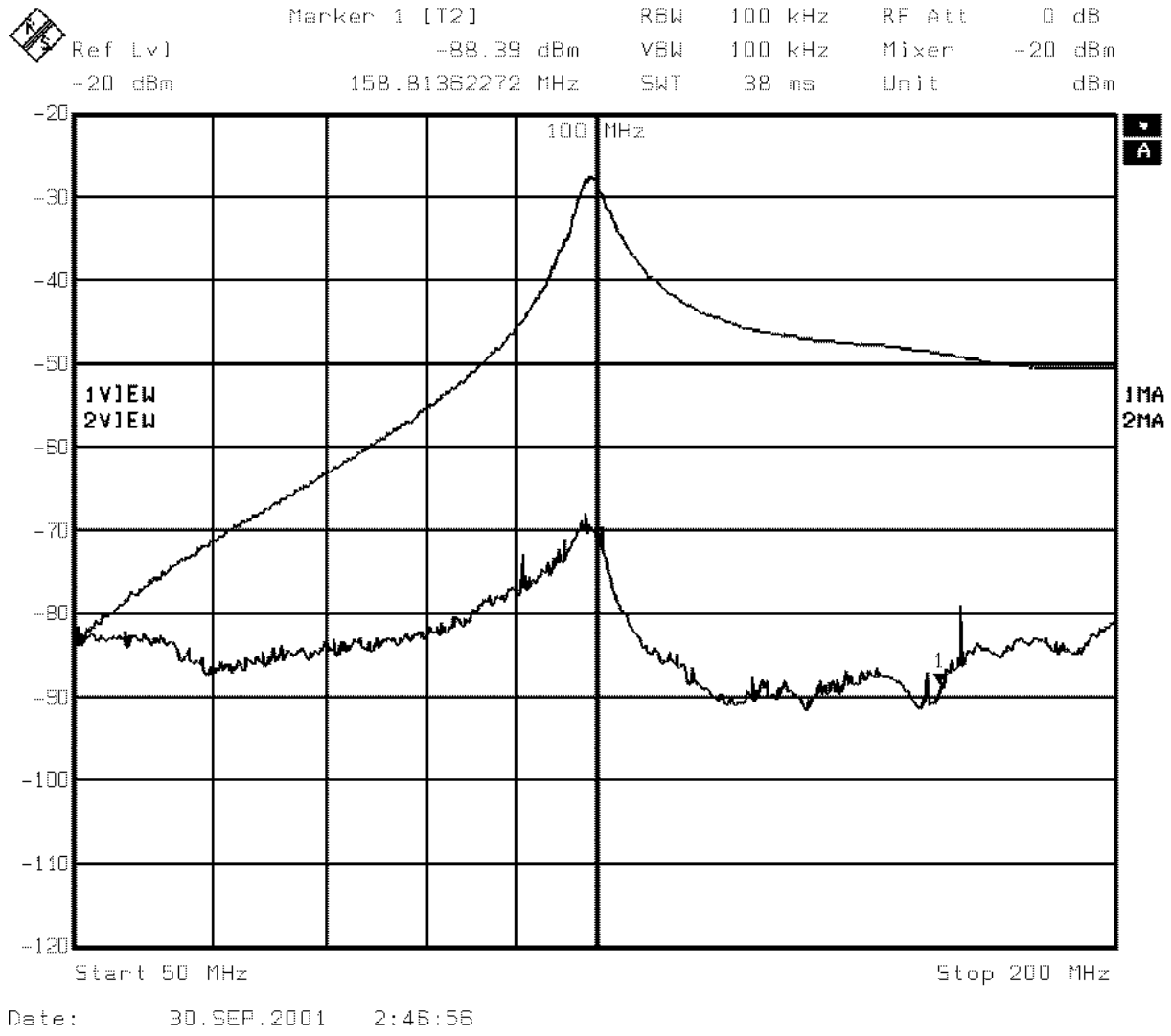
- Qs of 16, 5 and 40 at 80,95 and 110 MHz

DM-CM response of the filter



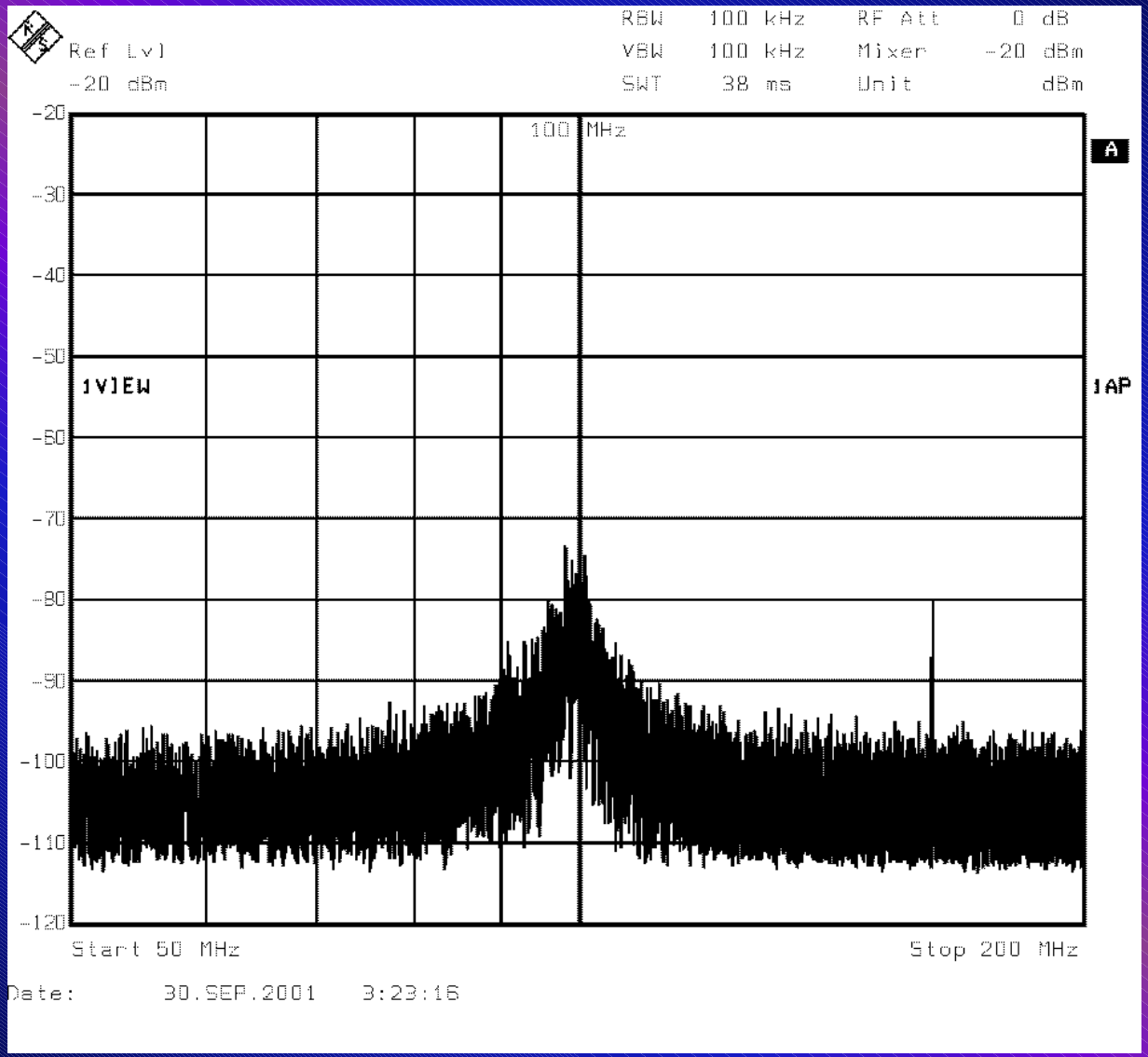
- CMRR is more than 40dB in the band of interest

Supply response of the filter



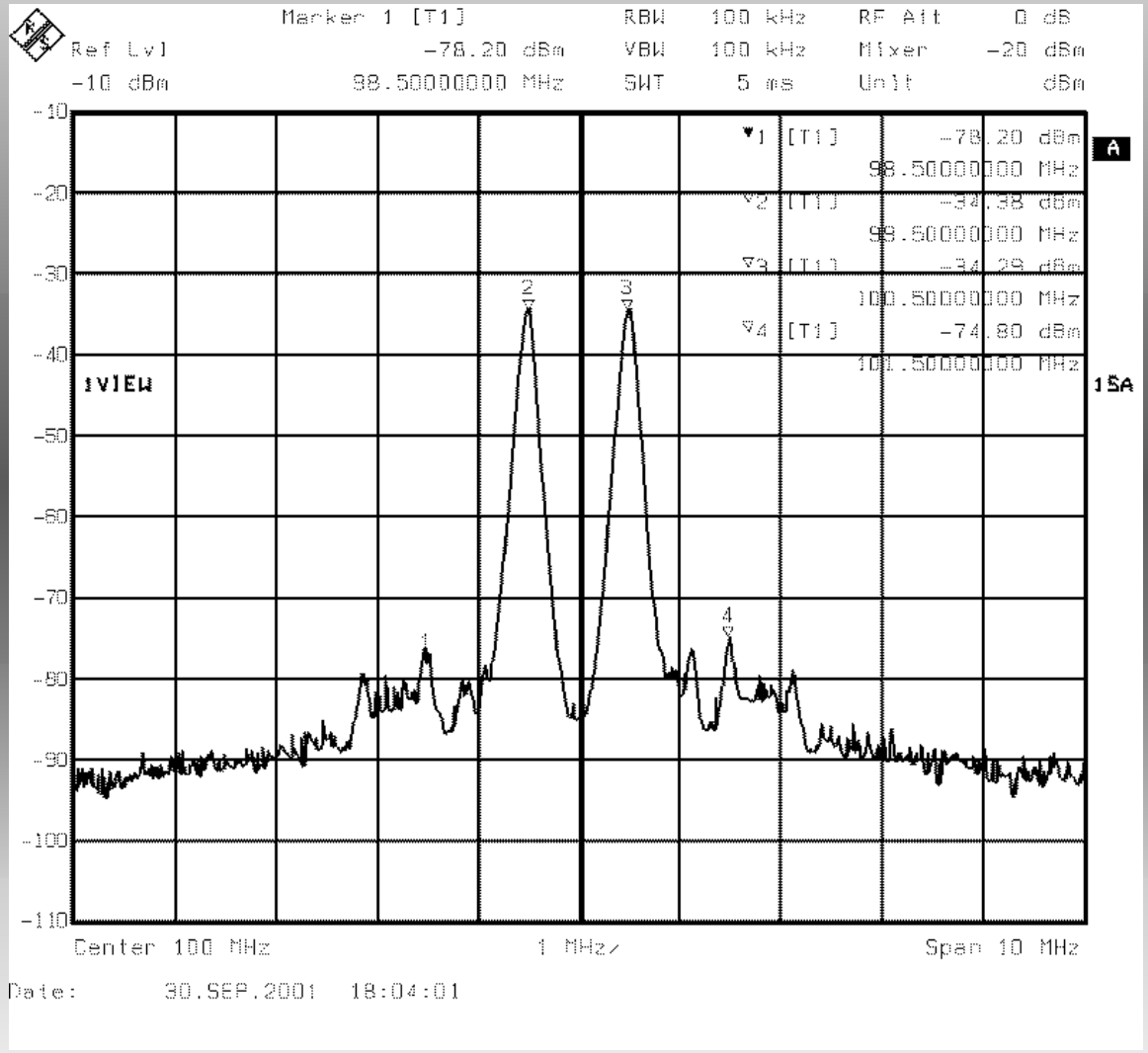
- PSRR$^-$ is more than 40dB in the band of interest

Noise response of the filter



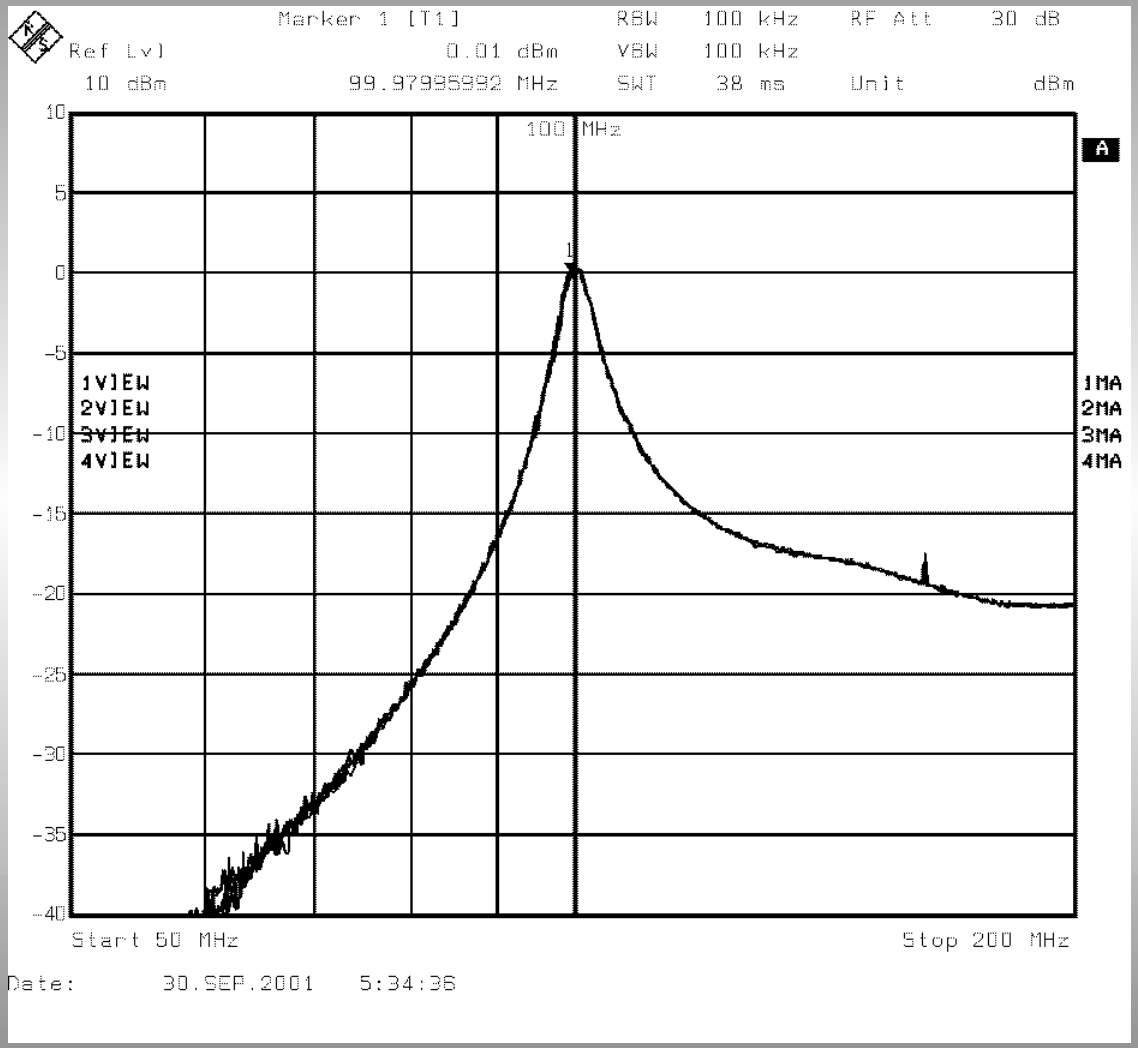
- Total integrated noise power at the output= -60dBm

Two-tone inter-modulation test



- IM_3 of 45dB when the input signal is 44.6mV

Filter response for four different ICs



- The tuning works!

ACKNLOWDGMENT

- José Silva Martinez
- Ahmed N. Mohieldin
- Aydin Karsilayan
- Praveen Kallam
- Ahmed Emira
- J. M. Stevenson

For discussions and material provided for this presentation. Also thanks to Randy Geiger who introduced me to this research area nearly 20 years ago.

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