Design of Three-Stage Class-AB 16 Ω Headphone Driver Capable of Handling Wide Range of Load Capacitance

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***Abstract*—In this paper, the effect of load capacitance variation on the location of the closed loop poles of three-stage amplifiers is analyzed and a frequency compensation scheme that automatically adjusts the damping factor according to the load capacitance is proposed. A class-AB 16 Ω headphone driver designed using the proposed scheme in 0.13 μm technology can handle 1 pF to 22 nF capacitive load while consuming as low as 1.2 mW of quiescent power. It can deliver a peak power of 40 mW (1.6 Vpp swing) to the load with −84.8 dB THD and 92 dB peak SNR. It occupies 0.1 mm^2 area.**

***Index Terms*—Class-AB amplifiers, class-AB drivers, audio power amplifiers, headphone drivers, multi-stage amplifiers, capacitive loaded amplifiers.**

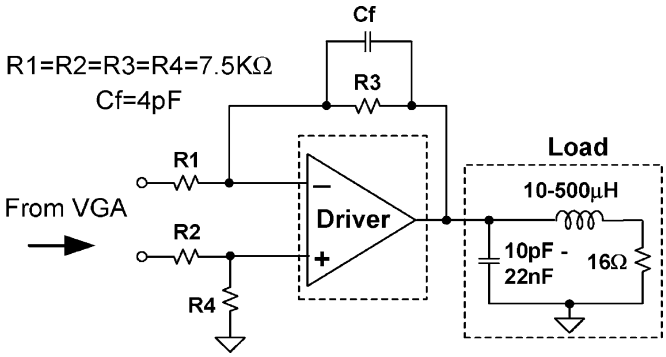

Fig. 1. 16 Ω driver configuration.

I. Introduction

DUE to rapid growth in mobile entertainment electronics, the demand for high-efficiency headphone drivers has generated a great deal of interest in recent times. Owing to electro magnetic interference (EMI) issues with class-D drivers, class-AB architecture is preferred for headphone applications [1]. In order to reduce design cycle time and time-to-market, a versatile driver that can be deployed to a variety of platforms is desirable. Capacitive loads as large as 20 nF are used in some platforms for electro static discharge (ESD) protection and EMI suppression. Other platforms may use low-capacitance diodes for ESD protection. Also, the end-users typically prefer to use the headphone output as an input for other devices like desktop speakers, FM transmitters, home theater systems, etc. Depending on the usage conditions, the cable capacitance can range from few tens of pF to few 100 pF. Also, a series inductor is employed in some platforms that functions as a FM choke. The target driver configuration with possible range of loads is shown in Fig. 1.

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Since the battery life is an important aspect of the portable gadgets, driver's power efficiency has to be maximized. The power efficiency ($\mathrm{P_{EFF}}$) is defined as the ratio of the average power delivered to the load to the average power dissipated from the supply. $\mathrm{P_{EFF}}$ of the class-AB stage can be expressed as (see Appendix A)

$$\mathrm{P_{EFF}} = \frac{1}{\mathrm{CF}(1 + 2\mathrm{CF}\mathrm{I_Q}/\mathrm{I_P})} \tag{1}$$

where $\mathrm{I_P}$ is the peak load current, $\mathrm{I_Q}$ is the quiescent current and CF is the peak-to-average ratio or the crest factor of the waveform.

Since the CF of a music waveform can be as large as 19 dB [3], $\mathrm{I_Q}$ significantly affects the $\mathrm{P_{EFF}}$ of the driver. From (1) it can be seen that $\mathrm{P_{EFF}}$ can be improved if $\mathrm{I_P}/\mathrm{I_Q} \gg 2\mathrm{CF}$.

Several solutions for low-voltage headphone driver design for portable equipments were recently published. A low-voltage two-stage class-AB driver was proposed in [4]. This design uses a folded-mesh biasing approach described in [5] to achieve 0.8 V operation. The main drawback of this design is that the power delivered to the headphone (peak power of 3.2 mW on 16 Ω load) is inadequate for many cases. In order to minimize the cross-over distortion without consuming large quiescent power, an interesting approach that uses an adaptive bias current was proposed in [1]. This technique, however, fails to tackle the distortion due to the triode region of operation of the output transistors, which is typically the dominant source of distortion in low-voltage designs. Another design presented in [6] is based on three-stage nested Miller compensated (NMC) class-AB amplifier. Since the three-stage amplifier has sufficiently large gain, it achieves a reasonable distortion performance while delivering adequate power (peak power of 53.5 mW on 16 Ω

load). The design also supports wide range of load capacitors spanning from no load to 12 nF. The drawback of this approach is that the quiescent power consumption of the amplifier is quite large (12.5 mW), which is mainly attributed to the NMC scheme. Some designs use a series resistor at the output to achieve stability with large capacitive load. However, this approach is undesirable for power efficiency and peak output power in case low-voltage, low-power drivers.

A design that achieves stable operation for capacitive loads ranging from 1 pF to 22 nF with only 1.2 mW of quiescent power dissipation was presented in brief by the authors [7]. In this paper, detailed analysis of three-stage amplifiers under large load variation and evolution of the proposed architecture is presented. Also, description of a new class-AB bias scheme used in the driver is provided.

The rest of the paper is organized as follows. An analysis of the three stage amplifier compensation and its behavior under large load variation is presented in Section II. A new equivalent circuit used for this analysis is formally verified in Appendix B. In Section III, an approximate solution for load invariant damping based on an intuitive approach is proposed and is corroborated by simulations. Transistor level implementation of a 16 Ω driver based on the proposed compensation scheme is described in Section IV. Experimental results are shown in Section V and conclusions are drawn in Section VI.

II. Behavior of Three Stage Amplifiers Under Large Load Variation

Two stage amplifiers that support a wide range of capacitive loads have been reported in [8], [9] but so far this capability has not been demonstrated in three-stage amplifiers. Several compensation schemes for three-stage amplifiers driving large capacitance load with power efficiency more than 10 times that of the conventional NMC scheme have been reported recently [10]–[14]. The damping factor control frequency compensation (DFCFC) presented in [10] has the core idea for reducing power consumption for large capacitive loads and is also suitable for low-resistance drivers. The main aim of these compensation schemes is to maximize the performance for a single value of capacitive load. However, all of these schemes are vulnerable to large peaking in frequency response and potential instability when the load capacitance is dropped to small values. In order to come up with a compensation scheme for a wide range of capacitive loads, an insightful analysis of the three-stage amplifier compensation scheme and the pole locus as a function of capacitive load is required.

A. Intuitive Interpretation of Three-Stage Amplifier Compensation and Power Efficiency Improvement in DFCFC

An equivalent circuit of a three-stage amplifier that assists in gaining insight on the behavior of its closed-loop poles is presented in this section. A three-stage amplifier configuration with first stage forming the dominant pole is shown in Fig. 2(a). $\mathrm{Gm1}$ represents the transconductance of the first stage of the amplifier. $\mathrm{A2}$ represents the gain of the second stage and $\mathrm{A3}$ represents the third stage gain inclusive of the load capacitance. $\mathrm{A2{*}A3}$ along with $\mathrm{Cc1}$ acts like an "active RC" integrator though the current generator is $\mathrm{Gm1}$ instead of a resistor. $\mathrm{Cc1}$

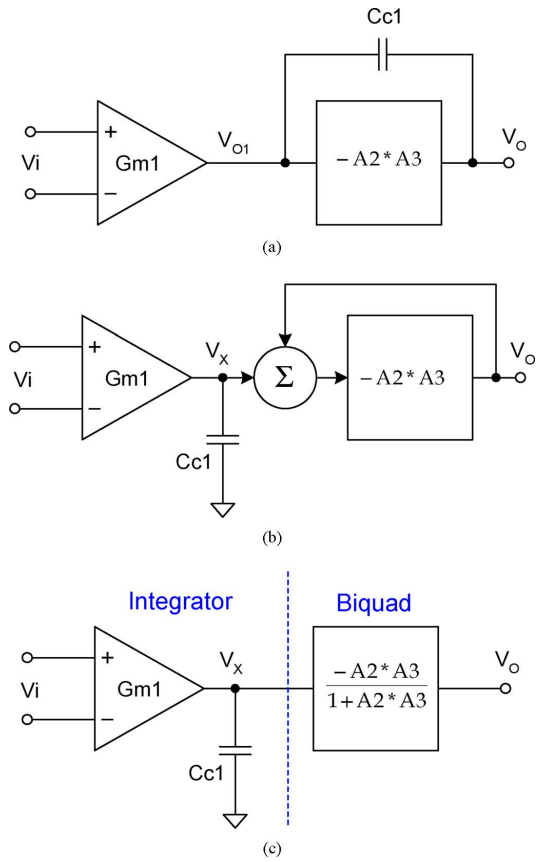

Fig. 2. (a) Basic three-stage amplifier with dominant pole on the first stage. (b) $\mathrm{Cc1}$ providing unity feedback around second and third stage. (c) High-frequency equivalent circuit.

provides the unity feedback assuming high output impedance for $\mathrm{Gm1}$ and ignoring the parasitic capacitance at the output node of $\mathrm{Gm1}$. Now, the full circuit can be modeled as an integrator $(\mathrm{Gm1}/\mathrm{sCc1})$ cascaded by $\mathrm{A2{*}A3}$ in unity feedback [see Fig. 2(b)], which yields the equivalent circuit in Fig. 2(c). This simplified equivalent circuit breaks up the problem of three-stage compensation to that of an integrator and a biquad design, which are very well understood. It also provides good insight and helps understanding of complicated cases without relying on exact transfer functions with several unimportant terms.

The equivalent circuit can be verified using a formal analysis (see Appendix B) and the following assumptions. 1) The capacitance at the output node of $\mathrm{Gm1}$ is much smaller compared to the compensation capacitance $\mathrm{Cc1}$. 2) The loading of $\mathrm{Cc1}$ at the output is small compared to that of the actual load capacitor at the output. 3) The feed-forward current via $\mathrm{Cc1}$ to the output is insignificant. Due to low resistance and large capacitance load, the frequency at which the forward current from the capacitor $\mathrm{Cc1}$ dominates the current from to output stage (i.e., the zero frequency) is very large. Hence, the effect of the feed-forward path can be safely ignored. Also, note that this equivalent circuit is not accurate at very low frequencies due to the ignorance of the output conductance of the gain stages and is intended for stability analysis and studying high-frequency behavior of the closed loop amplifier.

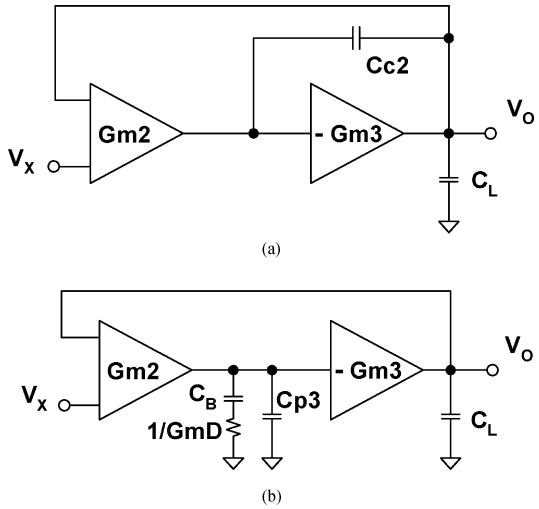

Fig. 3. (a) Second and third stage in unity feedback loop—NMC. (b) Second and third stage in unity feedback loop—DFCFC.

The biquad in the equivalent circuit is analyzed for the NMC and the DFCFC schemes. The biquad formed by the second and the third stage in the unity feedback loop for both of the cases are shown in Fig. 3. $\mathrm{Gm2}$ and $\mathrm{Gm3}$ represent the transconductance of the second and third stage, respectively. $\mathrm{Cc2}$ is the second Miller compensation capacitance. $\mathrm{Cp3}$ is the parasitic capacitance at the input node of the third stage. GmD is the conductance of the damping resistor and $\mathrm{C_B}$ is the blocking capacitance that ensures that the damping resistance does not reduce the gain of the amplifier at low frequencies (within signal bandwidth).

In case of NMC, the transfer function of the biquad section is given by

$$\frac{\mathrm{V_O}}{\mathrm{V_X}} = \frac{\dfrac{\mathrm{Gm2Gm3}}{\mathrm{Cc2C_L}}}{\mathrm{s}^2 + \mathrm{s}\dfrac{\mathrm{Gm3}}{\mathrm{C_L}} + \dfrac{\mathrm{Gm2Gm3}}{\mathrm{Cc2C_L}}} = \frac{\omega_{23}^2}{\mathrm{s}^2 + \mathrm{s}\dfrac{\omega_{23}}{\mathrm{Q_{BQ}}} + \omega_{23}^2}. \tag{2}$$

The square root of the product of the poles $\sqrt{(\mathrm{Gm3/C_L}) * (\mathrm{Gm2/Cc2})}$ is defined as the pole magnitude (ω_{23}) and the sum of the poles $(\mathrm{Gm3/C_L})$ is defined as the "loss bandwidth" $(\omega_{23}/\mathrm{Q_{BQ}})$ of the biquad, where $\mathrm{Q_{BQ}}$ refers to the quality factor of the biquad poles.

The closed loop poles of a typical amplifier with on-chip load are designed to fall in the Butterworth constellation [15]. It can be shown that the conditions to achieve third order Butterworth pole constellation for the three-stage amplifier in inverting unity gain configuration are $\omega_{23} = \sqrt{2}\omega_{\mathrm{CL}}, \mathrm{Q_{BQ}} = 1/\sqrt{2}$ and $\mathrm{Gm1/Cc1} = \omega_{\mathrm{CL}}$, where ω_{CL} is the closed loop pole magnitude [2]. This translates to the following conditions on the bandwidth of the gain stages:

$$\frac{1}{2}\frac{\mathrm{Gm3}}{\mathrm{C_L}} = \frac{\mathrm{Gm2}}{\mathrm{Cc2}} = \frac{\mathrm{Gm1}}{\mathrm{Cc1}} = \omega_{\mathrm{CL}}. \tag{3}$$

Note that for a given ω_{CL} and $\mathrm{C_L}$, the output stage transconductance $\mathrm{Gm3}$ is fixed. This limitation is due to the fact that the loss bandwidth of the biquad is solely determined by $\mathrm{Gm3/C_L}$, as indicated by (2).

In case of DFCFC biquad, the transfer function contains an additional pole-zero pair due to the damping network. The root locus of the overall amplifier is largely independent of this pole-zero pair and hence its effect can be ignored in this analysis. The transfer function of the DFCFC biquad at frequencies well above $\mathrm{GmD}/(2\pi\mathrm{C_B})$ is thus approximated by

$$\frac{\mathrm{V_O}}{\mathrm{V_X}} \approx \frac{\dfrac{\mathrm{Gm2Gm3}}{\mathrm{Cp3C_L}}}{\mathrm{s}^2 + \mathrm{s}\dfrac{\mathrm{GmD}}{\mathrm{Cp3}} + \dfrac{\mathrm{Gm2Gm3}}{\mathrm{Cp3C_L}}}. \tag{4}$$

ω_{23} and $\omega_{23}/\mathrm{Q_{BQ}}$ are given by $\sqrt{(\mathrm{Gm3/C_L}) * (\mathrm{Gm2/Cp3})}$ and $\mathrm{GmD/Cp3}$, respectively. The conditions for the Butterworth pole constellation can be verified to be

$$\frac{1}{2}\frac{\mathrm{GmD}}{\mathrm{Cp3}} = \frac{\mathrm{Gm1}}{\mathrm{Cc1}} = \omega_{\mathrm{CL}} \tag{5}$$

and

$$\frac{\mathrm{Gm2}}{\mathrm{Cp3}}\frac{\mathrm{Gm3}}{\mathrm{C_L}} = 2\omega_{\mathrm{CL}}^2 \tag{6}$$

An important change enabled by the damping network is that the loss bandwidth is determined by the independent parameter $\mathrm{GmD/Cp3}$. This allows the design to trade $\mathrm{Gm2/Cp3}$ for $\mathrm{Gm3/C_L}$ for a given product shown in (6). Since $\mathrm{Cp3}$ is the parasitic capacitance of the transistors, it can be several orders of magnitude smaller than the largest supported $\mathrm{C_L}$. Hence, for a given numerical value of the ratio, $\mathrm{Gm2/Cp3}$ can be realized with substantially lesser power than $\mathrm{Gm3/C_L}$. This helps to keep the power dissipation low and allows the quiescent power to be dictated by the distortion performance rather than the frequency compensation.

B. Effects of Load Capacitance Variation

Assuming that the three-stage amplifier is designed for Butterworth pole constellation for $\mathrm{C_L} = 20$ nF and using (2) and (4), it can be seen that the magnitude of the complex poles of the biquad increases as $\mathrm{C_L}$ is dropped from 20 nF. In case of NMC, the quality factor of the complex poles of the biquad is given by

$$\mathrm{Q_{BQ-NMC}} = \sqrt{\frac{\mathrm{Gm2}}{\mathrm{Cc2}}\frac{\mathrm{C_L}}{\mathrm{Gm3}}}. \tag{7}$$

Since the quality factor is proportional to $\sqrt{\mathrm{C_L}}$, it decreases as the load capacitance is reduced, eventually resulting in real poles for the biquad. The pole locus of the overall closed loop third order system is shown in Fig. 4. The poles move such that one real pole goes to high frequency while the other two poles are complex with magnitude and Q constrained to a narrow range. In case of DFCFC, the quality factor of the complex poles of the biquad is given by

$$\mathrm{Q_{BQ-DFCFC}} = \frac{1}{\mathrm{GmD}}\sqrt{\frac{\mathrm{Cp3\,Gm2\,Gm3}}{\mathrm{C_L}}}. \tag{8}$$

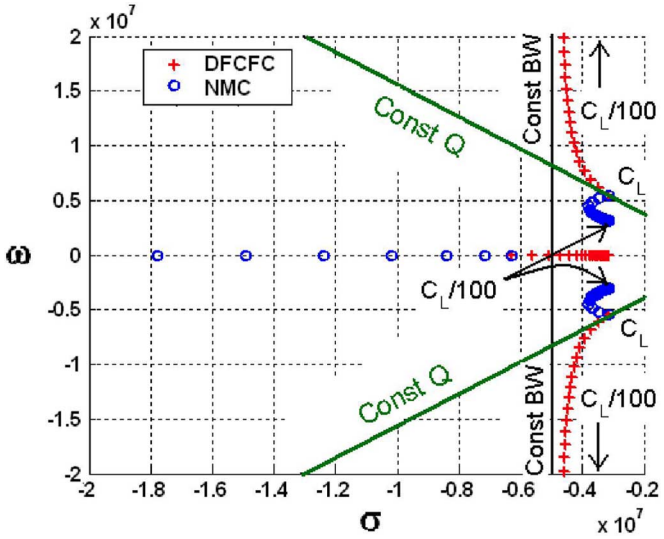

Fig. 4. Pole locus of NMC and DFCFC as the load capacitance is varied from C_L to $C_L/100$.

Since the quality factor is proportional to $1/\sqrt{C_L}$, it *increases as the load capacitance is dropped*. Dropping C_L from 20 nF to 200 pF, for instance, would increase $Q_{BQ-DFCFC}$ by 10 times (from 0.7 to 7). Note that the Q of the closed loop complex poles of the DFCFC in Fig. 4 eventually tracks Q_{BQ}, which follows a constant bandwidth (const. BW) path as indicated by (4). Thus, the large Q_{BQ} resulting from the small load capacitance leads to an under-damped third order system with large Q complex poles. Also note that this effect exists regardless of the assumption of Butterworth pole constellation for $C_L = 20$ nF.

The Butterworth pole constellation yields a phase margin of about 60.5° for the open loop amplifier, which is not really needed for the headphone driver and can be traded for power reduction. Since lower phase margin allows smaller product $(Gm2/Cc2) * (Gm3/C_L)$, the power consumption in the second and third stage of the amplifier can be reduced. Further reduction in power can be achieved by introducing a RC network in series with Cc1 [see Fig. 5(a)]. The resistor Rc provides a LHP zero and capacitor C2 helps retain the gain margin for small C_L. The model for the three-stage amplifier now changes to the one shown in Fig. 5(b). The unity feedback around second and third stage is modified to a feedback with a factor β as shown in Fig. 5(c) (see Appendix B for the derivation). The exact pole locus as a function of load capacitance for a 45° phase margin design with the RC network is presented in Section III.

III. Proposed Load-Capacitance-Aware Compensation Scheme

In the previous section, it was shown that the DFCFC scheme could result in unstable system if the capacitive load is reduced. From (4) and (8), it was predicted that Q_{BQ} becomes large when the load capacitance is dropped to small values. In other words, the damping factor ζ $(= 1/2Q_{BQ})$ of the complex poles of the DFCFC biquad is proportional to $\sqrt{C_L}$, which makes the system under-damped for small load capacitance. Since the Q of

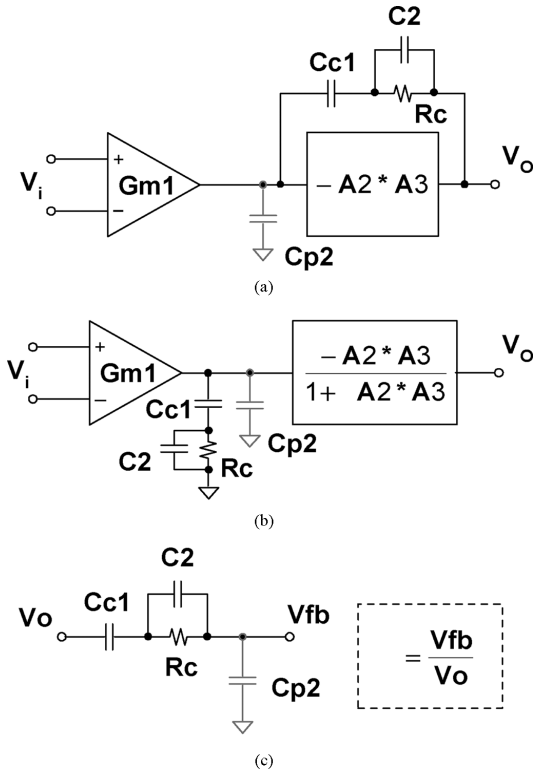

Fig. 5. (a) Three-stage amplifier with LHP zero resistor. (b) High-frequency equivalent circuit. (c) Feedback factor used in biquad transfer function.

the closed loop complex poles of the third order system closely follows Q_{BQ}, it is desirable to have a compensation scheme that has a Q_{BQ} independent of C_L. This provides a close approximation to the constant Q (const. Q) path shown in Fig. 4. Hence the aim of the new compensation scheme is to achieve constant Q_{BQ} (and hence constant ζ) and be more power efficient than NMC.

As explained in Section II-A, a separate damping network at the output of the second stage improves the power efficiency over NMC for large C_L. A damping network emulates a series RC network, where the damping resistor R_D provides the necessary loss and the blocking capacitance C_B prevents the R_D from reducing the low-frequency gain. The role of R_D is to provide the necessary loss in the biquad so that the Q of the complex poles can be fixed to a desired value. From (8), it can be seen that Q_{BQ} can be made independent of C_L if the resistor $1/GmD$ in Fig. 3(b) is replaced with a resistor R_D that is proportional to $\sqrt{C_L}$.

Due to the obvious difficulties in realizing the square root dependence using linear circuits, a piece-wise approach is taken in the proposed scheme. Fig. 6 shows the architecture of the proposed amplifier. The damping circuit formed by GmD, R_B and C_D emulates a damping resistance of $R1 \approx 1/GmD$ and an equivalent blocking capacitance of $Ceq1 \approx GmD * R_B * C_D$. Furthermore, C_{D2} provides the necessary small damping resistance in case of small C_L, namely, $R2 \approx C_L/(Gm3 * C_{D2})$. It also provides a series blocking capacitance $Ceq2 \approx C_{D2} * go3/Gm3$, where go3 is the output conductance of third stage. At high frequencies, the impedance is dominated by the damping resistors, which governs the Q of the complex poles.

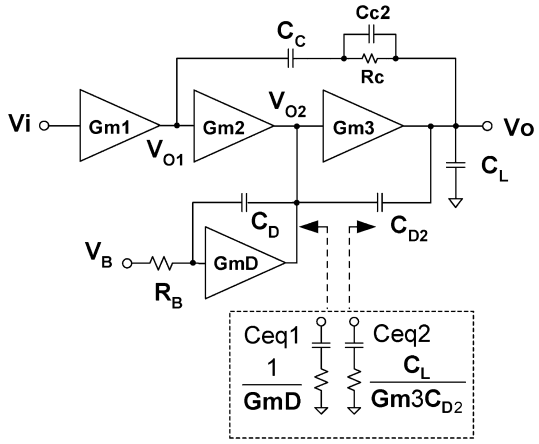

Fig. 6. Architecture of the proposed compensation scheme.

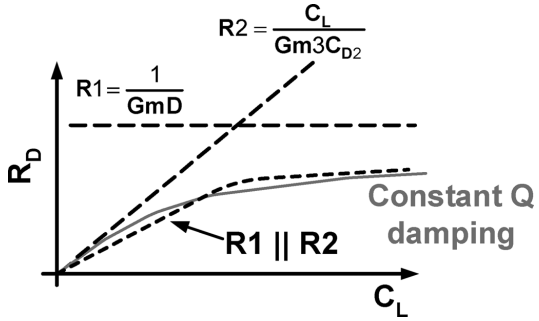

Fig. 7. Piecewise approximation for proportional-to-square-root resistor.

The quality factor of the complex poles of the biquad in this new scheme is approximated by

$$Q_{BQ-PROPOSED} \approx \frac{\sqrt{(C_{D2}+C_{p3})\,C_L Gm2 Gm3}}{GmDC_L + Gm3C_{D2}}. \quad (9)$$

The main concept in the proposed scheme can be better understood with the aid of Fig. 7. It illustrates that the parallel combination of R1 (constant resistance) and R2 (proportional-to-C_L resistance) provides a reasonable approximation of the desired proportional-to-$\sqrt{C_L}$ resistor. For large value of the C_L, GmD provides the necessary damping and for small values of C_L, the equivalent resistor seen through C_{D2} provides adequate damping. For intermediate values of C_L, both the damping resistances (R1 and R2) contribute to the loss. Due to the approximation, the small and large C_L region would be somewhat over-damped and the intermediate region is somewhat under-damped. It is worth noting that C_{D2} is much smaller than the second Miller capacitor used by NMC. This is the case since C_{D2} is meant to provide damping for small C_L conditions in the proposed scheme whereas the second Miller capacitance in the NMC scheme needs to provide damping even for the largest C_L.

The pole locus as a function of load capacitance is shown in Fig. 8 for the case of 45° phase margin design. As the load capacitance is dropped, the poles of the DFCFC amplifier are pushed to the RHP plane, yielding unstable systems. The proposed architecture provides necessary damping across a wide

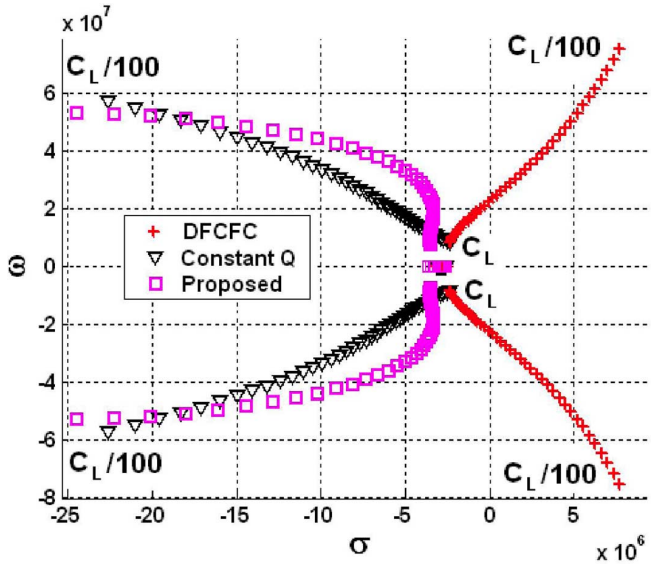

Fig. 8. Pole locus for 45° phase margin cases as the load capacitance is varied from C_L to $C_L/100$.

range of C_L and roughly retains a constant Q factor. Due to the piece-wise approximation of the proportional-to-square-root resistor, the proposed structure shows a small acceptable deviation from the constant Q_{BQ} case. Fig. 9 shows a family of Bode plots from simulations with various values of C_L ranging from C_L to $C_L/10000$ for the proposed scheme. Note that the proposed scheme exhibits gracious frequency response for a wide range of load capacitance. Process Monte Carlo stability simulations were performed on the transistor level implementation and the phase and gain margin histograms are shown in Fig. 10 for load capacitances of 20 nF and 200 pF. The histograms show that the compensation scheme is robust to process variations.

IV. Implementation of the Proposed 16 Ω Driver

The transistor level implementation of the 16 Ω driver using the proposed architecture is shown in Fig. 11. The design considerations of each of the stages are given below.

A. First Stage (Gm1)

Gm1, the input stage, is realized using the folded cascode transconductor formed by M9–M14. The input transistors M13 are carefully sized and matched to minimize the offset voltage and 1/f noise. The highest 1/f noise contribution of a PMOS-input folded cascode amplifier comes from the NMOS current source transistors (M9). Resistors R_f are used to minimize the 1/f noise contribution of M9. The bias voltages V_{B1}, V_{B2}, and V_{B3} are generated using standard low-voltage cascode bias generators while V_{B6} is generated by a simple diode connected transistor. The bias currents of M13 and M12 are made equal to ensure equal slew rate for positive and negative transitions.

B. Second Stage (Gm2)

Transistors M7, M7', and M8 realize the amplifier's second stage Gm2. This is implemented as "positive Gm stage" in order to ensure negative feedback around second and third stage. The transconductance of M8 is augmented by a current mirror gain

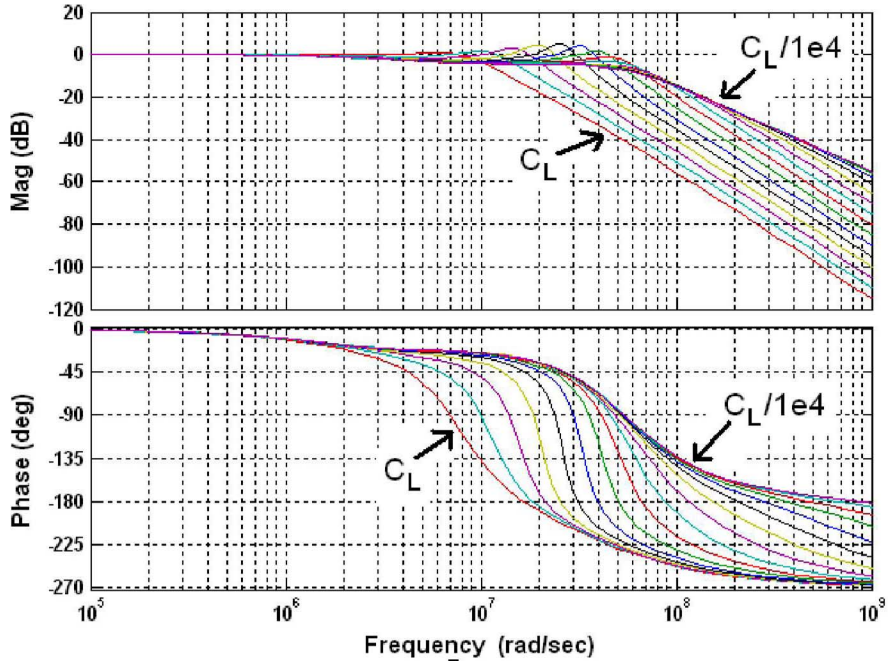

Fig. 9. Simulated Bode plots of proposed scheme as load capacitance is varied from $\mathrm{C_L}$ to $\mathrm{C_L}/1\mathrm{e}4$.

of 2 in M7, M7'. The output current of the second stage is pumped into the floating current mirror formed by M3 and M4. These floating current mirrors, described in [16], provide the necessary biasing for the class-AB output stage.

C. Proposed Damping Stage (GmD)

Due to large swings associated with the class-AB output stage, the damping network is split such that M5 and M6 realize GmD for the NMOS and the PMOS path respectively. M6 also serves as a bias current source for $\mathrm{Gm2}$. The gate of M5/M6 is biased using the resistor $\mathrm{R_B}$ and the drain node is connected directly to the $\mathrm{Gm2}$ output. This enables the circuit to work under large swing conditions without pushing M5/M6 into triode region. The damping circuit used in [10] is meant for an amplifier with predominantly capacitive load and it relies on the assumption that the voltage swings at node $\mathrm{V_{O2}}$ (in Fig. 6) is small. This assumption is not valid for low-resistance drivers with class-AB output where the input swing of the output stage $(\mathrm{Gm3})$ is intentionally kept large for power efficiency reasons. Hence, a damping network that works under large swing conditions is desirable. The proposed circuit, shown in Fig. 12, serves this purpose. The impedance of the proposed damping circuit is given by

$$\begin{aligned}\mathrm{Zin} &= \frac{\mathrm{sC_D}+\mathrm{G_B}}{\mathrm{sC_D}(\mathrm{GmD}+\mathrm{G_B})}\left\|\frac{1}{\mathrm{go_D}}\right. \\ &\approx \frac{\mathrm{G_B}}{\mathrm{sC_D}(\mathrm{GmD}+\mathrm{G_B})}+\frac{1}{\mathrm{GmD}} \qquad (10)\end{aligned}$$

where GmD is the transconductance of the OTA, $\mathrm{go_D}(\ll \mathrm{GmD})$ is the output conductance of the OTA and $\mathrm{G_B}(\ll \mathrm{GmD})$ is the conductance of the resistor $\mathrm{R_B}$ used to bias the OTA. Zin can be approximated as a capacitor of value $\mathrm{C_D GmD/G_B}$ at frequencies well below $\mathrm{G_B/C_D}$ and as a resistor of value $1/\mathrm{GmD}$ at frequencies much higher than that. Thus, the proposed circuit provides a damping network with a resistance of $1/\mathrm{GmD}$ in series with an equivalent capacitance of $\mathrm{C_D R_B GmD}$.

D. Output Stage (Gm3)

Fig. 13 shows the schematic of the output stage. In order to avoid a large DC blocking capacitor at the output, dual supply is used. The class-AB output stage and the level shifters (LS) are operated from a ± 1 V supply while the rest of the amplifier uses ± 0.6 V supply.

In order to prevent oxide breakdown in the gate-drain overlap region, cascoding is employed. When the output swings close to VDDD (VSSD), the output voltage is effectively shared between the VDS of the main transistor M1 (M2) and cascode transistor M1c (M2c). The cascode transistors (M1c, M2c) are biased such that the VDS of the output transistors are maintained to be <1.2 V under all swing conditions. The NMOS output devices are in triple well, which allows their sources and bodies to be 0.4 V below the substrate voltage. The level shifters are implemented using source followers. The NMOS level shifter also makes use of triple well transistors to handle voltage levels below the substrate potential.

E. Class-AB Bias Generation Circuit

The NMOS part of the class-AB bias generation circuit is illustrated in Fig. 14. The straightforward approach to generate the bias voltage $\mathrm{V_{B5}}$ is to pump current into three diode connected copy-transistors with sizes proportional to transistors M1, Mls, and M3 connected in series (similar to the biasing scheme in [16]). This, however, results in extremely large mirroring error. The main source of the error arises due to mismatch in the drain voltages of the main transistors M1, Mlsb, and M3 and their corresponding copy-transistors in the

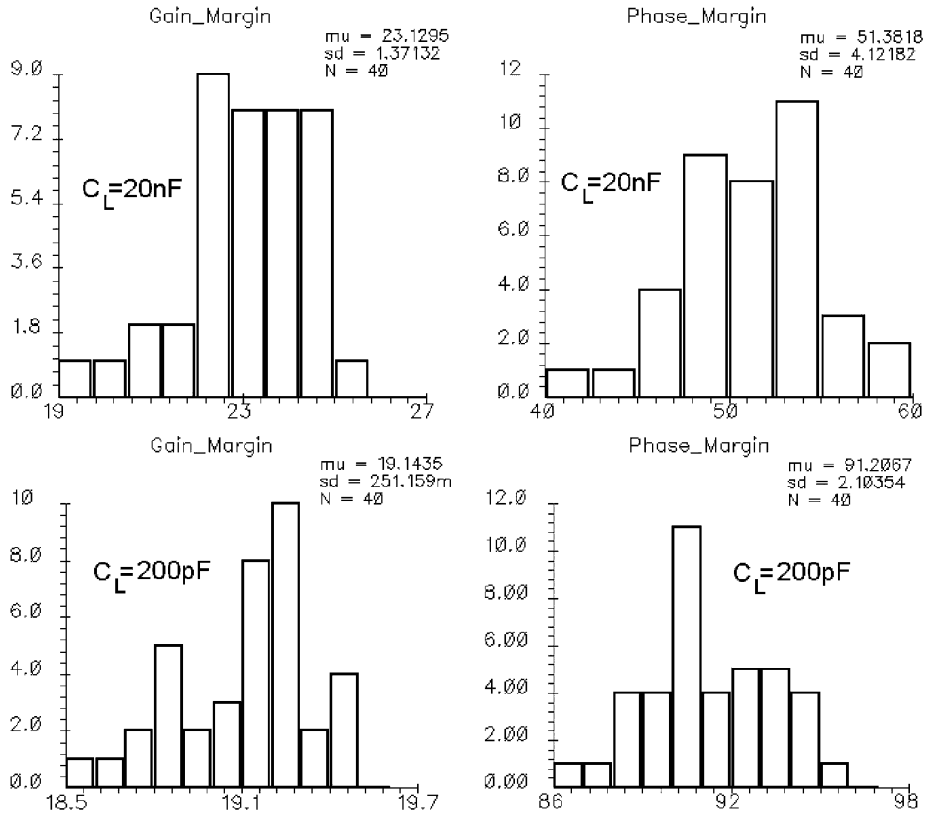

Fig. 10. Process Monte Carlo histograms for phase and gain margins.

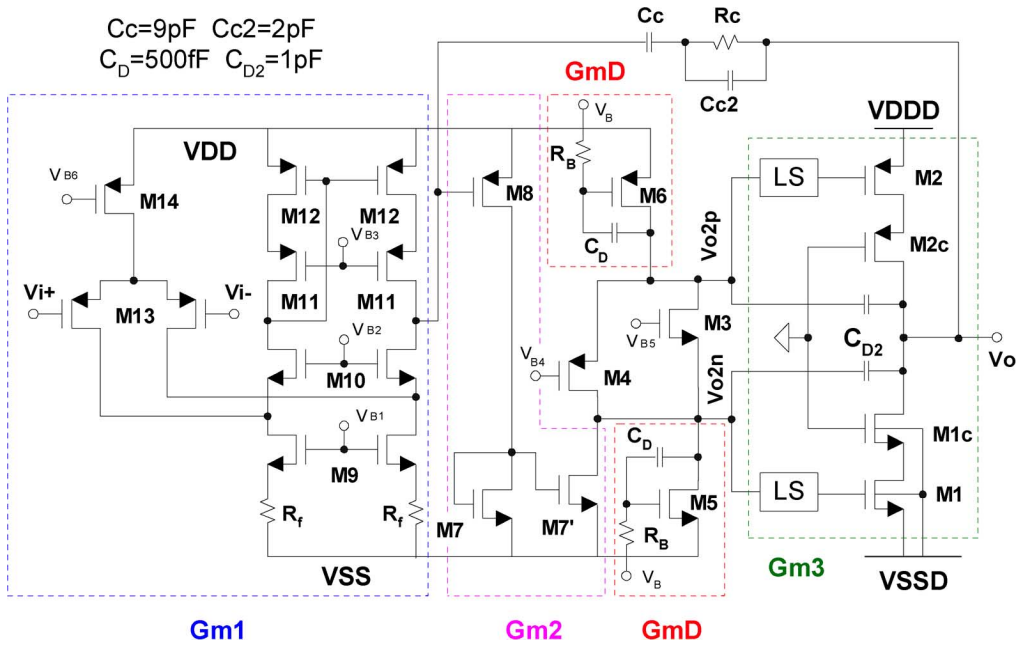

Fig. 11. Transistor level schematic of the proposed 16 Ω driver.

bias circuit. This mismatch results in different channel length modulation and drain induced barrier lowering experienced by these transistors (especially for M1 since it uses minimum length).

The proposed bias generation circuit takes into account the drain voltage of the output transistors M1 and M2 as well as the mirror transistors M3 and M4 (in Fig. 11). This is achieved by diode connecting the copy transistor M1b and M3b via level shifters formed by Mlsb, Ib2 and M3b', Ib3, respectively. In case of M3b, the size of M3b' and Ib3 is designed so that the drain voltage of M3b matches that of M3. For M1b, the drain voltage is set by the sum of Vgs of M1b and that of Mlsb, which was close to the drain voltage of M1 in this design. With this technique, the mirroring error is substantially reduced.

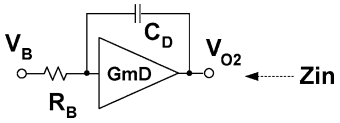

Fig. 12. Proposed damping network.

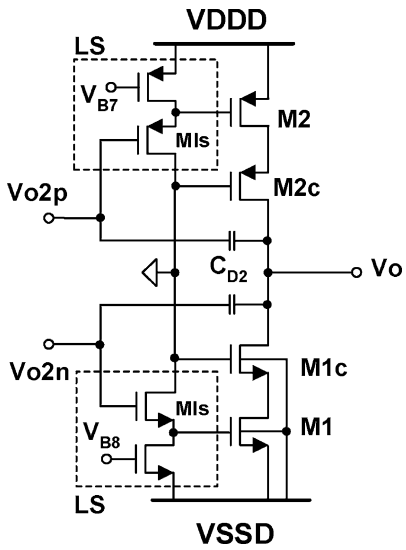

Fig. 13. Schematic of the output stage of the driver.

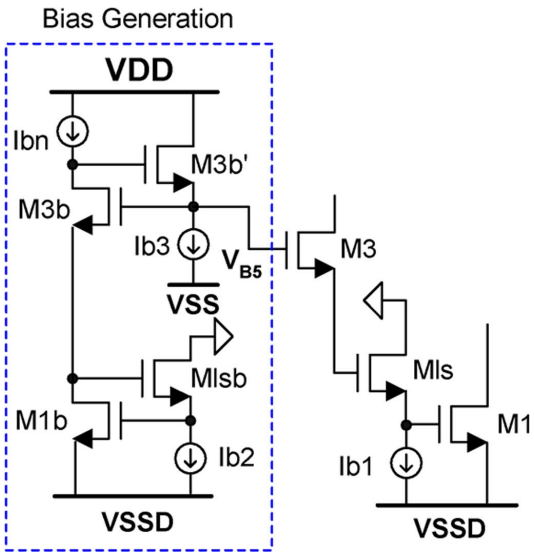

Fig. 14. NMOS part of class-AB bias generation circuit.

V. Experimental Results

The driver prototype was fabricated in UMC 130 nm CMOS technology and packaged in a SOIC20 package. The die photograph with markings of essential circuit components is shown in Fig. 15. The output stage is placed as close to the bond-pad as possible. The power supply and the ground lines of the output stage are double bonded to minimize parasitic resistance. The total layout area occupied by the driver is 0.1 mm^2 (350 μm × 290 μm).

The pulse responses of the driver measured for various load capacitors are shown in Fig. 16. Absence of ringing in all cases

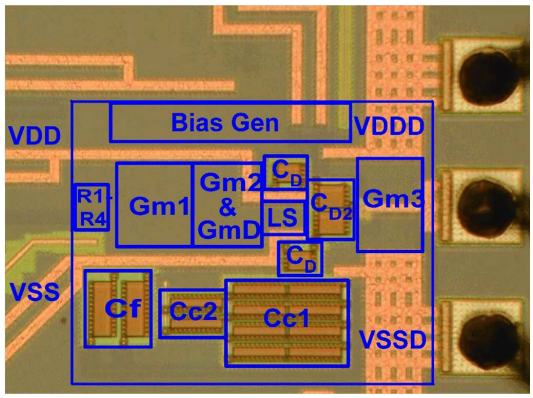

Fig. 15. Micrograph of the test chip.

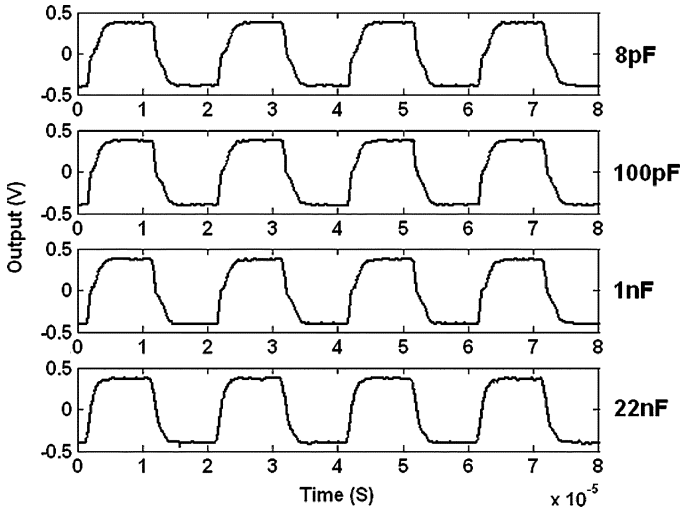

Fig. 16. Pulse response as load capacitance is varied from 8 pF to 22 nF.

confirms the automatic damping control across a wide range of load capacitors. The minimum capacitance in the test setup is limited to 8 pF by the probe capacitance. However, simulations confirm that there is no peaking/ringing behavior even in the case of 1 pF load. The slew rate is limited by the second stage to 0.4 V/μS, which is more than what is required by a full-scale 20 kHz signal. When fast changing input is applied, the second stage output momentarily charges in the opposite direction before returning to slewing state. This effect produces some cross over distortion for fast changing input and is more prominent for smaller load capacitance. This, however, is not an issue for signals in audio frequency range.

Fig. 17 shows the measured FFT of 1.4 Vpp, 1 kHz sine-wave output and the noise floor with zero input condition under 1 nF capacitor load in both cases. A maximum THD of −84.8 dB and a maximum unweighted SNR of 92 dB in 20 Hz–20 kHz bandwidth was measured with 1.6 Vpp 1 kHz tone. Since the headphone outputs are always single-ended, dominant second harmonic distortion is inevitable. Higher harmonics are observed due to small cross-over distortion in the class-AB stage that is unsuppressed by the loop gain.

Fig. 18 shows the THD+N as a function of output signal amplitude for a 1 kHz tone and as a function of frequency for 1.4 Vpp amplitude under 1 nF capacitor load in both cases.

TABLE I
COMPARISON OF MEASUREMENT RESULTS WITH STATE-OF-THE-ART

Parameter	[17]	[4]	[6]	This work
Technology	-	0.35μm CMOS	65nm CMOS (1.2V devices)	130nm CMOS (1.2V devices)
Capacitance load	0-300pF	0-300pF	0-12nF	1pF-22nF
Supply	3.0V	0.8V	2.5V	1.2V/2.0V
Output voltage	2.50Vpp	0.45Vpp	1.85Vpp	1.60Vpp
THD+N @ max. output	-90dB	-69dB	-68dB	-84dB
Total compensation capacitance	-	-	35pF	14pF
Quiescent power	12.0mW	2.5mW	12.5mW	1.2mW
FOM	8.1	1.3	4.3	33.3

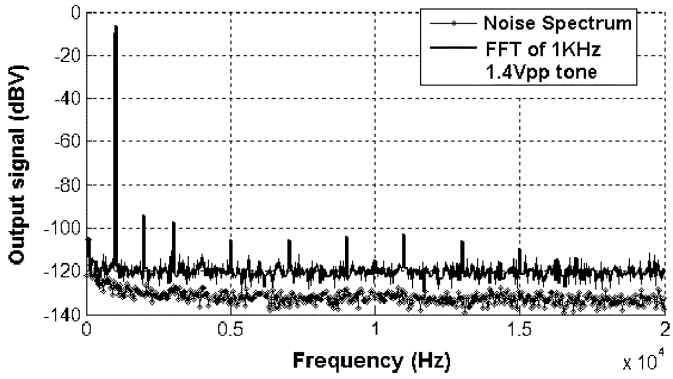

Fig. 17. Spectrum of 1 kHz tone and noise.

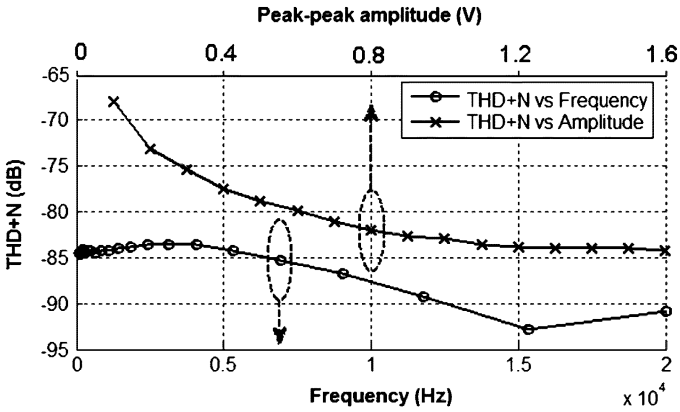

Fig. 18. THD+N across output amplitudes and load capacitances.

For small output amplitude cases, THD+N are limited by the noise and hence the decreasing trend. As expected, the THD+N measurements did not show any appreciable change with load capacitance variation. The output stage and the bias generation loop consume a quiescent current of 400 μA from ± 1 V supply while the rest of the amplifier consumes 330 μA from ± 0.65 V supply, which is intended to be the same supply as the core analog supply.

Some recent headphone driver designs are compared with the presented work in Table I. The quiescent power of the proposed driver is about 1/10th of that reported in [6] and [17]. A figure of merit (FOM) defined as a ratio of the peak power delivered to load to the quiescent power is included in the table. The total compensation capacitors used is less than half of that in [6], which translates to reduced area.

VI. CONCLUSION

A 16 Ω headphone driver design that can handle 1 pF–22 nF of load capacitance was demonstrated. A simple and intuitive method to analyze three-stage amplifiers was described and a load capacitance aware compensation scheme was introduced. Experimental result shows that the proposed driver has significant power efficiency improvement over the state-of-the-art. Since the design uses only the 1.2 V core devices, it may be easily ported to a smaller feature size technology.

APPENDIX A

The power efficiency $(\mathrm{P_{EFF}})$ of the class-AB stage is defined as the ratio of the average power delivered to the load $(\mathrm{P_L})$ to the average power dissipated from the supplies $(\mathrm{P_{AVG}})$. With the simplifying assumption of rail-to-rail output voltage swing, the $\mathrm{P_{AVG}}$ is given by

$$\mathrm{P_{AVG}} = \frac{\mathrm{V_P^2}}{\mathrm{CF} * \mathrm{R}} + 2\mathrm{V_P I_Q} \tag{A.1}$$

where $\mathrm{V_P}$ is the peak output voltage, $\mathrm{I_Q}$ is the quiescent current, R is the load resistance and CF is the crest factor of the waveform. The first term of $\mathrm{P_{AVG}}$ represents the signal dependant power dissipation, which is a product of supply voltage (positive and negative) of the class-AB stage $(\mathrm{V_P})$ and the average load current $(\mathrm{V_P}/(\mathrm{CF} * \mathrm{R}))$. The second term represents the power due to the quiescent current used to bias the class-AB stage.

Since $\mathrm{V_P}/\mathrm{CF}$ is the RMS output voltage, $\mathrm{P_L}$ is given by

$$\mathrm{P_L} = \frac{\mathrm{V_P^2}}{\mathrm{CF}^2 * \mathrm{R}}. \tag{A.2}$$

If the peak current delivered to the load is represented by $\mathrm{I_P} = \mathrm{V_P}/\mathrm{R}, \mathrm{P_{EFF}}$ can be expressed as

$$\mathrm{P_{EFF}} = \frac{1}{\mathrm{CF}\,(1 + 2\mathrm{CF}(\mathrm{I_Q}/\mathrm{I_P}))}. \tag{A.3}$$

APPENDIX B

Formal Verification of the Proposed Equivalent Circuit: Consider the general representation of a feedback gain stage driven by a current source as shown in Fig. 19(a). Using node analysis, the following expressions can be written:

$$\mathrm{V_{O1}}(\mathrm{Y_I} + \mathrm{Y_{FB}}) - \mathrm{Y_{FB}V_O} = \mathrm{I_I} \tag{B.1}$$

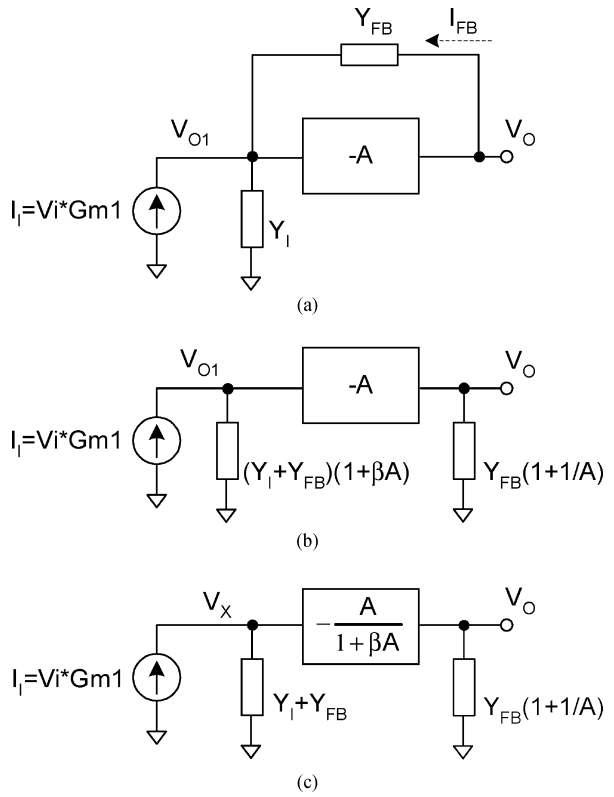

Fig. 19. Verification of the proposed equivalent circuit.

$$\mathrm{Y_{FB}V_O} - \mathrm{Y_{FB}V_{O1}} = \mathrm{I_{FB}} \tag{B.2}$$

$$\mathrm{V_O} = -\mathrm{AV_{O1}}. \tag{B.3}$$

Solving (B.1) to (B.3) leads to (B.4) and (B.5)

$$\mathrm{V_{O1}} = \frac{\mathrm{I_I}}{1+\mathrm{A}\beta}\frac{1}{\mathrm{Y_{FB}}+\mathrm{Y_I}} \tag{B.4}$$

where β is defined as $\mathrm{Y_{FB}}/(\mathrm{Y_{FB}}+\mathrm{Y_I})$

$$\mathrm{I_{FB}} = \left(1+\frac{1}{\mathrm{A}}\right)\mathrm{Y_{FB}V_O}. \tag{B.5}$$

Based on (B.4) and (B.5), Fig. 19(a) can be redrawn as shown in Fig. 19(b). This circuit can be modified to a node scaled version in Fig. 19(c) by reducing the gain term A to $\mathrm{A}/(1+\mathrm{A}\beta)$ and increasing the voltage at $\mathrm{V_{O1}}$ to $\mathrm{V_X} = (1+\mathrm{A}\beta) * \mathrm{V_{O1}}$. The second step is achieved by simply replacing the admittance $(\mathrm{Y_I}+\mathrm{Y_{FB}}) * (1+\mathrm{A}\beta)$ with $\mathrm{Y_I}+\mathrm{Y_{FB}}$.

There are two admittance components at the output node $\mathrm{V_O}$ in Fig. 19(b). The $\mathrm{Y_{FB}/A}$ component is manifestation of the feedforward current produced by the voltage at $\mathrm{V_{O1}}$ on $\mathrm{Y_{FB}}$. Due to the assumption of insignificant feedforward current in the concerned frequency range, this component can be dropped. The remaining $\mathrm{Y_{FB}}$ component of the admittance can be merged with the load or simply ignored if it is substantially smaller than the load admittance. Also, note that $\mathrm{Y_I} \ll \mathrm{Y_{FB}}$ leads to the unity feedback case ($\beta = 1$). Hence the equivalent circuits presented in Figs. 2 and 5 are formally verified.

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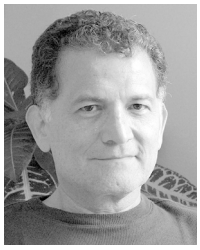

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