Low Voltage Analog Circuit Design Techniques:

A Tutorial

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Low Voltage Analog Circuit Design Techniques: Roadmap

Low voltage (LV) power supply circuit design techniques are addressed in this tutorial. In particular:

(i) Introduction;

(ii) Transistor models capable to provide performance and power consumption tradeoffs;

(iii) Low voltage implementation techniques, such as floating gates and bulk driven;

(iv) Basic building blocks not involving cascode structures, and

(v) LV circuit implementations examples.

Motivation

The need for analog circuits in modern mixed-signal VLSI chips for multimedia, perception, control, instrumentation medical electronics and telecommunication is very high.

- What are the challenges in designing low voltage circuits ?
  - To operate with power supplies smaller than 3.3 volts
  - To design circuits with the same performance or better than circuits designed for larger power supplies
  - To perform with technologies smaller than 0.5 micron
  - To come with new design alternatives,

(continues)

- Why are we concerned in designing low voltage circuits ?

  - Designers can not use conventional cascode structures, and other conventional design methodologies.

  - Circuits should have the same performance or better than circuits designed for larger power supplies

  - Circuit performance with technologies smaller than 0.5um must be better than circuits for larger technologies.

  -Third-generation communication applications require circuits (and systems) with improved dynamic range over a much wider bandwidth.

  - New building blocks and system must be designed to satisfy the needs of portable, lighter and faster equipment

Issues about low power supply voltage

Scaling down size technology and supply voltage does not scale linearly the " V_{TH} hat "

Mister 5 volts IC

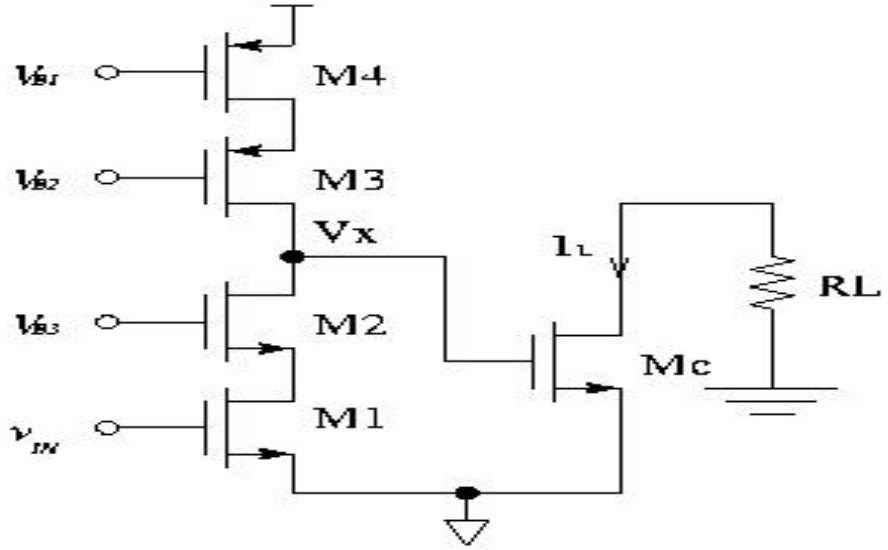
Mister 0.8 volts IC

Challenges of Low Voltage Analog Circuit Design

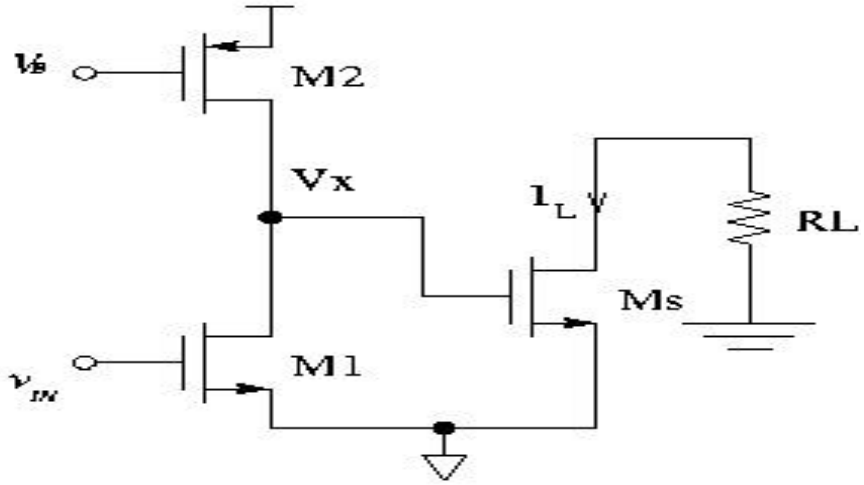
• Threshold and V_{DSAT} do not scale down linearly with power supply nor with smaller size technologies.

• Let us consider an illustrative example of a cascode and a simple inverting amplifiers, assume transistors M_C and M_S carry the same current I_L, V_T= 0.75V and $V_{DS(SAT)}$=0.2V

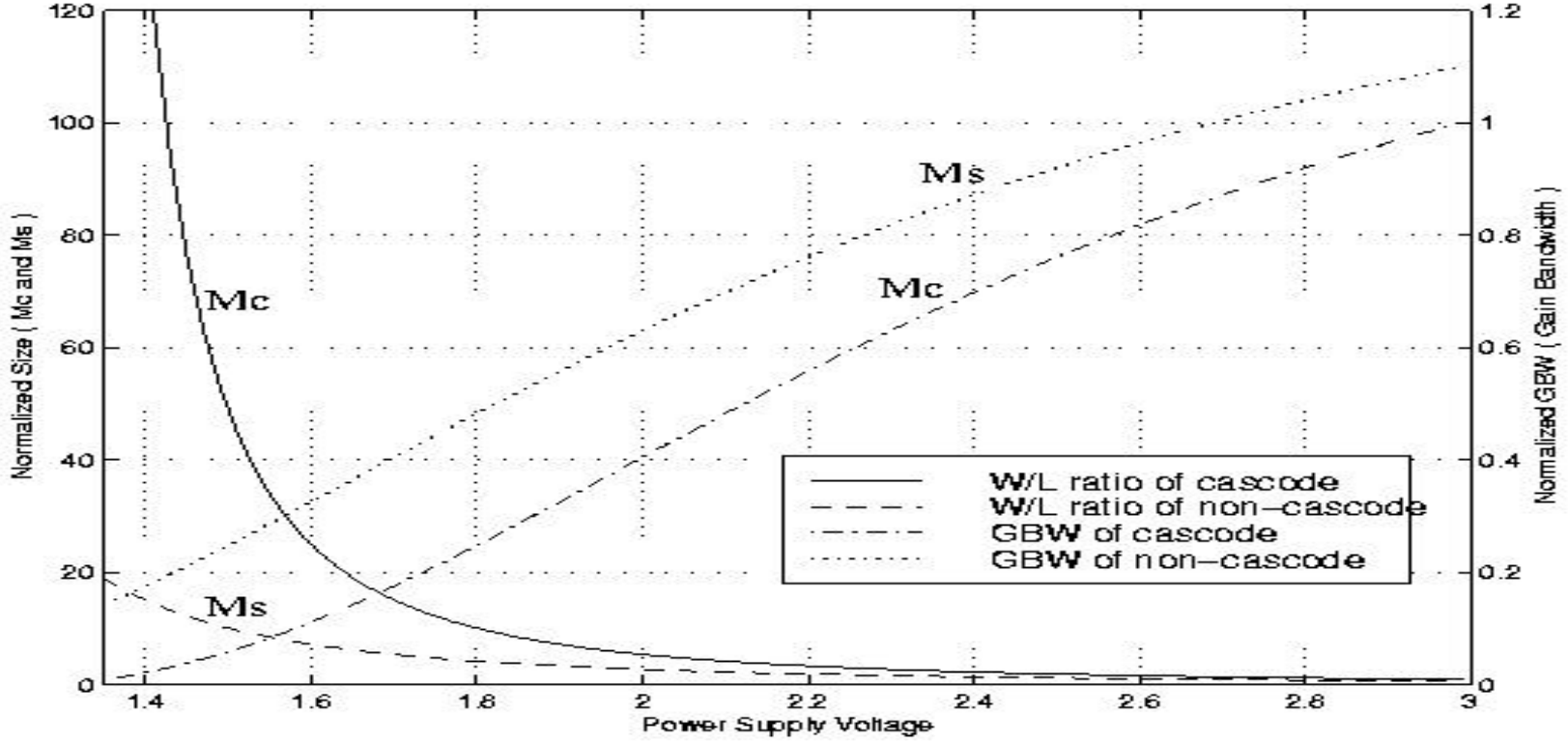
• Keeping the same output voltage swing for both circuits involve the tradeoffs shown in the plot of transistor sizes and GBW vs. Power Supply Voltage


M4
M3
Vx
M2
M1
Mc
RL

(a)


M2
Vx
M1
Ms
RL

(b)


Normalized Size (Mc and Ms)
Normalized GBW (Gain Bandwidth)
Power Supply Voltage
Mc
Ms
W/L ratio of cascode
W/L ratio of non-cascode
GBW of cascode
GBW of non-cascode

(c)

Transistor Regions of Operation

- How to determine how much bias current is needed for certain application ?

- When a designer operates transistors in saturation, what does it mean $V_{DS} > V_{DS(SAT)}$?

- Can a circuit have their transistors operating in the transition region ? What transistor model equation can be employed ?

One Equation-All Regions Transistor Model

- Features of ACM model:
  - physics-based model,
  - universal and continuous expression for any inversion,
  - independent of technology, temperature, geometry and gate voltage,
  - same model for analysis, characterization and design.
- Main design equations: (design parameters: I, g_m, i_f)

$$\frac{I}{\phi_t g_m n} = \frac{1+\sqrt{1+i_f}}{2}$$

$$f_T = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right)$$

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox}\phi_t} \frac{1}{\sqrt{1+i_f}-1}$$

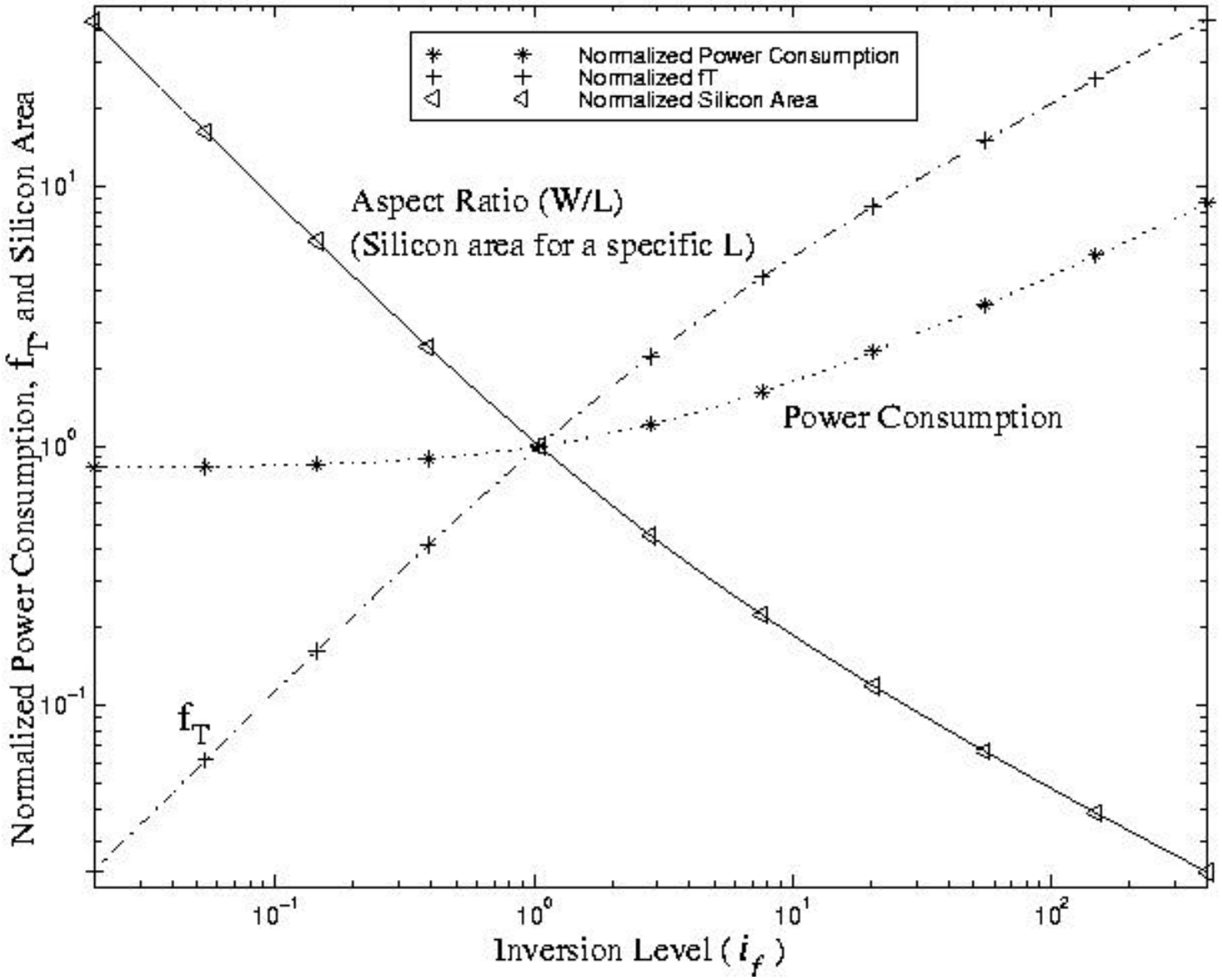
$$\frac{V_{DSAT}}{\phi_t} \cong \left(\sqrt{1+i_f}-1\right)+4$$

$$\frac{W}{L} = \frac{g_m}{2\mu C_{ox}\phi_t\left(\frac{I}{\phi_t g_m n}-1\right)}$$

I — drain current in transistor
g_m — transconductance in saturation
n — slope factor
ϕ_t — thermal voltage
i_f — inversion level of the transistor defined as $i_f = I/I_s$, where $I_s = \mu n C_{ox} \frac{\phi_t^2}{2}\frac{W}{L}$ is the normalization current.

$i_f << 1$ — weak inversion,

$i_f >> 1$ — strong inversion.


Normalized Power Consumption
Normalized fT
Normalized Silicon Area
Aspect Ratio (W/L)
(Silicon area for a specific L)
Power Consumption
f_T
Normalized Power Consumption, f_T, and Silicon Area
Inversion Level (i_f)
10^{-1}
10^{0}
10^{1}
10^{2}

Normalized Current

$$i_f = \frac{I_D}{I_S}$$

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L}$$

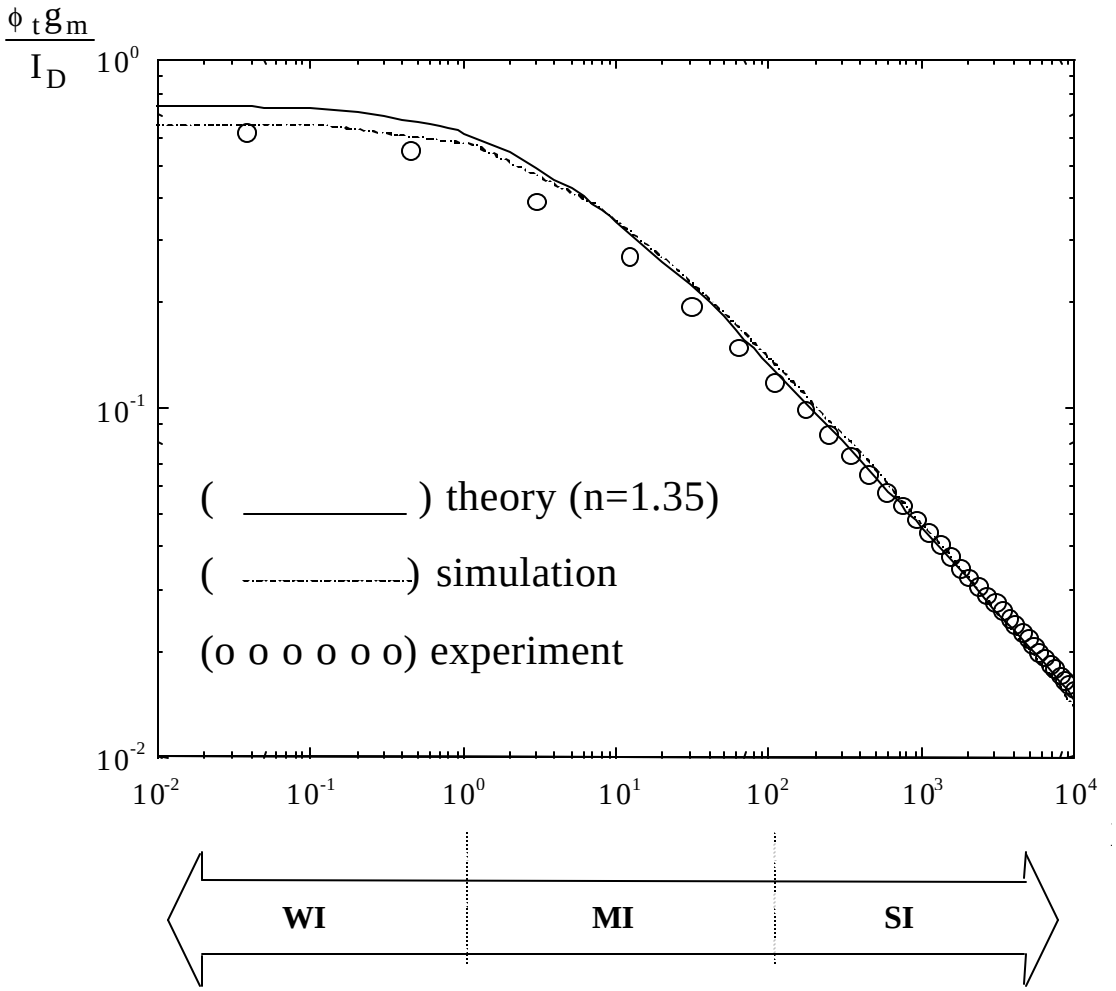
I_D: saturation current

I_S: normalization current

n: slope factor

Transconductance-to-Current Ratio

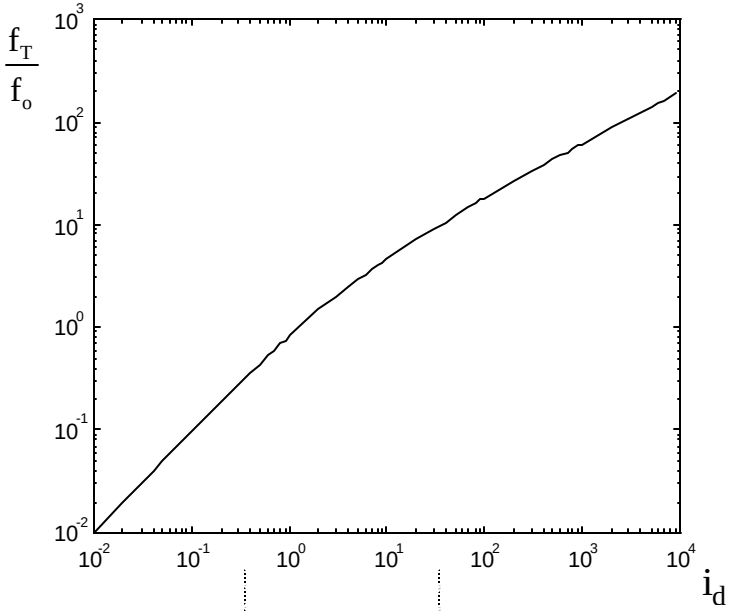
$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_d}}$$

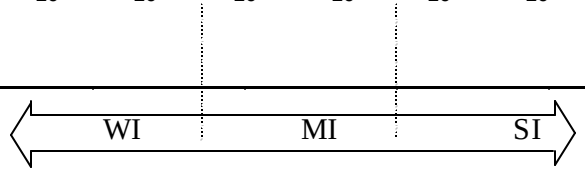


The intrinsic cutoff frequency

$$f_T \cong f_o 2\left(\sqrt{1+i_f}-1\right)$$

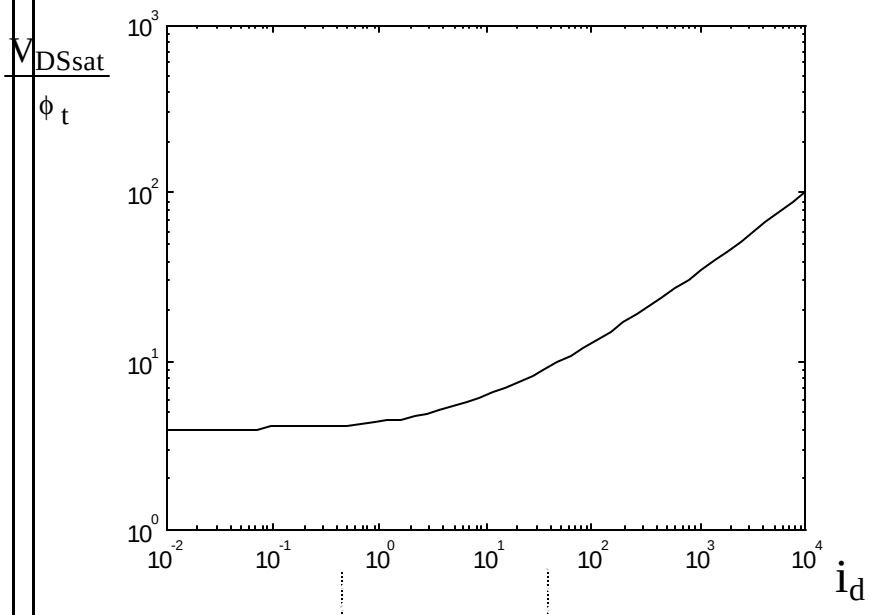
$$f_o = \frac{\mu \phi_t}{2\pi L^2}$$

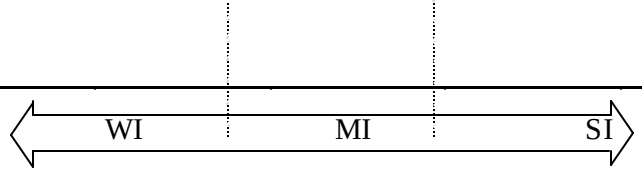




Drain-to-source saturation voltage

$$\frac{V_{DSsat}}{\phi_t} \cong \left(\sqrt{1+i_f}-1\right)+4$$





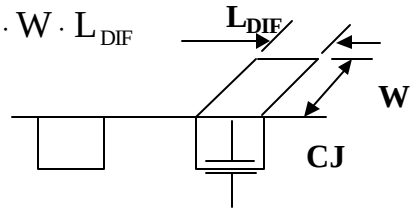
Correlation Between Area and Frequency Response

$$WL \cong 2\frac{CL}{C'_{ox}}\frac{GBW}{f_T}$$

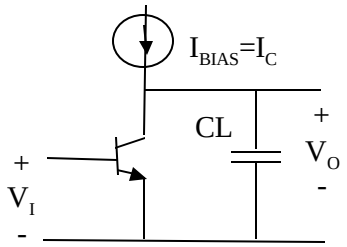
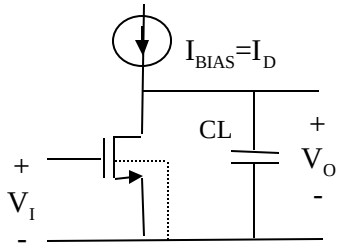
Correlation Between Junction Capacitance (CJ) and Frequency Response

Parasitic capacitance α GBW/f_T

$$CJ = CJ' \cdot W \cdot L_{DIF}$$



$$\frac{CJ}{CL} \cong 2\frac{CJ'}{C'_{ox}}\frac{L_{DIF}}{L}\frac{GBW}{f_T}$$

	BIPOLAR	MOS
DC Circuit		
Transconductance-to-current-ratio (g_m/I_D)	$\frac{g_m}{I_C} = \frac{1}{\phi_t}$	$\frac{g_m}{I_D} = \frac{1}{\phi_t}\left(\frac{2}{n\left(1+\sqrt{1+i_d}\right)}\right)$
DC Gain (A_{vo})	$A_{vo} = -\frac{VA}{\phi_t}$	$A_{vo} = -\frac{VA}{\phi_t}\left(\frac{2}{n\left(1+\sqrt{1+i_d}\right)}\right)$
Gain-Bandwidth Product (GBW)	$GBW = \frac{1}{2\pi CL}\frac{I_C}{\phi_t}$	$GBW = \frac{1}{2\pi CL}\frac{I_D}{\phi_t}\left(\frac{2}{n\left(1+\sqrt{1+i_d}\right)}\right)$
Intrinsic Cutoff Frequency (f_T)	$f_T \cong \frac{1}{2\pi\tau}$	$f_T \cong \frac{1}{2\pi\tau}2\left(\sqrt{1+i_d}-1\right)$
Minimum Output Voltage (V_O)	$\frac{V_{CEsat}}{\phi_t} \cong 6 \text{ to } 8$	$\frac{V_{DSsat}}{\phi_t} = \left(\sqrt{1+i_d}-1\right)+4$

Low Voltage Analog Circuit Design Techniques: Roadmap

Low voltage (LV) power supply circuit design techniques are addressed in this tutorial. In particular:

(i) Introduction;

(ii) Transistor models capable to provide performance and power consumption tradeoffs;

(iii) Low voltage implementation techniques, such as floating gates, self-cascode, low voltage current-mirrors and bulk driven;

(iv) Basic building blocks not involving cascode structures, and

(v) LV circuit implementations examples.

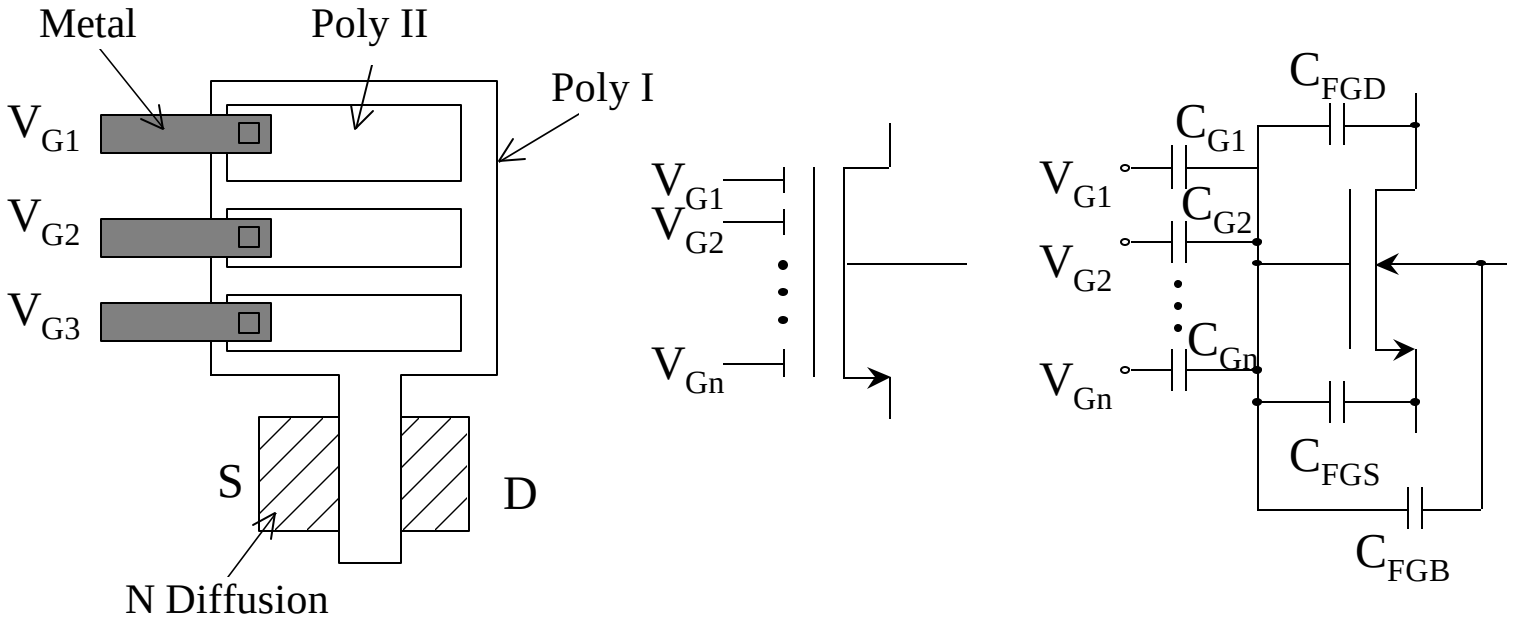
Floating Gate Transistors

The floating gate voltage V_F ,assuming that the initial charge Q_F in the floating gate is zero, is described by:

$$\mathbf{V_F = w_0V_0 + w_1V_1 + w_2V_2 + ... + w_nV_n}$$

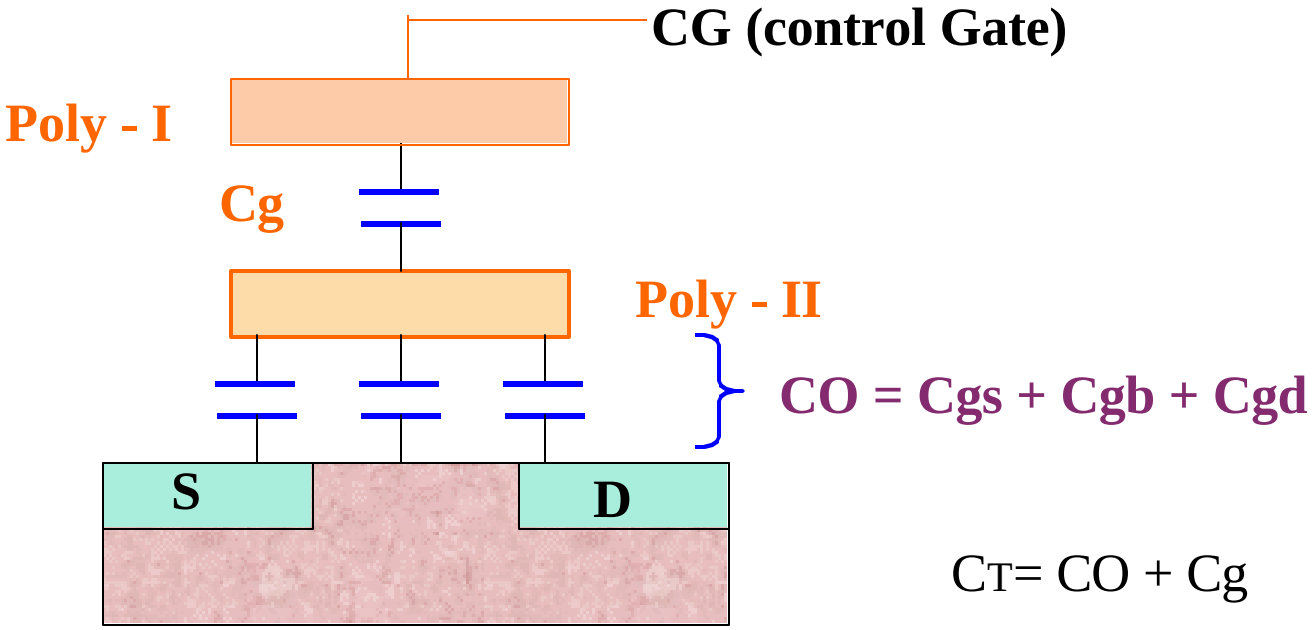
Where $w_i = C_i/C_{TOT}$

$C_{TOT} = C_0 + C_1 + C_2 + ... + C_n$



(a) Layout **(b)** Schematic Symbol **(c)** Equivalent Circuit

Floating Gate MOS Transistors



$C_T = CO + Cg$

Assuming Cg >> Cgd,Cgb, an approximate I_{DS} can be obtained:

$I_{DS} = K^o_{eff}[(V_{CGS} - V_{T,eff})V_{DS} - C_T V_{DS}^2/2Cg]$ ohmic

$I_{DS} = K^s_{eff}(V_{CGS} - V_{T,eff})^2$ saturation

Where: $V_{T,eff} = V_{TCO} - Q_{FG}/Cg$

$K^o_{eff} = Kp(Cg/C_T)(W/L)$, $K^s_{eff} = Kp(Cg/C_T)^2(W/L)$,

What is the effect of the FG on the transconductance and the output conductance, in the saturation region ?

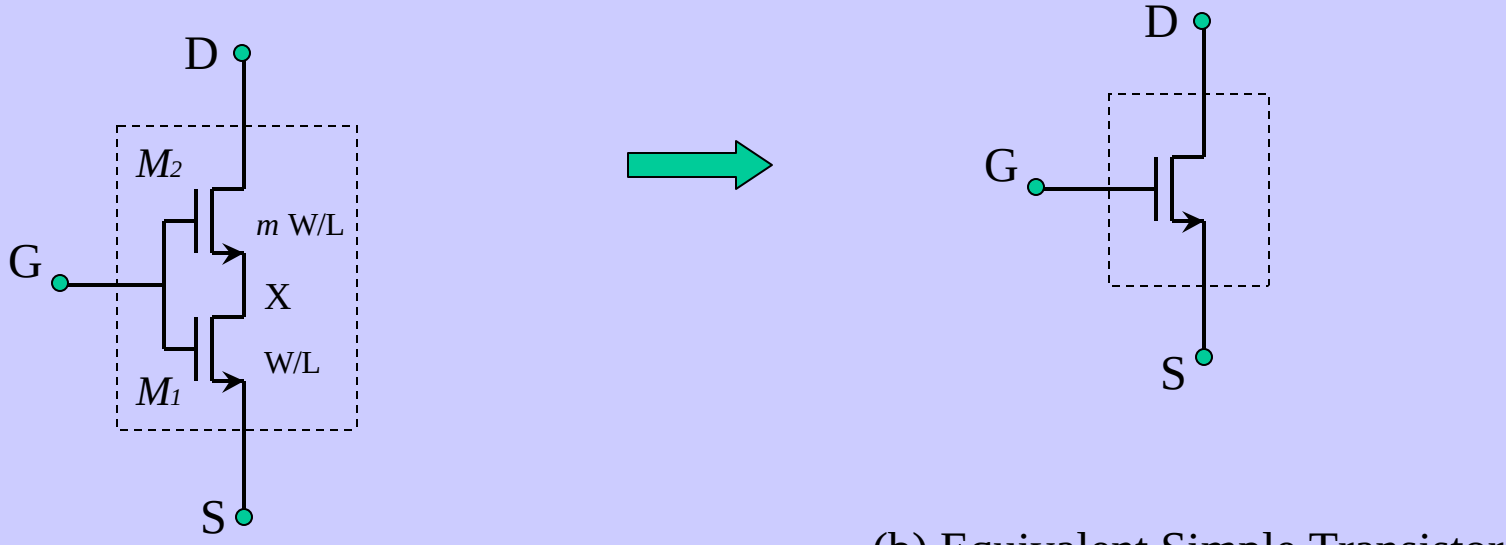
$$g_m = (2K^2_{eff} I_{DS})^2 = C_g g^c_m / C_T$$

$$g_o = g^c_o + C_{gd} g_m / C_g$$

Where g^c_m and g^c_o are the conventional transconductance and the output conductance of the conventional MOS transistor.

Thus, the FGT has a smaller transconductance and a larger output conductance than conventional MOS transistor

What is a Self-Cascode Composite Transistor?



(a) Self-Cascode Composite NMOS Transistor

(b) Equivalent Simple Transistor

In practical cases, for optimal operation the W/L ratio of M_2 should be larger than that of M_1, *i.e.* $m>1$.

The 2-transistor structure can be treated as a composite transistor, which has a much larger effective channel length (thus lower output conductance).

The lower transistor M_1 is equivalent to a resistor, but this resistor is input dependent..

The effective transconductance of the composite transistor is approximately equal to the transconctance of M_1: $gm_{\_eff} = gm2/m = gm1$

Equivalent Transistor Parameter

For the composite transistor work in saturation region, we know M_2 should in saturation and M_1 is in linear region. Thus, we can write equations for these two transistors as:

$$i_1 = \frac{\beta_2}{2}(V_{GS} - V_X - V_T)^2 \qquad i_1 = \beta_1\left(V_{GS} - V_T - \frac{1}{2}V_X\right)V_X$$

Solving i_1 we can obtain:

$$i_2 = \frac{1}{2}\frac{\beta_2\beta_1}{\beta_2 + \beta_1}(V_{GS} - V_T)^2$$

From (3), we have $\beta_{eq} = \dfrac{\beta_2\beta_1}{\beta_2 + \beta_1}$

If $\beta_2 = m \cdot \beta_1$ $\qquad \beta_{eq} = \dfrac{m}{m+1}\beta_1 = \dfrac{1}{m+1}\beta_2$

$$\Rightarrow \quad \beta_{eq}\Big|_{m->\infty} = \beta_1$$

Comments on V_{DSAT}

Because transistor M_1 always operates in linear region while the top transistor operates in saturation or linear region. Voltage between the source and drain terminal of M_1 is so small that there is no discernable V_{DSAT} difference in both the composite and simple transistors. Thus,self-cascode structure can be used in ***low voltage applications***.

$$V_{DSAT-eq} = V_{DSAT-M2} + V_{DS-M1} = V_{DSAT-M2} + I_{D2}R_{M1}$$

where $$R_{M1} = \frac{1}{\mu C_{OX}(V_{GS} - V_T)\frac{W}{L}}$$

The operating voltage of a regular cascode circuit is much higher than that of a single transistor. This characteristic makes regular cascode circuit not suitable for low voltage applications.

References

1. C. Galup-Montoro, etc., “Series-Parallel Association of FET’s for High Gain and High Frequency Applications”, *IEEE JSSC*, Sept. 1994

2. D. Ceuster, etc., “Improvement of SOI MOS current-mirror performances using serial-parallel association of transistors”, *Electronics Letters*, Feb. 1996

3. P. Furth, H. Om’mani, “A 500-nW Floating-Gate Amplifier with Programmable Gain”, IEEE 1999

4. I. Fujimori, T. Sugimoto, “A 1.5V, 4.1mW Dual-Channel Audio Delta-Sigma D/A Converter”, *IEEE JSSC*, Dec. 1998

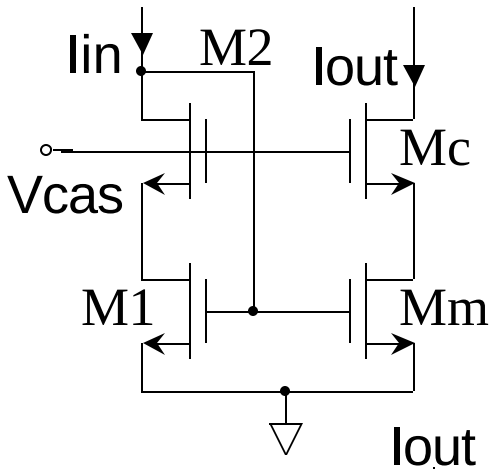
5. Personal note from Dr. Ugur Cilingiroglu

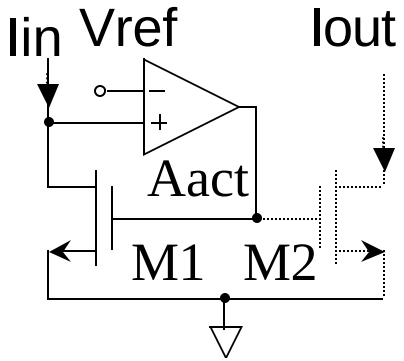
6. Yunchu Li, examples and SPICE tables

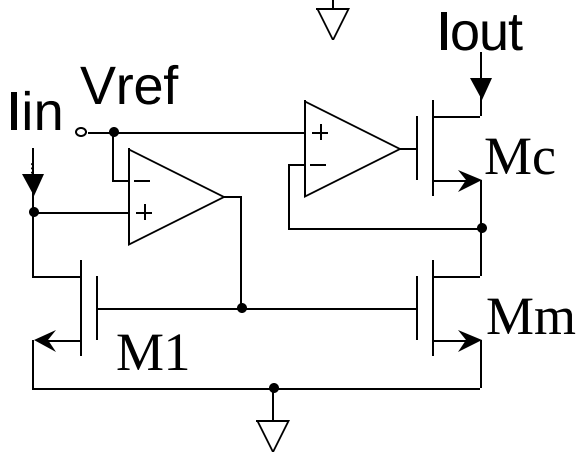
7. A.I.A. Cunha, M.C. Schneider, and C. Galup-Montoro, “An MOS transistor model for analog circuit design”, *IEEE J. Solid-State Circuits*, vol. 33, No. 10, pp 1510-1519, Oct. 1998

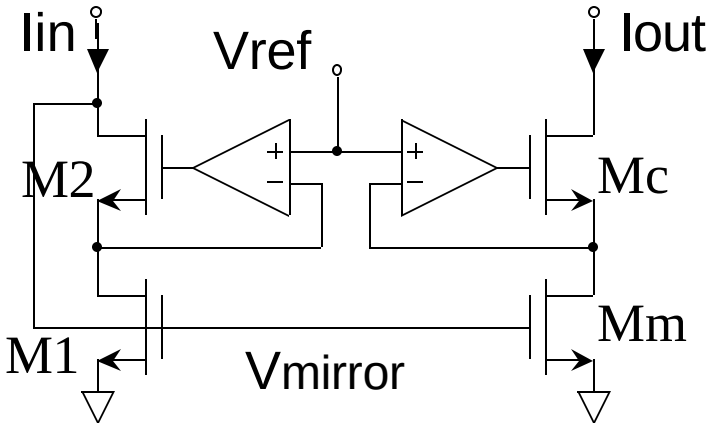
Potential LV Current-Mirrors

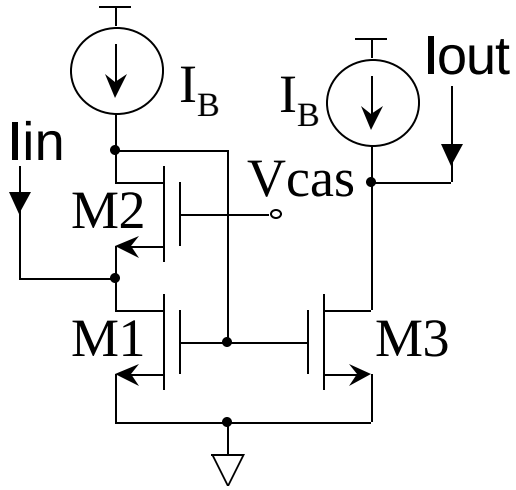
Goals: To reduce the input impedance and to increase the output impedance, while keeping the voltage operation

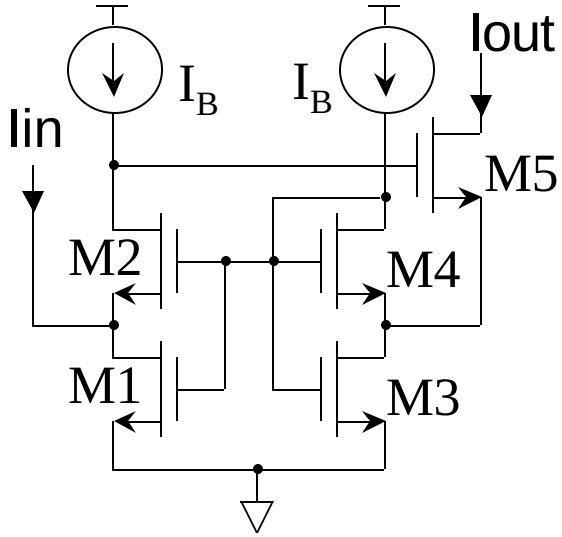


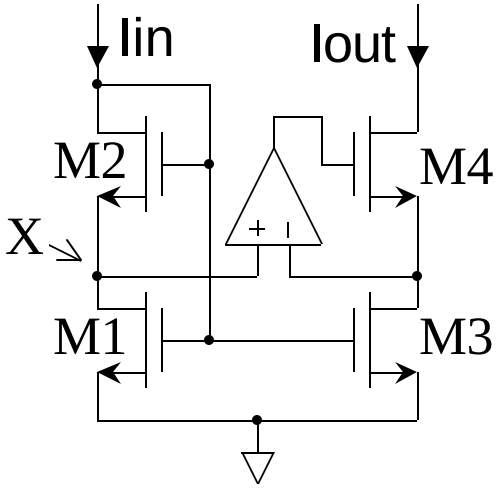


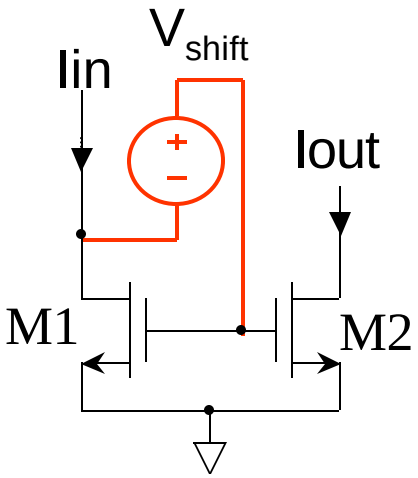


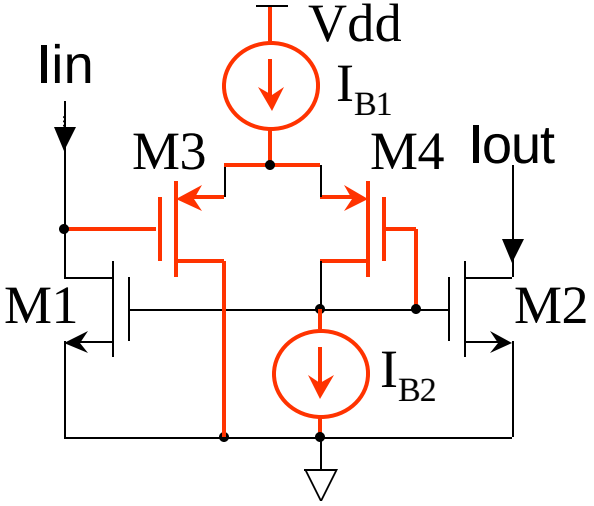


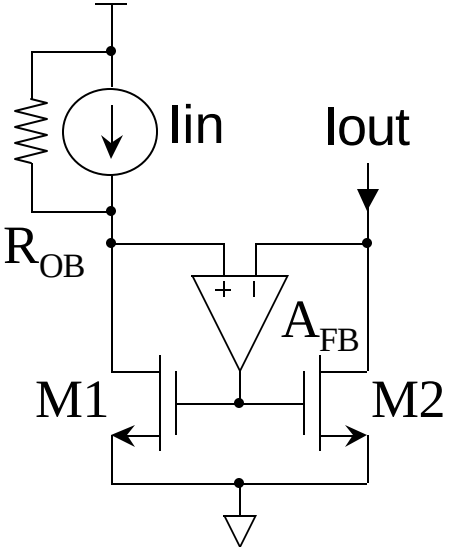

Iin
I_B
I_B
Iout
Vcas
M2
M1
M3


I_B
I_B
Iout
Iin
M5
M2
M4
M1
M3

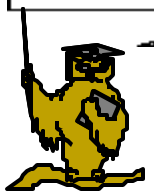

Iin
Iout
M2
M4
X
M1
M3


V_{shift}
Iin
Iout
M1
M2

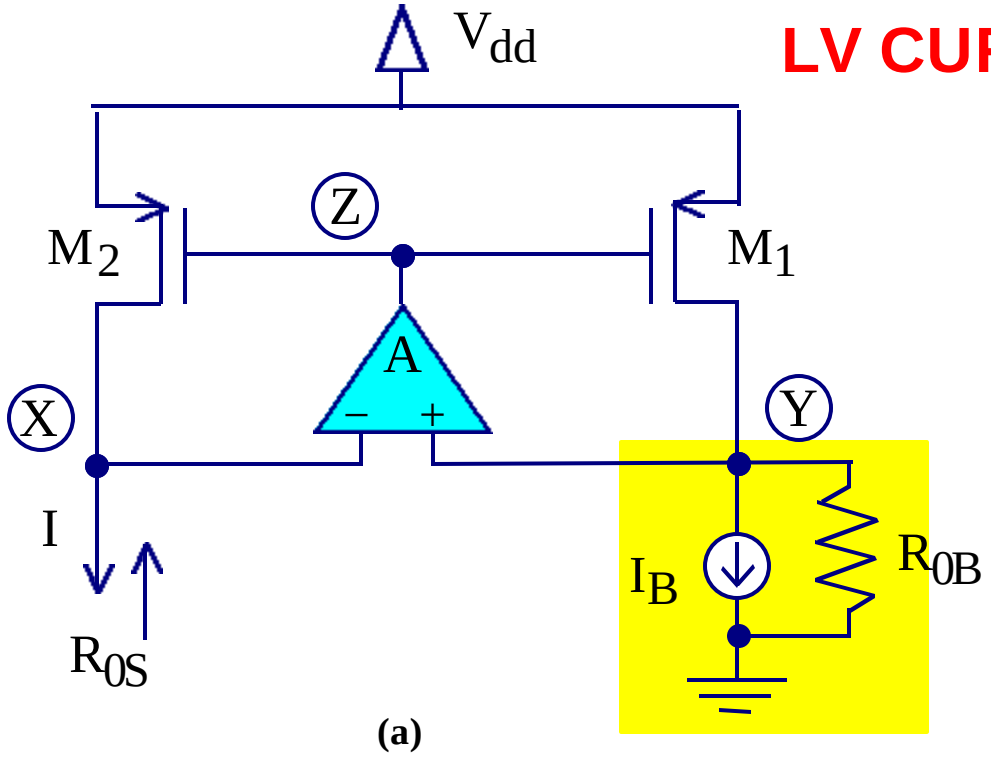

Vdd
Iin
I_{B1}
M3
M4
Iout
M1
M2
I_{B2}

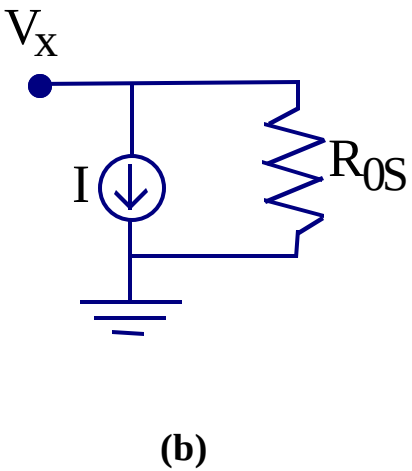

Iin
Iout
R_{OB}
A_{FB}
M1
M2

How can we obtain a large impedance and low head room for the tail current used in a differential pair ?



LV CURRENT-SOURCE





A conceptual Schematic of the low voltage current source. (a) Current source representation (b) Architecture

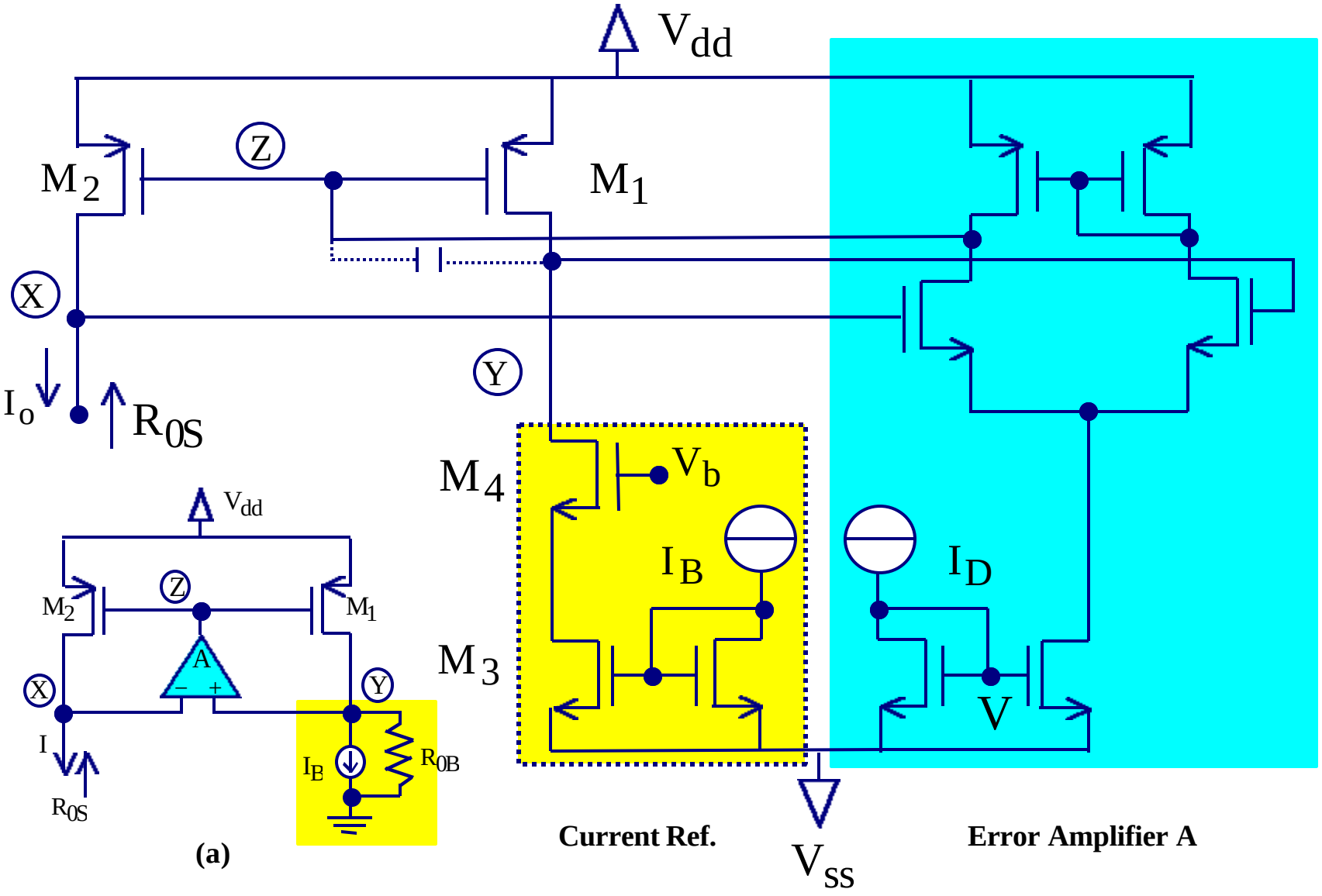
$$R_{os} = \frac{1 + g_{m1}A_o/(g_{o1} + g_{oB})}{g_{o2}(1 + A_o g_{m1}/(g_{o1} + g_{oB}) - A_o g_{m2}/g_{o2})} \quad (1)$$

where $g_{m1}(g_{m2}), g_{o1}(g_{o2})$ are the transconductance and output conductance of $M_1(M_2)$, respectively. A_o is the DC gain of the error amplifier "A" and $g_{oB}(R_{oB})$ is the output conductance (resistance) of the reference current source I_B. Assuming that $g_{m1} = g_{m2}$ and $g_{o1} = g_{o2}$, equation (1) can be simplified as:

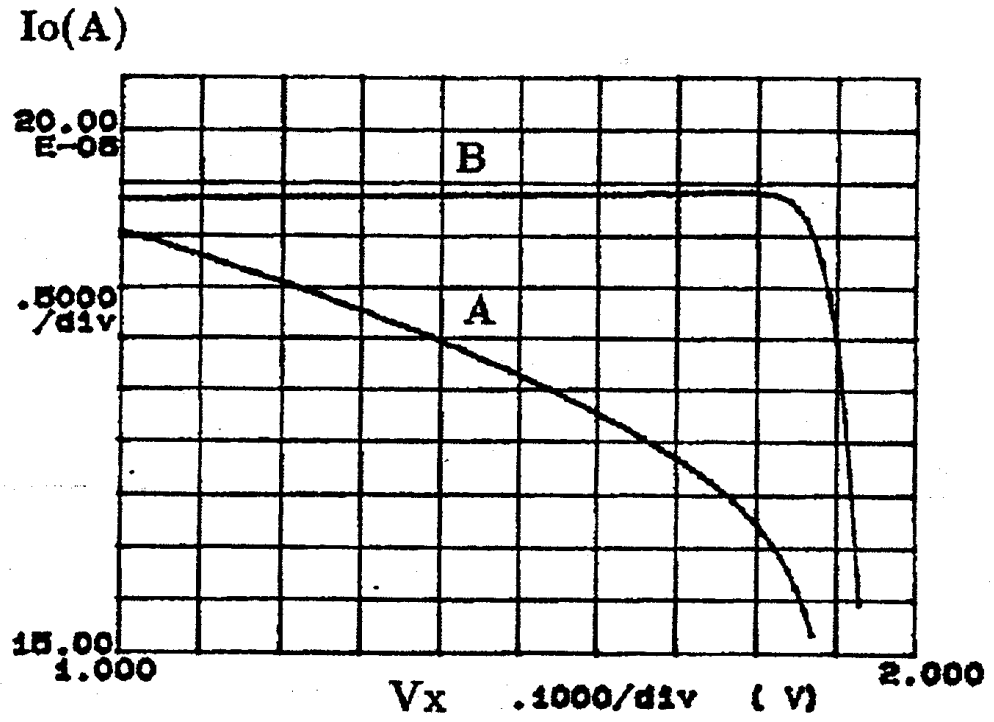
$$R_{os} \approx -R_{oB} \quad (2)$$

Note that the resistance is negative and is equal to the resistance of the reference source I_B.

$$R_{os} \approx -\frac{g_{m4}}{g_{o3}g_{o4}} \quad (3)$$



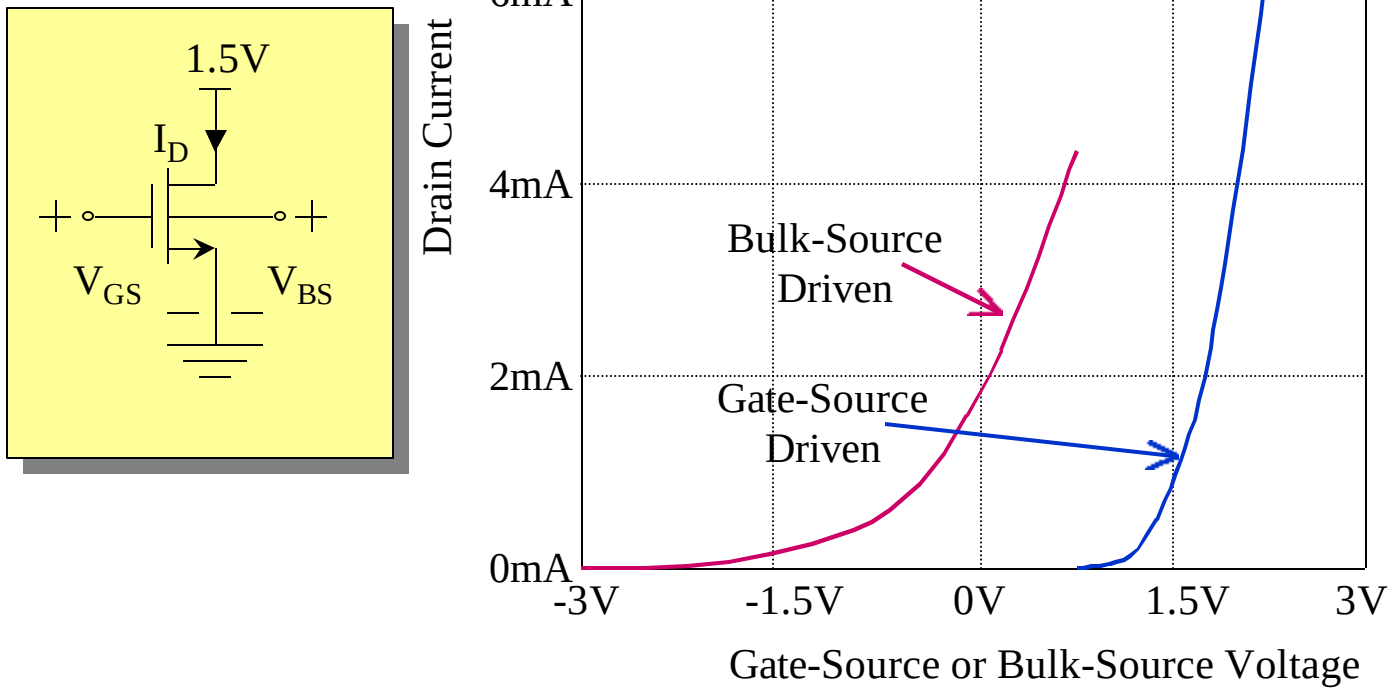
Full implementation of the LV current source.



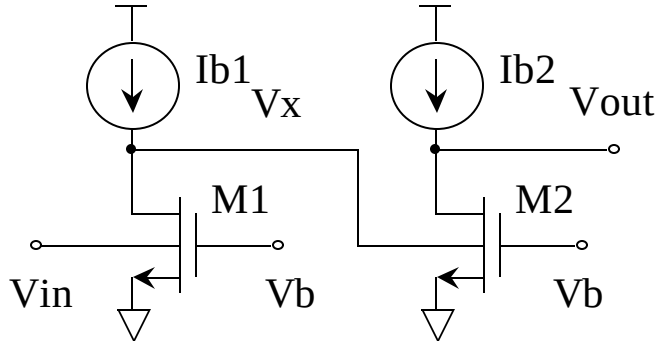
Measured output current of the simple (curve A) and LV (Curve B) current source.

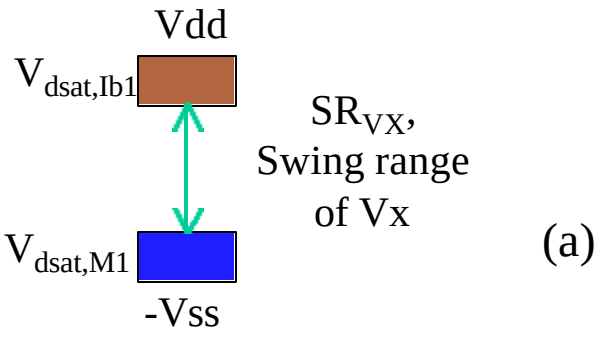
Bulk-Driven MOS Transistor Characteristics

- I_D vs. V_{BS} or V_{GS} of bulk-driven and conventional gate-driven MOS transistors



Overhead of Bulk-Driven MOS Transistors

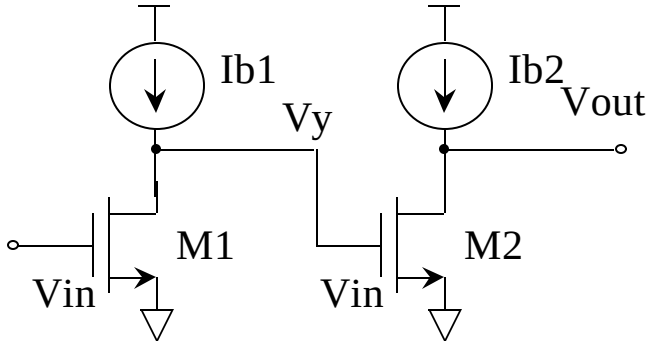


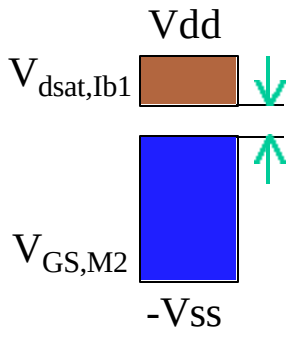


SR_{VX}, Swing range of Vx

(a)

$SR_{VX}=V_{sup}-V_{dsat,Ib1}-V_{dsat,M1}$





Swing range of Vy

(b)

$SR_{VY}=V_{sup}-V_{dsat,Ib1}-V_{GS,M2}$

$= V_{sup}-V_{dsat,Ib1}-V_{dsat,M2}-V_T$

The bulk-driven amplifier is more suitable for low voltage operation. Please notice that the maximum allowable voltage at Vx is V_{DIODE}.

Advantages of Bulk-Driven MOS Transistors

- The depletion characteristic allows zero, negative, and even small positive values of bias voltage to achieve the desired dc current. This can lead to larger input common mode voltage range and voltage swing that could not otherwise be achieved at low power supply voltages. (Please refer the following example in this section and bulk-driven differential pair discussed in following sections)
- We can use the conventional gate to modulate the bulk-driven MOS transistor.

- Example

  Assume for the low voltage amplifiers, power supply voltage is

  $V_{sup} = Vdd + |Vss| < V_{DIODE} + V_{dsat}$,

  where V_{DIODE} is the forward Si diode cut-in voltage.

  The voltage swing of Vx (Figure a, the amplifier with bulk-driven MOS FETs) has only $2V_{dsat}$'s decrease over V_{sup}. In such a low voltage, the conventional gate-driven amplifier (Figure b) fails to operate or may be greatly limited in voltage swing.

Disadvantages of Bulk-Driven MOS Transistors

- The transconductance of a bulk-driven MOS FET is substantially smaller than a conventional gate-driven MOS transistor. This may result in lower GBW and worse frequency response, but better linearity and smaller power supply requirements.
- For a conventional gate-driven MOSFET, the frequency response capacity is described by its transitional frequency, f_T,

$$f_{T,gate-driven} = \frac{g_m}{2\pi C_{gs}}$$

- For the bulk-driven MOSFET, f_T is given by

$$f_{T,bulk-driven} = \frac{g_{mb}}{2\pi (C_{bs} + C_{bsub})} = \frac{\eta g_m}{2\pi (C_{bs} + C_{bsub})}$$

where η is the ratio of g_{mb} to g_m and typically has a value in the range of 0.2 to 0.4.

Disadvantages of Bulk-Driven MOS Transistors (*cont'd*)

- For typical saturated strong inversion MOSFET operation, the following approximation stands,

$$f_{T,bulk-driven} \approx \frac{\eta}{3.8} f_{T,gate-driven}$$

- Another disadvantage of bulk-driven MOSFETs is that the polarity of the bulk-driven MOSFETs is process related. For an P well CMOS process, we only have N channel bulk-driven MOSFETs available, and for N well CMOS process, only P channel MOSFETs. This limits its application. We can not use bulk-driven MOS transistors in some circuit structures which requires both N and P MOSFETs.

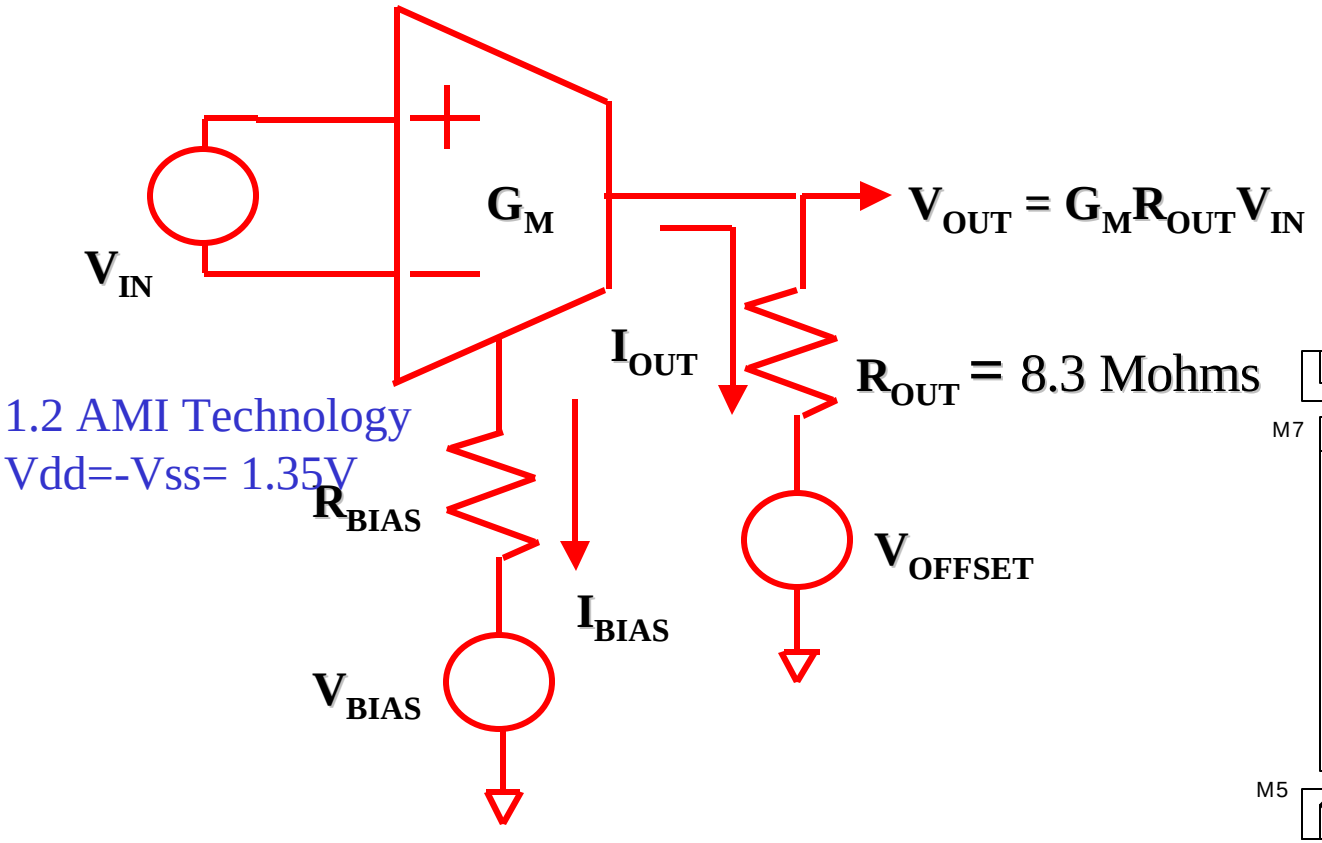
Disadvantages of Bulk-Driven MOS Transistors (*cont'd*)

- MOS transistors can be laid out in the same well, thus their characteristics will match better. Bulk driven transistors are in differential wells, it is inconvenient to design some circuits which require tight matching between transistors. For bulk-driven MOSFETs, it is not easy to utilize some layout techniques such as interdigitized and common centroid layout to make good matching.

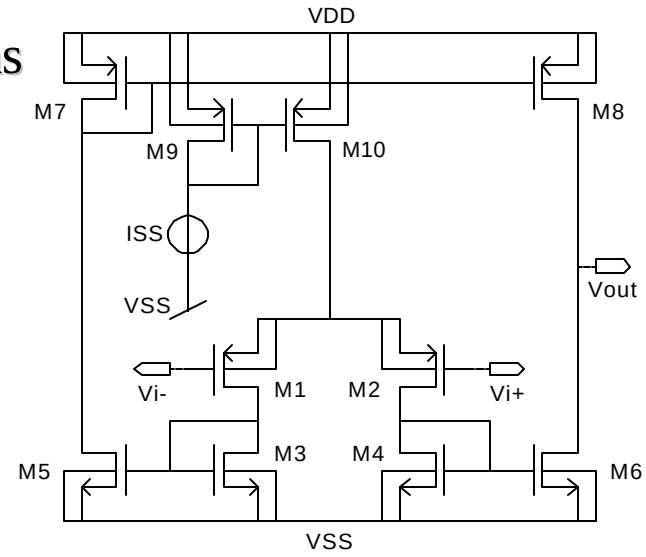
- Potentials to turn on the parasitic BJT transistors which may result in latch-up problem

- The equivalent noise of a bulk-driven MOS amplifier is larger than a conventional gate-driven MOS amplifier.

Example of OTAs using different approaches: Conventional, Current Divider-Source Degeneration (CD-SD), Floating Gate, and Bulk Driven

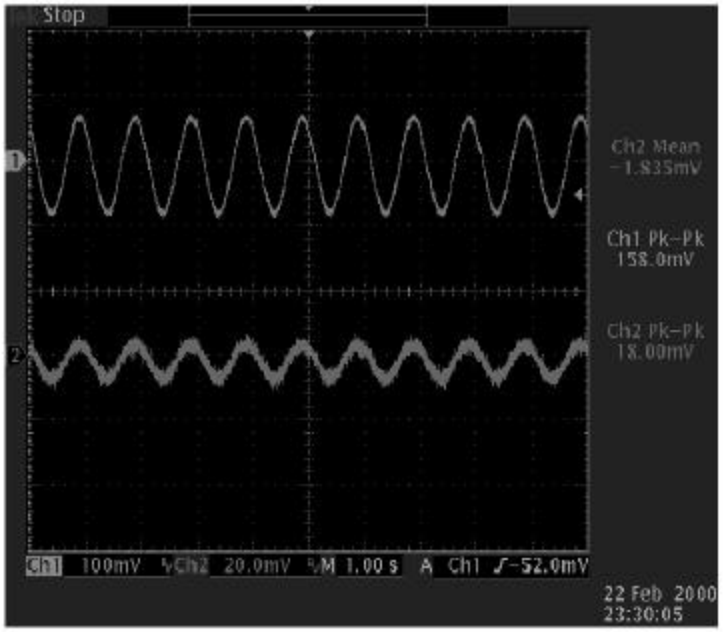


EXPERIMENTAL TEST SETUP

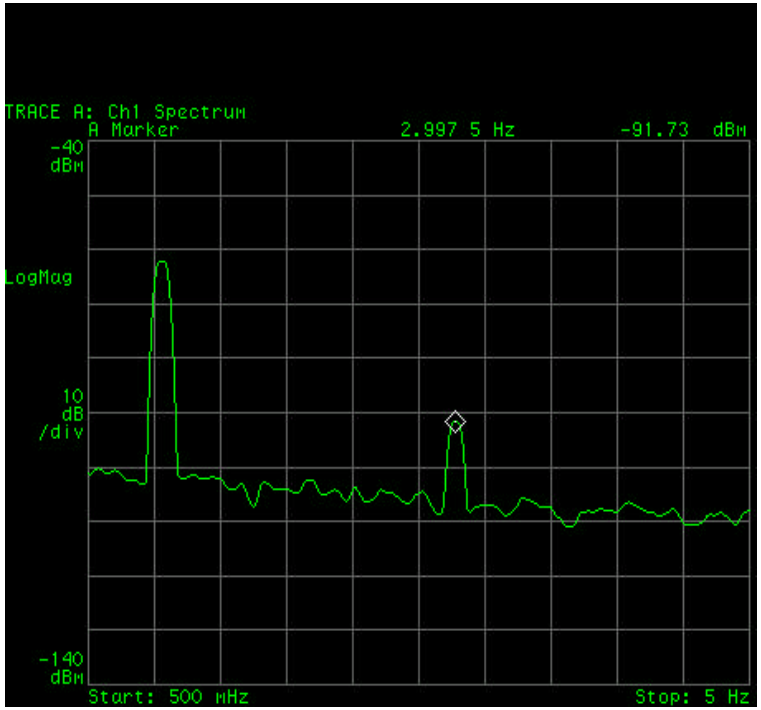


DESIGN A - REFERENCE OTA

DESIGN A - REFERENCE OTA

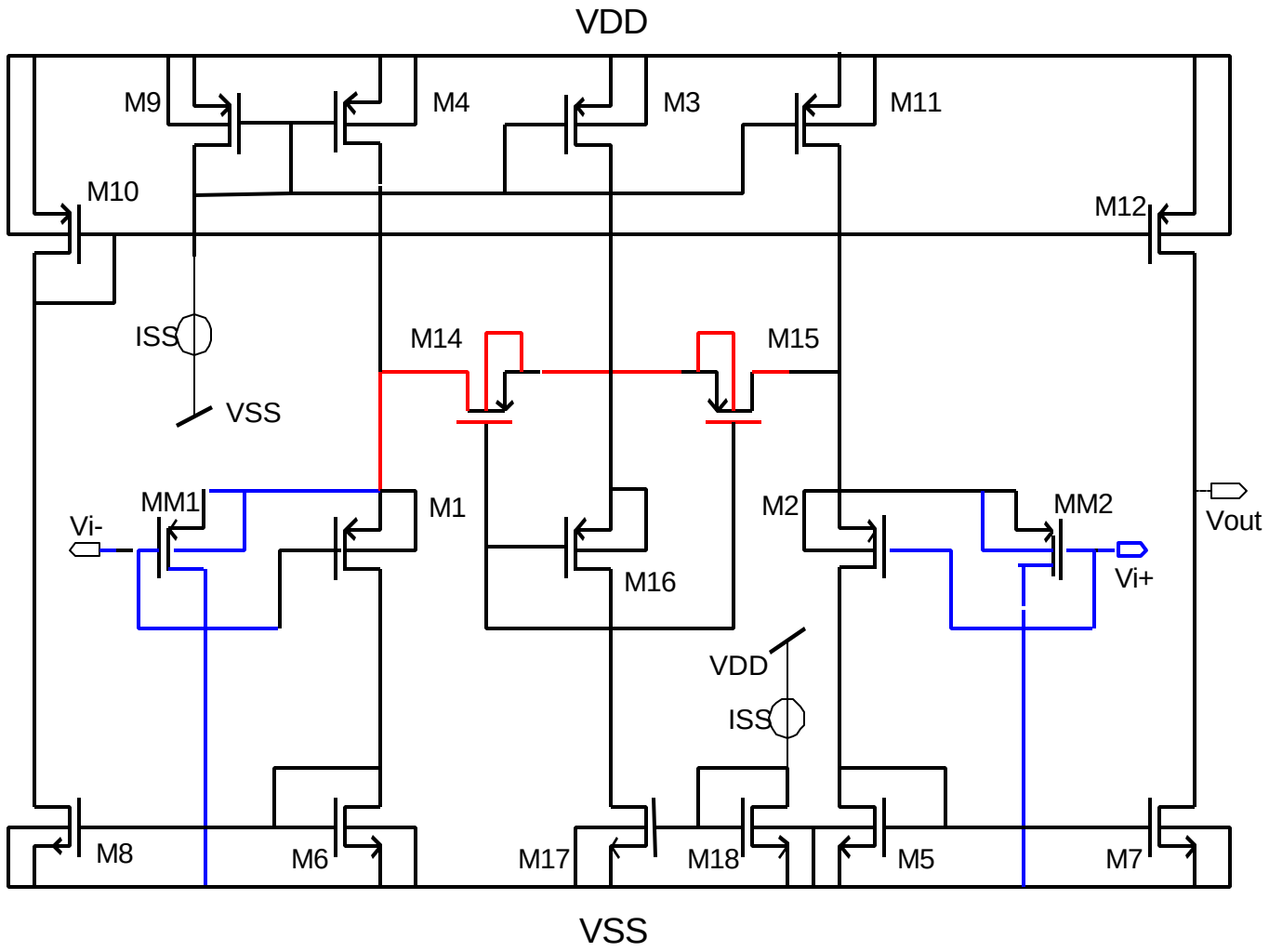


Input Ch1 160mVpp @ 1 Hz
Output Ch2 18mVpp

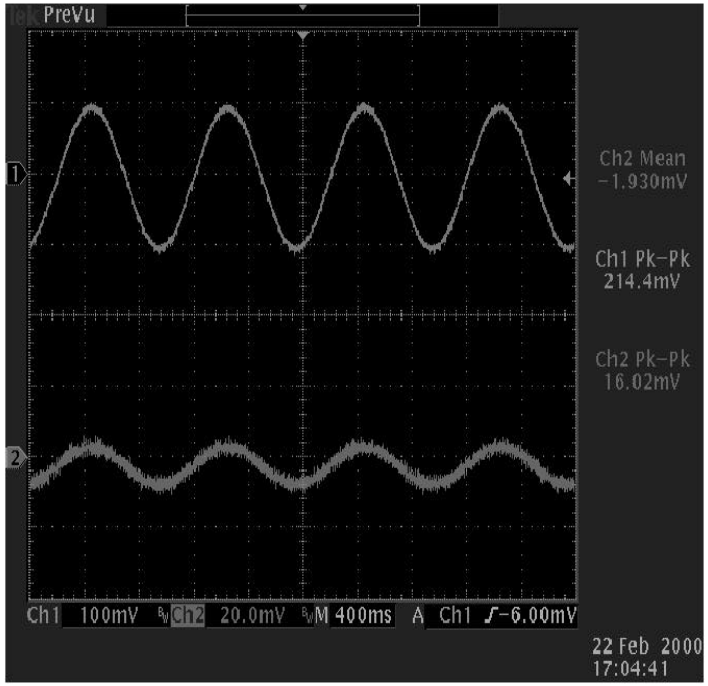


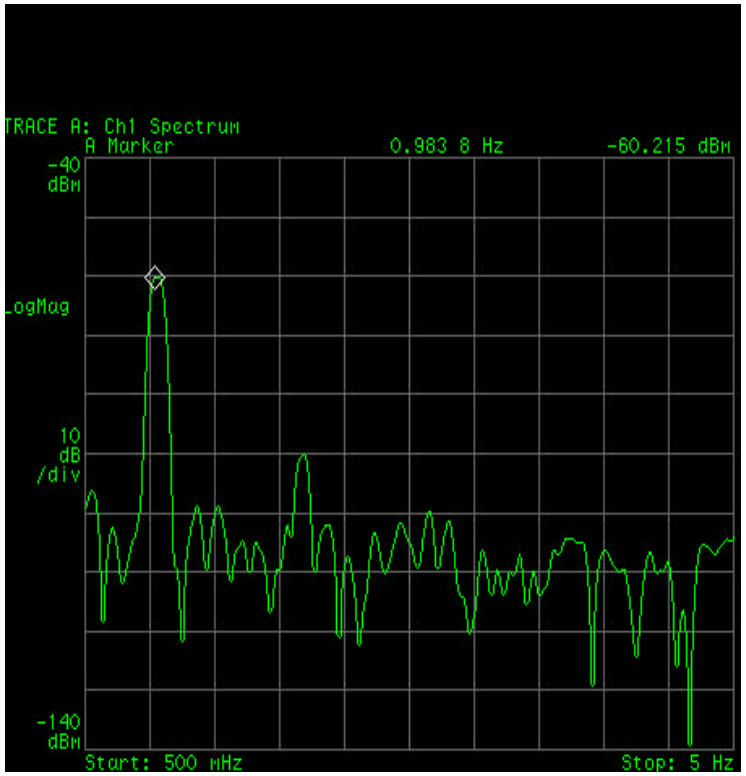
THD ~ -28dBm ~ 3.9% @160mVpp, 1Hz

DESIGN B - CURRENT DIVISION OTA and Source Degeneration



DESIGN B - CURRENT DIVISION and SD OTA

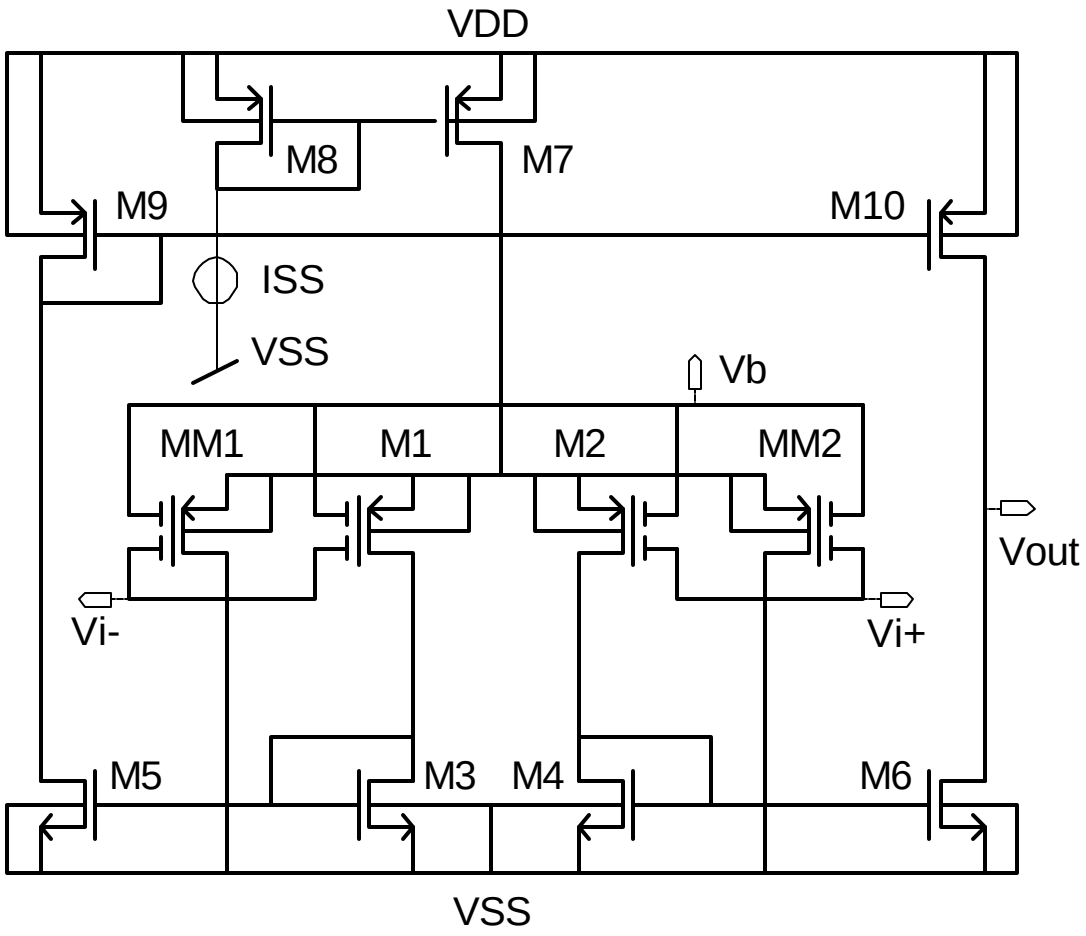




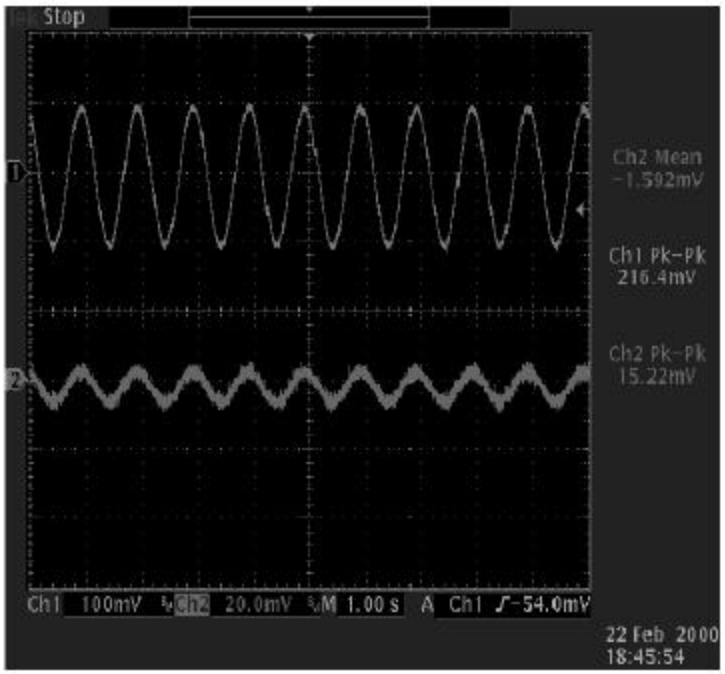
Input Ch1 214mVpp @ 1 Hz
Output Ch2 16mVpp

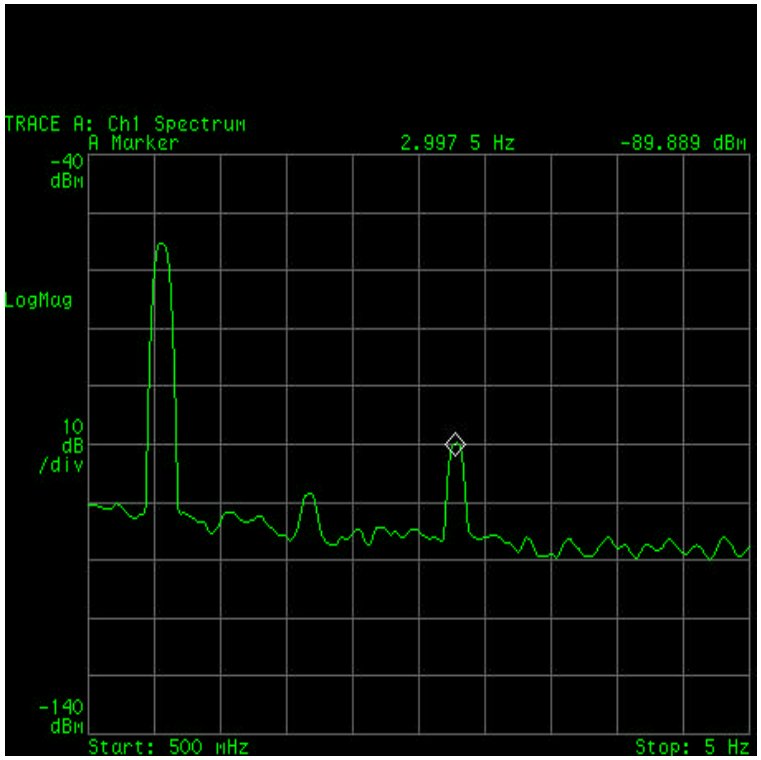
THD ~ -30dBm ~ 3.2% @214mVpp, 1Hz

DESIGN C - FLOATING GATE OTA, plus SD and CD



DESIGN C - FLOATING GATE OTA

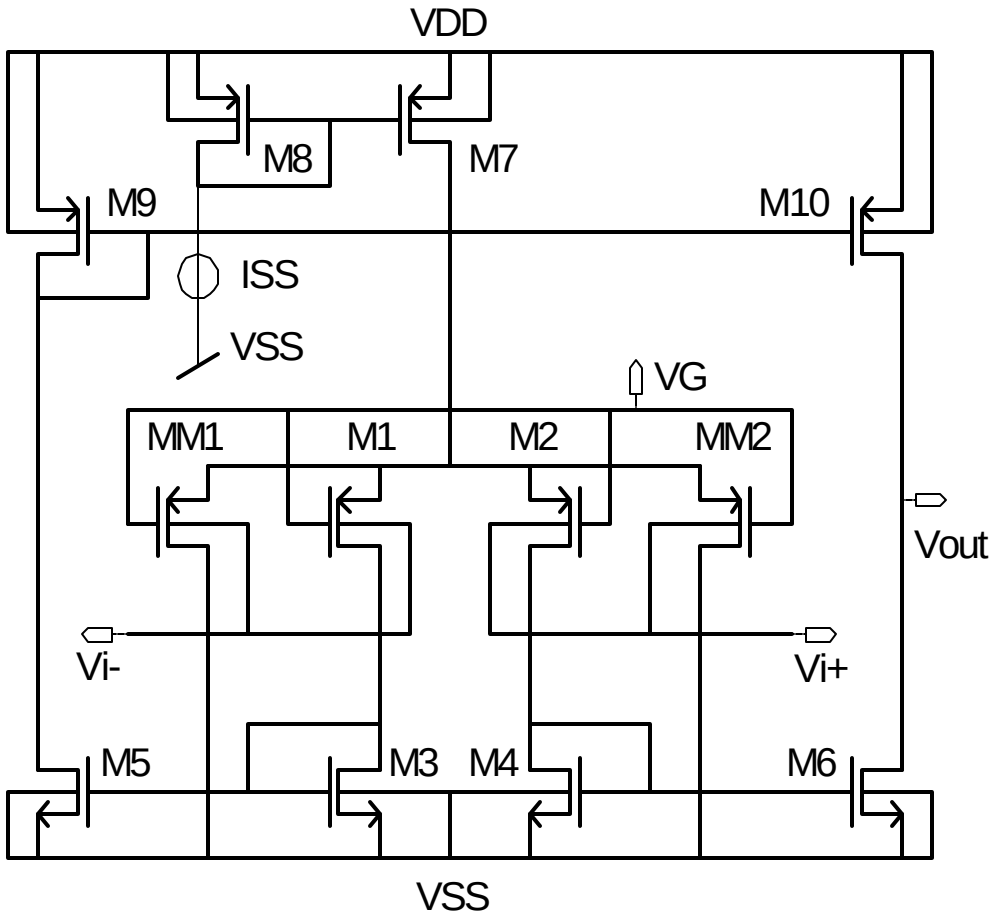




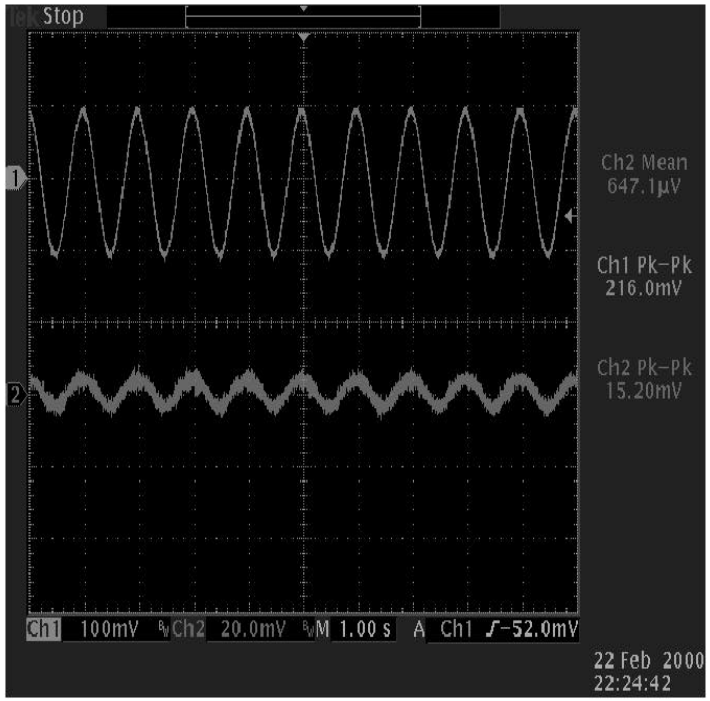
Input Ch1 214mVpp @ 1 Hz
Output Ch2 15.2mVpp

THD ~ -34dBm ~ 2% @214mVpp, 1Hz

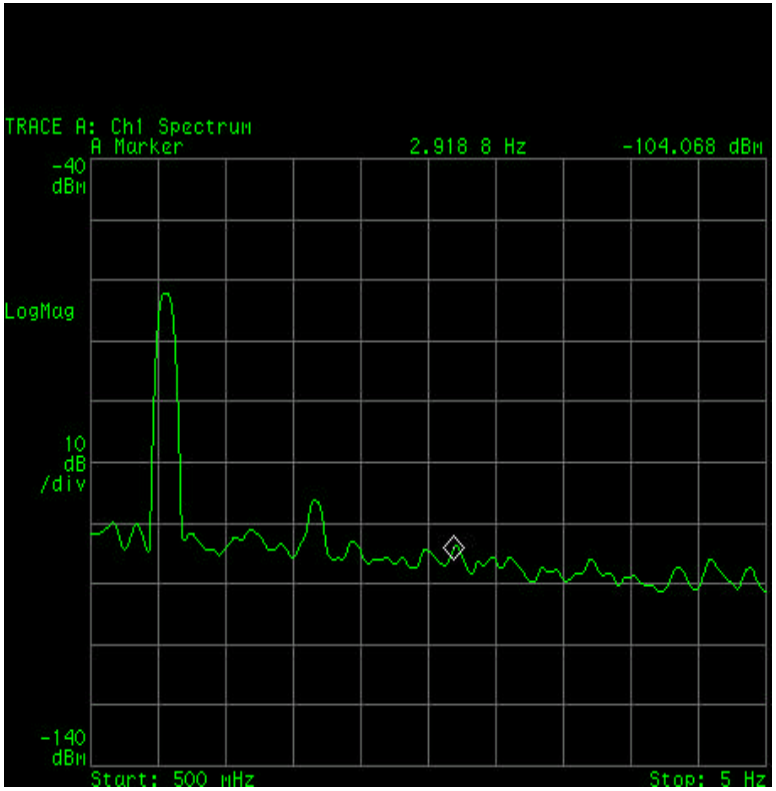
DESIGN D - BULK DRIVEN OTA, PLUS CD AND SD



DESIGN D - BULK DRIVEN OTA



Input Ch1 214mVpp @ 1 Hz
Output Ch2 15.2mVpp



THD ~ -39dBm ~ 1.1% @214mVpp, 1Hz

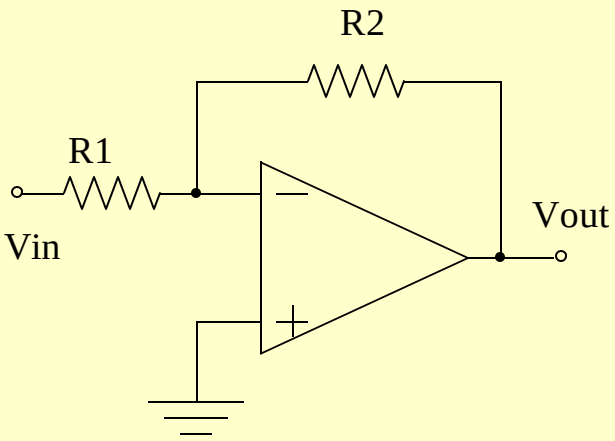
SIMULATION VS EXPERIMENTAL RESULTS

1.2 micron CMOS Technology

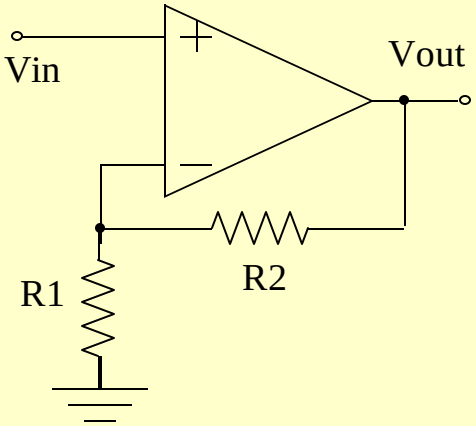
	SIMULATED RESULTS				EXPERIMENTAL RESULTS			
PAR \ DES	**A**	**B**	**C**	**D**	**A**	**B**	**C**	**D**
G_M (nA/V)	11.6	11.55	11.51	11.24	10.5	9.3	8.7	8.8
$\Delta\varphi$ @ 1Hz (°)	0.1	0.098	0.047	0.025	<1	<1	<1	<1
Offset (mV)	0.07	0.027	-0.086	0.045	-1.8	-1.9	-1.5	0.647
THD (%)	1@162 mVpp	1@240 mVpp	1@330 mVpp	1@900 mVpp	3.9@160 mVpp	5.6@242 mVpp	3.2@330 mVpp	5.9@900 mVpp
THD (%) @ 214mVpp	-	-	-	-	3.9	3.2	2	1.1
I_{BIAS} (nA)	2	100	200	500	4	120	230	560
$V_{DD} = \lvert V_{SS} \rvert$ (V)	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35
BIAS (V)	N/A	N/A	-1.35	-1.35	N/A	N/A	-1.35	-1.35

Rail-to-Rail Op Amps

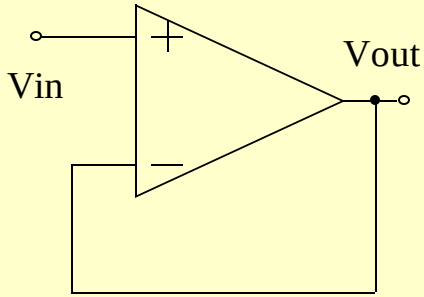
- There are two basic configurations for Op Amp applications:
  (a) inverting configuration, and,
  (b) non-inverting configuration.



(a) Inverting Configuration



(b) Non-Inverting Configuration



(c) Voltage Follower
(a special case of non-inverting configuration)

Why Rail-to-Rail Differential Input Stage?

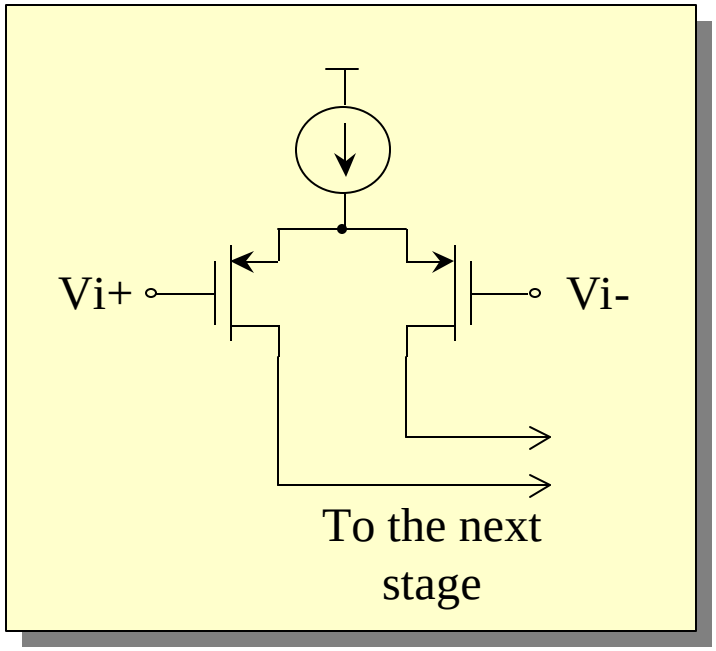
- The input and output swings of inverting and non-inverting configurations

Configuration	Input common mode voltage swing	Output voltage swing
Inverting	≈0	Rail-to-rail
Non-inverting	R1/(R1+R2) * Vsup	Rail-to-rail
Voltage follower	Rail-to-rail	Rail-to-rail

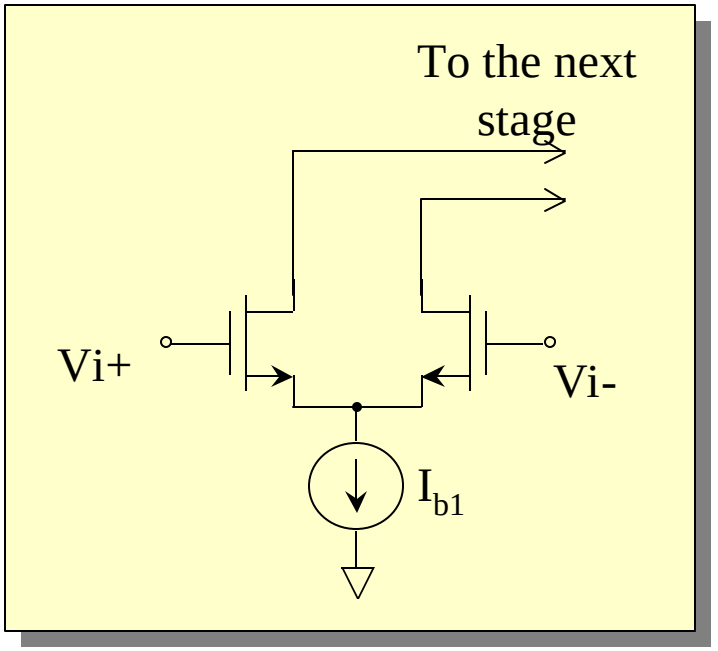
- From the table, we see that for inverting configuration, rail-to-rail input common mode range is not needed. But for non-inverting configuration, some input common mode voltage swing is required, especially for a voltage follower which usually works as an output buffer, we need a **rail-to-rail** input common mode voltage range! To make an Op Amp work under any circumstance, a differential input with **rail-to-rail** common mode range is needed.

How to Obtain a Rail-to-Rail Input Common Mode Range?

- We know that usually the input stage of an op amp consists of a differential pair. There are two types of differential pairs.

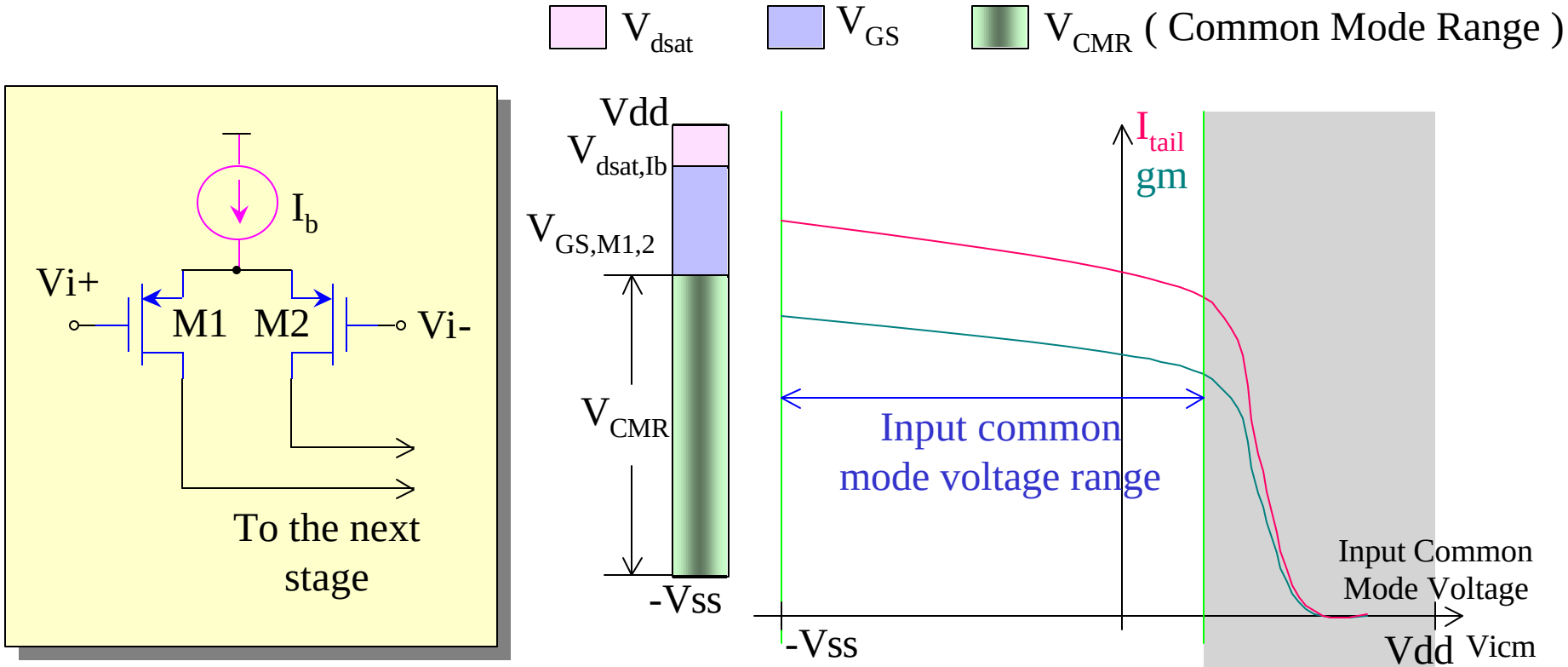


(a) P-type differential input stage



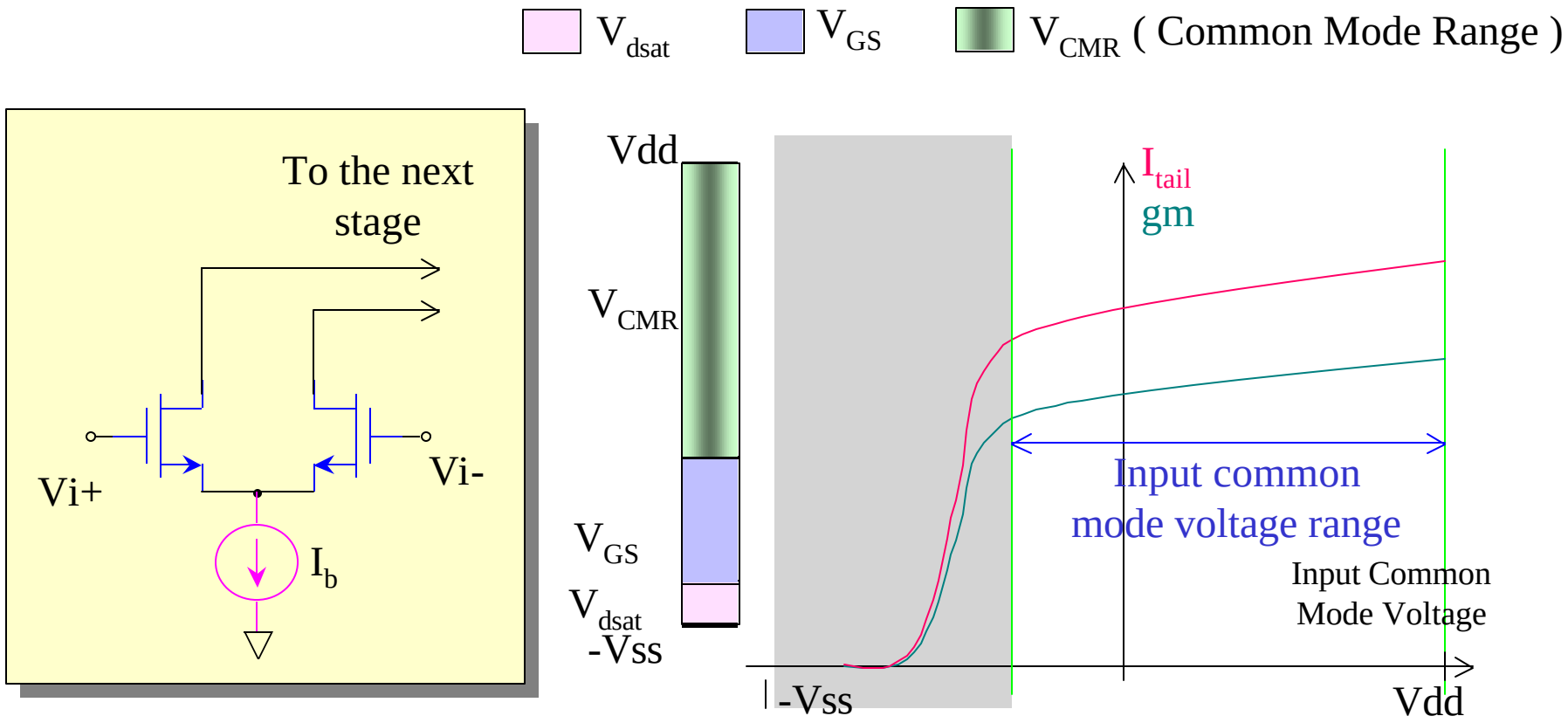
(b) N-type differential input stage

- First, let us observe how a differential pair works with different input common mode voltage
  - P-type input differential pair



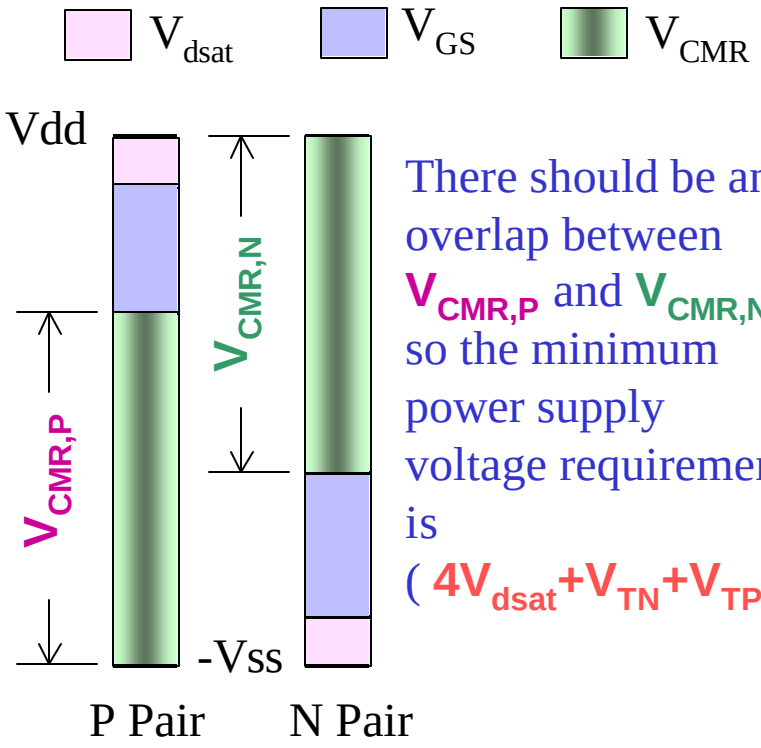
Where $V_{GS}=V_{dsat}+V_T$

– N-type differential input stage



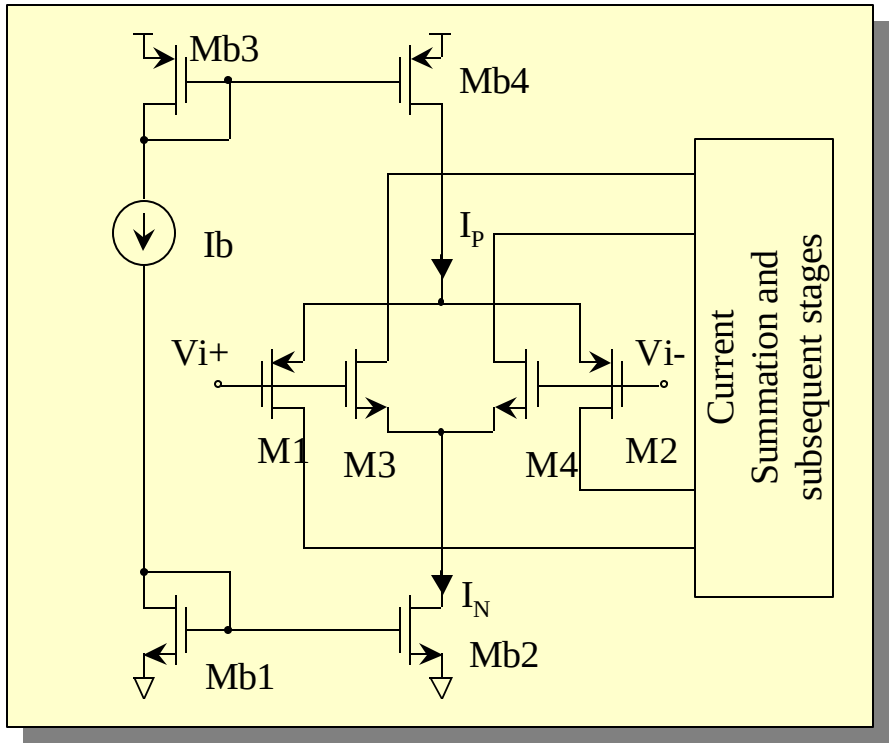
Again, how to Obtain a Rail-to-Rail Input Common Mode Range?

- Why not connect these two pairs in parallel and try to get a full rail-to-rail range?



There should be an overlap between $V_{CMR,P}$ and $V_{CMR,N}$, so the minimum power supply voltage requirement is ($4V_{dsat}+V_{TN}+V_{TP}$)

$V_{SUP} \geq 4V_{dsat}+V_{TN}+V_{TP}$

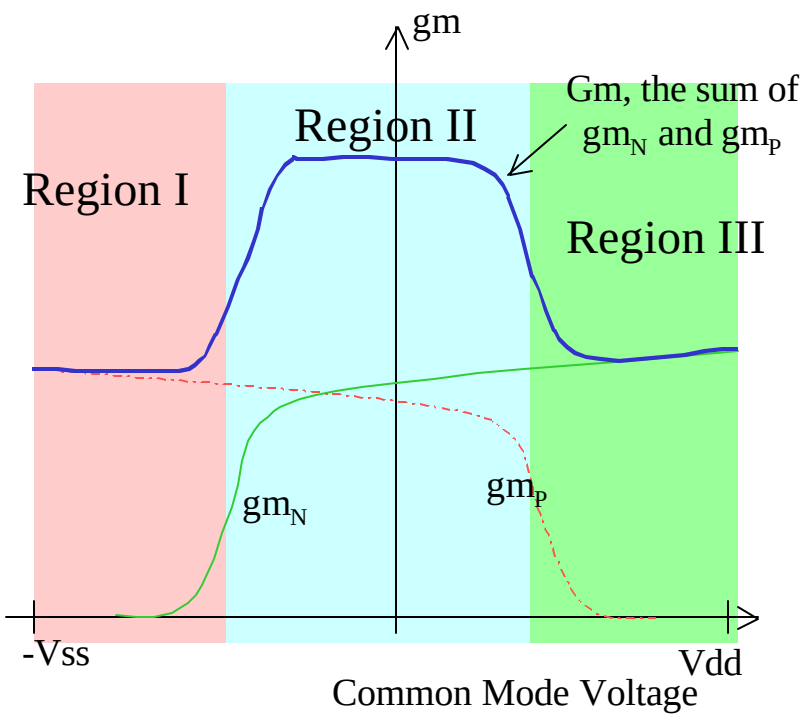


Simple N-P complementary input stage

Almost all of the rail-to-rail input stages are doing in this way by some variations! But how well does it work?

Observations on transconductance performance for the entire region.-

- Transconductance vs. Vicm



The total transconductance of the input stage varies from gm to 2gm, the variation is **100%** !

- If $K = \frac{1}{2} KP_N (\frac{W}{L})_N = \frac{1}{2} KP_P (\frac{W}{L})_P$ and

  $I_N = I_P = I_{TAIL}$

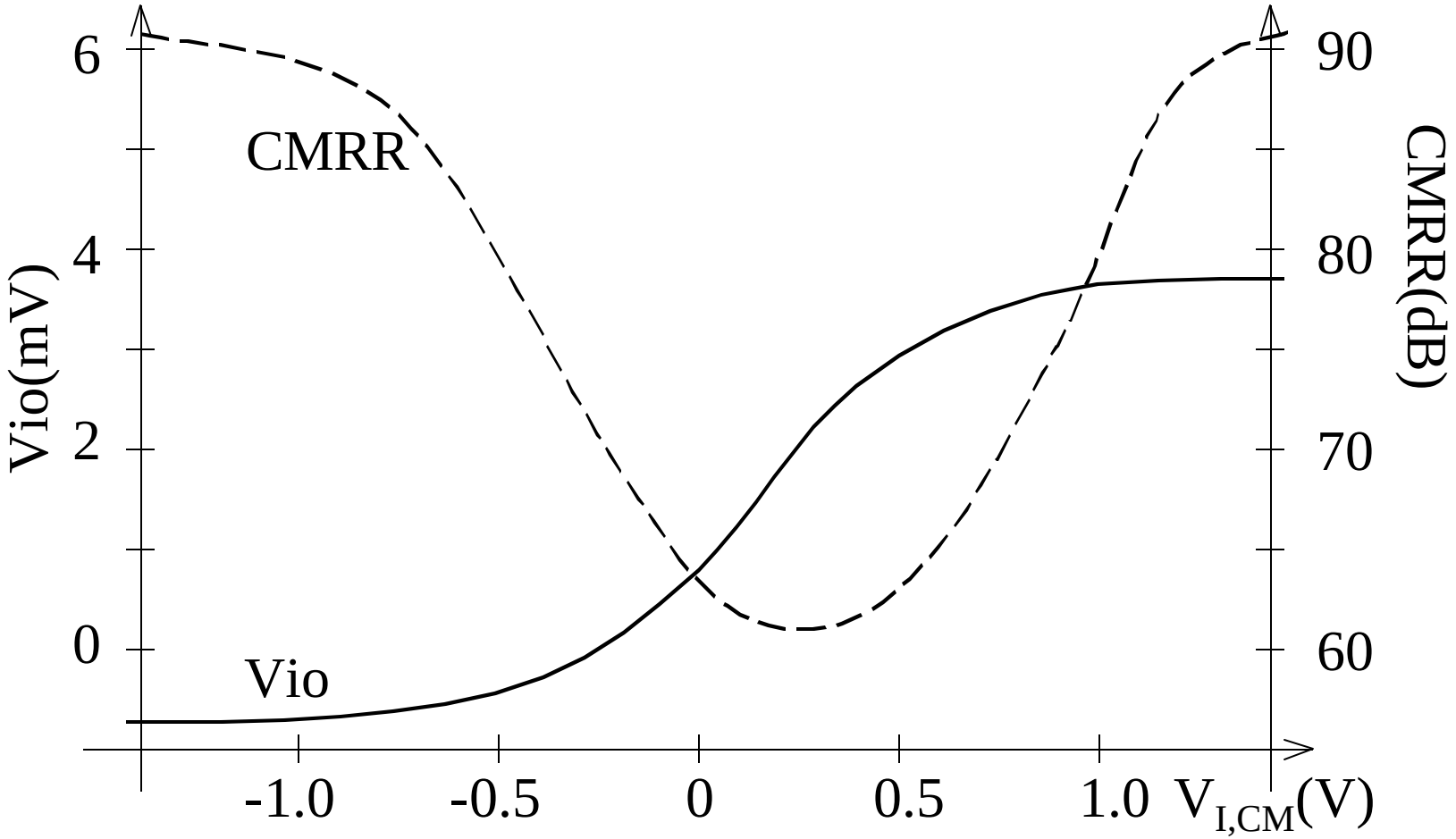
  then $gm_N = gm_P = gm = \sqrt{2KI_{TAIL}}$.

Region I. When Vicm is close to the negative rail, only P-channel pair operates.The N channel pair is off because its V_{GS} is less than V_T. The total transconductance of the differential pair is given by $gm_T = gm_P = gm$.

Region II. When Vicm is in the middle range, both of the P and N pairs operate. The total transconductance is given by $gm_T = gm_N + gm_P = 2gm$.

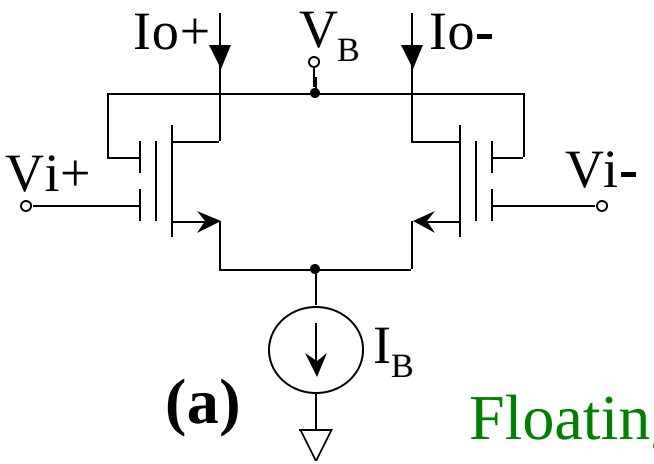
Region III. When Vicm is close to the positive rail, only N-channel pair operates. The total transconductance is given by $gm_T = gm_N = gm$.

How does the CMRR varies with the input common-mode signal ?



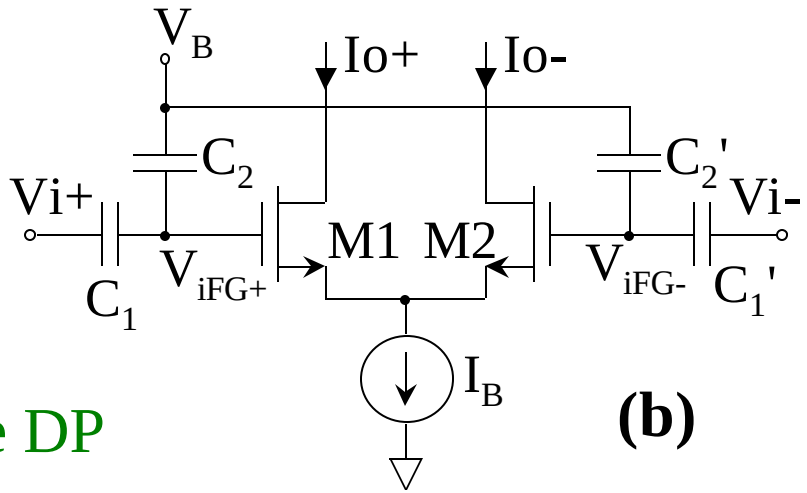
Rail-to-Rail Techniques: Summary and Comparison

Case	Principle	Δgm	Slew Rate	CMRR	Advantage	Limitations
1	$I_N + I_P = const$ [1][2][6]	N/A for weak inversion 40% if in strong inversion	Constant	56dB@10Hz, 52dB@100KHz, measured in [2]	Small gm variation (6%) in weak inversion operation	Only work well in weak inversion, can not used in high speed application
2	$\sqrt{I_N} + \sqrt{I_P} = const$ [3] [16]	-12% +6% (simulated in this presentation)	$\sqrt{2}$ times variation	80 dB / 53 dB (measured in [3])		Depends on quadratic characteristics of MOSFETs, which is not exactly followed for short channel transistors in sub-micron processes
3	4 times I_N or I_P when only one pair operates [3][4][6]	+15% systematic gm variation	2 times variation	70dB / 43 dB (measured in [4])	Somewhat simple	1) Same with case 2, but we can change 4 to other numbers to have smaller gm variation for short channel transistors 2) Systematic gm deviation of 15% even for ideal MOSFETs with quadratic characteristics
4	Current switch, backup pairs [5]	+20% systematic gm variation	Constant	N/A	Constant slew rate	Systematic gm deviation of 20% even for ideal MOSFETs with quadratic characteristics
5	6-pair structure, back pairs [7]	+20% systematic gm variation (analytical), ±10% (measured in [7])	Constant	N/A	Constant slew rate	Same with Case 4
6	Max/min selection [8][9]	7% (simulated [9]) 5% (strong inversion, measured [8]) 20% (weak inversion, measured [8])	Constant	N/A		Somewhat complex
7	Electronic zener [10]	8% (measured)		80 dB / 43 dB (measured in [10])		Same with Case 2
8	Level shift [11]	±4% after tuning 13% before tuning (measured)		≥80 dB (DC) (measured in [11])	Simple	Gm variation sensitive to V_T variation and power supply voltage change

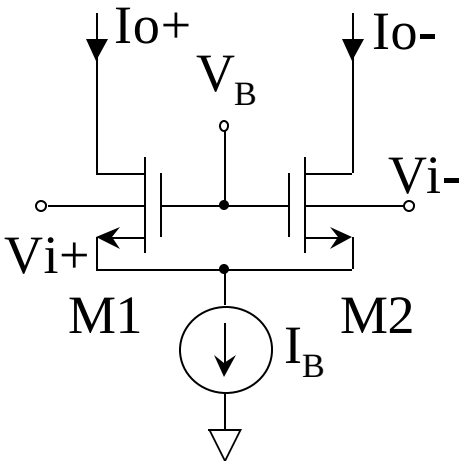


(a)

Floating Gate DP



(b)

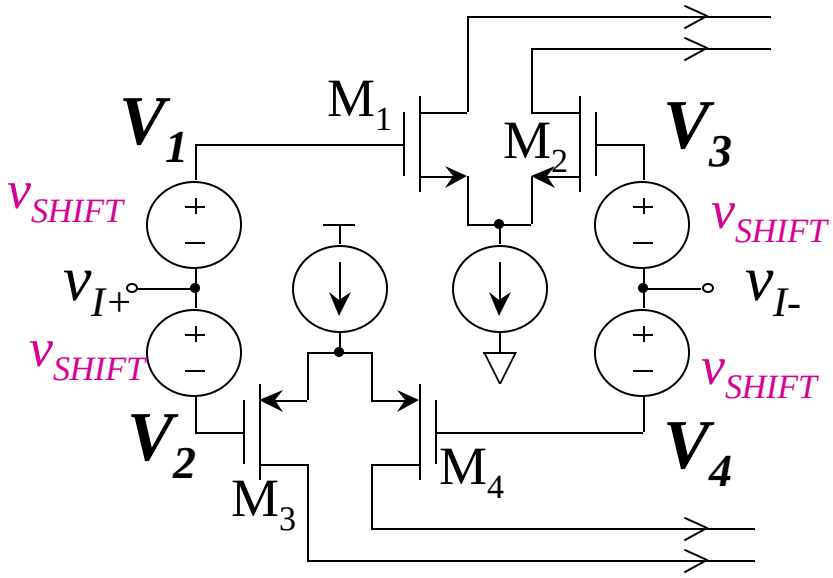


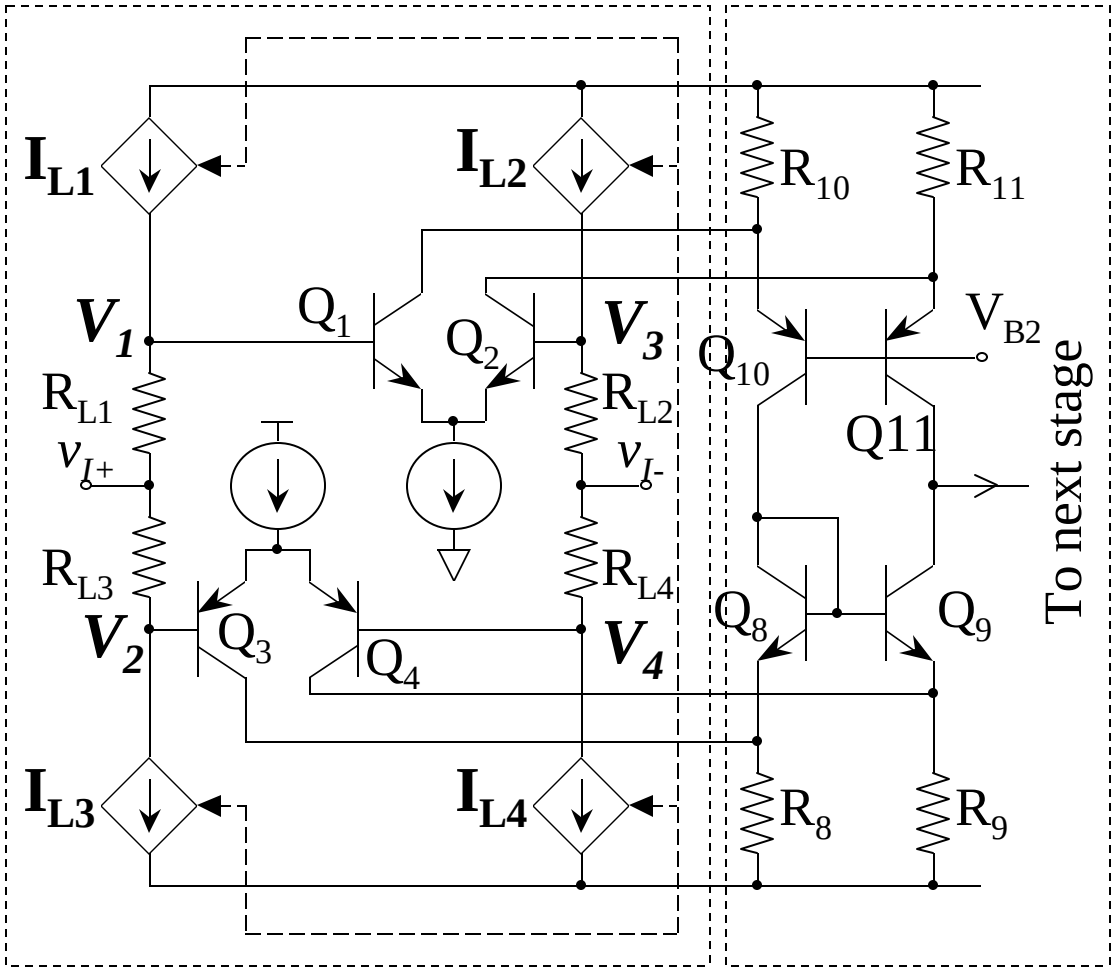
(c) Bulk Driven DP

Another Potential Solutions for Rail-to-Rail Amplifiers

One more Rail-to-Rail Op Amp Technique

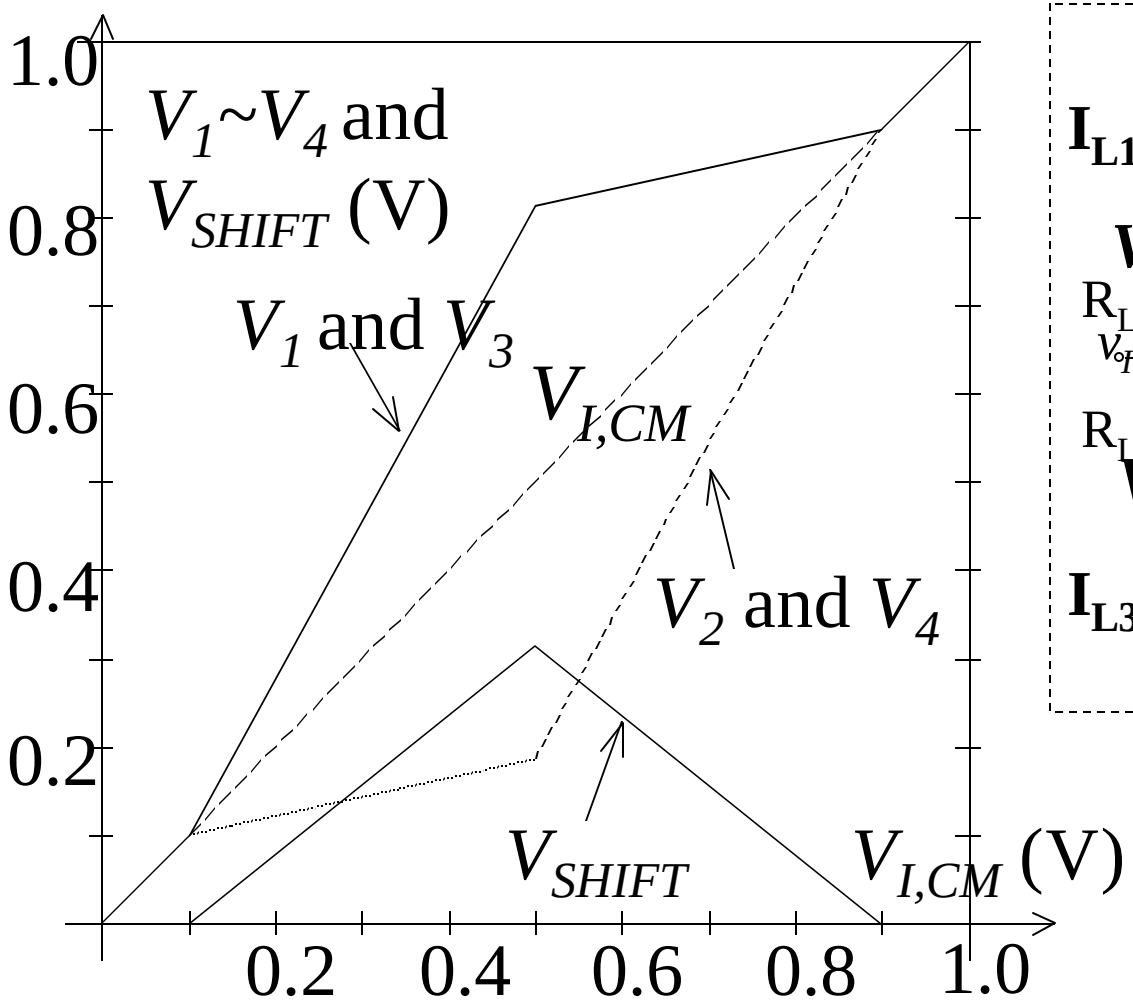
By using dynamic level shift, the rail-to-rail Amplifier can be obtained.

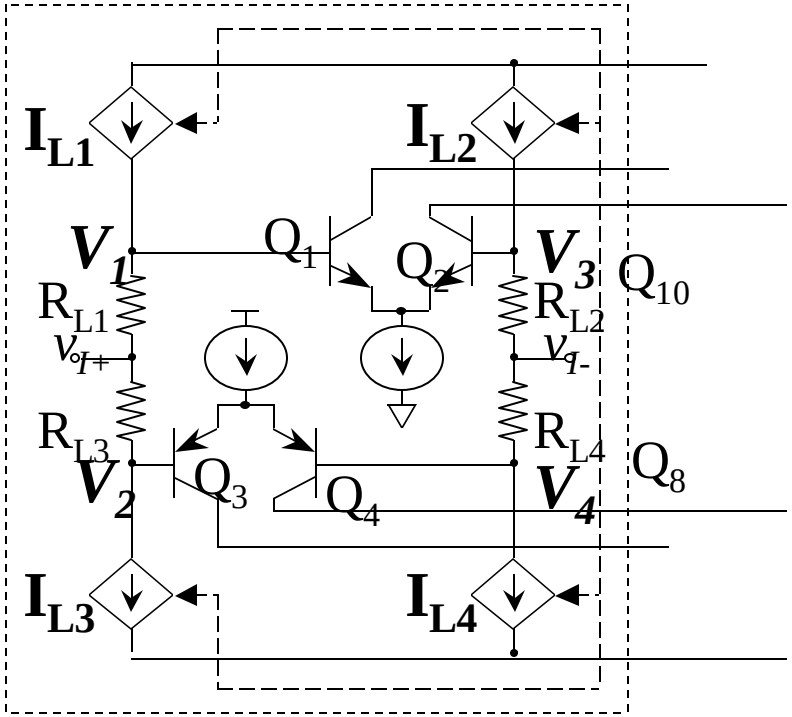


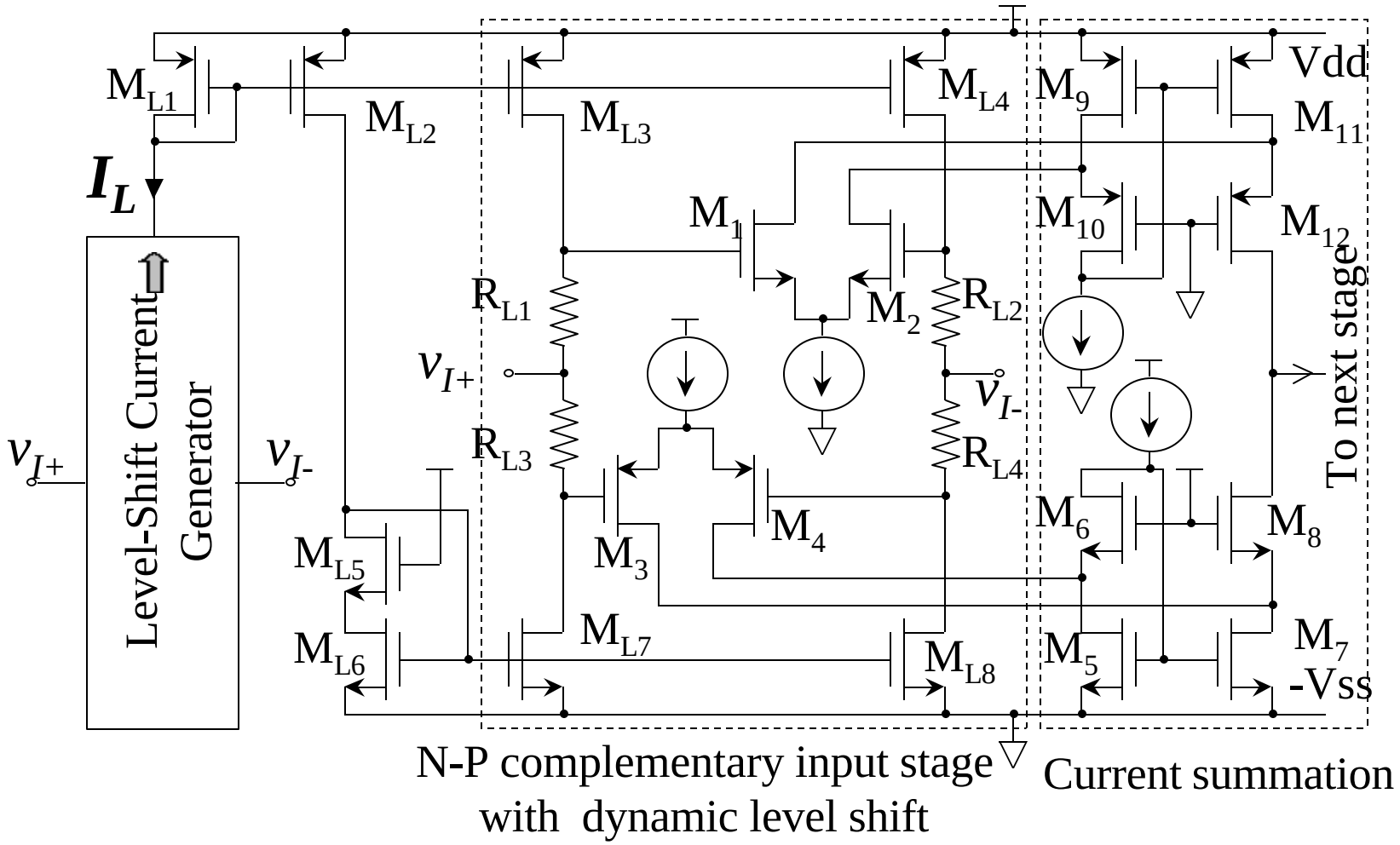


N-P complementary input stage with dynamic level shift

Current summation


1.0
0.8
0.6
0.4
0.2
V_1~V_4 and
V_{SHIFT} (V)
V_1 and V_3
$V_{I,CM}$
V_2 and V_4
V_{SHIFT}
$V_{I,CM}$ (V)
0.2
0.4
0.6
0.8
1.0


I_{L1}
I_{L2}
V_1
Q_1
Q_2
V_3
Q_{10}
R_{L1}
v_{o1+}
R_{L2}
v_{o1-}
R_{L3}
R_{L4}
Q_8
V_2
Q_3
Q_4
V_4
I_{L3}
I_{L4}


M_L1
M_L2
M_L3
M_L4
M_9
Vdd
M_11
I_L
M_1
M_10
M_12
R_L1
M_2
R_L2
v_I+
v_I-
R_L3
R_L4
Level-Shift Current Generator
To next stage
M_6
M_8
M_4
M_3
M_L5
M_L7
M_7
M_L6
M_L8
M_5
-Vss
N-P complementary input stage with dynamic level shift
Current summation

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Voltage Multistage Transconductance Amplifier Topologies For LV Power Supply.

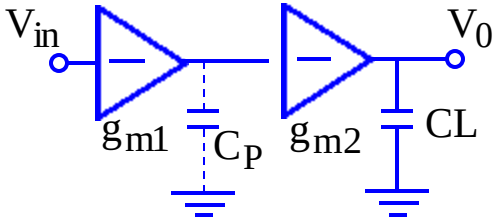
- **Good voltage gain can be obtained using cascode stages. But these stages are not amenable for LV power supply.**

- **Under LV conditions, high voltage can be obtained using cascade amplifiers. That is growing horizontally, rather than vertically.**

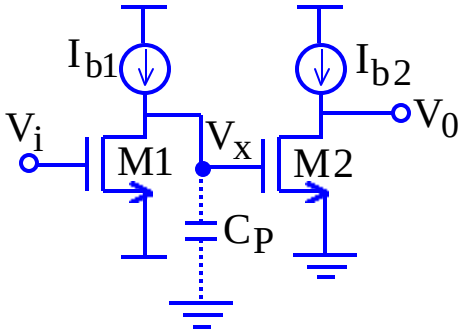
- **Direct Cascade of simple (inverting) stages gives the required voltage gain without control of poles and zeroes.**

- **Dynamic behavior for optimal performance requires feedback (and feedforward) circuits.**

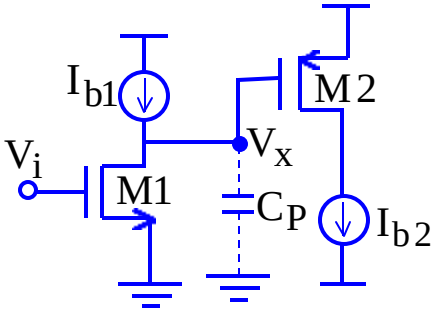
First Approach: Direct Cascade



Symbolic Representation



(a)



(b)

Two Possible Implementations

$$H(s) = \frac{V_0(s)}{V_{in}(s)} \cong \frac{+\,g_{m1}g_{m2}/C_pC_L}{1 + s\left(\frac{C_L}{g_{02}} + \frac{C_p}{g_{01}}\right) + \frac{C_pC_L}{g_{01}g_{02}}s^2}$$

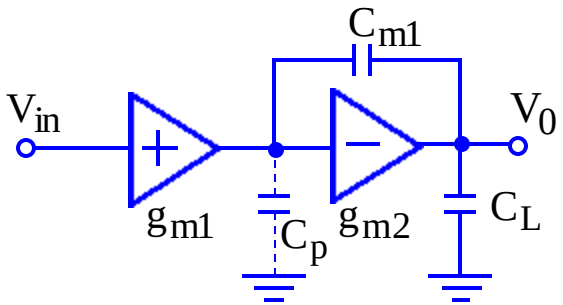
The poles are located at

$$\omega_{p_1} = \frac{g_{01}}{C_p}\ ,\ \omega_{p_2} = \frac{g_{02}}{C_L}$$

$$H(o) = \frac{g_{m1}g_{m2}}{g_{01}g_{02}}$$

How do you bring one pole close to the origin?

-Use feedback



Neglect C_p (i.e., $C_p << C_{m1}$)

$$H(s) = \frac{V_0(s)}{V_{in}(s)} = \frac{g_{m1}(g_{m2} - sC_{m1})/C_LC_{m1}}{s^2 + s\left(g_{01}(C_L + C_{m1})/C_LC_p + g_{m2}/C_L + g_{02}/C_L\right) + g_{01}g_{02}/C_LC_{m1}}$$

The poles are approximately located at :

$$\omega_{p_2} \cong (g_{m2} + g_{02})/C_L \quad \text{and} \quad \omega_{p_1} \cong \left(\frac{g_{01}}{C_{m1}}\right)\frac{g_{02}}{g_{m2}} = \left(\frac{g_{01}}{C_{m1}}\right)\frac{1}{A_{V_{02}}}$$

The good news is that :

$\omega_{p_1} << \omega_{p_2}$ Good for stability

$H(o) = g_{m1}g_{m2}/g_{01}g_{02}$ Large DC voltage gain

The bad news is a zero at the RHP

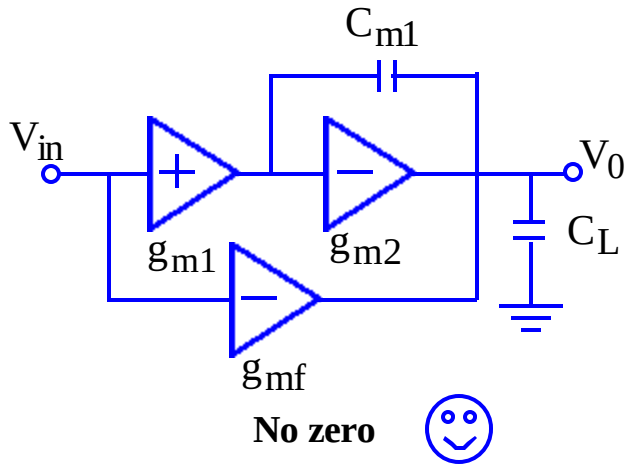
$$\omega_{z_1} = \frac{g_{m2}}{C_{m1}}$$

Now we will use a feedforward circuit to cancel the zero at the RHP.

This will impact the complexity and performance of the design.

Recall that before applying the feedforward we had:

$$H(s) = \frac{V_0(s)}{V_{in}(s)} = \frac{g_{m1}(g_{m2} - sC_{m1})/C_L C_{m1}}{s^2 + s\left(g_{01}(C_L + C_{m1})/C_L C_p + g_{m2}/C_L + g_{02}/C_L\right) + g_{01}g_{02}/C_L C_{m1}}$$



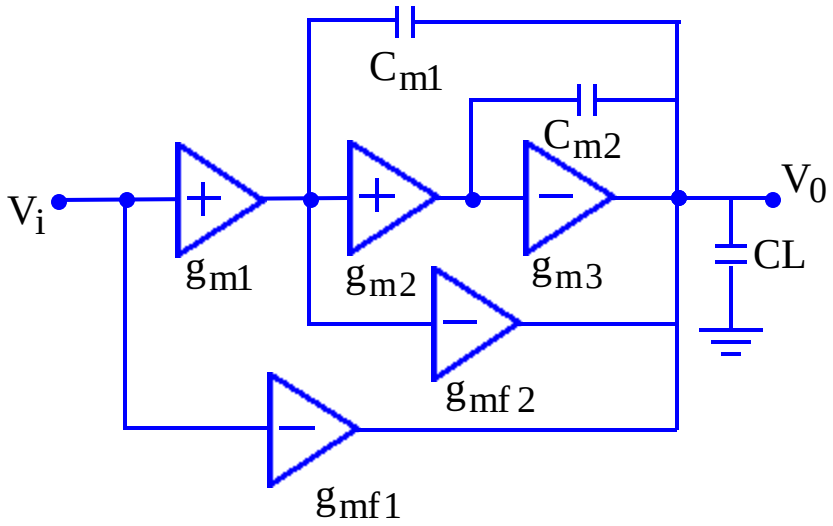
No zero

Now the corresponding H(s) becomes:

$$H(s)\Big|_{g_{mf} = g_{m1}} = \frac{-g_{m1}g_{m2}}{s^2 C_{m1}C_L + sC_{m1}g_{m2} + g_{01}g_{02}}$$

This can be extended to higher-order systems, let us consider first a third-order system.

Nested G_m-C Compensation Amplifier.



Three-stage amplifier topology with NGCC

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{g_{m1}g_{m2}g_{m3} + sg_{m1}(g_{mf\,2} - g_{m2})C_{m2} + (g_{mf\,1} - g_{m1})C_{m1}C_{m2}}{g_{01}g_{02}g_{03} + sg_{m2}g_{m3}C_{m1} + s^2(g_{m3} + g_{mf\,2} - g_{m2})C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}}$$

By making $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$,

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{-g_{m1}g_{m2}g_{m3}}{g_{01}g_{02}g_{03} + sg_{m2}g_{m3}C_{m1} + s^2g_{m3}C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}}$$

This H(s) can be written as

$$H(s) = \frac{-A_0}{\left(1+ s\frac{A_0}{f_1}\right)\left(1+ \frac{s}{f_2}+ \frac{s^2}{f_2 f_3}\right)}$$

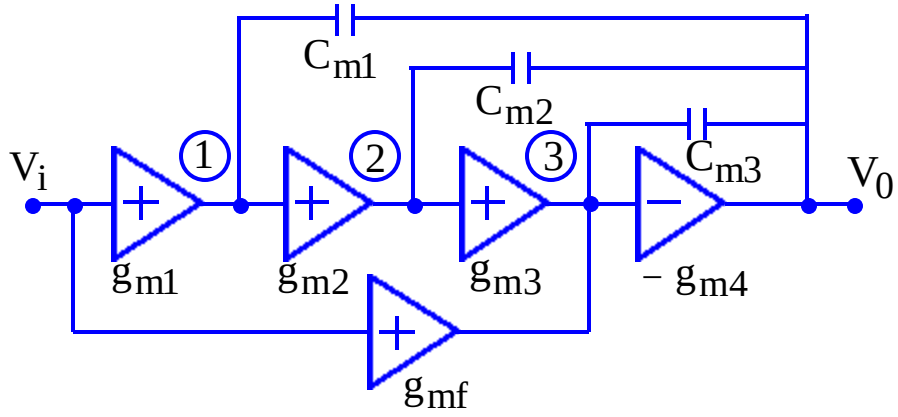
$$A_0 = \frac{g_{m1}g_{m3}g_{m2}}{g_{01}g_{03}g_{02}} \text{ and } f_1 = GB = \frac{g_{m1}}{C_{m1}}$$

$$f_2 = \frac{g_{m2}}{C_{m2}} \text{ , } f_2 f_3 = \frac{g_{m2}g_{m3}}{C_{m2}C_L} \text{ ; } f_i = \frac{g_{mi}}{C_{mi}}$$

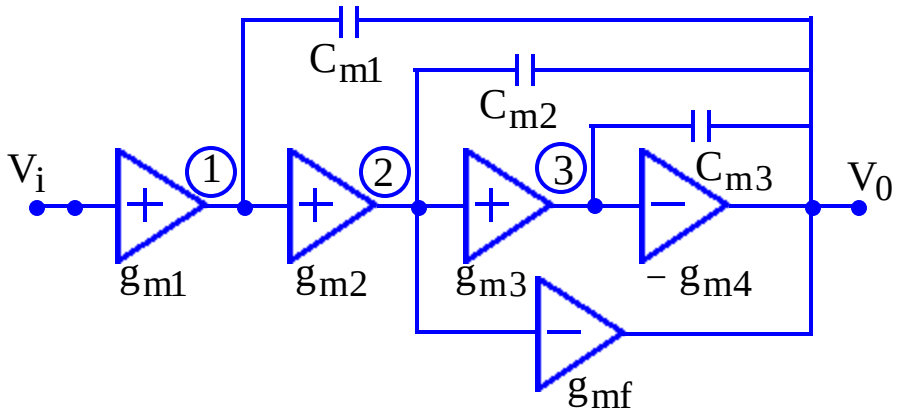
Note that the dominant pole is located at

$$P_1 = \frac{f_1}{A_0} = \frac{\frac{g_{m1}}{C_{m1}}}{\frac{g_{m1}g_{m2}g_{m3}}{g_{01}g_{02}g_{03}}} = \frac{g_{01}g_{02}g_{03}}{g_{m2}g_{m3}C_{m1}} = \left(\frac{g_{01}}{C_{m1}}\right)\frac{1}{A_{V0_2}A_{V03}}$$

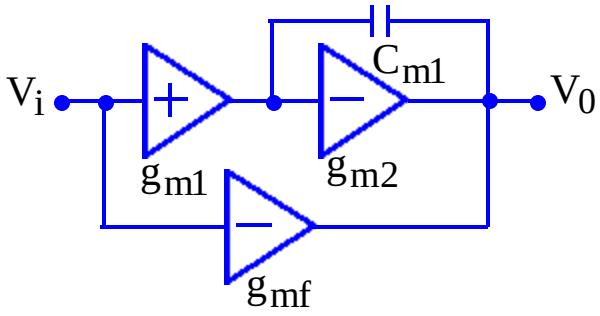
Multipath Nested Miller Compensation Technology
Potential Feedforward Schemes: An Amplifier Topologies Re-Visit.



(a) Multipath nested miller compensation topology. FF

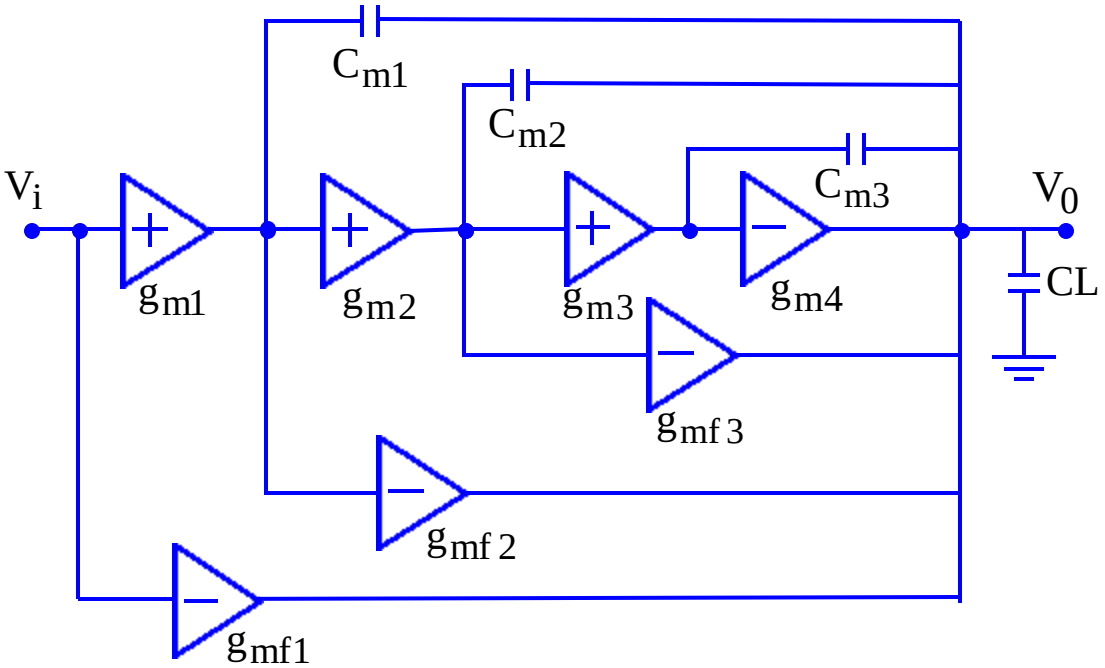


(b) An abstract model for the amplifier proposed by Castello, et.al.



(c) The amplifier with multipath miller zero cancellation.

Let Us Now Compare Several Four-Order Topologies



$$H(s) = \frac{-A_0}{\left(1+\frac{s}{P_1}\right)\left(1+a_1 s + a_2 s^2 + a_3 s^3\right)}$$

$$P_1 = \frac{GB}{A_0}$$

$$a_1 = \frac{1}{f_2}, a_2 = \frac{1}{f_2 f_3}, a_3 = \frac{1}{f_2 f_3 f_4}$$

$$\frac{1}{f_2 f_3} = \frac{C_{m2} C_{m3}}{g_{m2} g_{m3}}, \frac{1}{f_i} = \frac{C_{mi}}{g_{mi}}$$

Four stage amplifier topology with NGCC (Fan You et al)

$$f_1 < f_2 < f_3 \le f_4 \quad , \quad f_1 = GB$$

$$f_4 > \frac{f_2}{1 - f_2 / f_3}$$

- Power Comsumption

$$P = (V_{DD} - V_{ss}) I_n \left[1 + \sum_{i=1}^{n-1} \frac{\alpha_i f_i}{f_n}\right], \quad \alpha_i = \frac{C_{mi}}{C_L}, \quad \alpha_i f_i = \frac{g_{mi}}{C_L}$$

I_n and f_n are current and frequency normalization factors, respectively.

Comparison of Several Topologies.

$$\frac{V_0(s)}{V_i(s)} = -A_0 \frac{1 - b_1 s - b_2 s^2 - b_3 s^3}{(1 + s/P_1)(1 + a_1 s + a_2 s^2 + a_3 s^3)}, \qquad k_i = \frac{g_{mi}}{g_{oi}}, i = 1,3 \quad \text{and} \quad f_i = \frac{g_{mi}}{C_{mi}}$$

Where

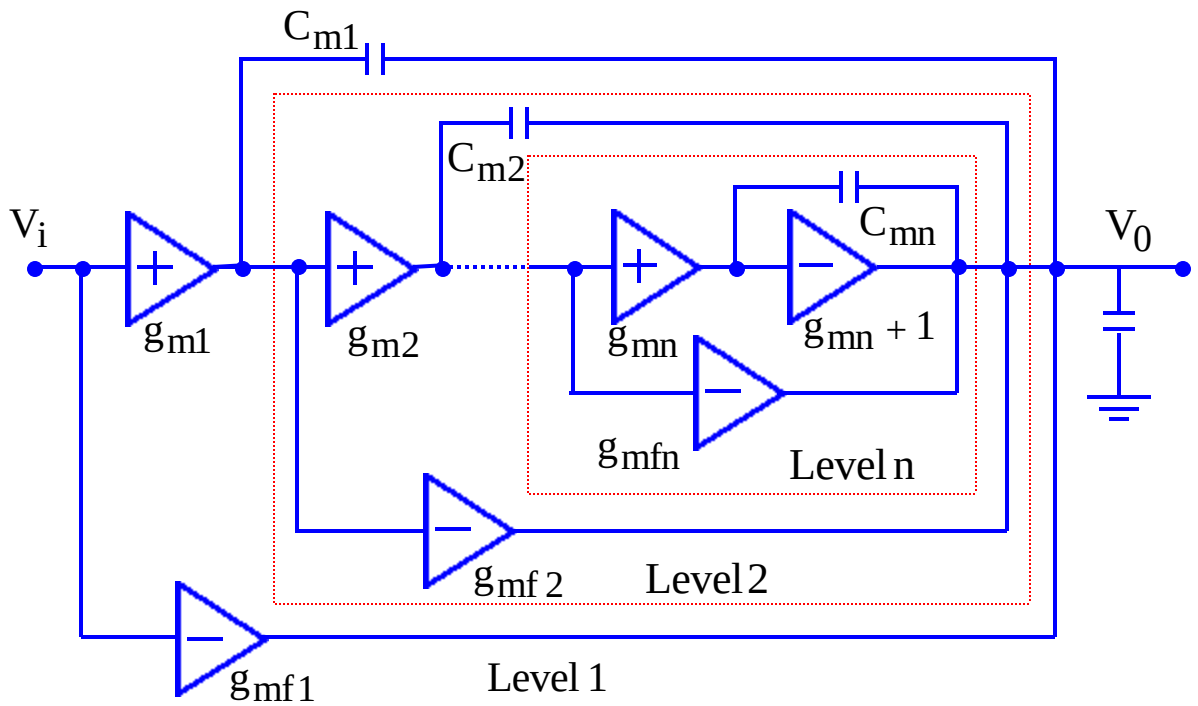
$$A_0 = k_1 k_2 k_3 k_4, \; P_1 = \frac{f_1}{A_0} = \frac{GB}{A_0}$$

Comparison of Polynomial Coefficients for Four Stage NMC and NGCC Amplifier.

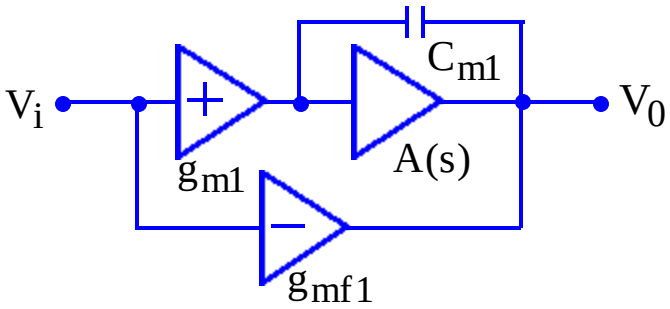
$P_h(s)$	a_1	a_2	a_3	Design
NMC	$\frac{(g_{m4}C_{m2} - g_{m2}C_{m3})}{g_{m2}g_{m4}}$	$\frac{(g_{m4} - g_{m2} - g_{m3})C_{m2}C_{m3}}{g_{m2}g_{m3}g_{m4}}$	$\frac{C_{m2}C_{m3}C_L}{g_{m2}g_{m3}g_{m4}}$	← **Complex**
NGCC	$\frac{C_{m2}}{g_{m2}}$	$\frac{C_{m2}C_{m3}}{g_{m2}g_{m3}}$	$\frac{C_{m2}C_{m3}C_L}{g_{m2}g_{m3}g_{m4}}$	← **Simple**

$Z(s)$	b_1	b_2	b_3
NMC	$\frac{C_{m3}}{g_{m4}}$	$\frac{C_{m2}C_{m3}}{g_{m3}g_{m4}}$	$\frac{C_{m1}C_{m2}C_{m3}}{g_{m2}g_{m3}g_{m4}}$
NGCC	0	0	0

Nested G_m-C Compensation (NGCC) N^{th}-Order

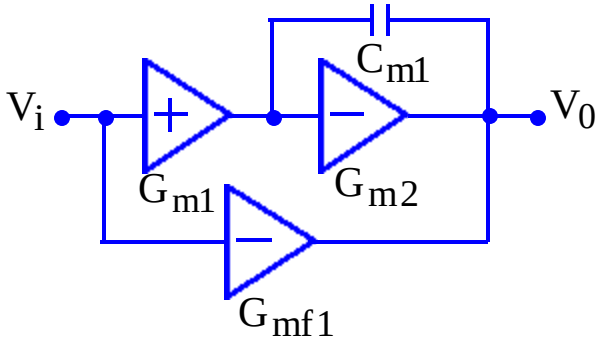


Conceptual multistage amplifier topology with NGCC.

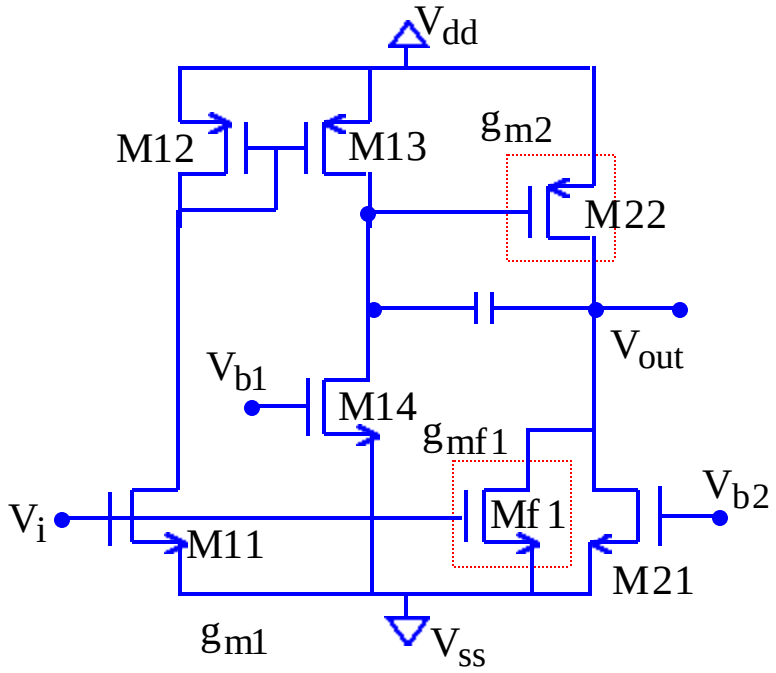


Abstract model.

How to Implement a Positive G_m?



(a) Representation



(b) Transistor Level

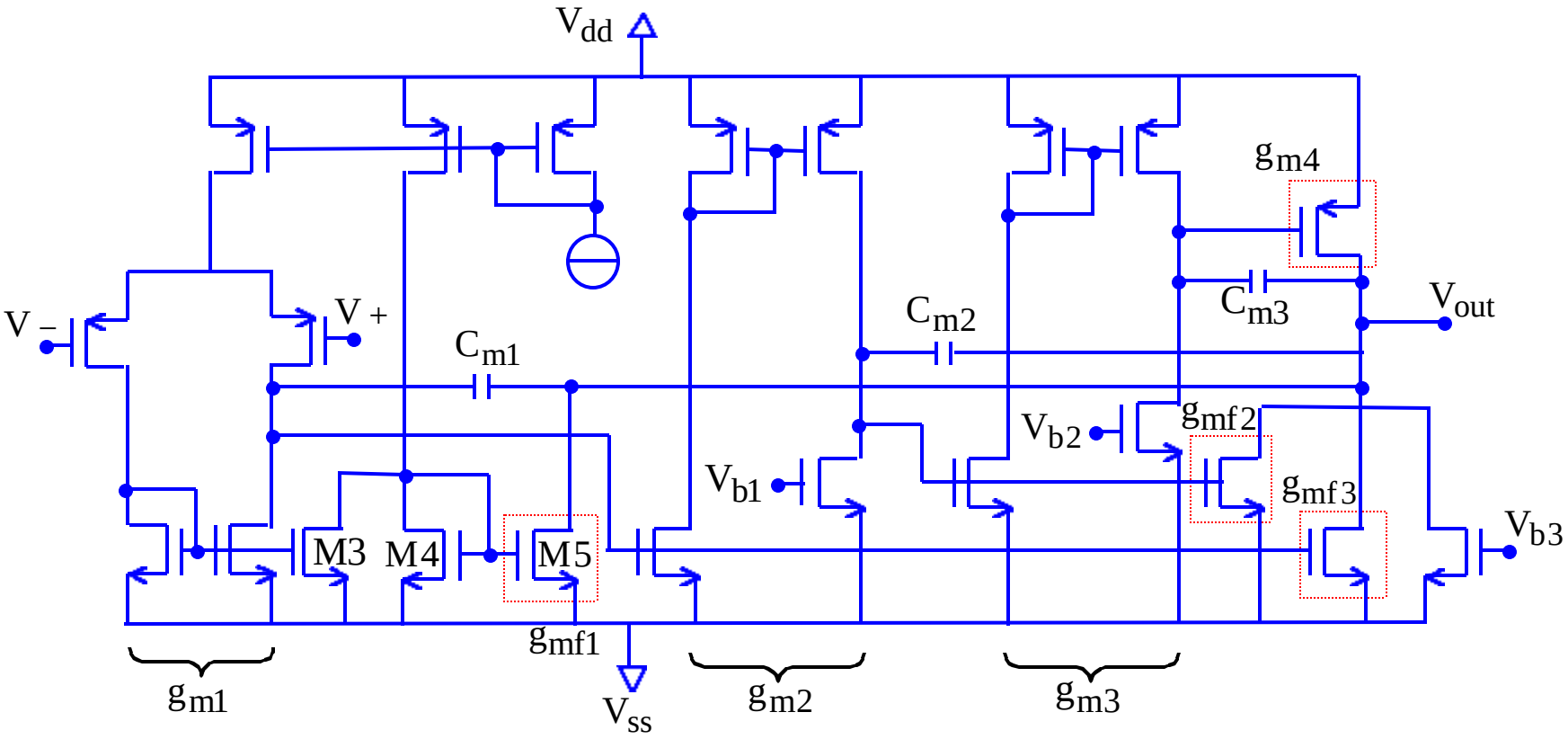
$G_{m1} \Rightarrow M11 - M14$, $g_{mM11} = g_{m1}$

$G_{m2} \Rightarrow M21 - M22$, $g_{mM22} = g_{m2}$

$G_{mf1} \Rightarrow Mf1$

- If $G_{m2} > G_{mf1}$, M22 current > Mf1 current, then add M21 to provide additional current.
- If $G_{m2} > G_{mf1}$, Remove M21 and add a PMOS transistor in parallel to M22.

Design Example of a Four-Stage Amplifier



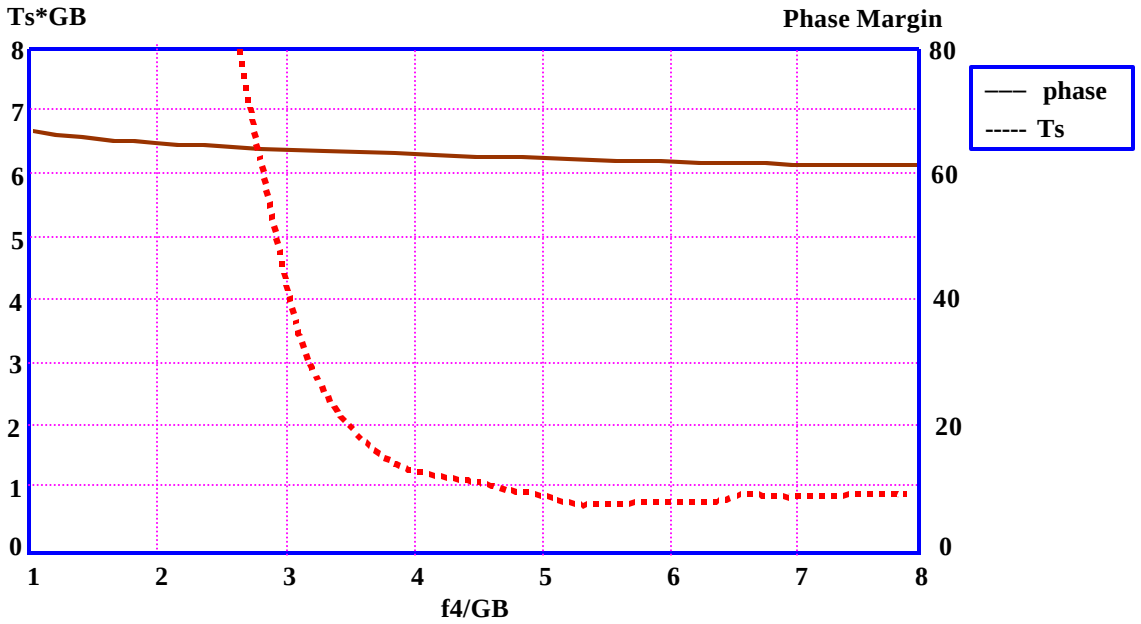
Four stage operational amplifier with NGCC topology

Measured Performance of the 4-Stage NGCC Op Amp.

Power Consumption	0.68mW	1.40mW
DC Gain	≈ 100dB	≈ 100dB
Gain Bandwidth	610kHz	1.0MHz
Phase Margin	60^{o}	58^{o}
Input Offset	5.2mV	5.2mV
Slew Rate	2.5V/μS	5.0V
Power Supply	± 1.0V	± 1.0V
Load Condition	$10k\Omega \,//\, 20\,pF$	10kΩ //20pF
Area	$0.22mm^{2}$	$0.22mm^{2}$

What is the effect of f_4 /GB?

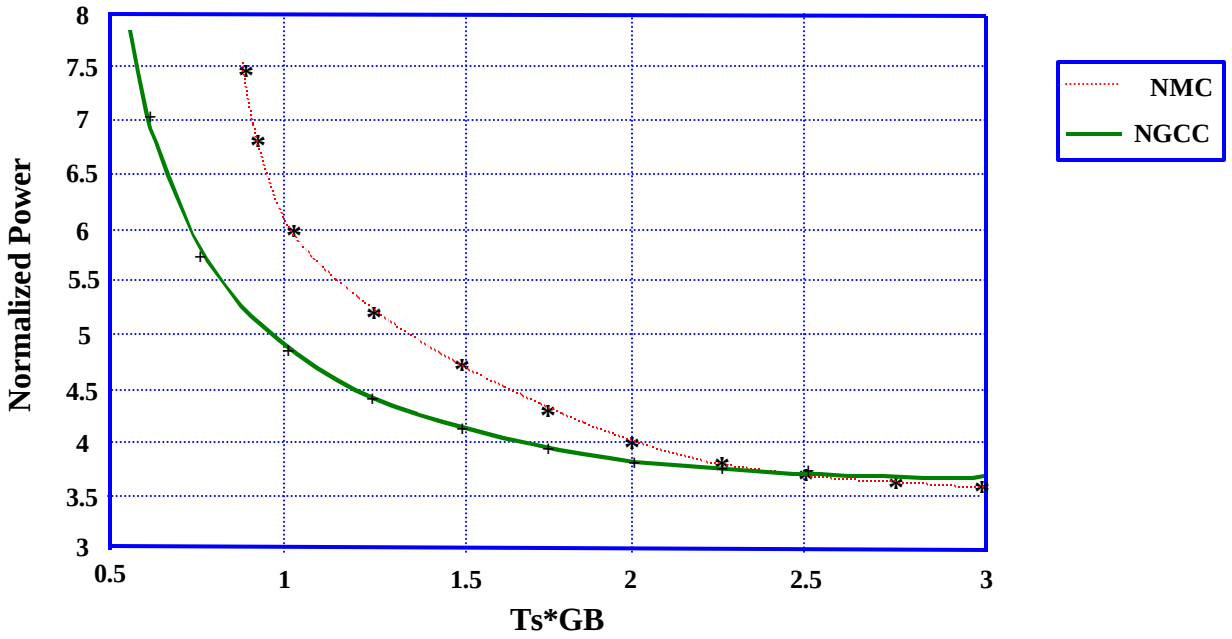
How far should one push f_4?



The phase margin and normalized settling time (TsGB) of an NGCC amplifier vs. f_4/GB.

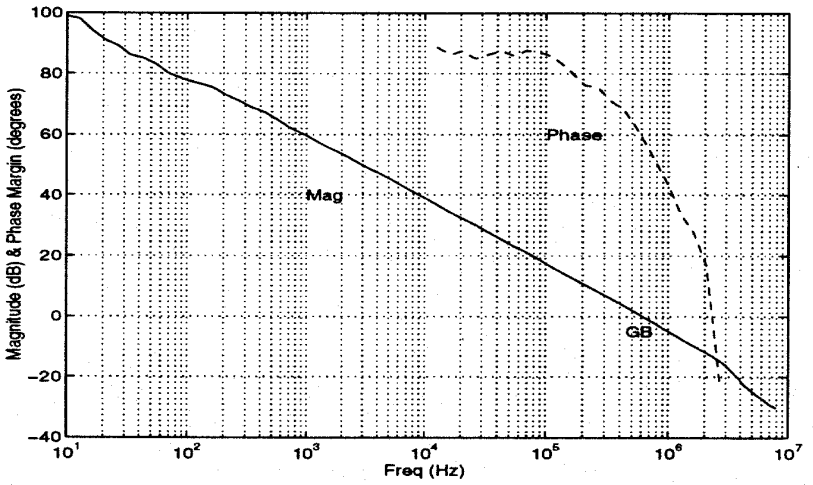
- **Trade-off between phase margin versus setting time.**

How do the Two Topologies Compare for Power Consumption?

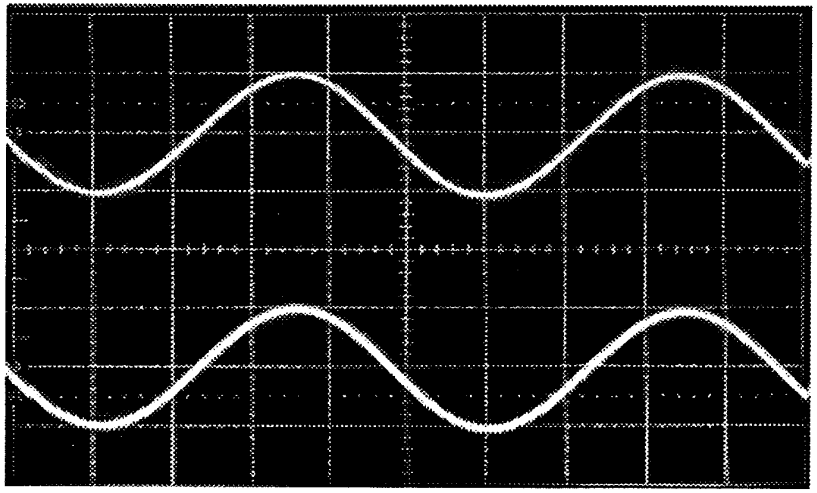


The normalized power consumption of the NGCC and the NMC amplifiers as a function of the normalized settling time.

More Experimental Results.



Measured frequency response of 4-stage NGCC amplifier



Measured 1.0Vp-p 100 KHz sin-wave at input and output nodes of a unity follower.

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K.N. Leung, P.K. T. Mok, W.-H. Ki, and J. K. O. Sin, “ Three-Stage Large Capacitive Load Amplifier with Damping Factor-Control Frequency Compensation, “*IEEE J. of Solid-State Circuits*, Vol. 35, No. 2, pp. 221-230, February 2000

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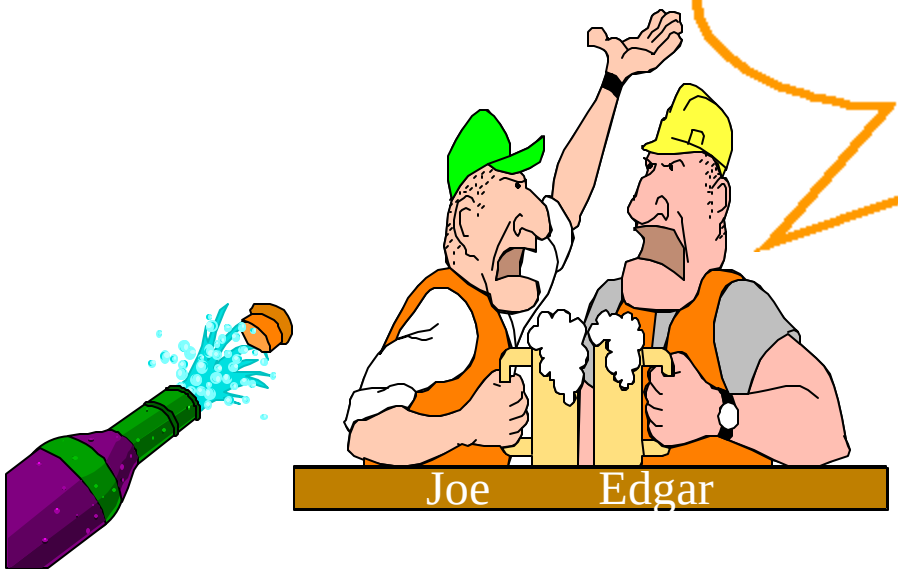
Conclusions

- Low power supply and smaller size technologies require new analog circuit techniques
- Power Consumption and area are critical specifications in portable equipment, clever design methodologies are needed.



THANK YOU