ECEN 665 (ESS) : *RF Communication Circuits and Systems*

# Low Noise Amplifiers

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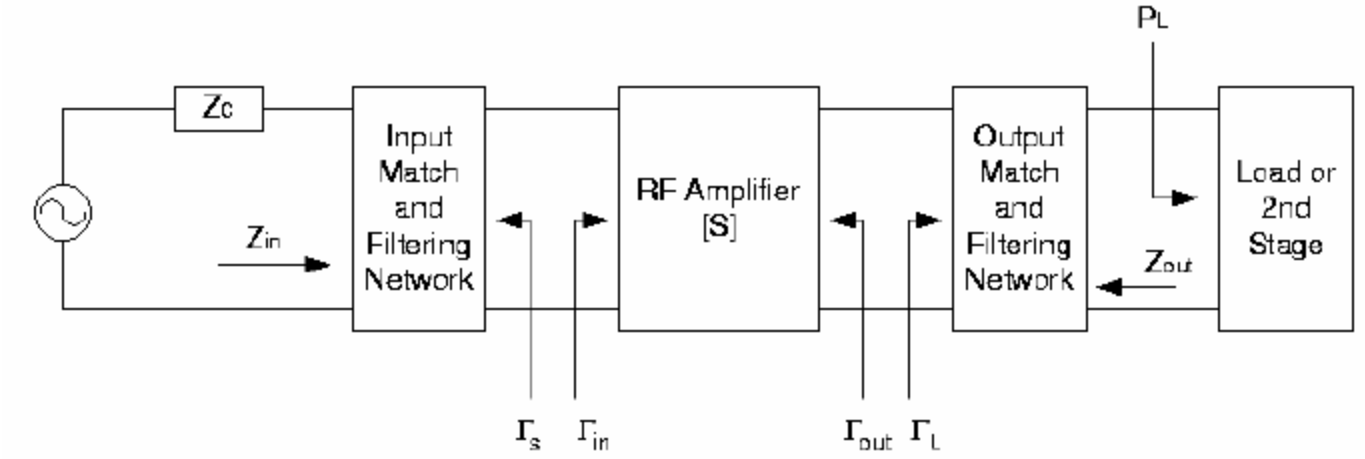
*Part of the material here provided is based on Dr. Chunyu Xin's and Dr. Xiaohua Fan's dissertation*

# What is an LNA?




- Amplifier S matrix: $[S] = \begin{pmatrix} s_{11} & s_{21} \\ s_{12} & s_{22} \end{pmatrix}$
- Source reflection coefficient: $\Gamma_S$
- Load reflection coefficient: $\Gamma_L$
- Input reflection coefficient: $\Gamma_{in} = s_{11} + \frac{s_{12}s_{21}\Gamma_L}{1 - s_{22}\Gamma_L}$
- Output reflection coefficient: $\Gamma_{out} = s_{22} + \frac{s_{12}s_{21}\Gamma_S}{1 - s_{11}\Gamma_S}$

# LNA Requirements

- Gain(10-20dB)
  - to amplify the received signal;
  - to reduce the input referred noise of the subsequent stages
- Good linearity
  - Handling large undesired signals without much distortion
- Low noise
  - for high sensitivity
- Input matching
  - Max power gain
  - Preceding filters require 50 Ω termination for proper operation
  - Can route the LNA to the antenna which is located an unknown distance away without worrying about the length of the transmission line

# LNA Metrics: Gain

- Defines small signal amplification capability of LNA
- For IC implementation, LNA input is interfaced off-chip and usually matched to specific impedance (50 Ω or 75 Ω). Its output is not necessary matched if directly drive the on-chip block such as mixer. This is characterized

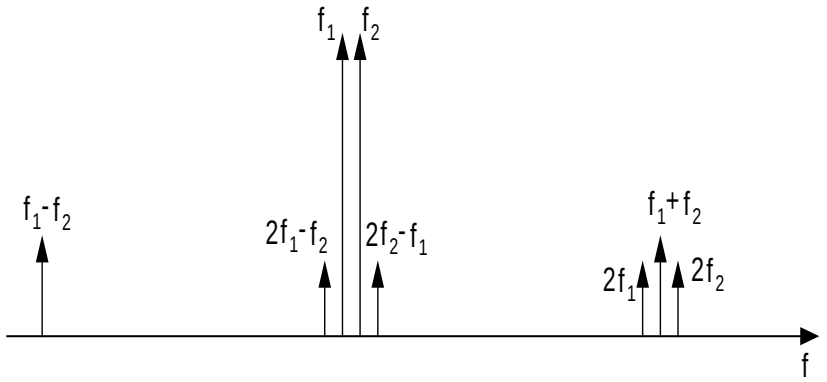
  by voltage gain or transducer power gain by knowing the load impedance level.
- Transducer power gain: Power delivered to the load divided by power available from source.

For unilateral device:

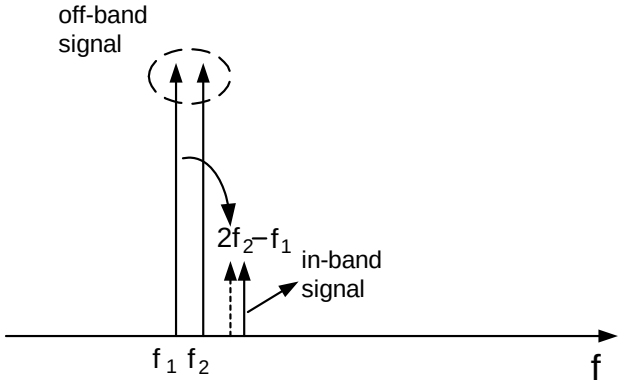
(i.e. s12 = 0)

$$G_T = \frac{1-|\Gamma_S|^2}{|1-s_{11}\Gamma_S|^2}|s_{21}|^2\frac{1-|\Gamma_L|^2}{|1-s_{22}\Gamma_L|^2}$$

# LNA Metrics: Nonlinearity Model




Output signal spectrum with f1 and f2




Nonlinear System (up to 3rd order):

$$Y_t = a_0 + a_1 X_t + a_2 X_t^{\,2} + a_3 X_t^{\,3}$$

Two tone input signal:

$$X_t = A\cos(w_1 t) + A\cos(w_2 t)$$

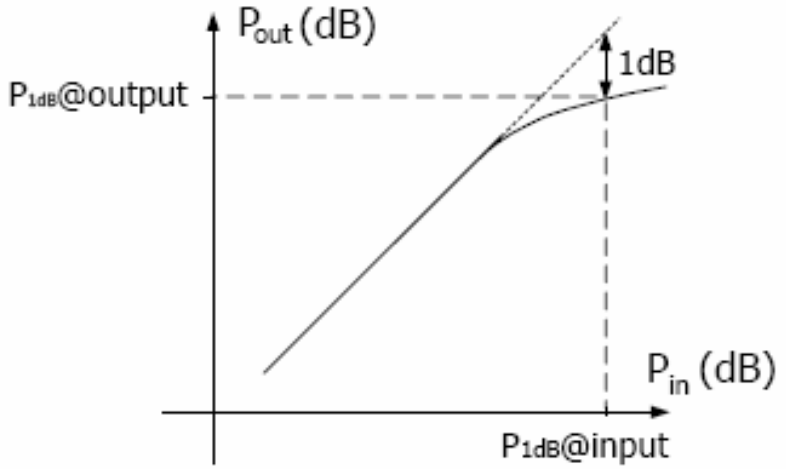
- Usually distortion term: 2f1-f2, 2f2-f1 fall in band. This is characterized by 3rd order non-linearity.
- Large in-band blocker can desensitize the circuit. It is measured by 1-dB compression point.

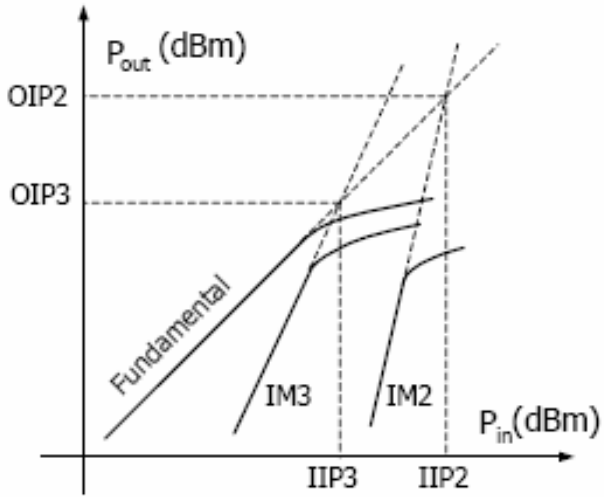
# LNA Metrics: Linearity measurement

- 1dB compression:
  Measure gain compression for large input signal

- IIP3/IIP2:
  Measure inter-modulation behavior

- Relationship between IIP3 and P1dB:
  For one tone test: IIP3-P1dB=10dB
  For two tone test: IIP3-P1dB=15dB



# LNA Metrics: Noise Figure

- Noise factor is defined by the ratio of output SNR and input SNR. Noise figure is the dB form of noise factor.
- Noise figure shows the degradation of signal's SNR due to the circuits that the signal passes.

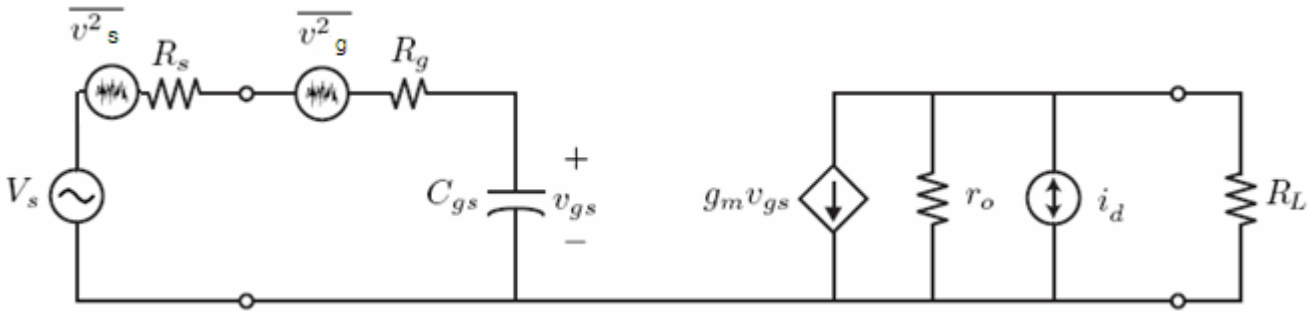
$$Sensitivity = \underbrace{Noisefloor(dBm)}_{-174dBm+10\log BW} + SNR + NF_{tot}$$

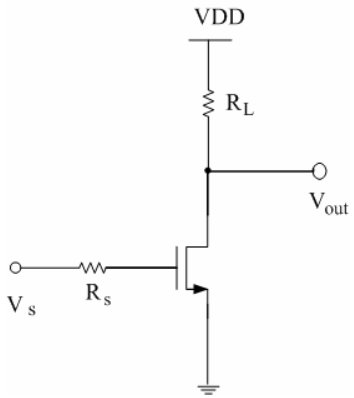
- Noise factor of cascaded system:

$$F_{tot} = F_{LNA} + \frac{F_{afterLNA} - 1}{G_{LNA}}$$

  - LNA's noise factor directly appears in the total noise factor of the system.
  - LNA's gain suppress the noise coming from following stages

# MOS Amp Noise Figure Calculation




- the current gain of the MOS amp is given by:

$$i_o = g_m v_{gs} = g_m \frac{v_s}{R_s + R_g + \dfrac{1}{j\omega C_{gs}}}\left(\frac{1}{j\omega C_{gs}}\right)$$

$$= v_s \frac{g_m}{1 + j\omega C_{gs}\left(R_s + R_g\right)} \approx v_s \frac{g_m}{j\omega C_{gs}\left(R_s + R_g\right)};\ \omega_T = \frac{g_m}{C_{gs}}$$

# Noise Figure by Current Gain

$$i_o = G_m(\omega) v_s \qquad G_m(\omega) = -j \frac{\omega_T}{\omega} \frac{1}{R_s + R_g}$$

- the total output noise current is given by:

$$\overline{i_{o,T}^2} = G_m{}^2 \left( \overline{v_g^2} + \overline{v_s^2} \right) + \overline{i_d^2}$$

- the noise figure can be easily computed:

$$F = \frac{\overline{i_{o,T}^2}}{\overline{i_o^2}} = \frac{\overline{i_{o,T}^2}}{G_m^2 \overline{v_s^2}} = 1 + \frac{\overline{v_g^2}}{\overline{v_s^2}} + \frac{\overline{i_d^2}}{G_m^2 \overline{v_s^2}},$$

$$\overline{v_g^2} = 4kTR_g, \overline{v_s^2} = 4kTR_s, \overline{i_d^2} = 4kT \frac{\gamma}{\alpha} g_m$$

# Noise Figure Calculation(cont.)

- Substitution of the the various noise sources leads to :

$$F = 1 + \frac{R_g}{R_s} + \frac{\left(\frac{\gamma}{\alpha}\right) g_m}{R_s} \left(\frac{\omega}{\omega_T}\right)^2 \left(R_s + R_g\right)^2$$

$$\approx 1 + \frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m R_s$$

  - This expression contains both the channel noise and the gate induced noise
  - $R_g = R_{poly} + \frac{1}{5g_m}$ is a good approximation

# Minimum Noise for MOS Amp

- the optimal value of Rs :

$$\frac{\partial F}{\partial R_s} = -\frac{R_g}{R_s^2} + \left(\frac{\gamma}{\alpha}\right) g_m \left(\frac{\omega}{\omega_T}\right)^2 = 0$$

$$R_{s,opt} = R_s = \frac{\omega_T}{\omega} \sqrt{\frac{R_g}{\left(\frac{\gamma}{\alpha}\right) g_m}}$$

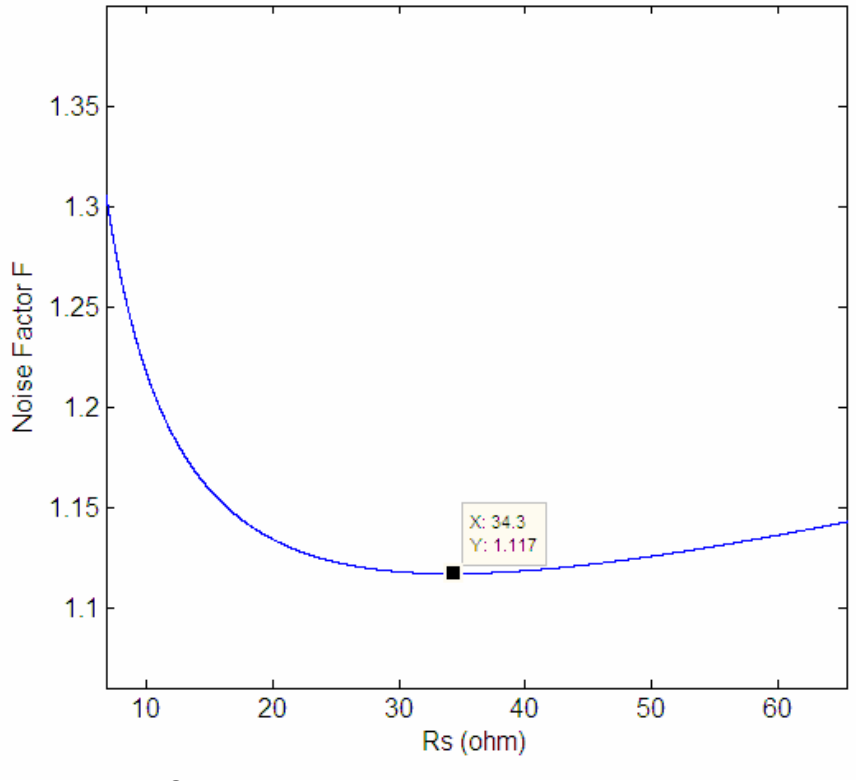
- Thus the minimum Noise Figure is:

$$F_{\min} = 1 + 2\left(\frac{\omega}{\omega_T}\right) \sqrt{\left(\frac{\gamma}{\alpha}\right) g_m R_g}$$

# F vs. Rs

- For an LNA operating at 5.2GHz in 0.18 μm CMOS process, according to experience and published literatures, we can choose $R_g = 2\,\Omega$, $\gamma = 3$, $\alpha = 0.75$, $\omega_T = 2\pi * 56GHz$, $g_m = 50mA/V$ and plot F vs. Rs:

$$F = 1 + \frac{R_g}{R_s} + \left(\frac{\gamma}{\alpha}\right)\left(\frac{\omega}{\omega_T}\right)^2 g_m R_s$$



# MOS Amp Example

- Find $R_{s,opt}$ for a typical amplifier. Assume $f_T = 75GHz$ $f = 5GHz, (\gamma/\alpha) = 2$ , $R_{poly}$ is minimized by proper layout, thus intrinsic gate resistance is given by:

$$R_g = R_{poly} + \frac{1}{5g_m} \cong \frac{1}{5g_m}$$

- To make the noise contribution from this term 0.1:

$$\frac{R_g}{R_s} = 0.1 \Rightarrow g_m = \frac{10}{5R_s} = 40mS \Rightarrow R_{s,opt} \approx 119\Omega,\ F_{\min} = 1.08$$

- In practice, it'll be difficult to get such a low Noise figure and get useful gain with the simple common source due to the bad power match
- Conflict of minimum noise vs. optimum matching
- That's why we need input matching schemes for LNA!

# LNA Metrics: Input Matching

- Why do we need it?
- We have learned how to choose optimum source impedance for minimum noise figure
- One important requirement for LNA is 50 ohm matching
- The input of a common source amplifier is primarily capacitive and provides very poor power match!

Maximum power transfer: $Z_{in} = Z_s^*$

$$P_{in\_LNA\_\max} = \frac{V_1^2}{|Z_{in}|} = \frac{V_s^2 |Z_{in}|}{\left(|Z_{in} + Z_s|\right)^2} = \frac{V_s^2}{2\,\mathrm{Re}(Z_s)} = \frac{P_{in}}{2}$$

- What should we do to have both good NF and good power match?

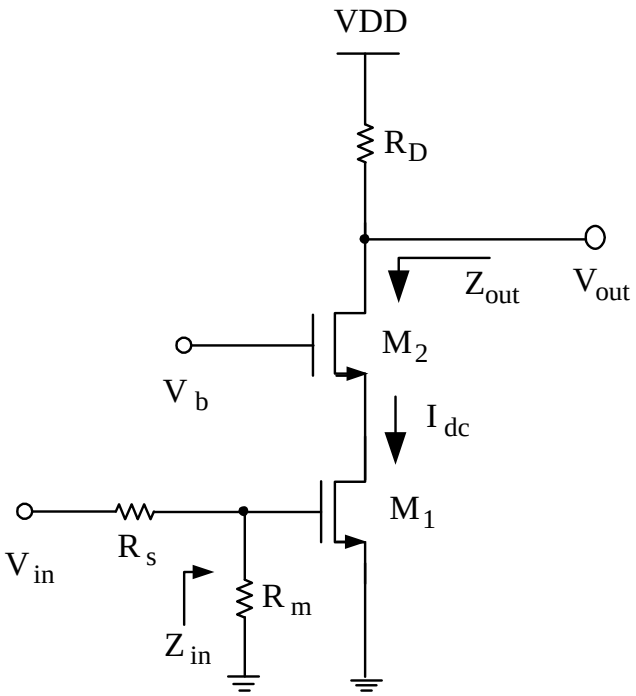
# LNA Input Matching Topologies

- Wideband LNA:
  - Resistive termination
  - Common Gate
  - Resistive shunt-feedback
- Narrowband LNA:
  - Inductive degenerated
  - Resistive terminated

# Resistive Termination LNA

- Since the input of a CS MOS devices is primarily capacitive then we can terminate the input with a resistor Rm=Rs to match the input (at low frequencies)

- It can be used in both narrowband and the wideband application. But its high NF(usually NF>6dB) characteristic limits its application.

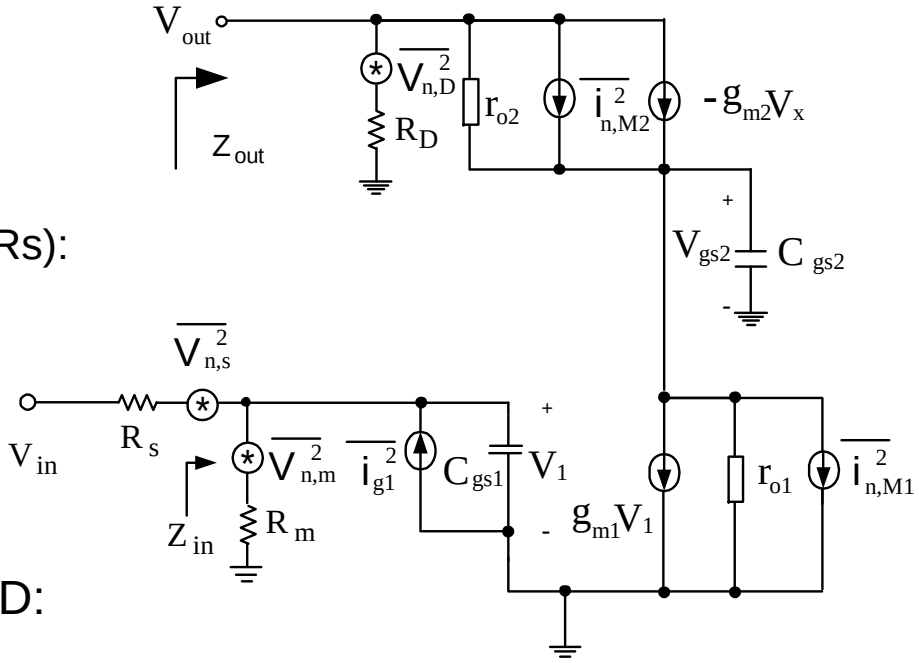


# Noise Analysis

Output noise due to source resistor Rs:

$$V_{n,s}^2 = KTR_s A_v^2 = KTR_s (g_{m1} R_D)^2$$

where $A_v \cong g_{m1} R_D$ and $R_D << Z_{out}$




Output noise due to matching resistor Rm(=Rs):

$$V_{n,m}^2 = KTR_s (g_{m1} R_D)^2$$

Output noise due to thermal noise of M1:

$$i_{n,m1}^2 = 4KT \frac{\gamma}{\alpha} g_{m1}$$

Output noise due to the load resistor, RD:

$$V_{n,s}^2 = KTR_D$$

Output noise due to thermal noise of M2:

$$i_{n,m2}^2 = 4KT \frac{\gamma}{\alpha} g_{m2} \left( \frac{sC_{gs2}}{g_{m2} + sC_{gs2}} \right)^2 = i_{n,m1}^2 \frac{g_{m2}}{g_{m1}} \left( \frac{sC_{gs2}}{g_{m2} + sC_{gs2}} \right)^2$$

# Noise Analysis

- The noise factor of the LNA is:

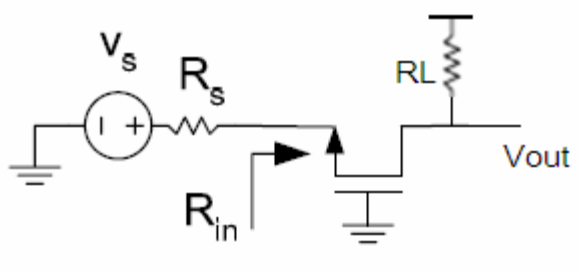
$$F = \frac{\text{total output noise}}{\text{noise due to the source resistor}} \geq \frac{V_{n,s}^2 + V_{n,m}^2 + V_{n,m1}^2 + V_{n,D}^2 + V_{n,m2}^2}{V_{n,s}^2}$$

- Noise from RD is attenuated by LNA gain. The noise transfer function of M2 is smaller due to source degeneration. Both are ignored for simplicity:

$$F = 1 + \frac{R_m^2}{R_s^2} + \frac{4\gamma}{\alpha g_{m1} R_s} = 2 + \frac{4\gamma}{\alpha g_{m1} R_s}$$

- Therefore, even when gmRs>>4 $\gamma$ , Fmin>2 (NF>3dB)
- Resistor termination provides a good power match but greatly degrades the NF
  - The terminating resistor adds its own noise
  - It also drops the gain by 6dB (compared to CS with no termination). As a result the input referred noise of the device and those of the following stages increase by the same factor

# Common Gate(CG) LNA




- Input impedance:

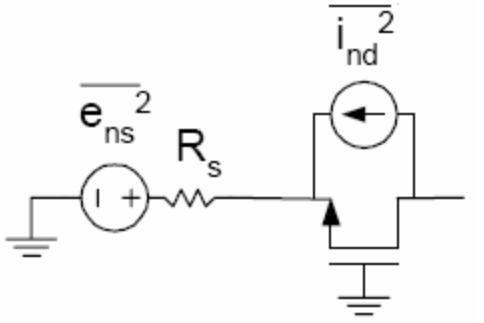
$$Z_{in} = \frac{1}{g_m + j\omega C_{gs}}$$

$$\text{if } \omega C_{gs} << g_m \Rightarrow \omega << \frac{g_m}{C_{gs}} \Rightarrow \omega << \omega_T \Rightarrow Z_{in} \approx \frac{1}{g_m}$$

- Noise Figure:

ignoring poly gate resistance, gate noise, and ro, the output current noise is:

$$\overline{i_{no}^2} = \overline{i_{no,ind}^2} + \overline{i_{no,R_s}^2}$$

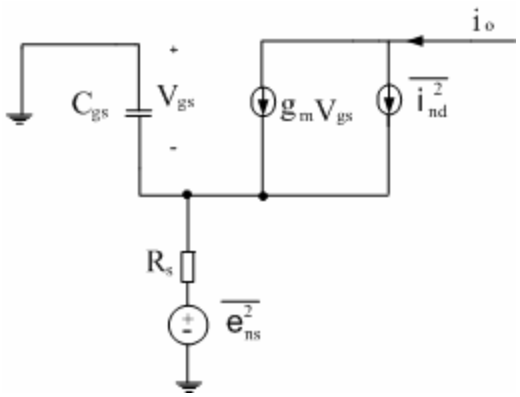



$\overline{i_{no,ind}^2}$: drain current noise

$\overline{i_{no,R_s}^2}$: output noise current due to source resistance

$$\overline{i_{no,R_s}^2} = \frac{\overline{e_{ns}^2}}{(R_s + R_{in})^2} = \left(\frac{g_m}{1 + g_m R_s}\right)^2 \overline{e_{ns}^2}$$

# Noise Analysis



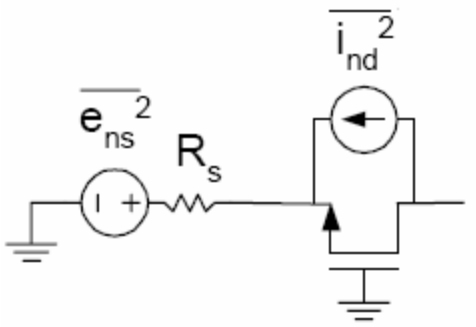

$$\left.\begin{aligned} i_o &= i_{nd} + g_m v_{gs} \\ v_{gs} &= -\left(i_{nd} + g_m v_{gs} + j\omega C_{gs} v_{gs}\right) R_s \Rightarrow v_{gs} = -\frac{i_{nd} R_s}{1 + g_m v_{gs} + j\omega C_{gs} v_{gs}} \end{aligned}\right\} \Rightarrow$$

$$i_o = i_{nd} \frac{1 + j\omega C_{gs} R_s}{1 + g_m v_{gs} + j\omega C_{gs} R_s} \approx i_{nd} \frac{1}{1 + g_m R_s}, \quad \left(\text{assume } \omega C_{gs} R_s << 1\right)$$

- Notice that if gm=1/Rs (power match) then only half of drain current noise goes to the output

# Noise Analysis

- Noise Factor:




$$F = 1 + \frac{\overline{i_{nd}^2}\left(\frac{1}{1+g_m R_s}\right)^2}{e_{ns}^2\left(\frac{g_m}{1+g_m R_s}\right)^2} = 1 + \frac{\gamma g_{d0}}{g_m^2 R_s}$$

- Under the input matching condition: Rs=1/gm we have:

$$F = 1 + \frac{\gamma g_{d0}}{g_m} = 1 + \frac{\gamma}{\alpha} = \begin{cases} \frac{5}{3} = 2.2dB & \text{Long channel} \\ \geq 3 = 4.8dB & \text{Short channel} \end{cases}$$

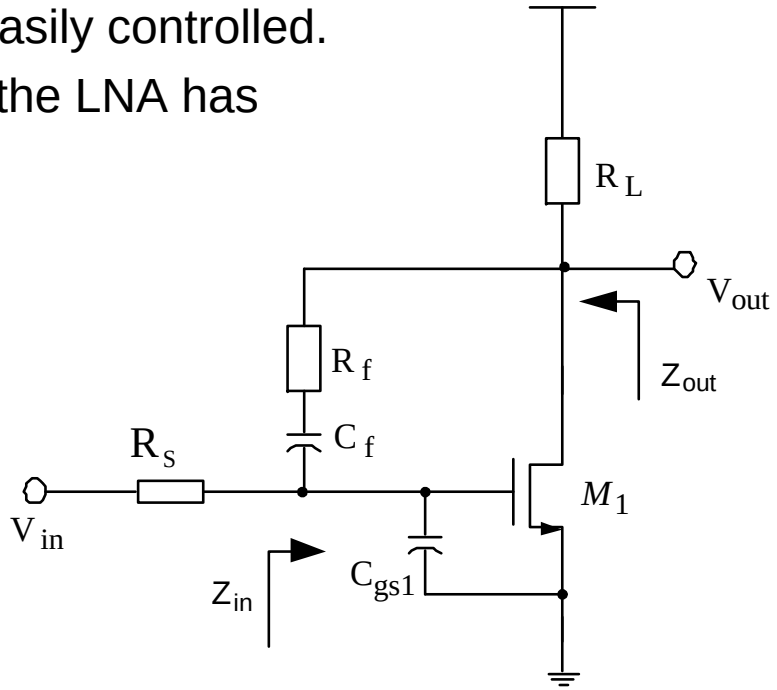
# Resistive Shunt-feedback LNA

- The negative feedback network is used to implement the input matching
- The input impedance is determined by open loop gain and the resistor values ($R_f$, $R_L$), which are easily controlled.
- The resistor is a noise component and the LNA has moderate noise performance.

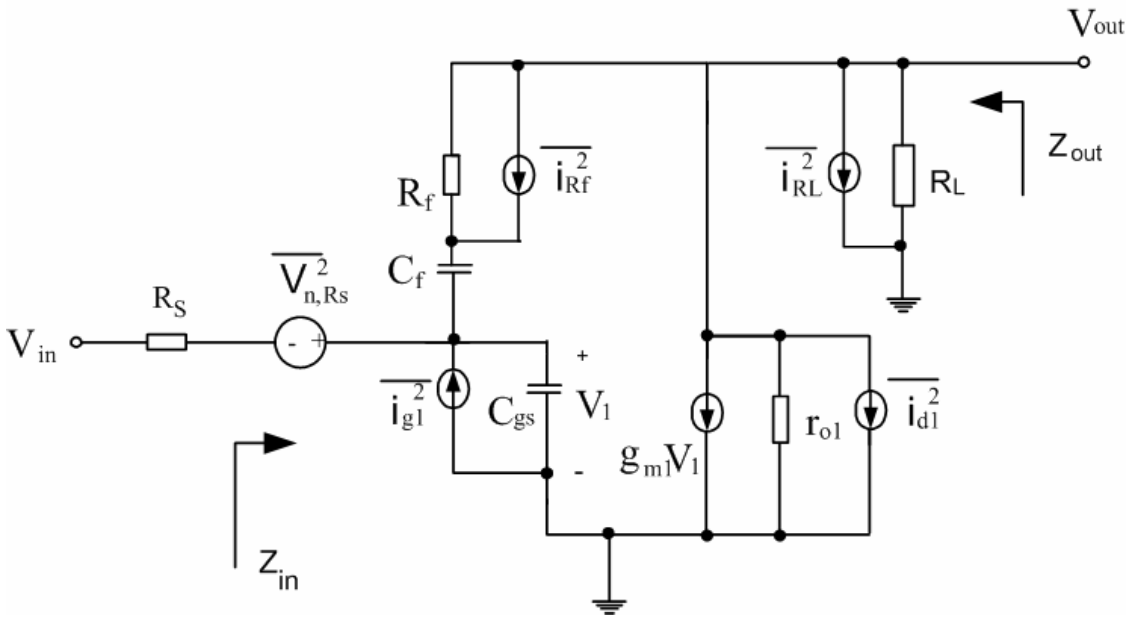
Voltage gain: $$A_v = \frac{R_L\left(1 - g_{m1}R_f\right)}{R_f + R_L}$$

Input impedance: $$Z_{in} = \frac{R_f + R_L}{1 + g_{m1}R_L} // \frac{1}{sC_{gs1}}$$

Output impedance: $$Z_{out} = R_L // \frac{R_s + R_f}{1 + g_{m1}R_s}$$



# Noise Analysis




- Noise Factor:

$$F = 1 + \frac{4\times\overline{i_{R_f}^2}}{\overline{V_{n,R_s}^2}}\left(\frac{Z_{out}}{A_v} - \frac{R_s}{2}\right)^2 + \frac{4\times\overline{i_{R_L}^2}\cdot Z_{out}^2}{\overline{V_{n,R_s}^2}\cdot A_v^2} + \frac{4\times\overline{i_{d1}^2}\cdot Z_{out}^2}{\overline{V_{n,R_s}^2}\cdot A_v^2}$$

$$= 1 + \frac{R_f}{R_s}\left(\frac{1+g_{m1}R_s}{1-g_{m1}R_f}\right)^2 + \frac{1}{R_sR_L}\left(\frac{R_f+R_s}{1-g_{m1}R_f}\right)^2 + \frac{\gamma g_{m1}}{\alpha R_s}\left(\frac{R_f+R_s}{1-g_{m1}R_f}\right)^2$$

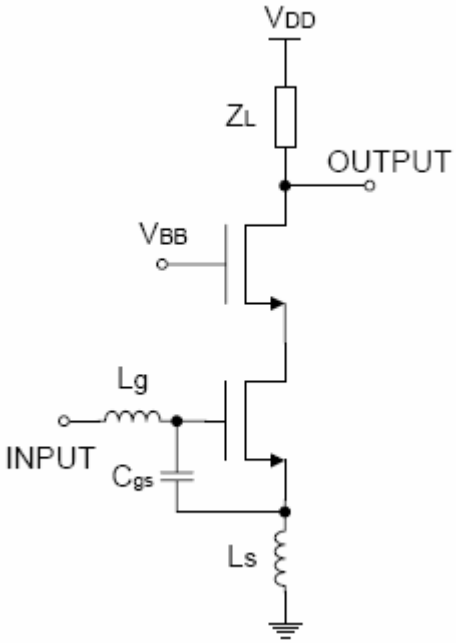
# Inductive degenerated LNA

- Input impedance behaves like a series RLC circuit, gate inductor Lg is added to tune the resonant frequency to align with the operating frequency:

$$Z_{in} = s\left(L_g + L_s\right) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}$$

- Matching occurs when: $Z_{in}\left(j\omega_0\right) = R_s$

$$\omega_o^2 = \frac{1}{\left(L_g + L_s\right)C_{gs}}, \text{ and } R_s = \frac{g_m L_s}{C_{gs}} = \omega_T L_s$$




- Ls can be selected by: $L_s = \frac{R_s}{\omega_T}$

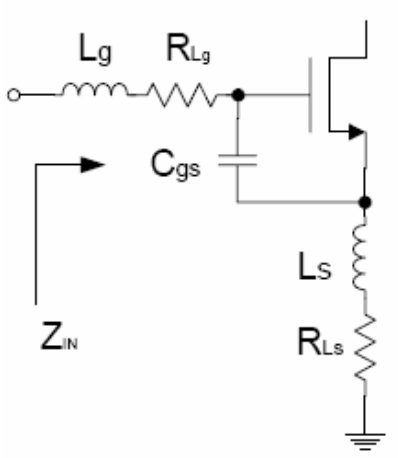
  if this value is too small to be practical, a capacitor can be inserted in shunt with $C_{gs}$ to artificially reduce $\omega_T$

# Input impedance-non-idealities

$$Z_{in} = s\left(L_g + L_s\right) + \frac{1}{sC_{gs}} + \omega_T L_s + \frac{1}{s\frac{1}{\omega_T R_{Ls}}} + R_{Lg} + R_g + R_{Ls} + R_{g,NQS}$$

$$\omega_o = \frac{1}{\sqrt{\left(L_g + L_s\right)\left(C_{gs} \,//\, \frac{1}{\omega_T R_{Ls}}\right)}} \qquad R_g = \frac{R_{poly,sh} W}{12 n^2 L} \qquad R_{g,NQS} = \frac{1}{5 g_m}$$

$$Z_{in}\left(j\omega_0\right) = \omega_T L_s + R_{Lg} + R_g + R_{Ls} + R_{g,NQS}$$




- Inductance loss $R_{Lg}$ : offset $Z_{in}$
- $R_{Ls}$ : offset $Z_{in}$ and $w_0$
- Gate resistance $R_g$ : offset $Z_{in}$
- NQS gate resistance $R_{g,NQS}$ : offset $Z_{in}$

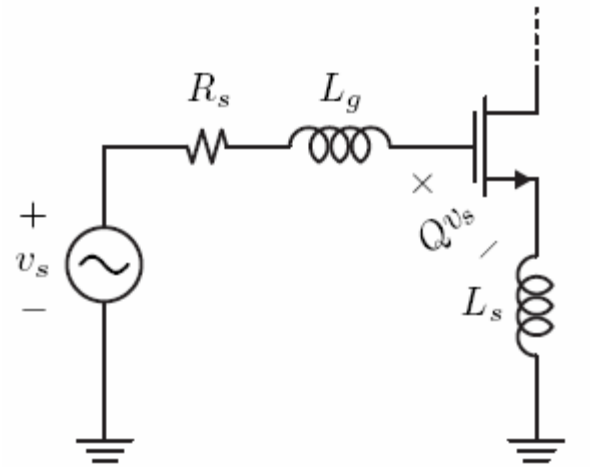
# Q Boosting

- At resonance we get Q boosting effect:

$$Q = \frac{1}{(R_s + L_s\omega_T)C_{gs}\omega_0} = \frac{1}{2R_sC_{gs}\omega_0}$$

$$v_{gs} = Q \times v_s$$

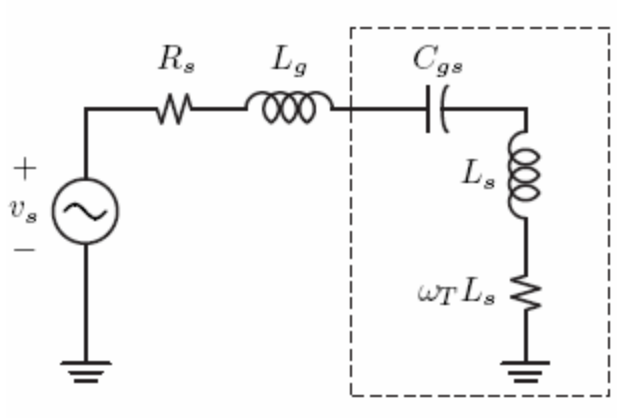
$$i_d = g_m v_{gs} = \underbrace{Qg_m}_{G_m} v_s = \underbrace{\frac{1}{2R_s}\left(\frac{\omega_T}{\omega_0}\right)}_{G_m} v_s$$



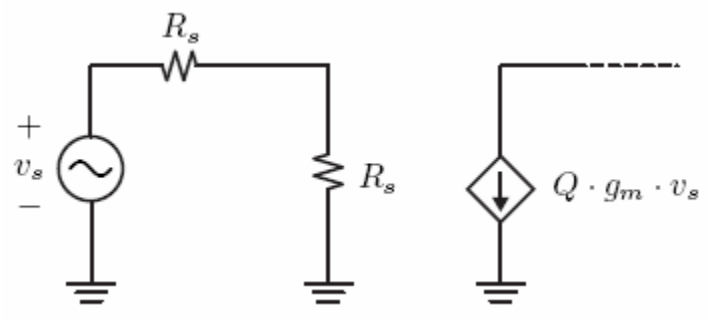

- Need to watch out for linearity as vgs is Q times larger than the input signal
  - Short channel devices operating in velocity saturation regime (i.e., large overdrive voltage) are more forgiving as their gm is relatively constant.

# Equivalent input network

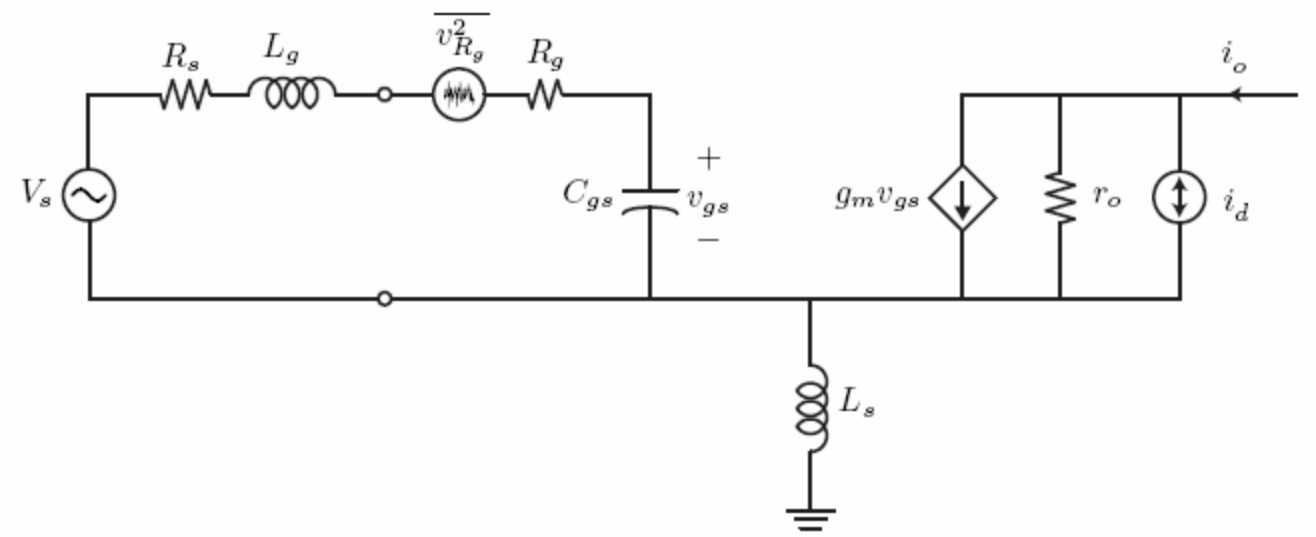
- From the source, the amplifier input(ignoring Cgd) is equivalent to:




- At resonance, the complete circuit is as follows:



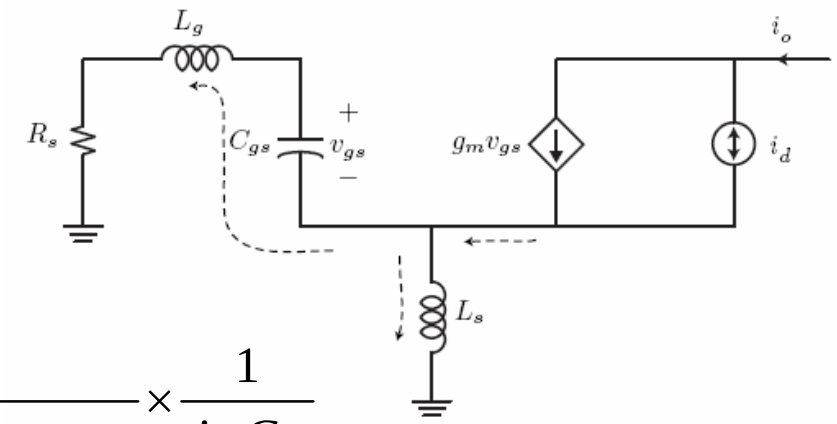
# Noise Analysis




- The output noise current due to Rs and Rg is simply calculated by multiplying the voltage noise sources by Gm
- The calculation of output noise current due to drain noise is more involved: $\overline{i_d^2}$ flows partly into the source of the device, it activates the gm of the transistor which produces a correlated noise in shunt with $\overline{i_d^2}$
- Output noise current: $\overline{i_{no}^2} = G_m^2\left(\overline{v_{R_s}^2} + \overline{v_{R_g}^2}\right) + \overline{i_{d,out}^2}$ , $G_m = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_o}\right)$

# Noise Analysis: Drain Noise

- The noise component flowing into the source is given by the current divider:




$$v_{gs} = -\left(g_m v_{gs} + i_d\right) \times \frac{j\omega L_s}{j\omega L_s + \frac{1}{j\omega C_{gs}} + j\omega L_g + R_s} \times \frac{1}{j\omega C_{gs}}$$

$$= -\left(g_m v_{gs} + i_d\right) \times \frac{j\omega L_s}{R_s} \times \frac{1}{j\omega C_{gs}} \text{ (at resonance)} \qquad \Rightarrow g_m v_{gs} = -\frac{i_d}{2}$$

- Note that we are not including $R_g$ in the small signal model

# Total Output Noise

- Let's first ignore the correlation of the gate noise and drain current noise. Notice only ¼ of the drain noise flows to output

$$\overline{i_{no}^2} = G_m^2\left(\overline{v_{R_s}^2} + \overline{v_{R_g}^2}\right) + \frac{1}{4}\overline{i_d^2} \qquad G_m = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_o}\right)$$

$$F = \frac{\overline{i_{no}^2}}{G_m^2\overline{v_{R_s}^2}} = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}g_m R_s\left(\frac{\omega_o}{\omega_T}\right)^2$$

Note that the Noise figure at resonance is the same as CS amplifier w/o inductive degeneration. Inductive degeneration did not raise $F_{min}$ but matched the input !

# Total Output Noise(cont.)

- If we consider the correlation of the gate noise and drain current noise then one can show (*)

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\chi g_m R_s \left(\frac{\omega_o}{\omega_T}\right)^2$$

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + Q_L^2\right)$$

$$Q_L = Q_{C_{gs}} = \frac{1}{\omega_o R_s C_{gs}} = \frac{\omega_o\left(L_g + L_s\right)}{R_s}$$

- Optimal Noise figure happens for a particular $Q_L$. Possible to obtain a noise and power match

* D.K. Shaeffer, T.H. Lee, "A 1.5V 1.5GHz CMOS Low Noise Amplifier", JSSC, Vol. 32, No. 5. May 1997

# Optimal $Q_L$

- If we try to optimize the noise figure while power dissipation is kept constant then:
  - $Q_{L,opt}$ will be independent from the frequency and around 4.5
  - Fmin is not too sensitive to $Q_L$ and only changes by less than 0.1dB for $Q_L$ between 3.5 and 5.5
  - Smaller $Q_L$ results in larger bandwidth and smaller inductors, while a larger $Q_L$ results in narrower bandwidth and larger inductors

# Linearity

- Linearity of a MOS transistor in saturation region:

$$V_{IIP3,strong\ MOS}^2 = \frac{4}{3}\frac{V_{eff}}{\theta}\left(2+\theta V_{eff}\right)\left(1+\theta V_{eff}\right) > \frac{8}{3}\frac{V_{eff}}{\theta}$$

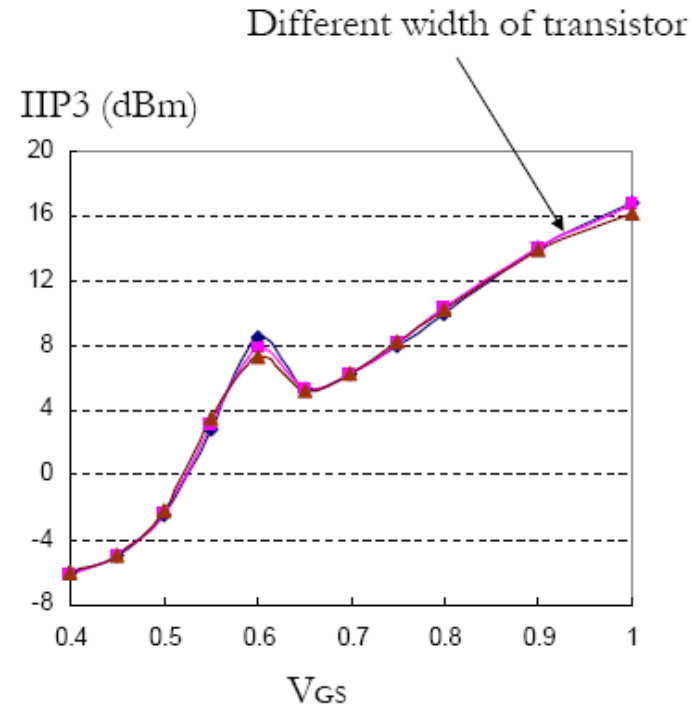
$$V_{eff} = V_{gs} - V_{th} \qquad \theta = \frac{1}{E_{sat}L}$$

$E_{sat} \sim 1V/\mu m$ for L~0.35 $\mu$ m-0.18 $\mu$ m

- IIP3 is independent of W

$$V_{IIP3,LNA}^2\left(V^2\right) = \frac{16}{3}\frac{P_D^2}{P_o^2\theta^2}\left(2+\rho\right)\left(1+\frac{1}{\rho}\right)^3$$

$$\rho = \theta V_{eff} \qquad P_o = \frac{3}{2}\frac{v_{sat}E_{sat}}{\omega_o R_s}V_{DD}$$




MOS transistor's IIP3 v.s. gate drive voltage

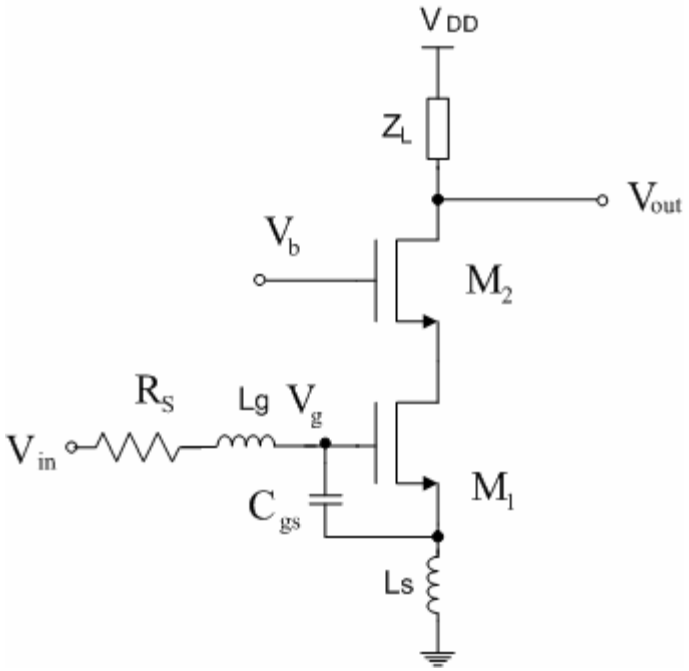
# Design Recipe for Inductive degenerated LNA

- Step 1: Choose $Q_L$ for optimal NF$\Rightarrow$ $C_{gs}$ $\Rightarrow$ Width(W)

$$\left(Q_L = 1/\omega_o R_s C_{gs}\right)$$

- Step 2: Determine the current($I_d$) from power budget
- Step 3: From W & $I_d \Rightarrow g_m$ and $V_{eff}$
- Step 4: From $g_m$ and $V_{eff} \Rightarrow \omega_T$ and $F_{min}$
- Step 5: Select $L_s$ and $L_g$ for the input network

$$L_s = R_s/\omega_T \qquad L_g = \left(1/\omega_o^2 C_{gs}\right) - L_s$$



# Design Recipe: Iterations

- NF is not low enough?
  - Increase $\omega_T$ by increasing $I_d$ (with fixed device size)
  - For fixed current density, increasing Q will reduce device size thus reduce total power - NF will increase
- Linearity doesn't meet spec?
  - Reduce Q (in short channel devices the improvement is limited)
  - Burn more current (not gaining much due to velocity saturation)
  - Apply proper linearization techniques
- Need to increase gain?
  - Larger $Q_L$
  - Larger $g_m$
  - Larger Load($Z_L$)

# Design Example:

- Specs:

| | |
|---|---|
| Frequency | 2.4GHz |
| S11 | <-10dB |
| S21 | >15dB |
| NF | <2dB |
| IIP3 | >-10dBm |
| Current | <10mA |
| Supply | 1.8V |
| Process | 0.18 μ m CMOS |

- Step 1: Choose $Q_L$ = 4.5. then

$$C_{gs} = 1/2Q_L\omega_o R_s = 147\ fF$$

Choose minimum length L = 0.18 μ m

→ W = 110 μ m

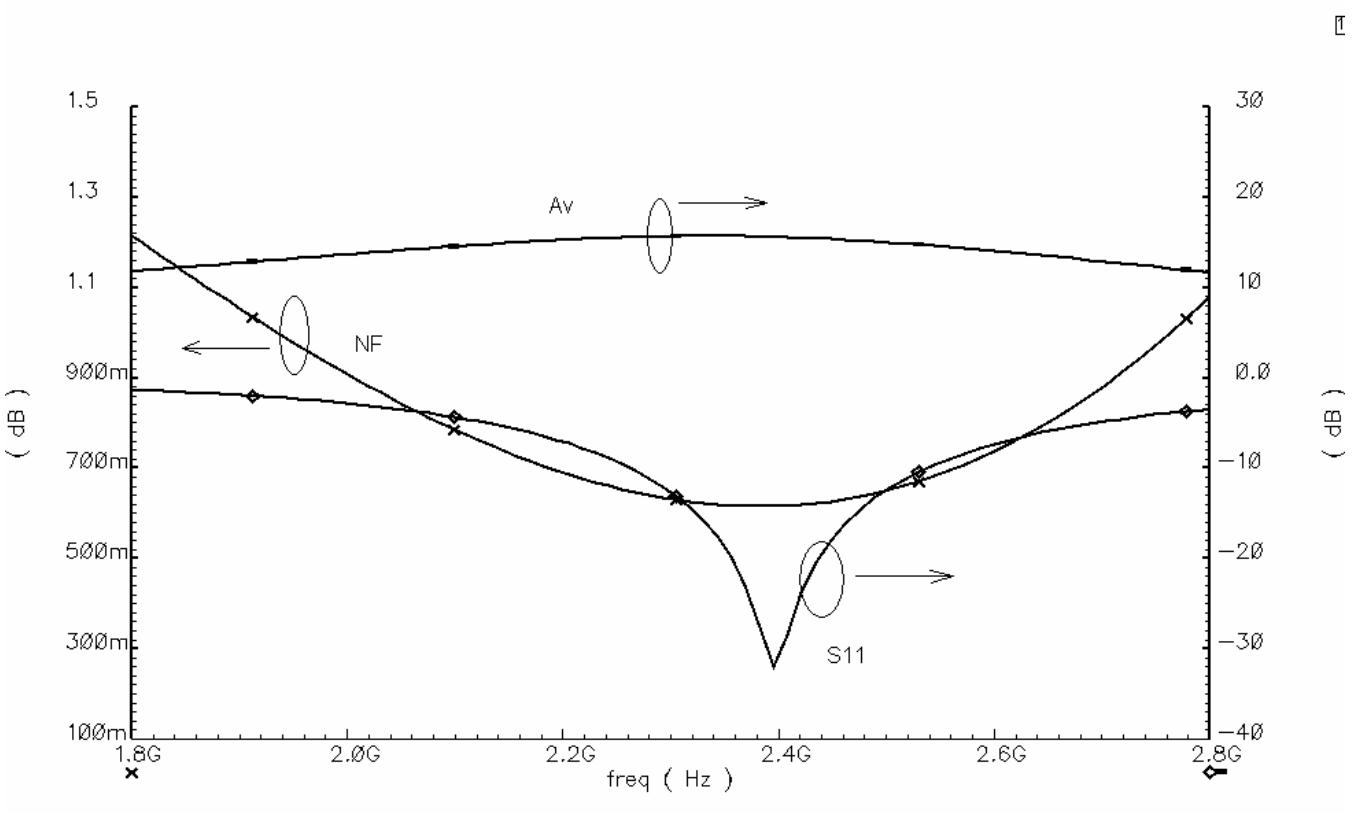
- Step 2: Choose the current $I_d$ = 9mA
- Step 3: From W & $I_d$ → $g_m = 52\text{mA/V}$
- Step 4: From $g_m$ and $C_{gs}$ → $f_T$ = 56GHz
- Step 5: Select $L_s$ and $L_g$ for the input network:

$$L_s = R_s/\omega_T = 0.14nH$$

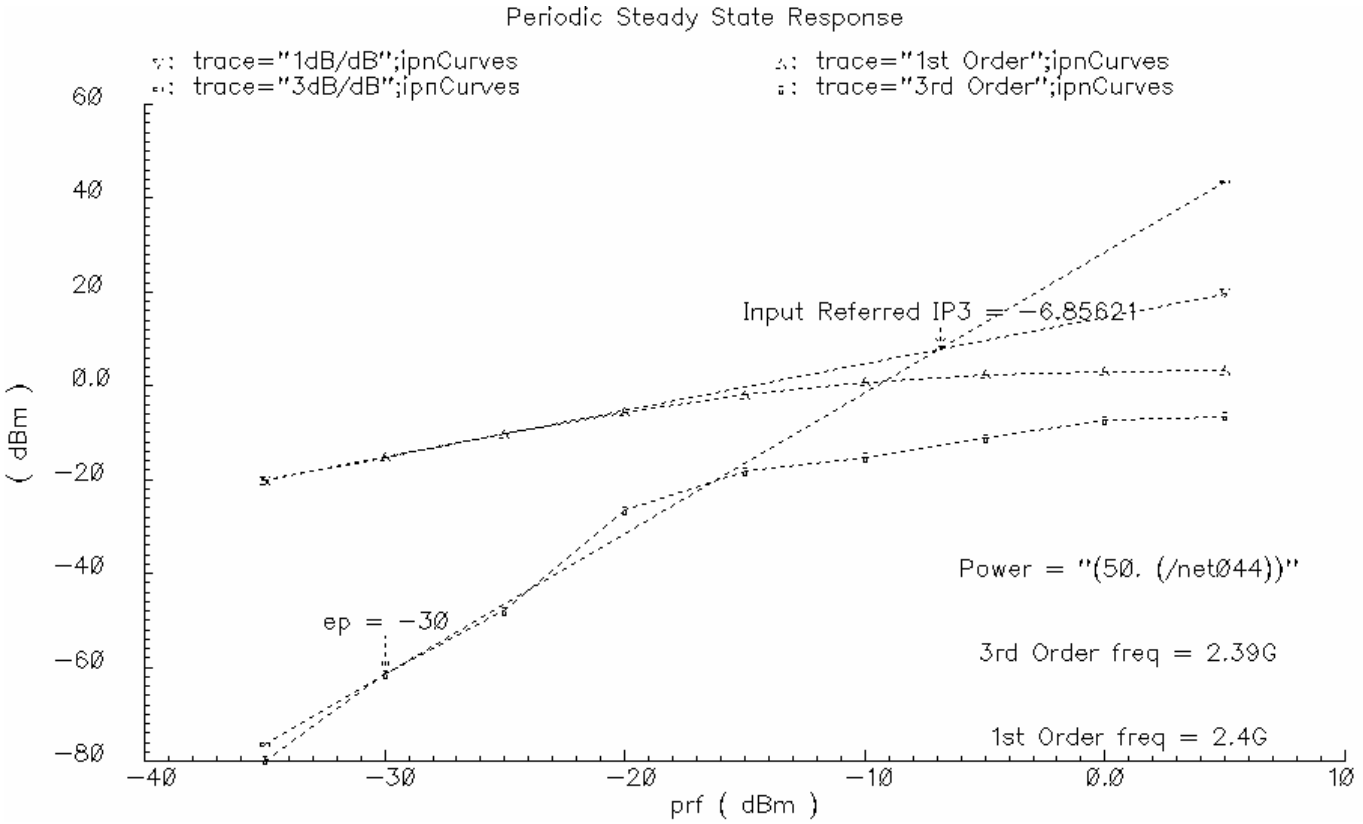
$$L_g = 1/\omega_o^2 C_{gs} - L_s = 31nH$$

- Step 6: S21 requirement→ $Z_L = 24\ \Omega$

# Simulation Results: S21, S11, NF



# Simulation Results: IIP3



# Summary:

- Parameters:

| | Calculated | Simulated |
|---|---|---|
| M1 | 110 µ m/0.18 | 110 µ m/0.18 |
| M2 | 110 µ m/0.18 | 110 µ m/0.18 |
| $L_g$ | 31nH | 20nH |
| $L_s$ | 0.14nH | 0.28nH |
| $I_d$ | 9mA | 8.6mA |
| $Z_L$ | 24 Ω | 26 Ω |

- Performance:

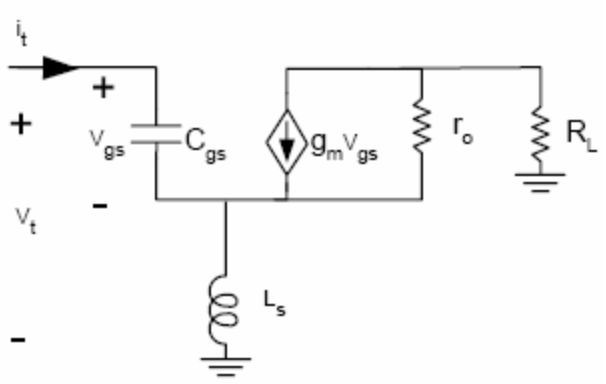
| | Specs | Simulation |
|---|---|---|
| Frequency | 2.4GHz | 2.4GHz |
| S11 | <-10dB | -32dB |
| S21 | >15dB | 15.7dB |
| NF | <2dB | ~0.62dB |
| IIP3 | >-10dBm | -6.85dBm |
| Current | <10mA | 8.6mA |
| Supply | 1.8V | 1.8V |

# Effect of $R_L$ on input match

- We ignored the effect of load impedance on input impedance in previous derivations. Let's revisit it:
- It can be shown that:

$$Z_{in} = \frac{1}{jC_{gs}\omega} + jL_s\omega + \frac{r_o}{r_o + R_L + jL_s\omega}\left[L_s\omega_T + \frac{(L_s\omega)^2}{r_o}\right]$$

$$\approx \frac{1}{jC_{gs}\omega} + jL_s\omega + \frac{r_o}{r_o + R_L}\left[L_s\omega_T\right]$$




- $R_L$ can be large and it can drop the real part of the input impedance when we use resonators at output
- Notice that the output impedance influenced the input impedance even in the absence of $C_{gd}$!

# Differential v.s. Single-ended LNA

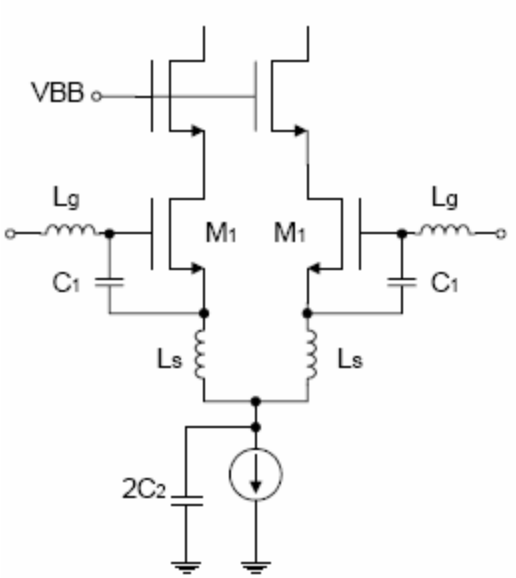
## Differential

- ✓ reject common mode noise and interferer
- ✓ shield the bond wire
- x double area and current
- x need balun at input
- x common-mode stability
- x linearity limited by bias current

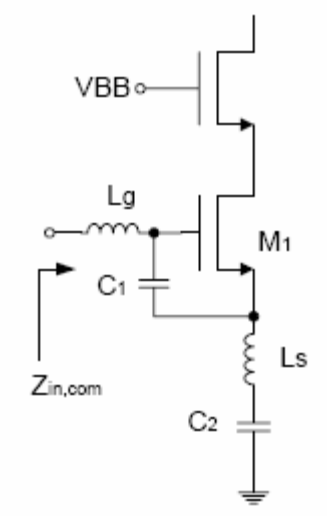
## Single-ended

- ✓ compact layout size
- ✓ less power for same NF and linearity
- x susceptive to bond wire and PCB trace
- x drive single-balance mixer; or use output balun to drive double-balance mixer

# Differential LNA Common-mode Stability Issue




Typical differential LNA




Common-mode half circuit

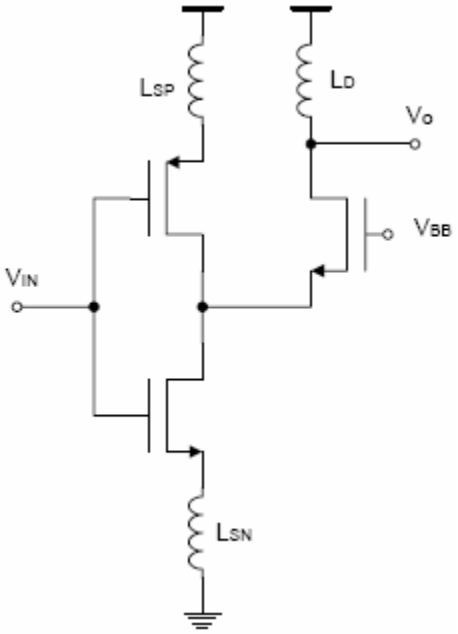
$$Z_{in,com} = j\omega\left(L_g + L_s\right) + \frac{C_1 + C_2}{j\omega C_1 C_2}$$

$$+ \frac{g_m L_s}{C_1} - \frac{g_m}{\omega^2 C_1 C_2}$$

Real part: $R_{in,com} = \frac{g_m}{C_1}\left(L_s - \frac{1}{\omega^2 C_2}\right)$

- For passive termination, the real part of the source impedance will always be positive. IF $R_{in,com}$ happens to be negative and cancel the real part of source impedance, oscillation **MAY occur.**

# Variant of Inductive Degenerated LNA

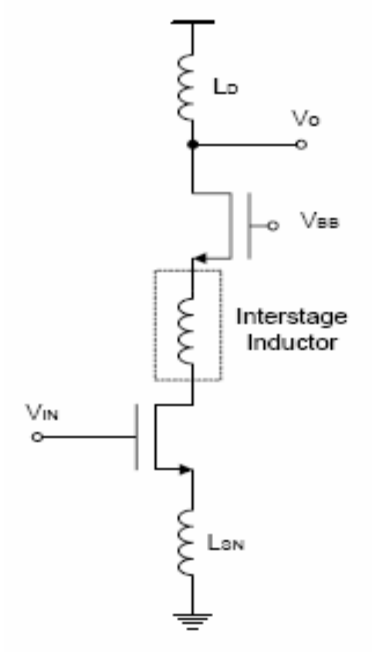



Single-ended version of current reuse LNA (bias not shown)

- nMOS-pMOS shunt input
- Current reuse to save power
- Larger area due to two degeneration on chip inductor
- NF: 2dB, Power gain: 17.5dB, IIP3: -6dBm, Id: 8mA from 2.7V power supply

F. Gatta, E. Sacchi, et al, “A 2-dB Noise Figure 900MHz Differential CMOS LNA,” IJSSC, Vol. 36, No. 10, Oct. 2001 pp. 1444-1452

# Variant of Inductive Degenerated LNA




Single-ended version of current reuse LNA (bias not shown)

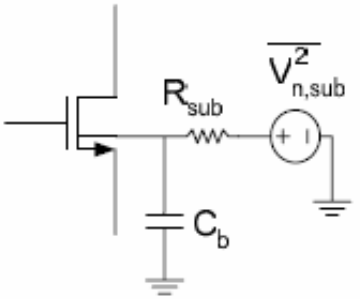
- Inter-stage inductor with parasitic capacitance form impedance match network between input stage and cascoded stage boost gain lower noise figure.
- Input match condition will be affected

Chunyu Xin, and Edgar Sánchez-Sinencio, “A GSM LNA Using Mutual-Coupled Degeneration”, IEEE Microwave and Wireless Components Letters, VOL. 15, NO. 2, Feb 2005

# Comparison of LNA Architectures

| | Resistive Termination | Common Gate | Shunt Feedback | Inductive Degeneration |
|---|---|---|---|---|
| Noise Figure | >6dB | 3~5dB | 2.8~5dB | ~2dB |
| Gain | 10~20dB | 10~20dB | 10~20dB | 15~25dB |
| Sensitivity to Parasitic | Less | Less | Less | Large |
| Input Matching | Easy | Easy | Easy | Complex |
| Linearity | -10~10dBm | -5~5dBm | -5~5dBm | -10~0dBm |
| Power | 1~50mW | ~5mW | >15mW | >10mW |
| Highlight | Effortless input matching | Easy input matching | Broadband input/out matching | Good narrowband Matching, small NF |
| Drawback | Large NF | Large NF | Stability | Large area |

# Substrate Noise

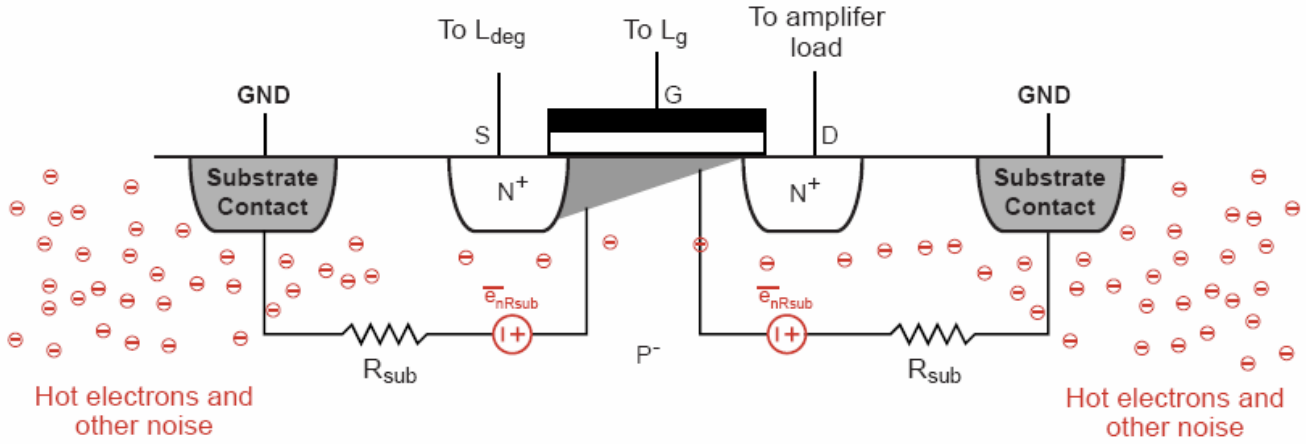



- A MOS device is in fact a 4 terminal device.
  The $4_{th}$ terminal is the substrate.
- The bulk-source potential modulates the drain current with a transconductance of $g_{mb}$ which has the same polarity as $g_m$ (i.e., increasing the bulk potential increases the drain current)
- The substrate has a finite (nonzero) resistance and therefore has thermal noise
- To reduce $R_{sub}$ we should put many substrate contacts close to the device

$$\overline{i^2_{no,sub}} = \frac{4kTR_{sub}}{1+\left(\omega R_{sub} C_b\right)^2}\Delta f \cdot g^2_{mb}$$

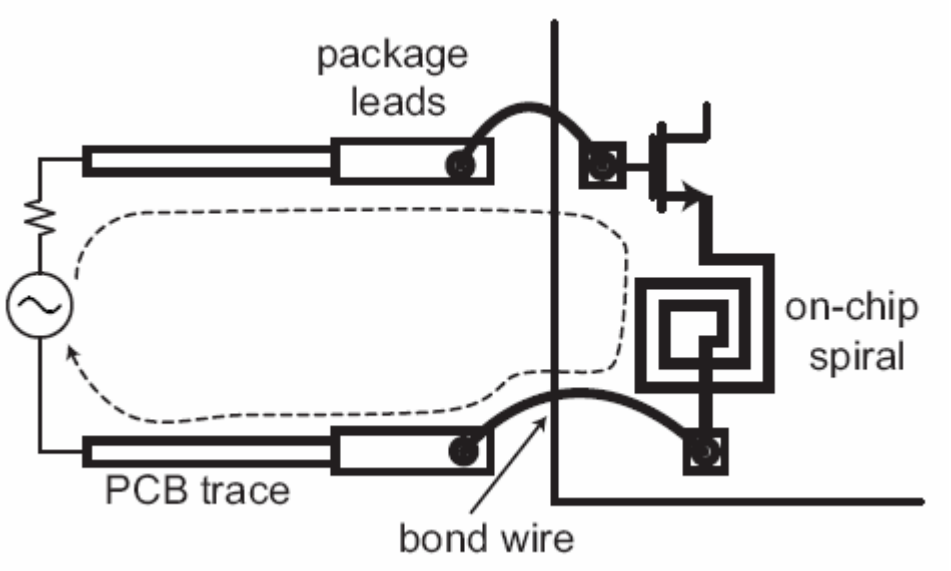
- Substrate noise characterization: John T. Colvin et.al: “Effects of Substrate Resistances on LNA Performance and a Bondpad”, *JSSC* Sep. 1999

# Substrate Noise(cont.)



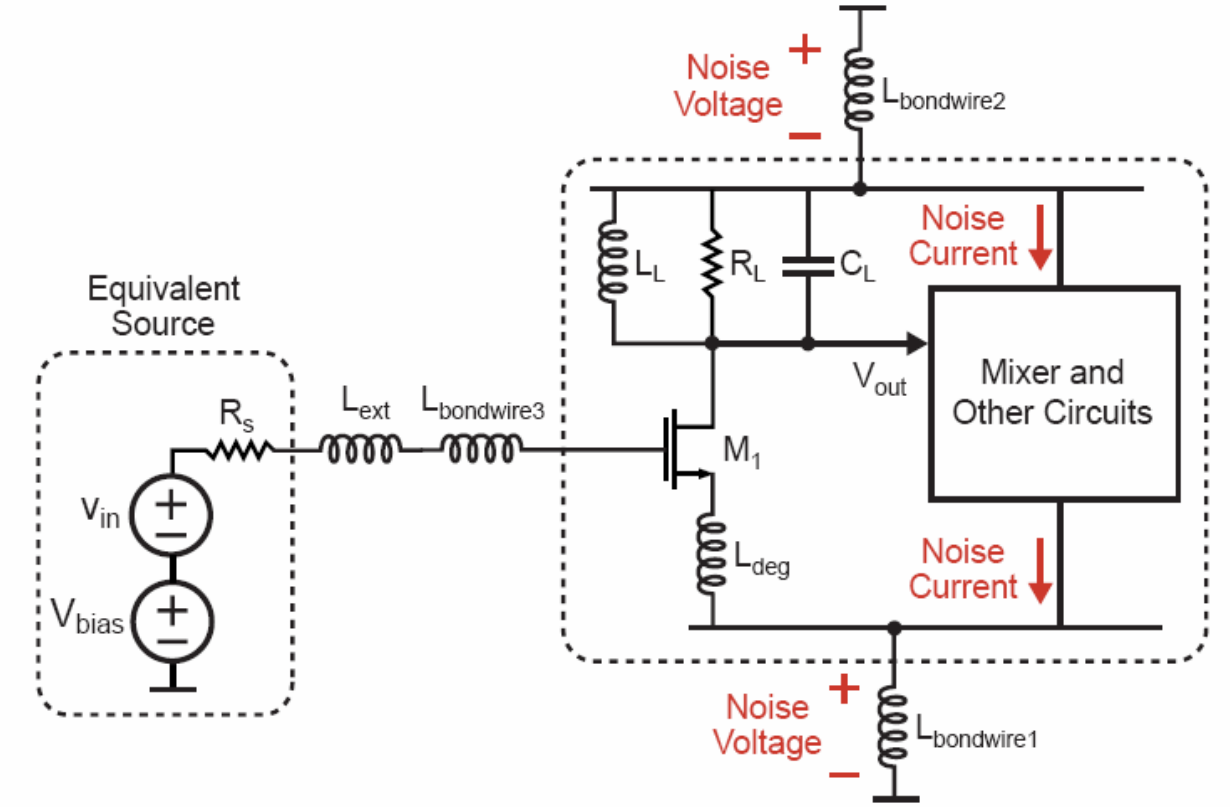

- Solution: Place as many substrate contact as possible!
- Pros:
  - Reduces possibility of latch up issues
  - Lowers $R_{sub}$ and its associated noise(Impacts LNA through backgate effect ($g_{mb}$)
  - Absorbs stray electrons from other circuits that will otherwise inject noise into the LNA
- Cons: takes up a bit extra area

# Package Parasitics




- As interface to the external world, the LNA must transit from the silicon chip to the package and board environment, which involves bondwires, package leads, and PCB trace.

# Package Parasitics(cont.)




- Two effects from bondwire and package inductance:
  - Value of degeneration inductor is altered
  - Noise from other circuits couples into LNA

# Package Parasitics(cont.)

- Some or all of the degeneration inductor $L_s$ can be absorbed into the *bondwire* inductance
- These parasitics must be absorbed into the LNA design.
- This requires a good model for the package and bondwires. It should be noted that the inductance of the input loop depends on the arrangement of the bondwires, and hence die size and pad locations.
- Many designs also require ESD protection, which manifests as increased capacitance on the pads.
- For more details, please read:

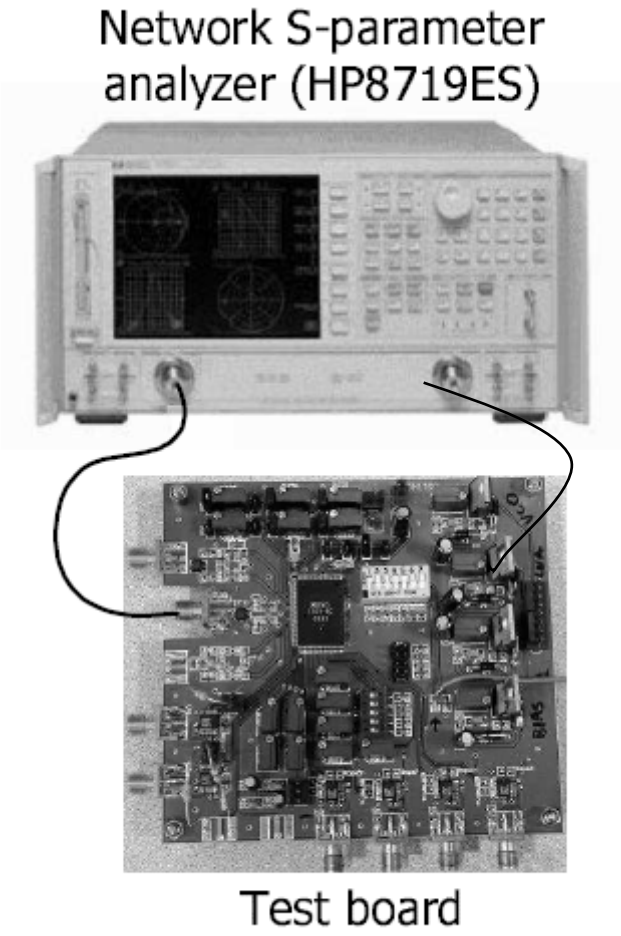
1. B. Razavi, “Design of Analog CMOS Integrated Circuits *(chapter 18)* ” McGraw-Hill, New York 2001.

2. Andrzej Szymañski et.al: “Effects of package and process variation on 2.4 GHz analog integrated circuits”, *Microelectronics and Reliability*, Jan. 2006

# Cadence Simulation for LNA

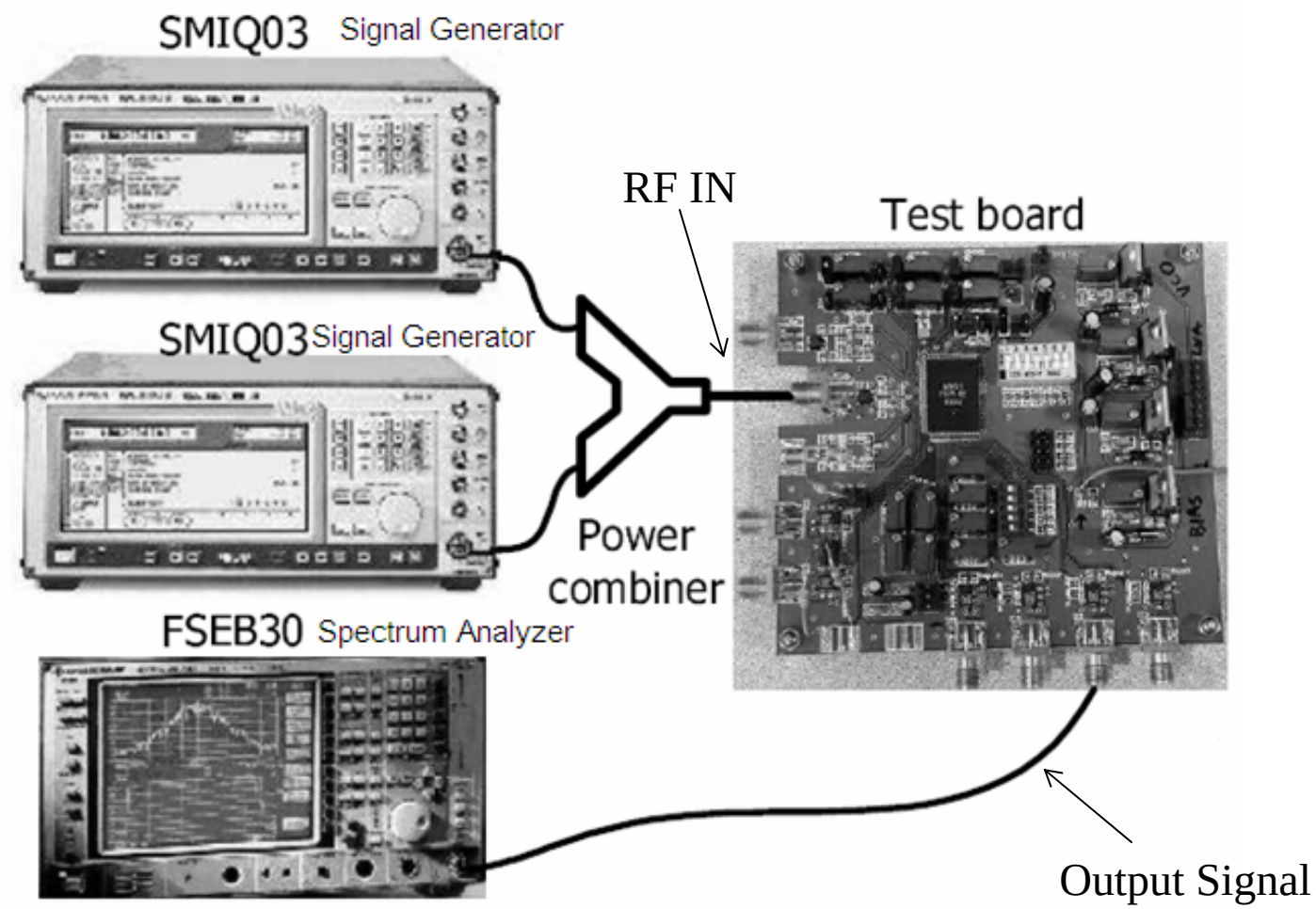
- Characterization of the major Figure of merit of an LNA in Cadence
- S-parameter simulation
  - input and output match
  - noise figure
  - gain
- Periodic steady state (pss) simulation/SPSS
  - IIP2/IIP3, 1dB point
- Please refer to Lab 3 manual

# LNA Testing: S parameter

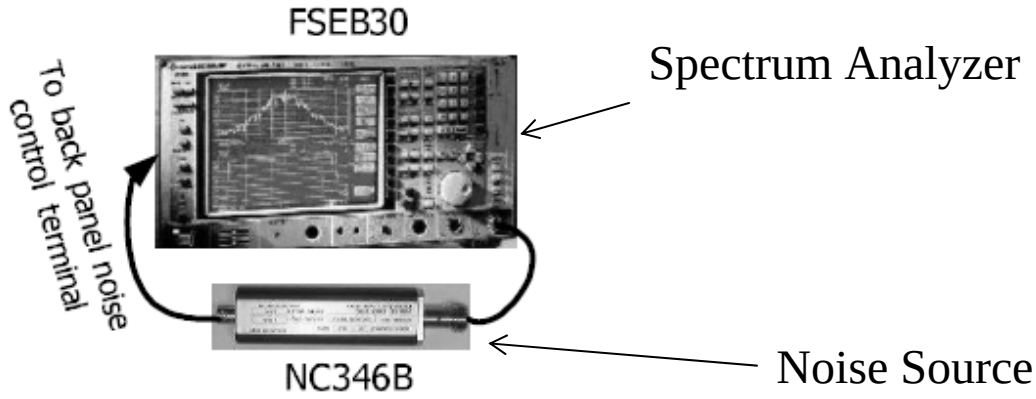



- Before doing the measurement:
  - Calibrate two lines.
  - Adjust the power level

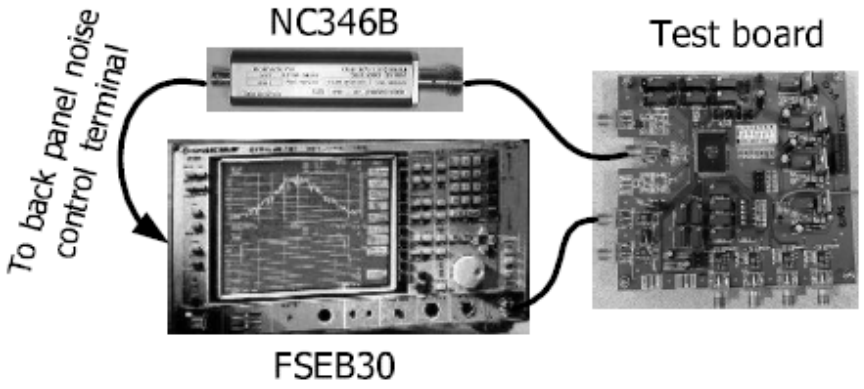
# LNA Testing: Linearity(IIP3/IIP2)



# LNA Testing: Noise Figure




Step 1: Instrument calibration




Step 2: Measurement