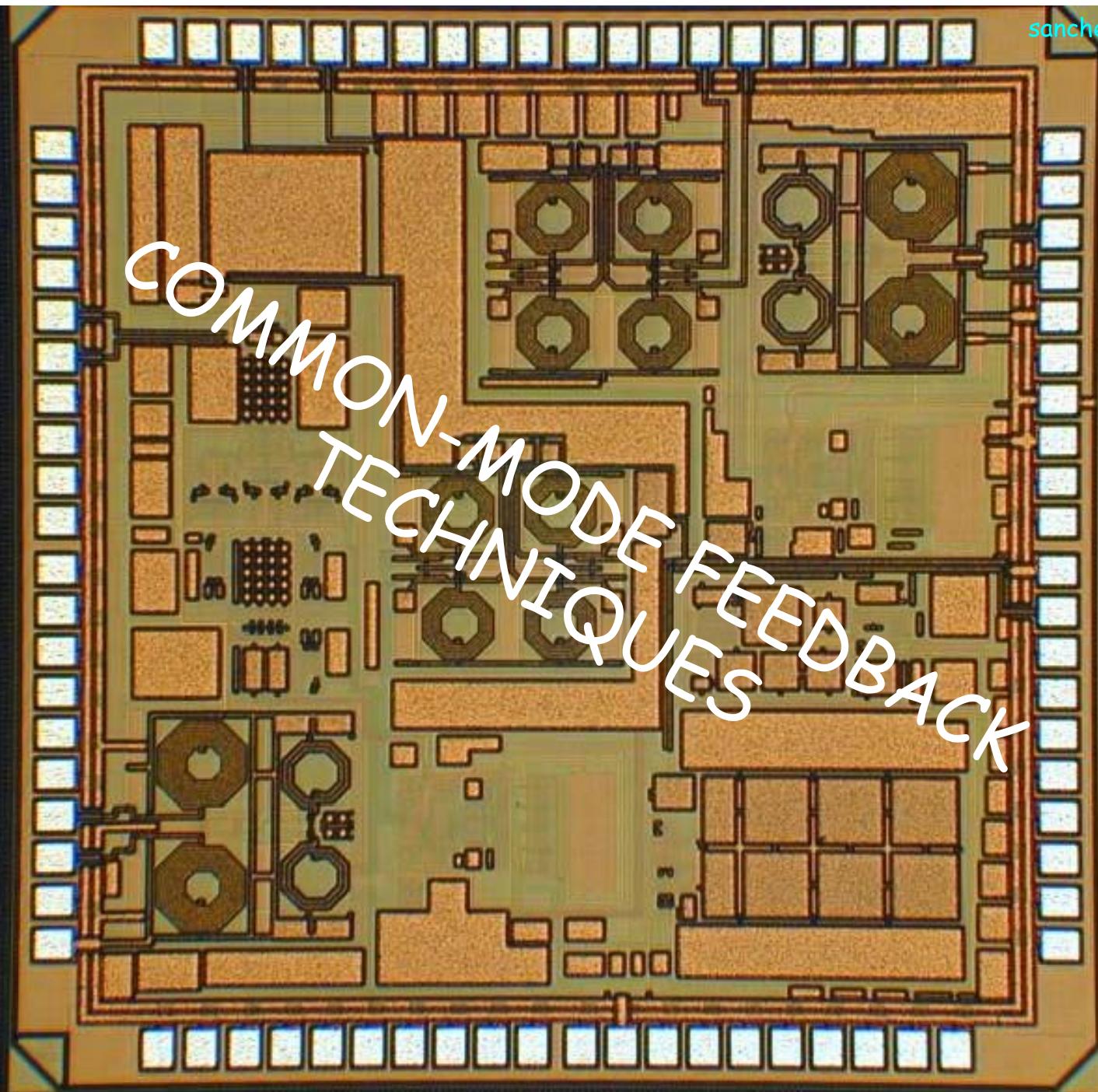


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## Why do we need to use Common-Mode Feedback Circuits ?

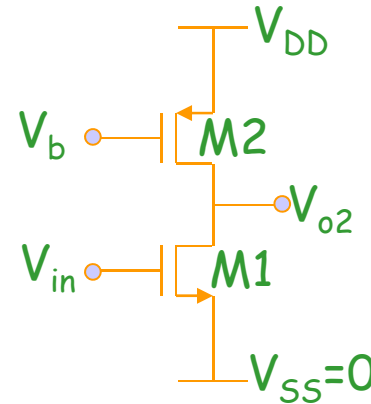
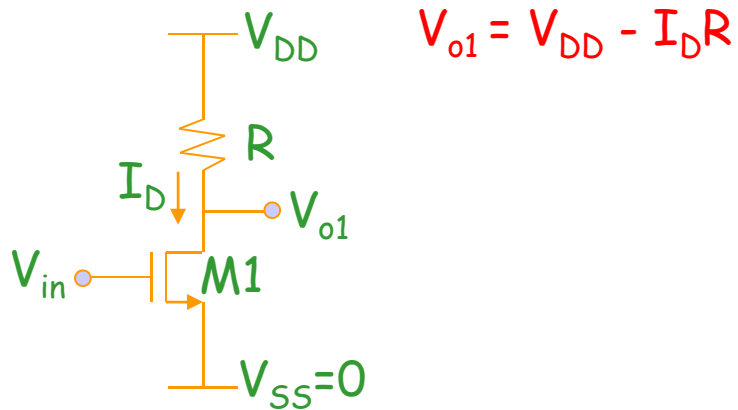
- In the past, circuits have mainly one input and one output and both referred to ground.
- Low voltage power supply make single ended circuits very difficult to perform optimally. An alternative to single-ended circuits is to use fully differential circuits.
- To double the output swing a fully differential circuit are used.
- The output terminals of fully differential circuits are equal and opposite polarity.
- Additional properties of fully differential circuits are: improved output swing, linearity and common-mode rejection ratio.
- How are the differential outputs referred to ?
- How are the common-mode signals eliminated in a Fully differential circuit ?

- **A CMFB circuit, in a fully differential circuit, is generally needed for two reasons:**

- (1) To control the common mode voltage at different nodes that cannot be stabilized by the negative differential feedback. This is usually chosen as a reference voltage yielding maximum differential voltage gain and/or maximum output voltage swing

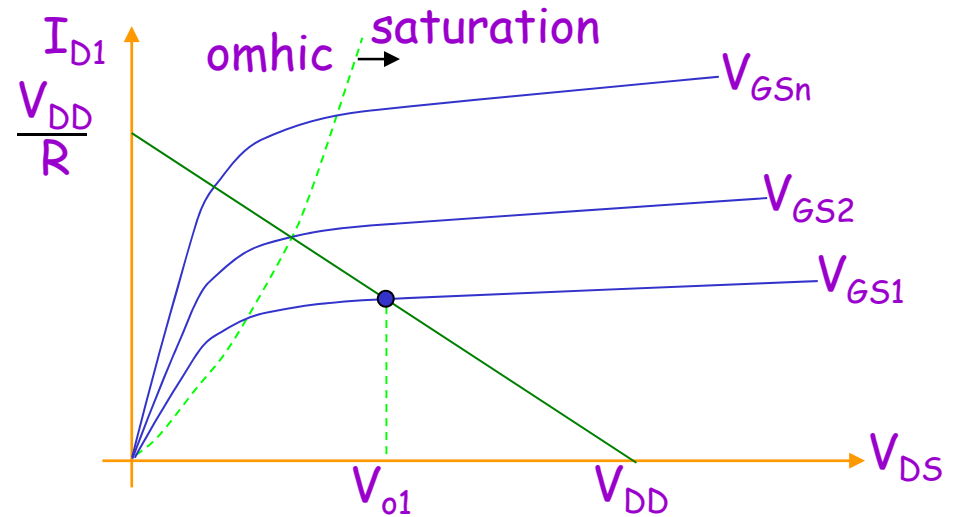
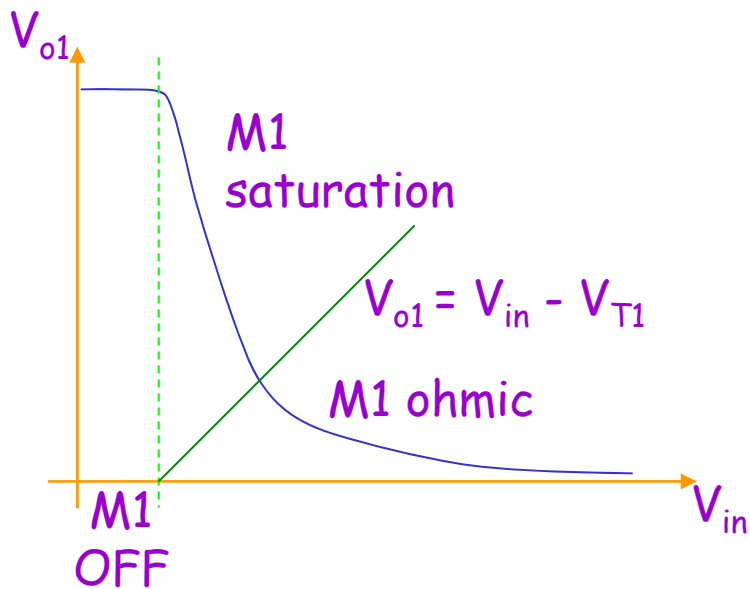
- (2) To suppress the common mode components, that tends to saturate different stages, through applying common mode negative feedback.

## Background and motivation .

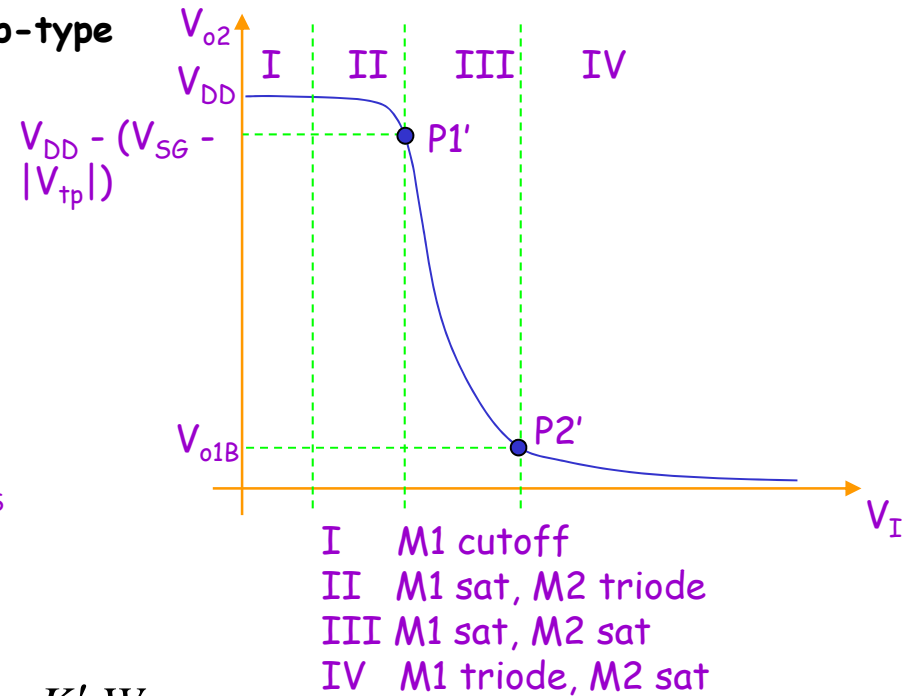
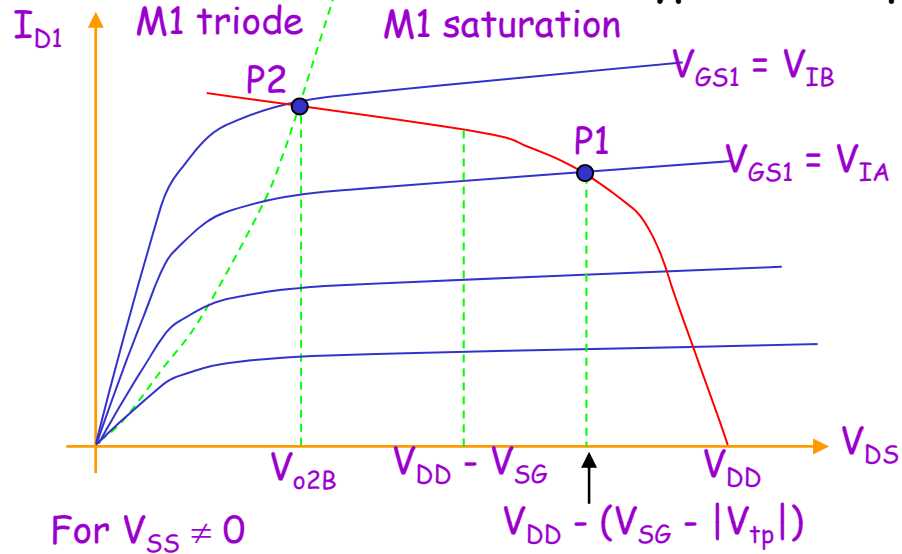


Can we determine the DC operating points for  $V_{o1}$  and  $V_{o2}$ ?

Let us first consider the case of one transistor and one resistor.



Second case: Two transistors one n-type and one p-type



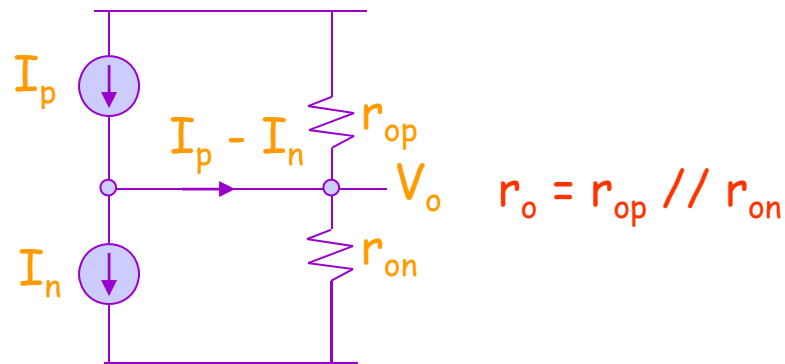
$$\frac{K'_N W_1}{2L_1} (V_{in} - V_{SS} - V_{T_1})^2 (1 + \lambda_N (V_{O1} - V_{SS})) = \frac{K'_P W_2}{2L_2} (V_{DD} - V_b - V_{T_2})^2 [1 + \lambda_P (V_{DD} - V_{O1})]$$

KCL

$$I_{D_1} = I_{D_2}$$

- Small variations due to process (or to the input) could force the operations in III to move to regions II or IV.
- $V_{O2}$  is difficult to fix and the regions of operation of M1 and M2 are very sensitive to process variations and input variations.

What is the effect of mismatch between the p-type current source and the n-type current source?



$V_o$  due to the transistor mismatches, in  $I_{D1}$  and  $I_{D2}$ , is given by

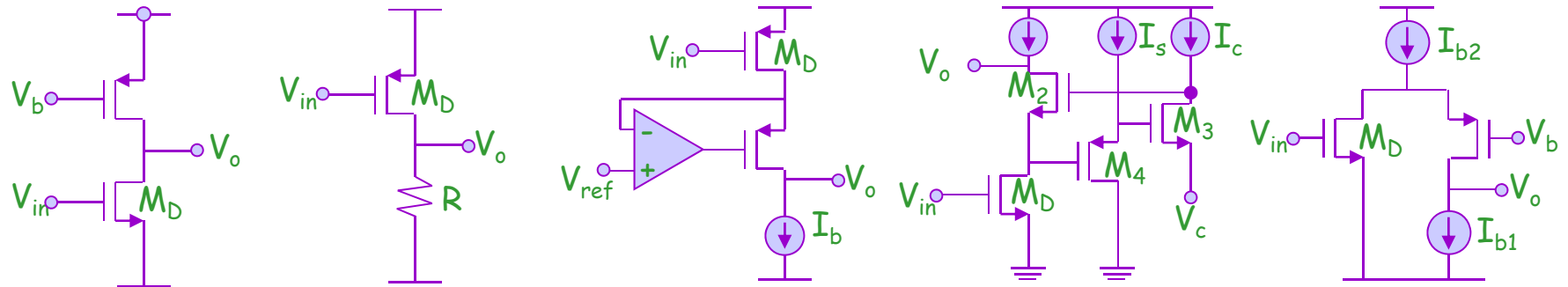
$$V_o = (I_p - I_n) r_o = \Delta I R_o$$

For instance for  $\Delta I = 15 \mu\text{A}$  and  $r_o = 266 \text{ k}\Omega$ , this results in  $V_o = 4 \text{ V}$ . Since this error can not be produced, M2 is forced into triode region.

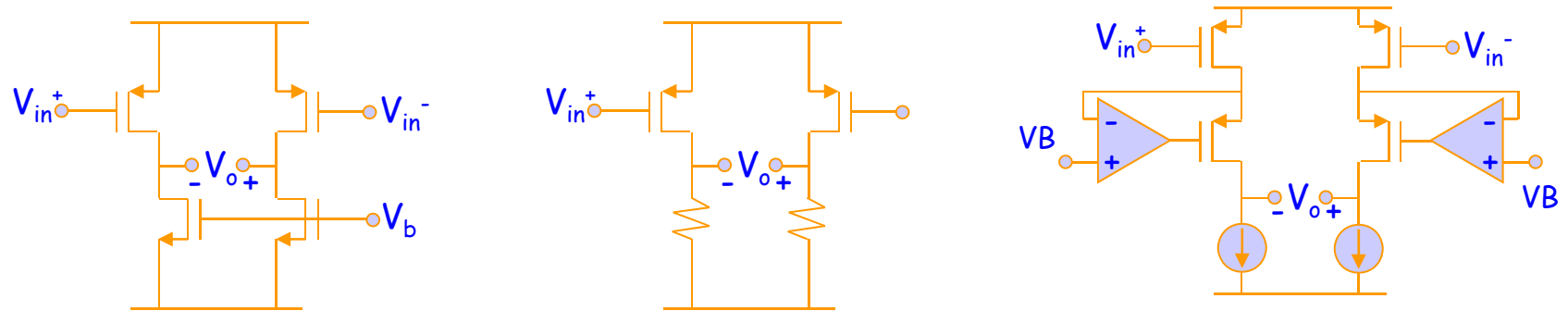
We will study techniques to force  $\Delta I$  close to zero.

# Examples of voltage amplifiers types

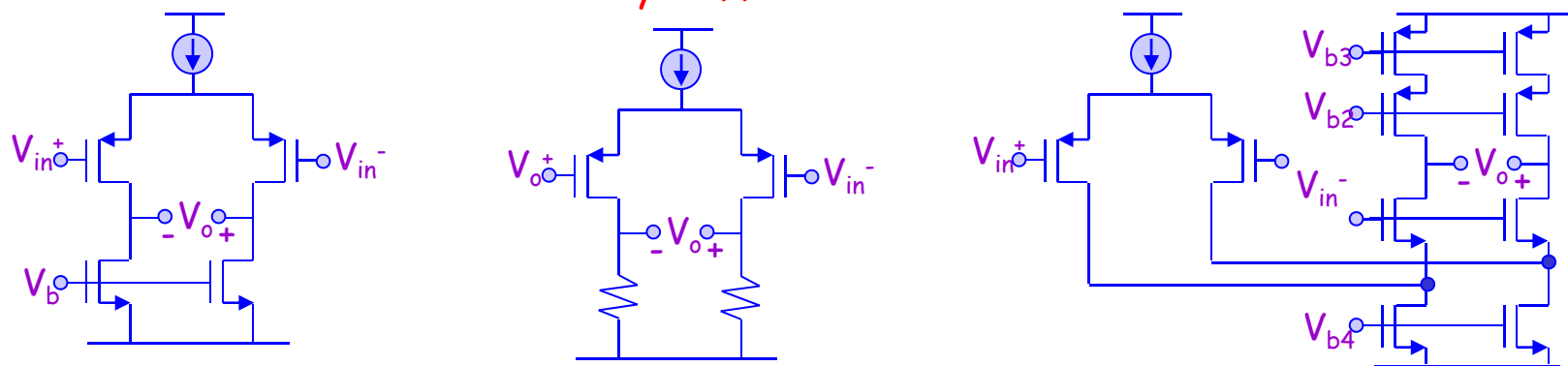
## • Single-Input Single-Output Amplifiers



## • Pseudo Differential Amplifiers

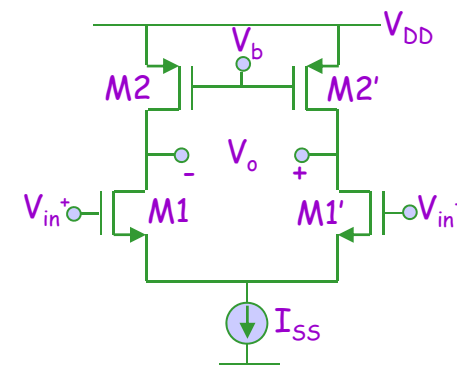
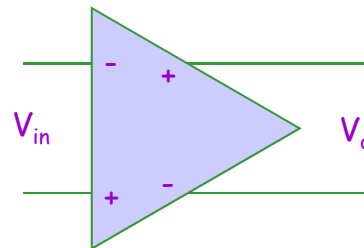
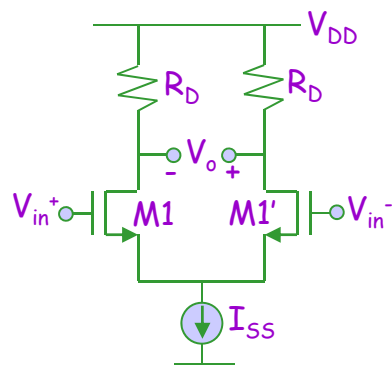


## Fully-Differential



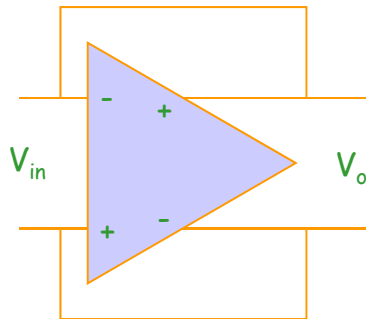
## How is the common source amplifier related to common-mode feedback?

- Fully differential (FD) circuits need common-mode feedback to operate properly and to fix the DC of the output nodes.
- FD amplifiers consist of common source circuits embedded in differential pairs. Thus, the properties of the single-input common source circuits are part of the FD amplifiers.





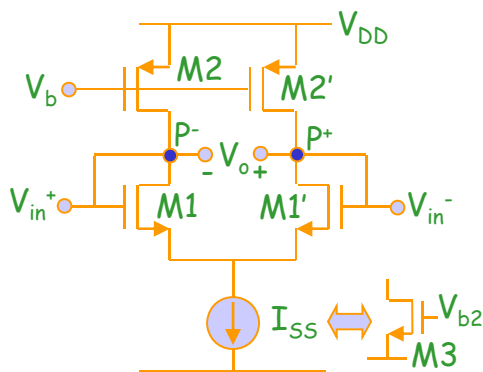
- In a number of applications the inputs and output are short circuited, i.e.,



- From previous slide, for the load resistor  $R_D$ , the input and output common-mode levels is well defined

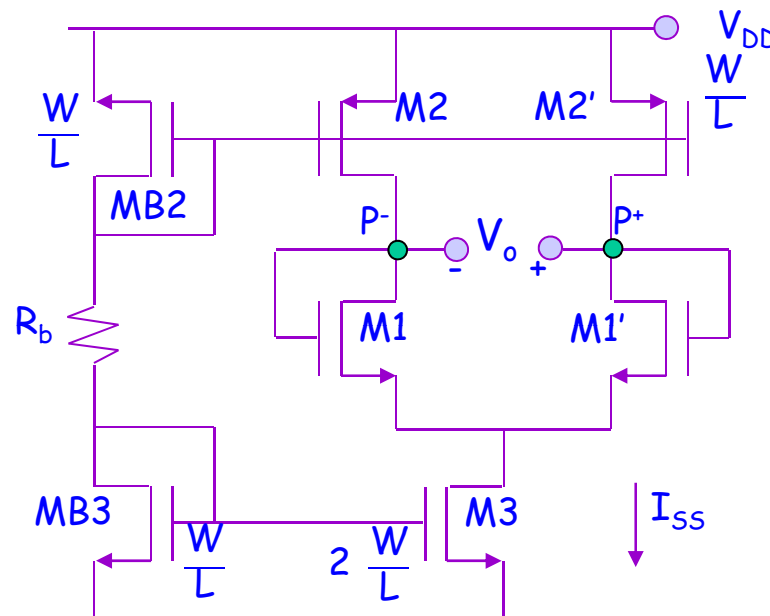
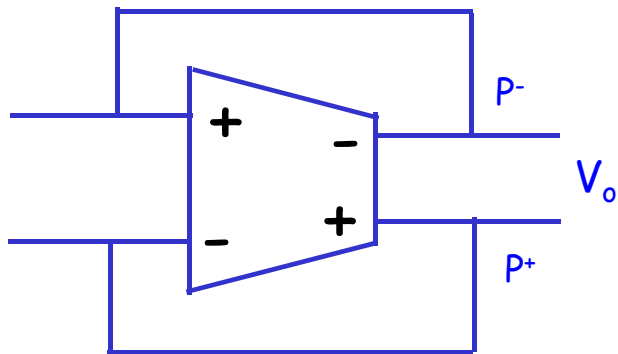
$$V_{o,cm} = V_{DD} - I_{SS}R_D / 2$$

- For the case of a current source load implemented by PMOS transistors  $M2$  and  $M2'$  the common-mode level is not well defined.



- CM Levels depend on how close  $I_{DM2}$  and  $I_{DM2'}$  are to  $I_{SS}/2$ .
- In practice  $I_{SS}$  is implemented by a NMOS current source, and similarly for  $M2$  and  $M2'$  by means of a PMOS current source.
- These two current sources are not ideal creating a finite error between  $I_{D, M2, M2'}$  and  $I_{SS}/2$ .

## Effects of drain current mismatches on the DC output voltage: An example of a FD "resistor equivalent":



Suppose that the drain currents of  $M2$  and  $M2'$  (in the saturation region) are slightly smaller than  $I_{SS}/2$ , to satisfy KVL at nodes  $P^-$  and  $P^+$ , then  $V_{p^-}$  and  $V_{p^+}$  must drop forcing  $M3$  to enter in triode region, producing only  $2I_{DM2, DM2'}$ .

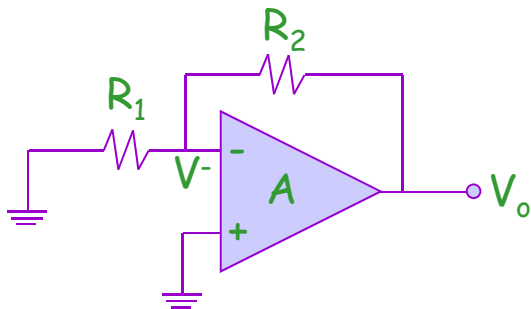
Also if drain currents of  $M2$  and  $M2'$  are slightly greater than  $I_{SS}/2$  then both  $M2$  and  $M2'$  must enter into the triode region, so that their drain currents remain  $I_{SS}/2$ .

## Closed loop negative feedback effects on the DC output voltage

- The high impedance nodes are difficult to fix their DC operating points. This is the case of Single-Ended Differential Amplifiers (Op Amps and OTAs).
- Op Amps in open loop yield

$$V_o = \begin{cases} V_{DD} \\ \text{or} \\ -V_{SS} \end{cases}$$

Fortunately, Linear Applications of single ended circuits are based on negative feedback, and this feedback circuitry also fixes the DC operating point, i.e.,



Closed-Loop Negative Feedback

$$V_o = A (0 - V^-)$$

$$\text{but } V^- = \frac{V_o R_1}{R_1 + R_2}$$

and

$V_{o,dc} = 0$   
for symmetric power supplies.

## I/O characteristics of a FD Amplifier.

$$V_{o,dm} = V_o^+ - V_o^- = A (V^+ - V^-)$$

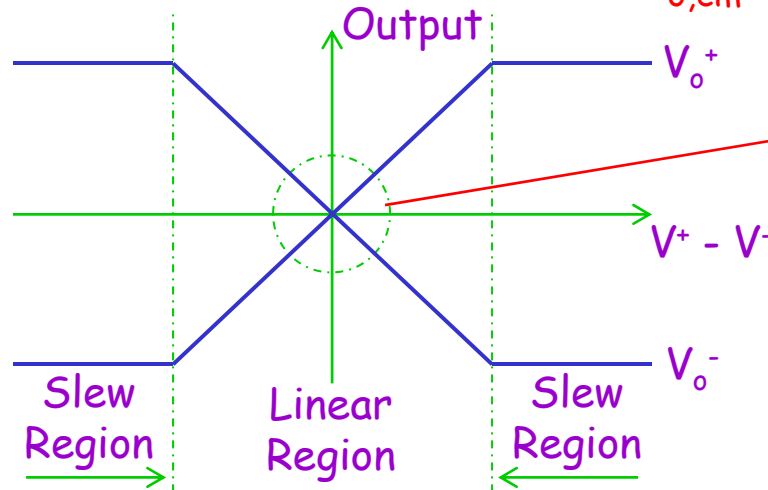
$$V_{o,dm} = A V_{o,dm} \frac{R_1}{R_1 + R_2}$$

Therefore  $V_{o,dm} = 0$  if  $V^+ = V^-$  (well defined)

But

$$V_{o,cm} = 1/2 (V_o^+ + V_o^-) = ? \text{ (undefined)}$$

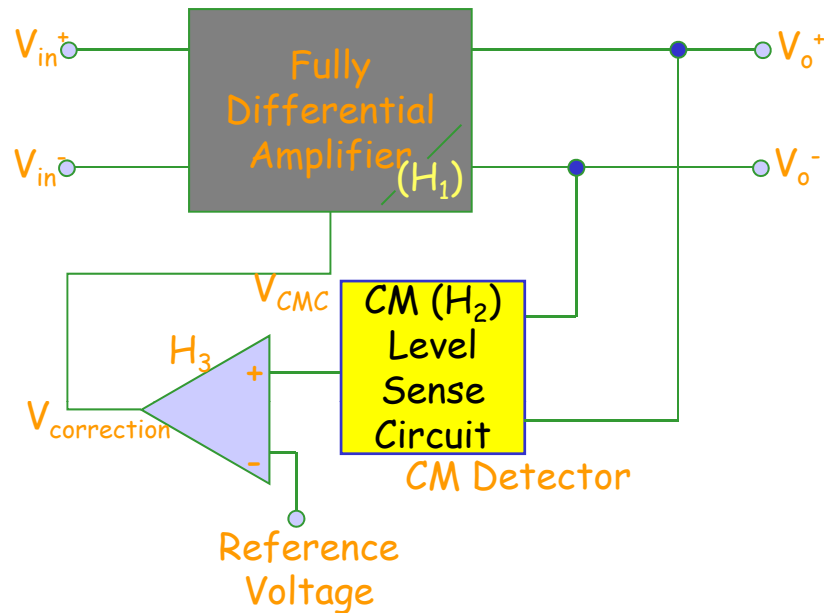
Where should the value of  $V_{o,cm}$  be set? Determined?



This is the region where  $V_{o,cm}$  must be fixed. Yielding maximum output voltage swing and (maximum) differential voltage gain.

I/O characteristics of a FD Amplifier.

$V_{o,cm}$  is usually fixed by an additional negative (common-mode) feedback circuit such that the differential voltage gain is maximized.



### Conceptual Architecture of Common-Mode Feedback

Stability requires to have negative feedback:

$$\text{PHASE } (H_1 H_2 H_3) < 135^\circ \text{ FOR } \omega < \omega_u$$

### • Basic Operations

— Sensing the output CM level, i.e.,

$$\frac{V_o^+ + V_o^-}{2} = V_{o,cm}$$

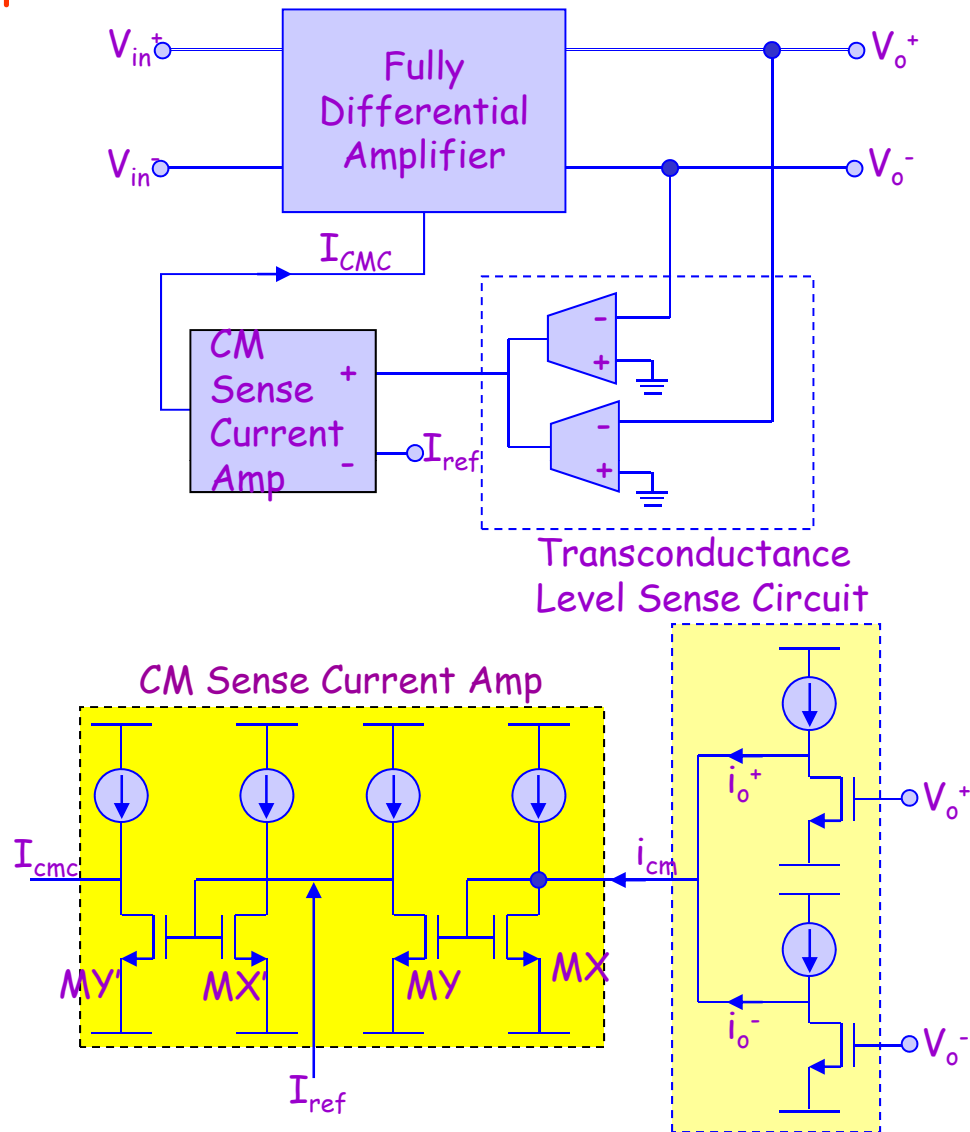
— Comparison with a voltage reference i.e.,

$$V_{o,cm} - V_{ref}$$

— Injecting the error correcting level to the amplifier bias circuitry.

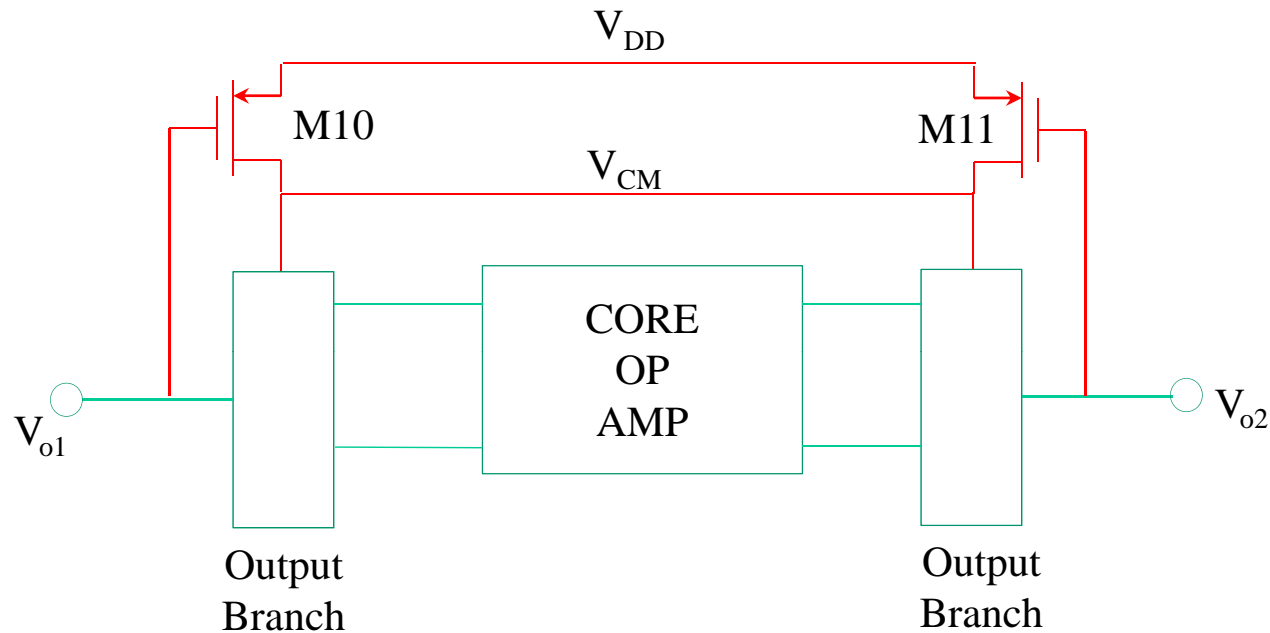
— Avoid injection of CM signals to nodes of the amplifier which do not correct the  $V_{o,cm}$ .

If the output signals are current signals, the CMF architecture could be represented as follows:



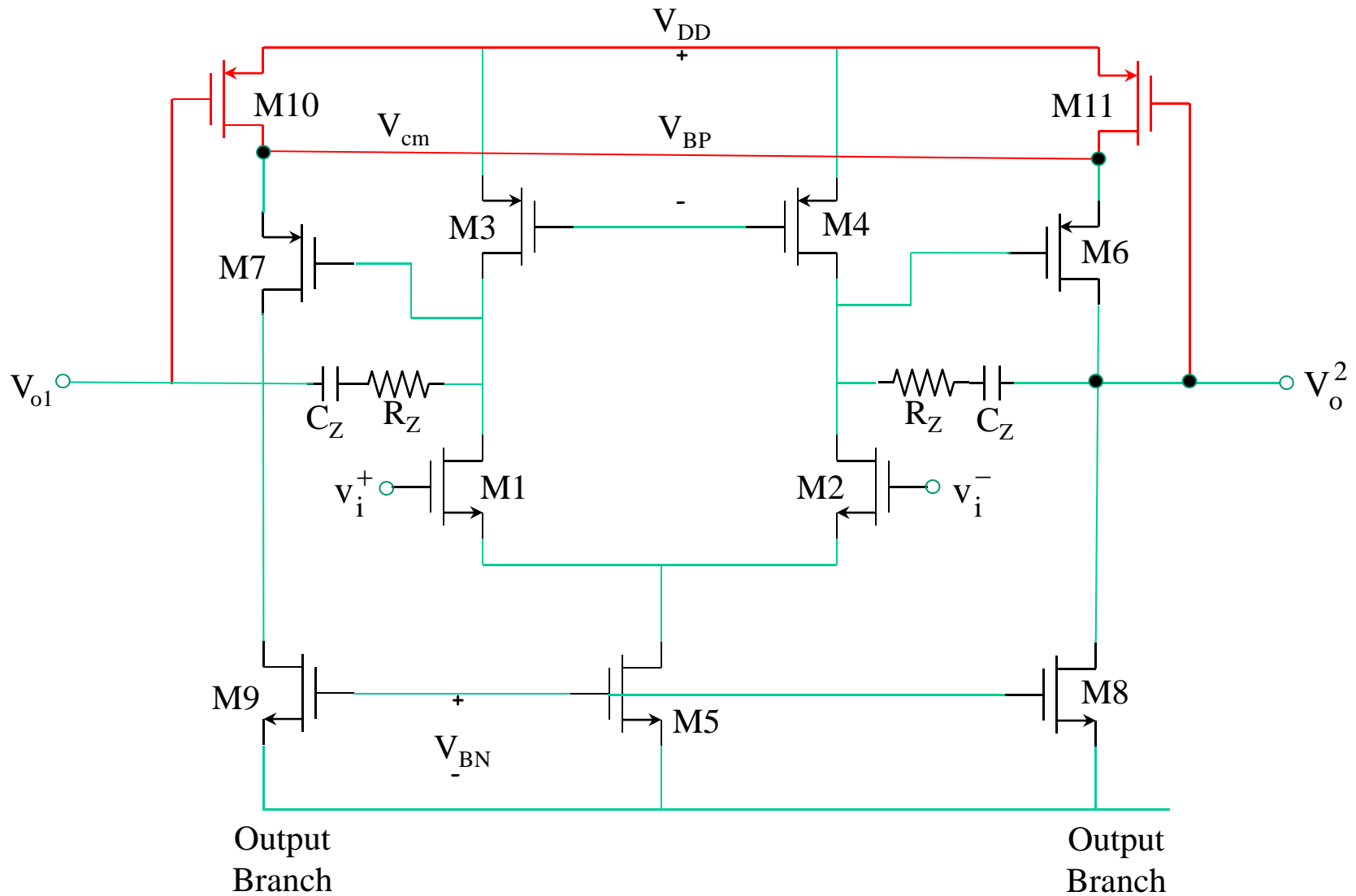
A conceptual current mode implementation of Level Sense Circuit, CM Sense Current Amplifier (Comparator)

## A Simple CM Feedback Without Reference



- Simple approach
- Core Op Amp can be a two-stage, folded cascode or other
- Needs higher power supply
- Sacrifices output voltage swing.

## EXAMPLE OF LOCAL CM FEEDBACK WITHOUT REFERENCE TWO-STAGE AMPLIFIER

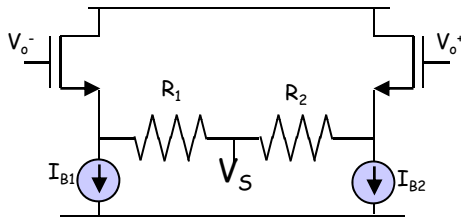




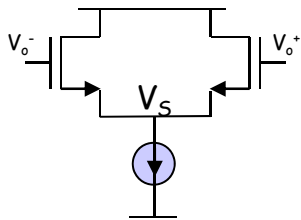
# CM signal detectors : two conventional cases

$$V_S = \alpha_1 v_{o,cm} + \alpha_2 v_{o,dm} + \alpha_3 v_{o,dm}^2$$

## CM Detector 2



## CM Detector 3



### Performance

$$\alpha_1 = 1$$

$$\alpha_2 = \frac{\Delta R}{4R} + \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\frac{\Delta R}{2R} + \frac{\Delta I_B}{4I_B} + \frac{\Delta\beta}{4\beta}}{2R + \sqrt{\frac{2}{\beta I_B}}}$$

$$+ \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\Delta V_T + \frac{\Delta I_B}{2I_B} \sqrt{\frac{2I_B}{\beta}}}{I_B \left( 2R + \sqrt{\frac{2}{\beta I_B}} \right)^2}$$

$$\alpha_3 = \frac{1}{2I_B} \cdot \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{1}{\left( 2R + \sqrt{\frac{2}{\beta I_B}} \right)^2}$$

$$\alpha_1 = 1$$

$$\alpha_2 = \frac{\Delta\beta}{4\beta} + \frac{\Delta V_T}{4} \cdot \sqrt{\frac{\beta}{I_B}}$$

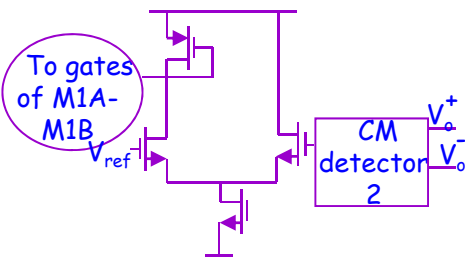
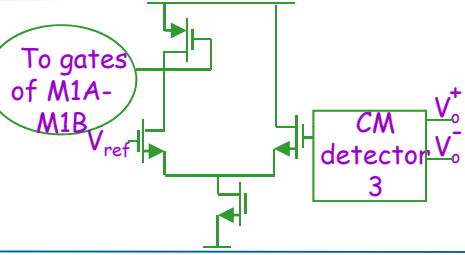
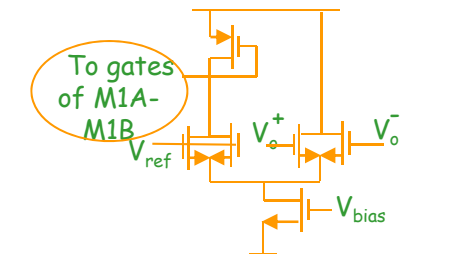
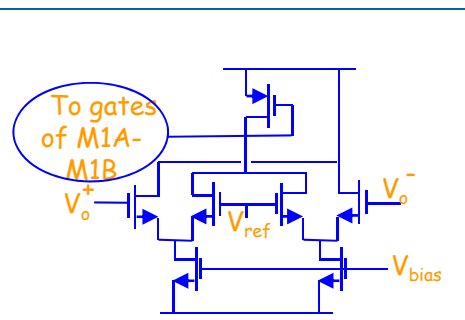
$$\alpha_3 = \frac{1}{8} \sqrt{\frac{\beta}{I_B}}$$

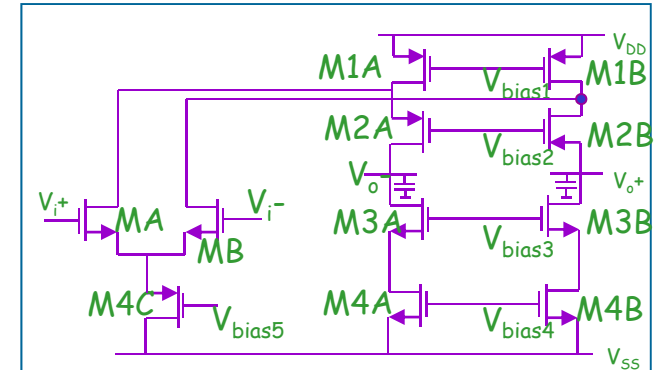
### Observations

- High DC offset due to source followers
- Other buffers can be used to reduce the DC offset
- Mismatching between the passive resistors is the dominant error in  $\alpha_2$

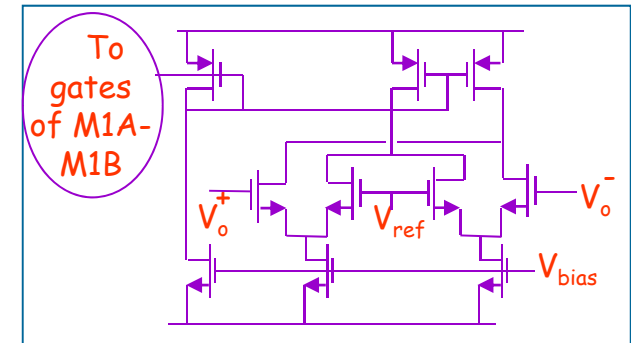
- High DC offset
- Highly non-linear CM signal detector

# Amplifier performance with CM control by current steering.

| STRUCTURE   | $A_{DC}^*$  | $\frac{A_{CM}}{A_{DM}} = \frac{GBW_{CM}}{GBW_{DM}}$ | THD<br>$\pm 1V_{p-p}$ @ 100KHz |
|---|---|---|--------------------------------|
|  <p>To gates of M1A-M1B<br/><math>V_{ref}</math></p> <p>CM detector 2<br/><math>V_o^+</math><br/><math>V_o^-</math></p>          | <p>mean=8.2 dB<br/><math>\sigma=11.1</math> dB<br/>WC=21 dB</p>   | 1.1   | 0.05 %                         |
|  <p>To gates of M1A-M1B<br/><math>V_{ref}</math></p> <p>CM detector 3<br/><math>V_o^+</math><br/><math>V_o^-</math></p>          | <p>mean=20 dB<br/><math>\sigma=9.5</math> dB<br/>WC=33.7 dB</p>   | 1.2   | 0.22 %                         |
|  <p>To gates of M1A-M1B<br/><math>V_{ref}</math></p> <p><math>V_o^+</math><br/><math>V_o^-</math><br/><math>V_{bias}</math></p> | <p>mean=22.1 dB<br/><math>\sigma=9.6</math> dB<br/>WC=36.2 dB</p> | 1.3   | 0.06 %                         |
|  <p>To gates of M1A-M1B<br/><math>V_o^+</math><br/><math>V_{ref}</math><br/><math>V_o^-</math><br/><math>V_{bias}</math></p>   | <p>mean=9.4 dB<br/><math>\sigma=8.5</math> dB<br/>WC=23 dB</p>    | 1.2   | 0.015 %                        |

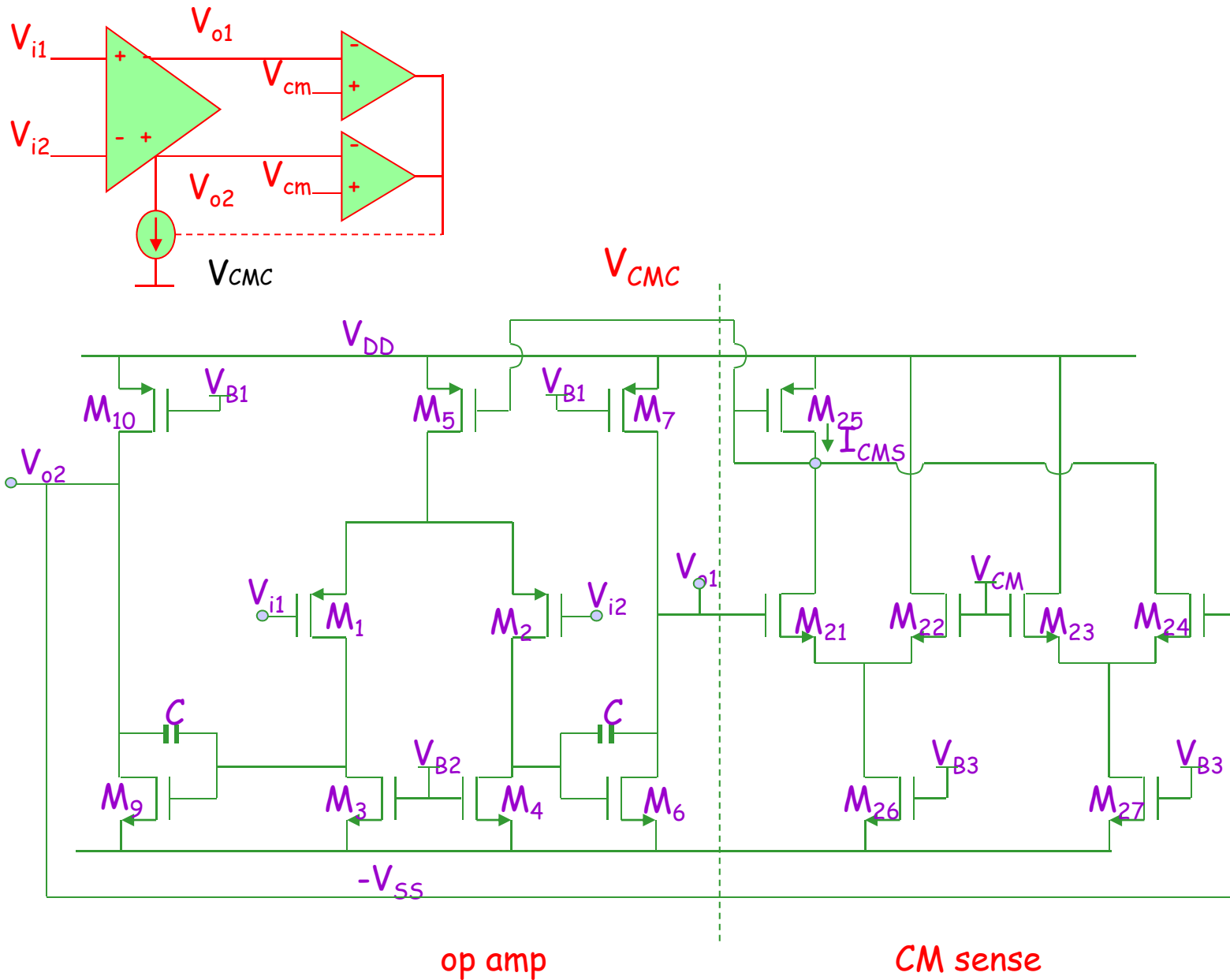


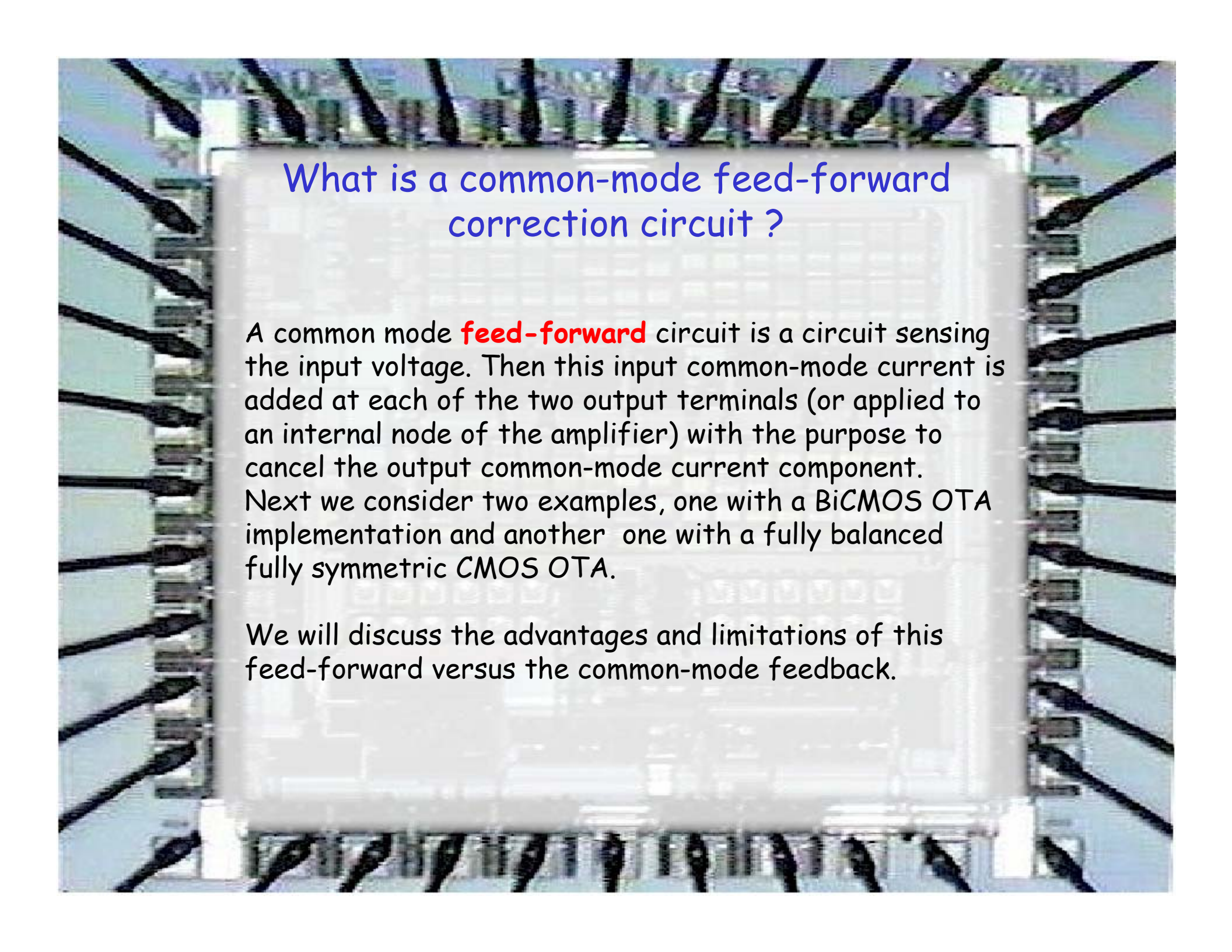
A folded amplifier as an example of a FD amplifier



Low-distortion CM steering loop.

# Example of a compensated Op Amp and a CM sense circuit



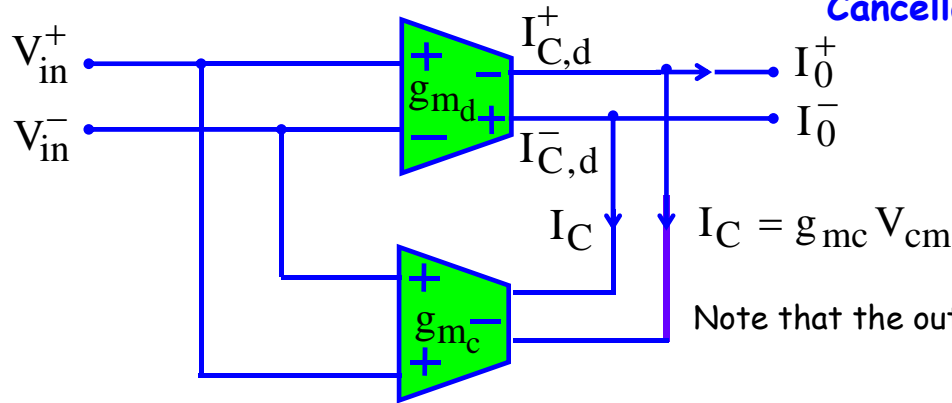
A photograph of a microchip with a grid of pins, overlaid with a semi-transparent white box containing text. The text is centered and discusses common-mode feed-forward correction circuits.

## What is a common-mode feed-forward correction circuit ?

A common mode **feed-forward** circuit is a circuit sensing the input voltage. Then this input common-mode current is added at each of the two output terminals (or applied to an internal node of the amplifier) with the purpose to cancel the output common-mode current component. Next we consider two examples, one with a BiCMOS OTA implementation and another one with a fully balanced fully symmetric CMOS OTA.

We will discuss the advantages and limitations of this feed-forward versus the common-mode feedback.

**Cancellation of the output common mode current signal**



$$g_{md} = g_{mc}$$

Note that the output of  $g_{mc}$  has two identical current copies

(a)

$$V_{in}^+ = V_{cm} + V_{in}/2$$

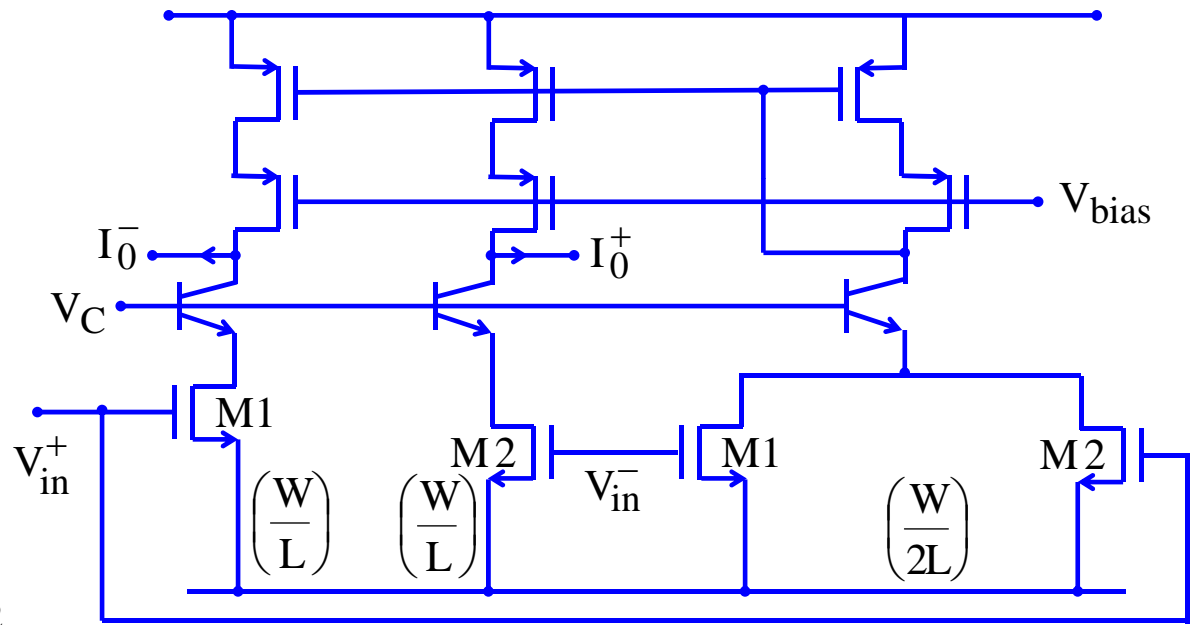
$$V_{in}^- = V_{cm} - V_{in}/2$$

$$I_{C,d}^+ = g_{md} (V_{cm} + V_{in}/2)$$

$$I_{C,d}^- = g_{md} (V_{cm} - V_{in}/2)$$

$$I_0^+ = I_{C,d}^+ - I_C = g_{md} V_{in}/2$$

$$I_0^- = I_{C,d}^- - I_C = -g_{md} V_{in}/2$$

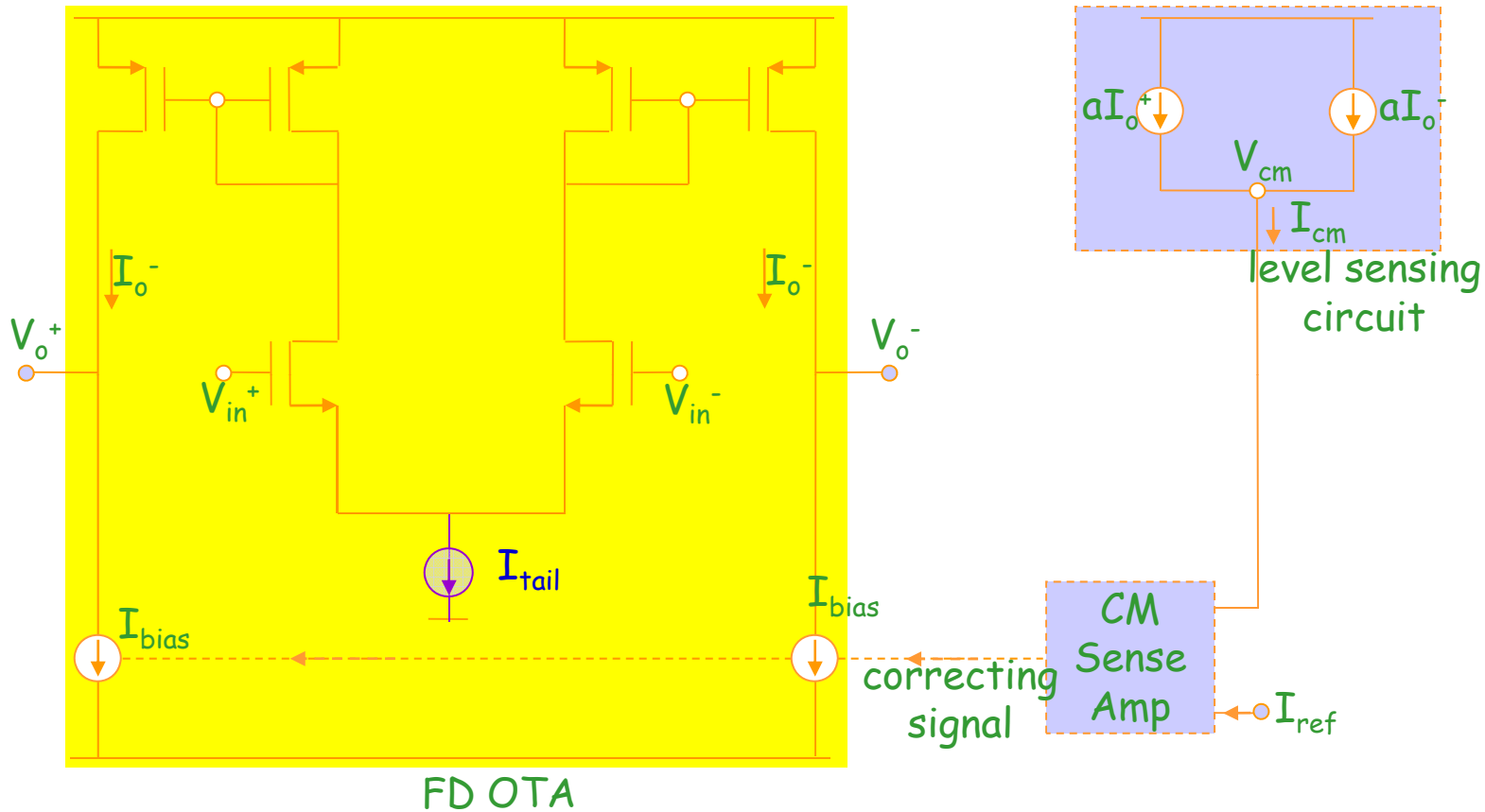


(b)

**Pseudodifferential BiCMOS transconductor with feed-forward common-mode cancellation. (a) Conceptual idea. (b) BiCMOS implementation.**

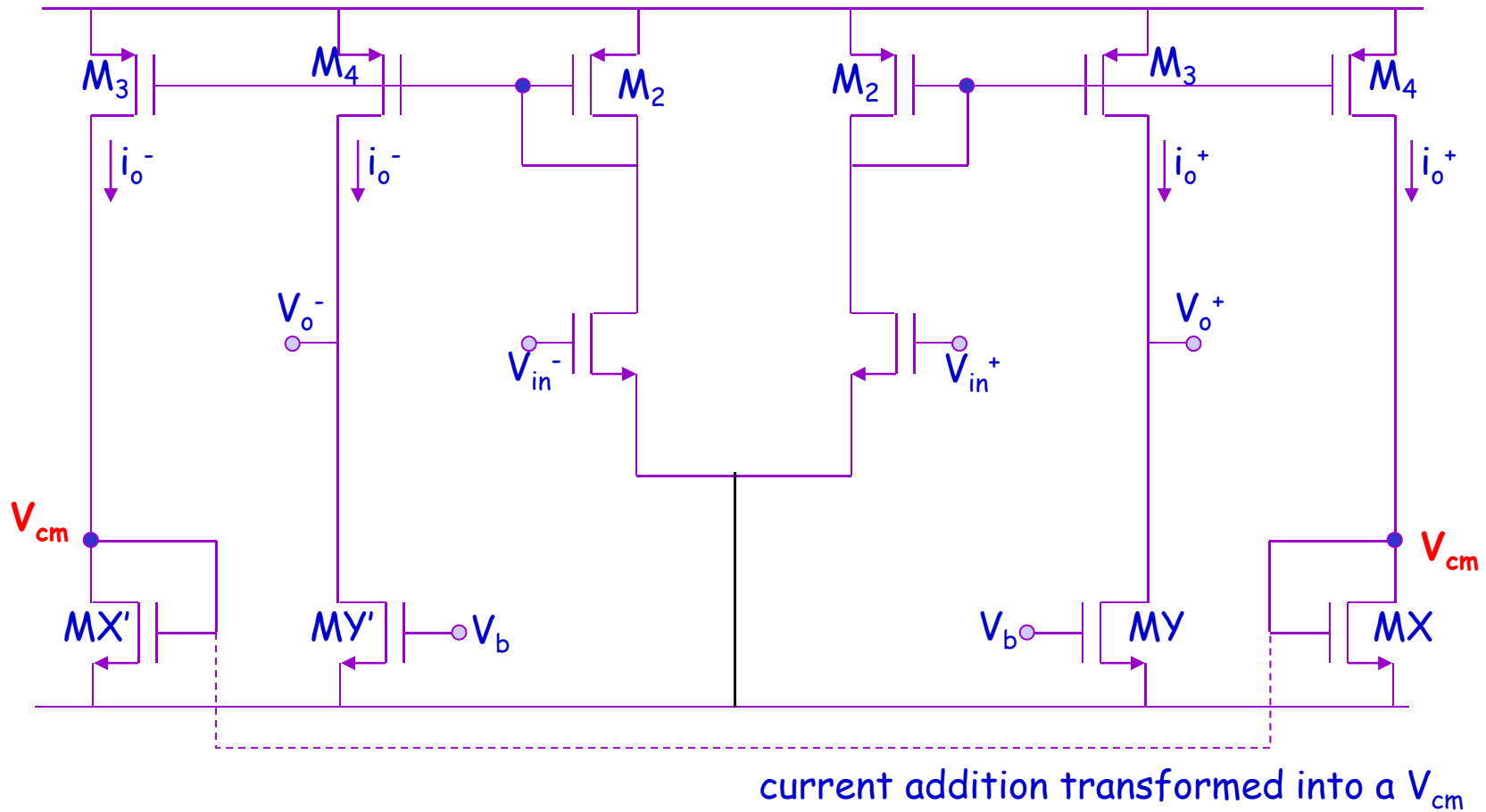
[\*] F. Rezzi, A. Baschiroto, and R. Castello, "A 3V 12-55 MHz BiCMOS Pseudo Differential Continuous-Time Filter", *IEEE Trans. Circuits Systems I*, vol. 42, pp 896-903, November 1995.

Let us explore how a common-mode feedforward can be sensed and then applied. Consider a fully differential OTA with two current-mirrors



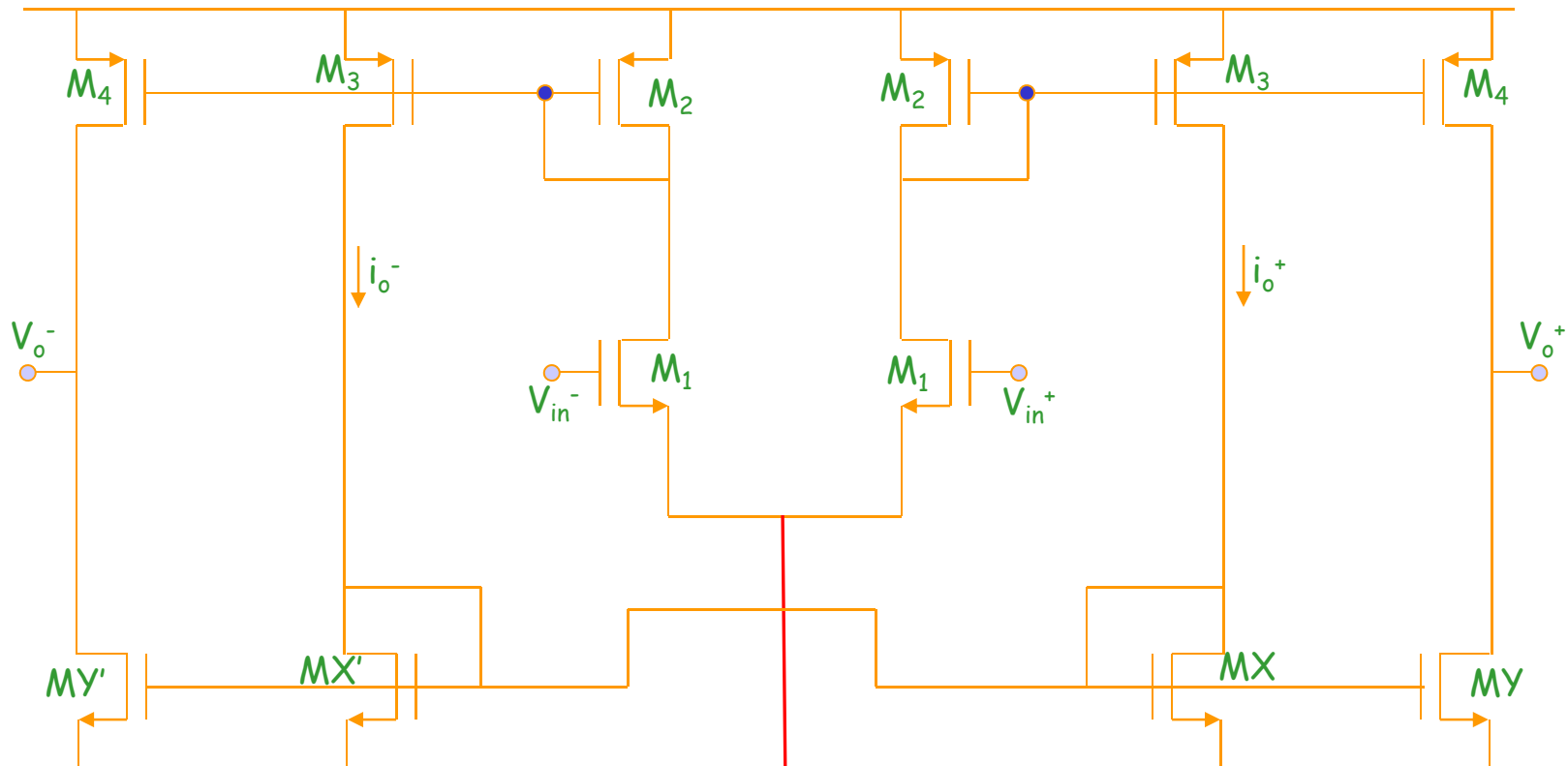
- Correcting signal can be voltage or current. Note that  $I_o^+$ , and  $I_o^-$  are equal to  $g_{m\_DRIVER} (V_{in}^+ - V_{in}^-)$  and  $g_{m\_DRIVER} (V_{in}^- - V_{in}^+)$ , respectively. That is, we are sensing the input voltage. We are not sensing the output voltage.
- $aI_o^+$  and  $aI_o^-$  are copies of  $I_o^+$  and  $I_o^-$ , respectively. In practice the value of  $aI_o$  is  $a = 1$  or  $a = 1/2$ .

# FD OTA with common-mode feedforward (current-mode)



- Since  $V_{reference} = 0$ ,  $V_{correction} = V_{cm}$  and can be applied to  $MY'$  and  $MY$ .

## FD OTA CMFF (current-mode)

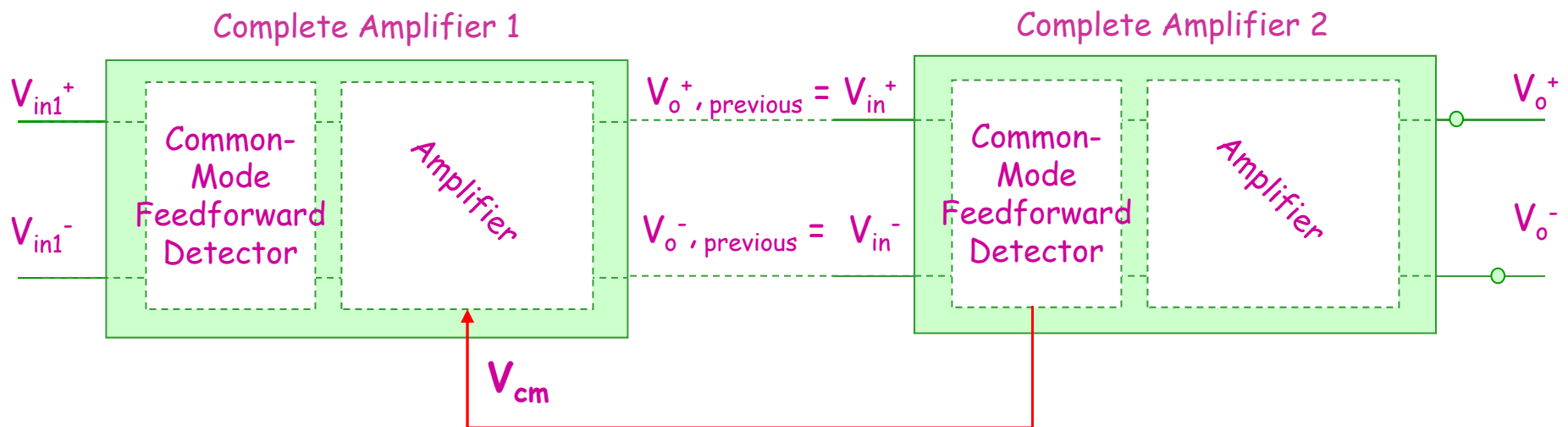


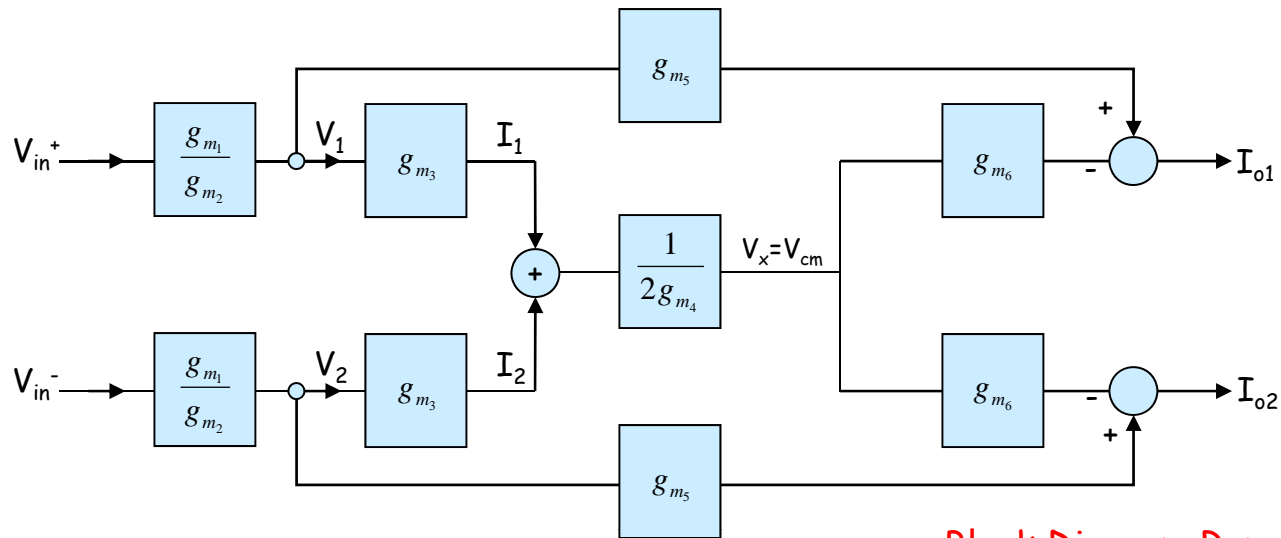
- OTA FD CMFF Implementation (Self-Bias)



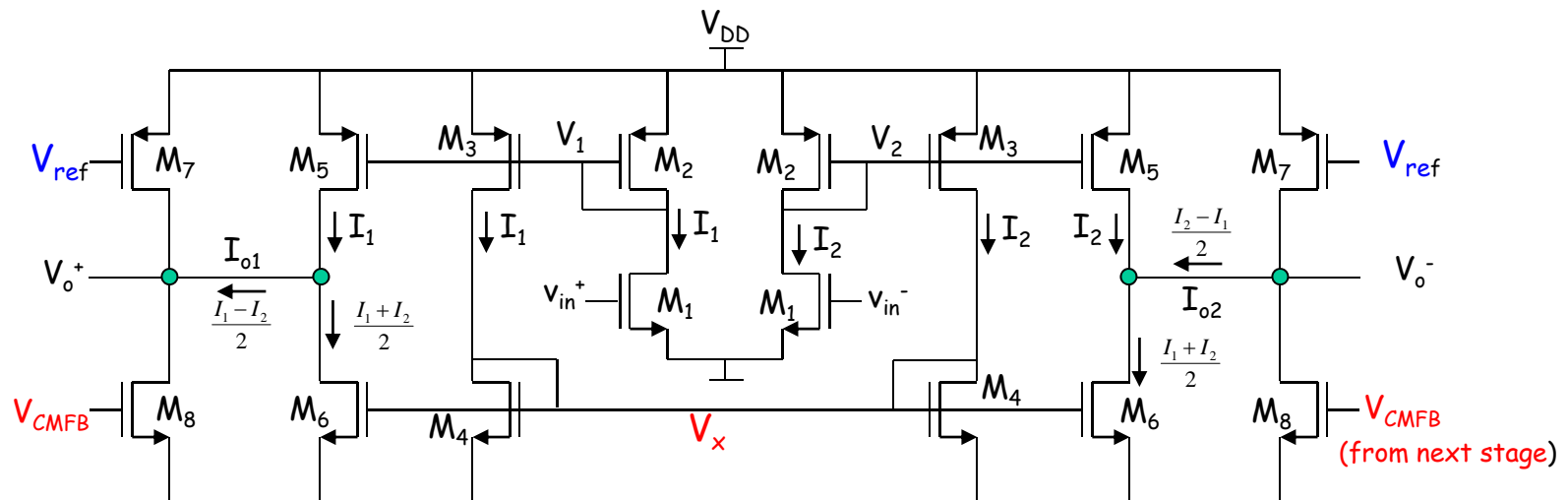
## Common feedback of more than one amplifier and their interconnections

- Observe that only one CMFB circuit is needed per output. If the Amp 1 is connected with a CMFB, any other amplifier connected to this amplifier does not need the extra CMFB.
- Furthermore, in some architectures the CM detector is a feedforward and forms part of the amplifier. An example of this type has been discussed before i.e., the Fully Balanced 4 current-mirror OTA





Block Diagram Representation

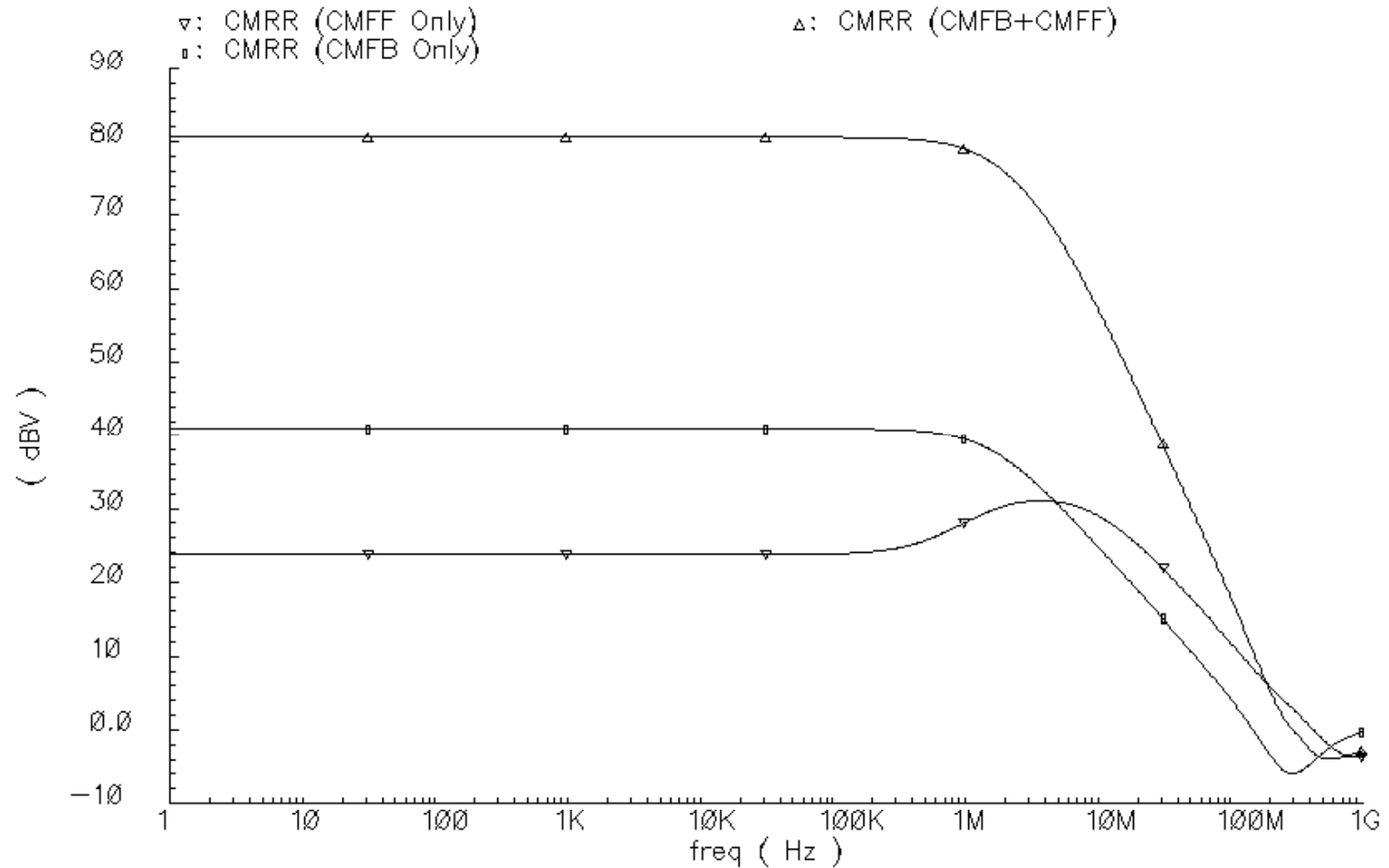


NEXT OTA IS DETECTING THE COMMON MODE FROM THIS OTA AND FEEDING BACK TO THIS OTA

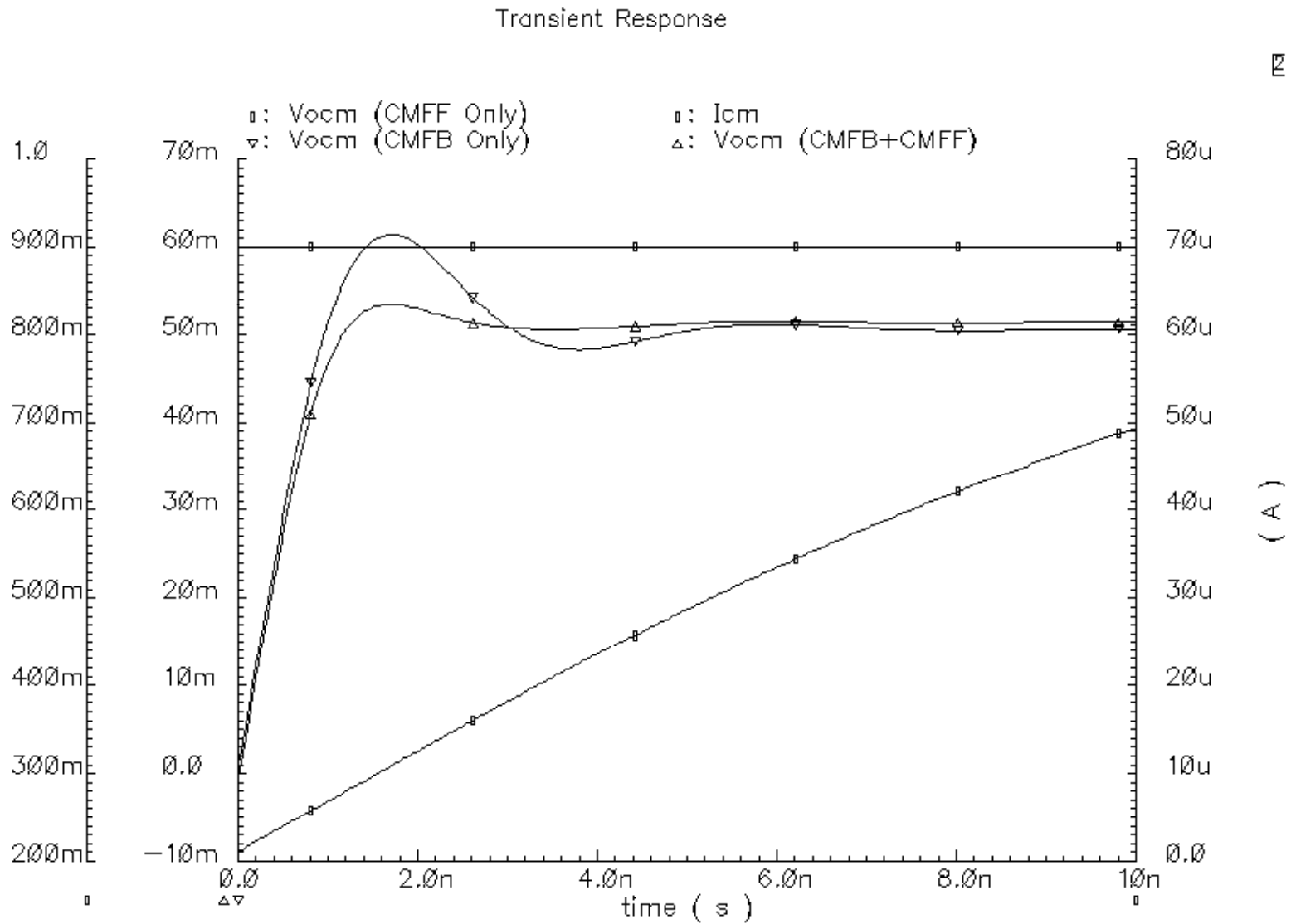
# Common-Mode Rejection Ratio (CMRR):

a) CMFF   b) CMFB   c) CMFB & CMFF

Common Mode Rejection Ratio

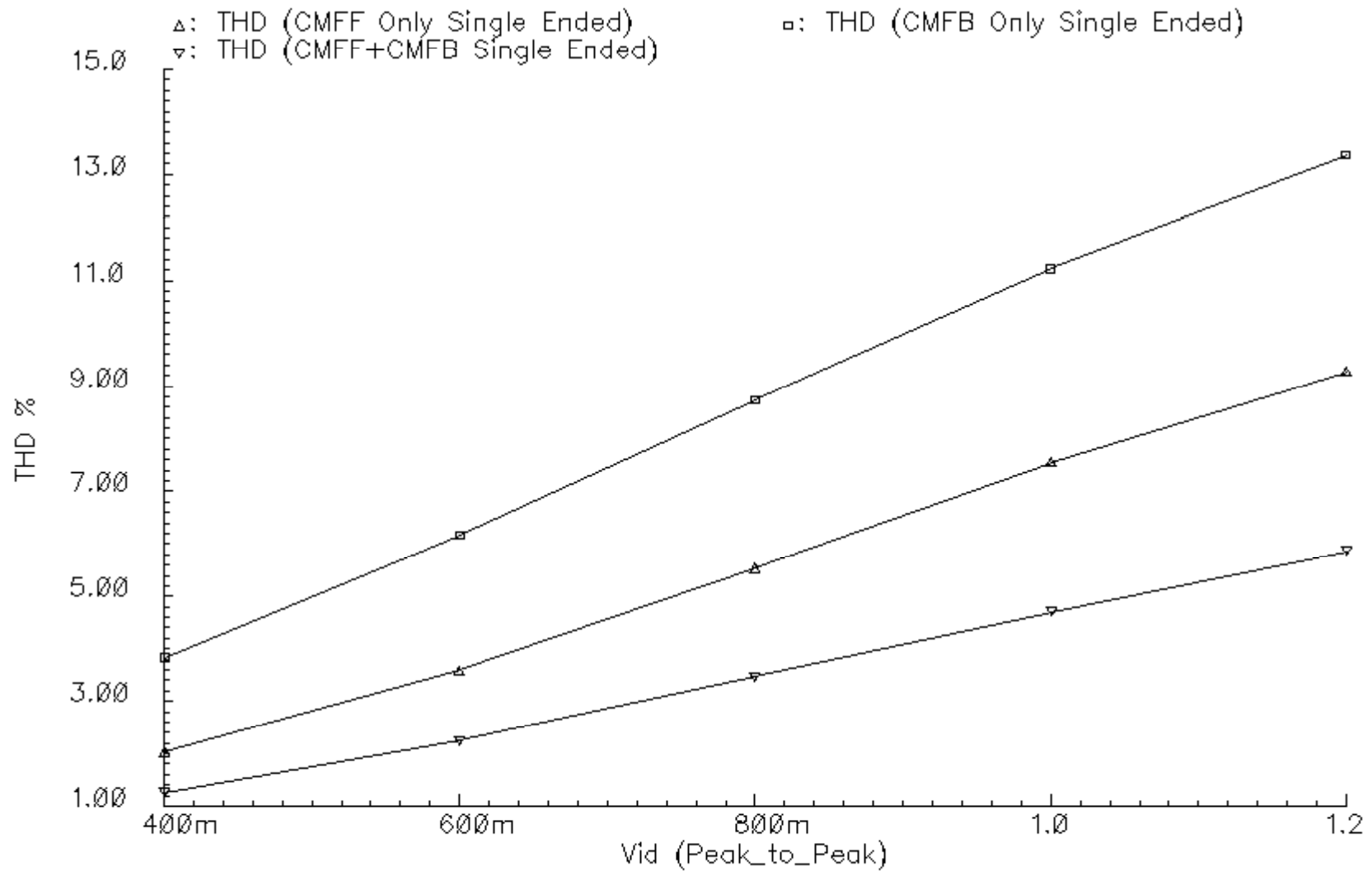


# Transient Response



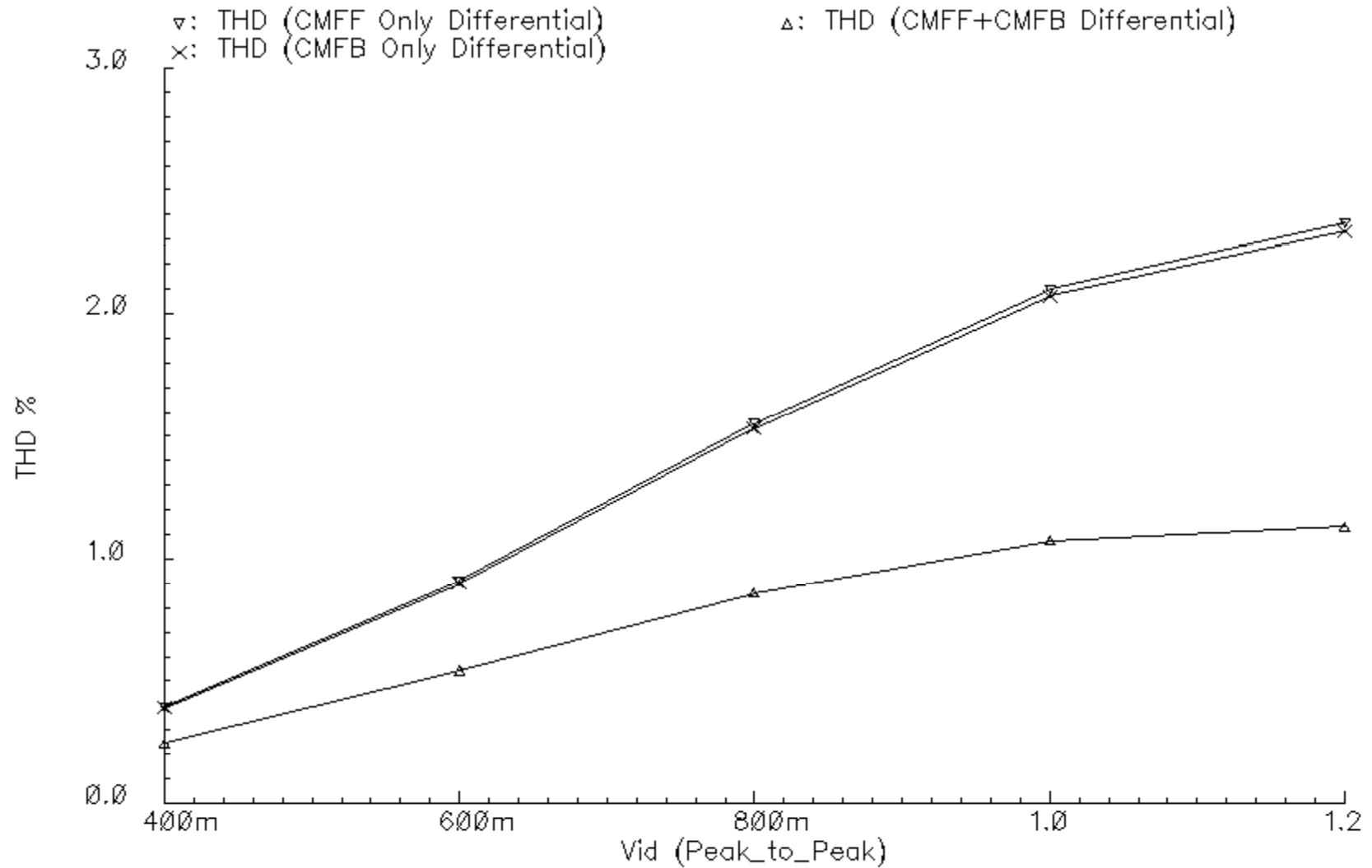
# Total Harmonic Distortion (Single-ended)

Total Harmonic Distortion

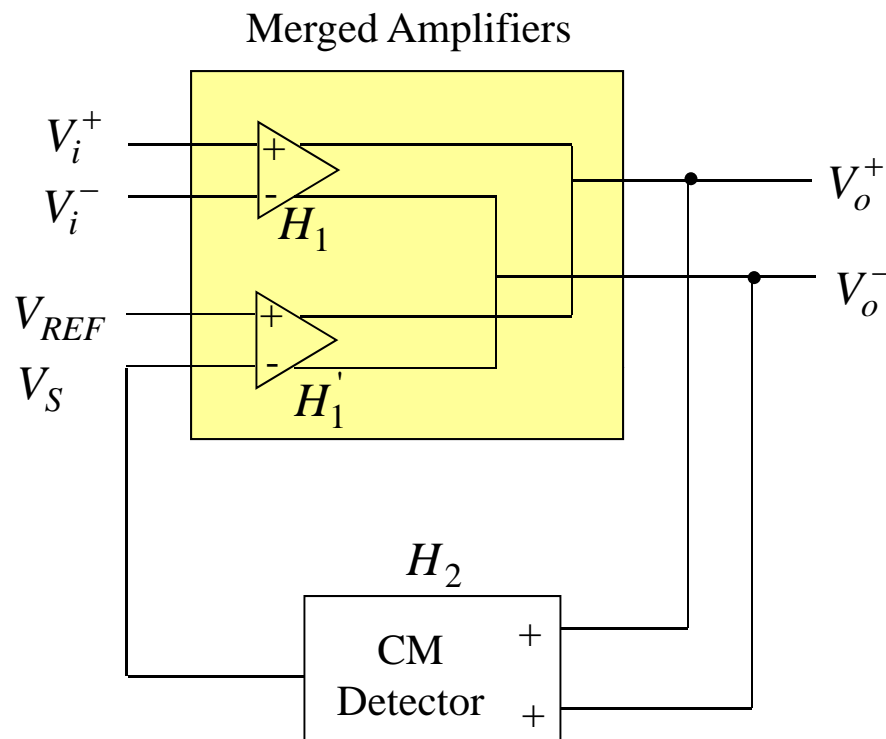


# Total Harmonic Distortion (Double-ended)

Total Harmonic Distortion



# COMMON-MODE FEEDBACK AMPLIFIERS: Characterization and Simulation



Fully Differential Amplifier  
With Common-Mode Feedback

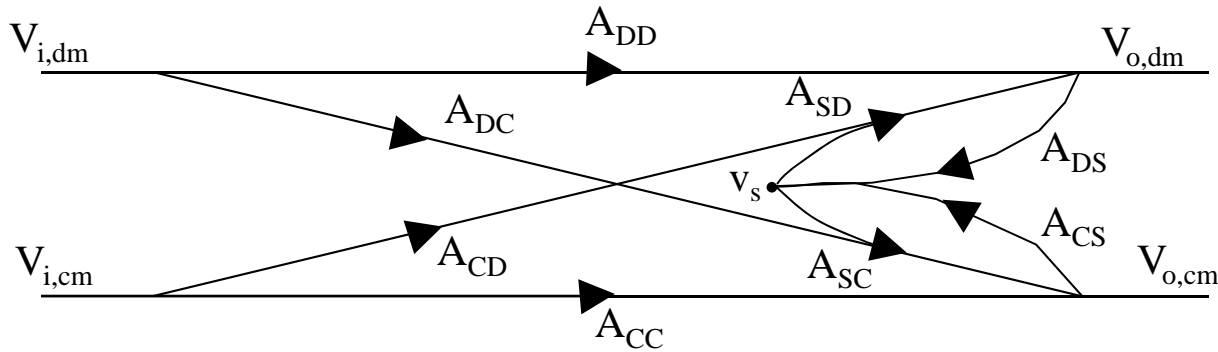
Ideal Response

$$v_s = \alpha_1 v_{o,cm} \quad ; \quad \alpha_1 = \frac{1}{2}$$

Taking into account mismatches on the Amplifiers  $H_1$  and  $H_1'$  yields:

$$v_s = \alpha_1 v_{o,cm} + \alpha_2 v_{o,dm} + \alpha_3 v_{o,dm}^2$$

Let assume the linearized ideal case  $\alpha_1 \neq 0, \alpha_3 = 0$  and  $\alpha_2 \neq 0$ .  
 Note here that the notation is changed to  $\alpha_1 = A_{CS}$ ,  $\alpha_2 = A_{DS}$



Using MASON's Rule

$$LG_{CM} = A_{SC} A_{CS}$$

$$LG_{DM} = A_{SD} A_{DS}$$

$$\Delta LG_{CM} = A_{CS} A_{SD}$$

$$\Delta LG_{DM} = A_{DS} A_S$$

$$D = 1 - LG_{CM} - LG_{DM}$$

$$A_{DD, \text{effective}} = \frac{A_{DD}(1 - LG_{CM}) + A_{DC} \Delta LG_{CM}}{D} \cong A_{DD}$$

$$A_{CC, \text{effective}} = \frac{A_{CC}(1 - LG_{DM}) + A_{CD} \Delta LG_{DM}}{D}$$

$$A_{DC, \text{effective}} \cong -A_{DD} \frac{A_{DS}}{A_{CS}}$$

$$A_{CD, \text{effective}} \cong A_{CD}$$



To investigate the non-linear effects, assume  $\alpha_1 \neq 0$ ,  $\alpha_3 \neq 0$  and  $\alpha_2 = 0$ . Thus  
 The following expressions can be approximated.

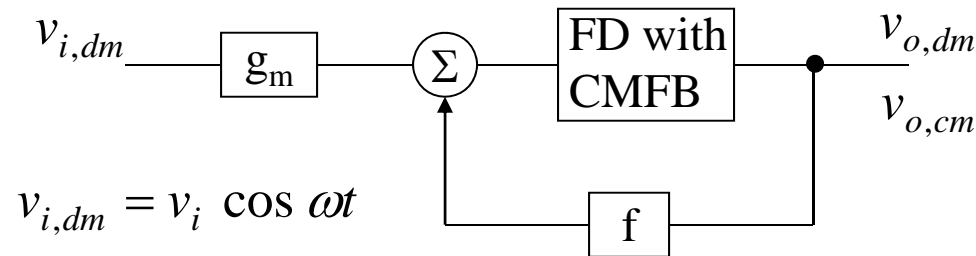
$$v_{o,dm} = A_{DD} g_m v_{i,dm} - A_{DD} f v_{o,dm} + A_{SD} v_s$$

$$v_{o,cm} = A_{DC} g_m v_{i,dm} - A_{DC} f v_{o,dm} + A_{SC} v_s$$

where

$$v_s \cong A_{CS} v_{o,cm} + \alpha_3 v_{o,dm} ; \alpha_1 = A_{CS}$$

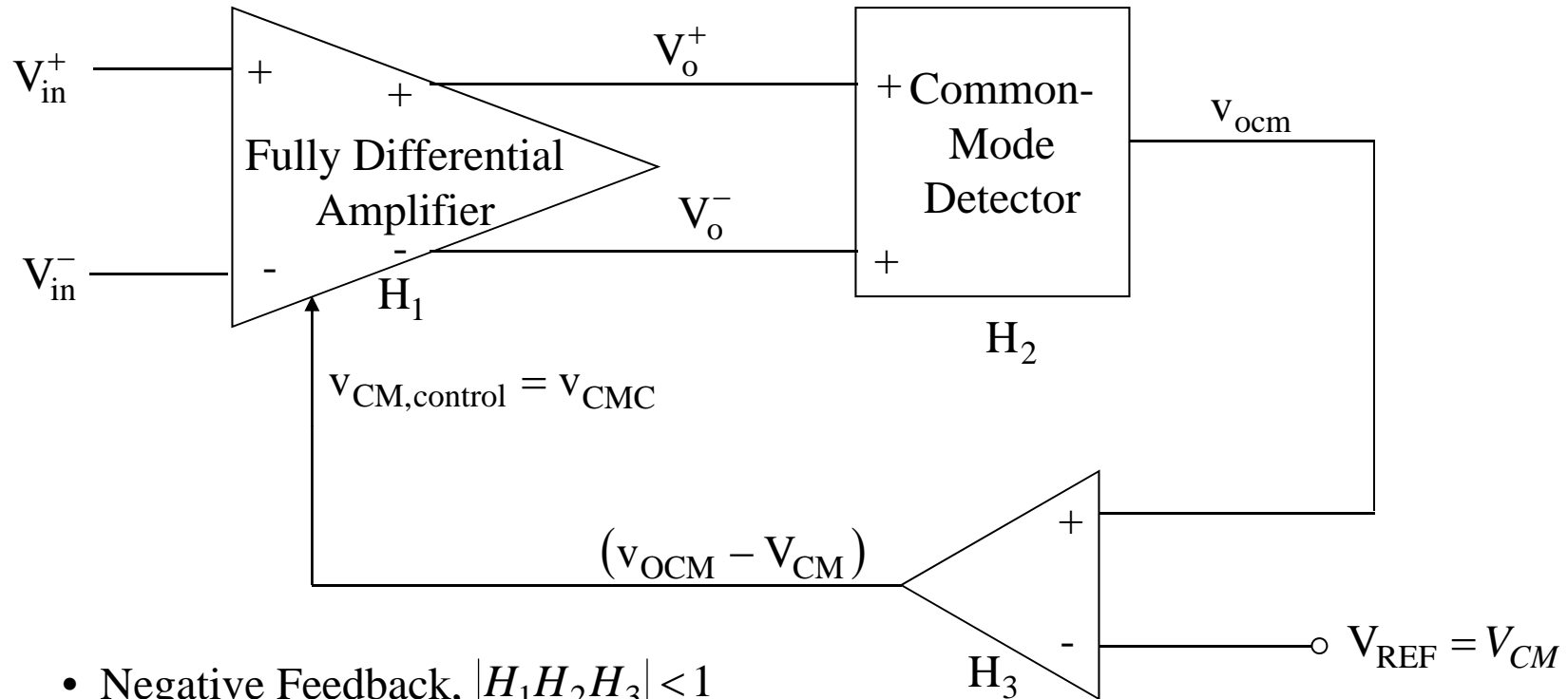
It can be shown that:



$$HD_2 \cong \frac{1}{2} \frac{\alpha_3 A_{SD} A_{CL}}{LG_{CM} LG_{DM,ex}} V_i ; \quad HD_3 \cong \frac{1}{2} \frac{\alpha_3^2 A_{SD}^2 A_{CL}^2}{LG_{CM}^2 LG_{DM,ex}^2}$$

$$A_{CL} = \frac{g_m}{f} ; \quad LG_{DM,ex} = f A_{DD}$$

# COMMON-MODE FEEDBACK LOOP



- Negative Feedback,  $|H_1 H_2 H_3| < 1$

$$H_{CM} = \frac{V_{OC}}{V_{inC}} = \frac{H_{1CM}}{1 + H_1' H_2 H_3} = \frac{H_{1CM}(s)}{1 + H_1'(s) H_2(s) H_3(s)}$$

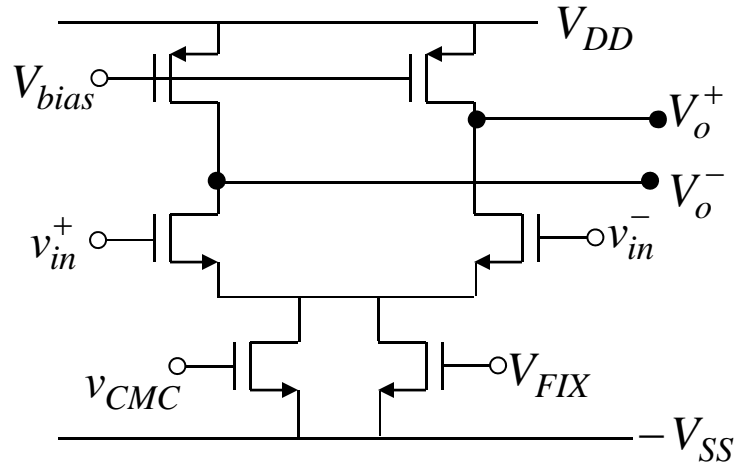
In Common - Mode

$$H_{DM} = H_1$$

In Differential - Mode

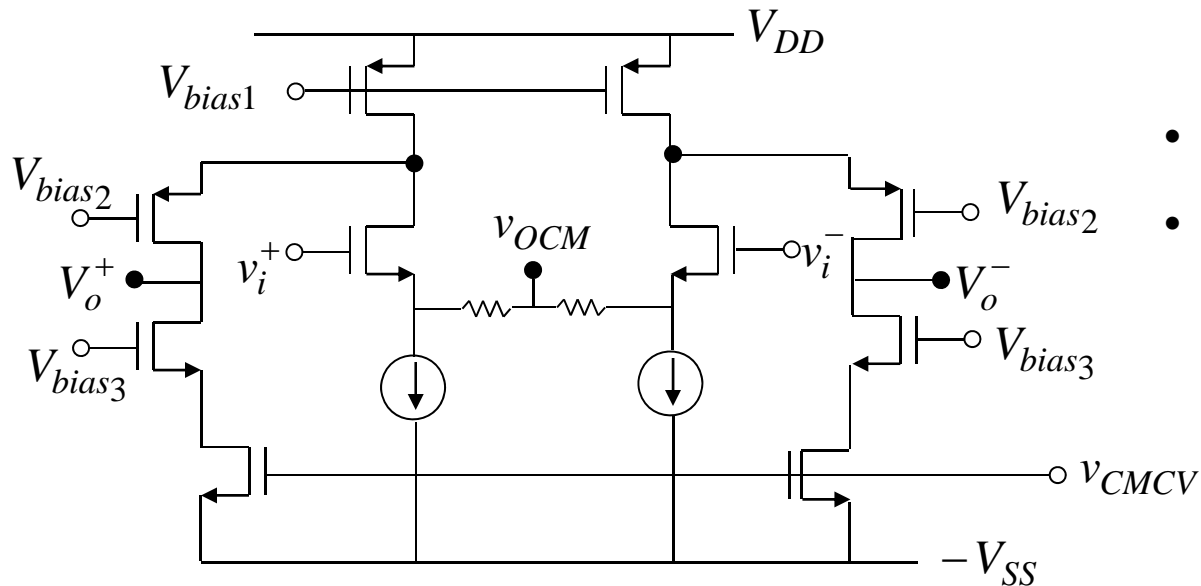
- Stability determined by open loop  $H_1' H_x H_3$
- H<sub>3</sub> is the CM-sense (or comparator) Amplifier.
- Goal to force  $v_{OCM} = V_{REF}$

- $H_1'$  is defined as the gain between input  $v_{CMC}$  and the output  $(V_o^+ - V_o^-)$   
i.e. two examples



$V_{FIX}$  determines the current for  $v_{CMC} = 0$ .

A Simple Fully-Differential Op Amp

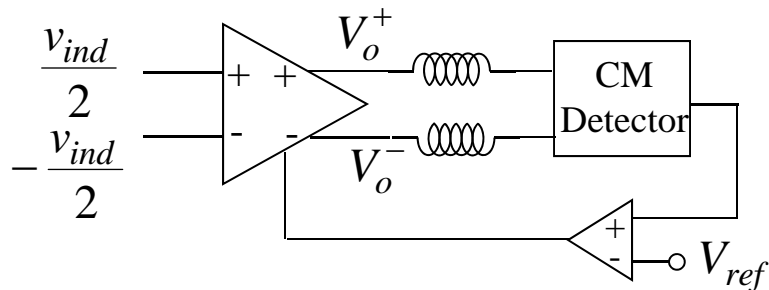


- Inherent CM detector
- $v_{OCM} \cong -V_{GS}$  ?

A Simplified Folded-Cascode Fully Differential Op Amp

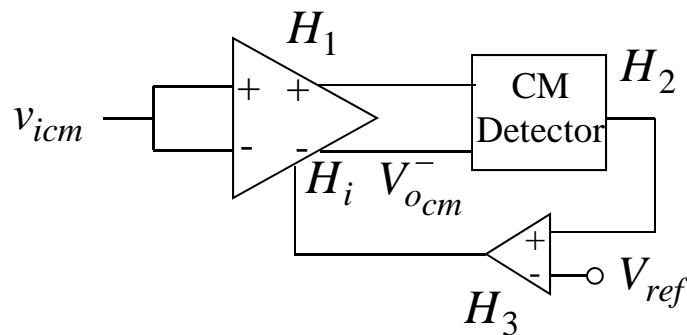
# STABILITY REMARKS

- The poles of the common-mode feedback are given by the open loop gain  $H_1'(s)H_2(s)H_3(s)$
- The bandwidth of the common-mode gain and the differential-mode gain.
- For differential inputs in an ideal amplifier



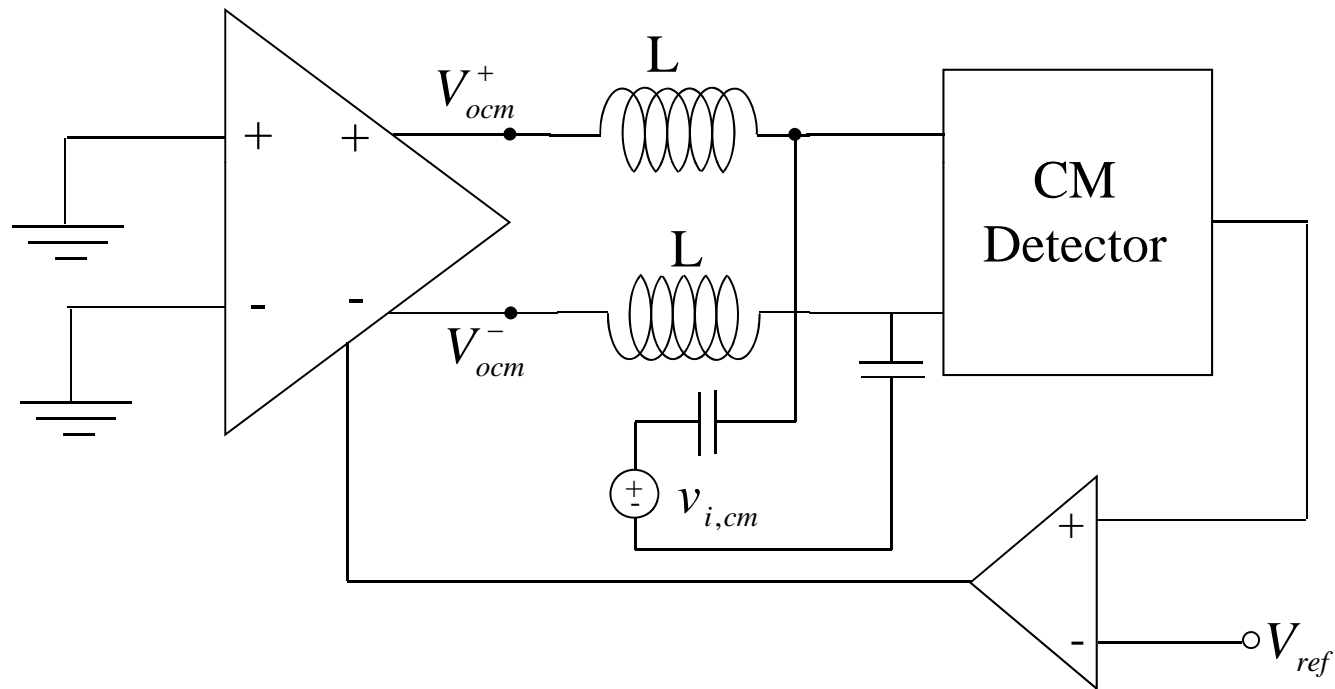
Differential-Mode.  
How to simulate this D-M?

Common-Mode



$$H_{CM} = \frac{H_{1CM}}{1 + H_1' H_2 H_3} \quad \text{i.e. } H_2 = \frac{1}{2}$$

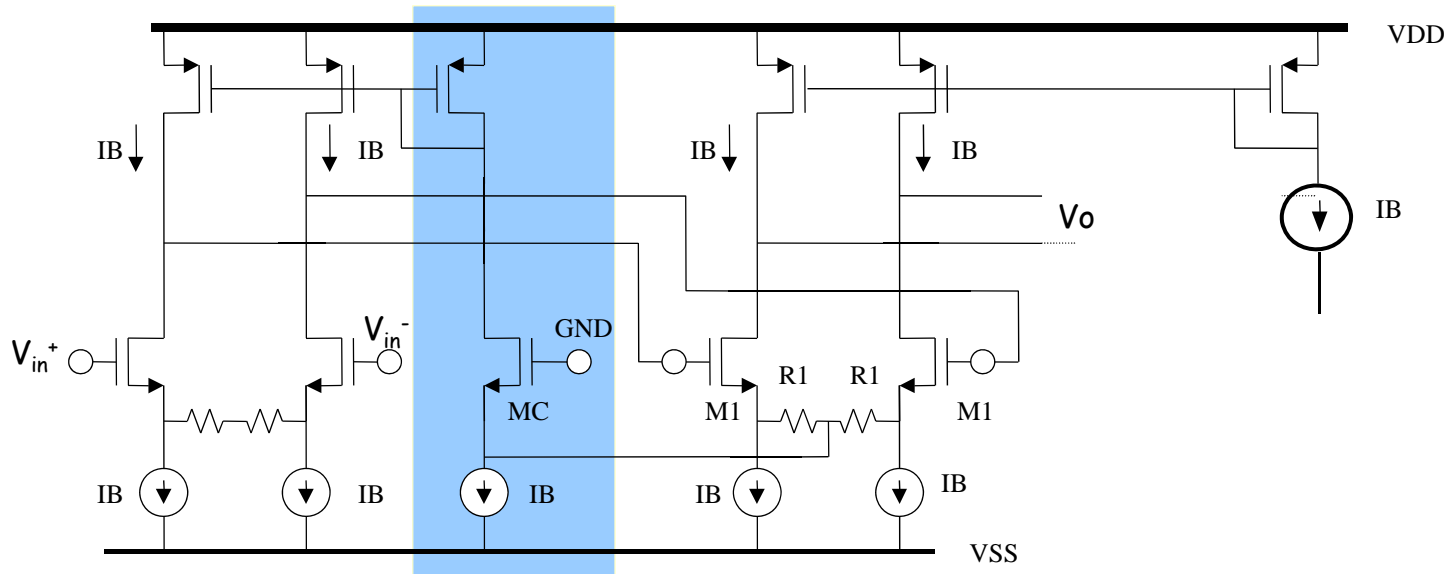
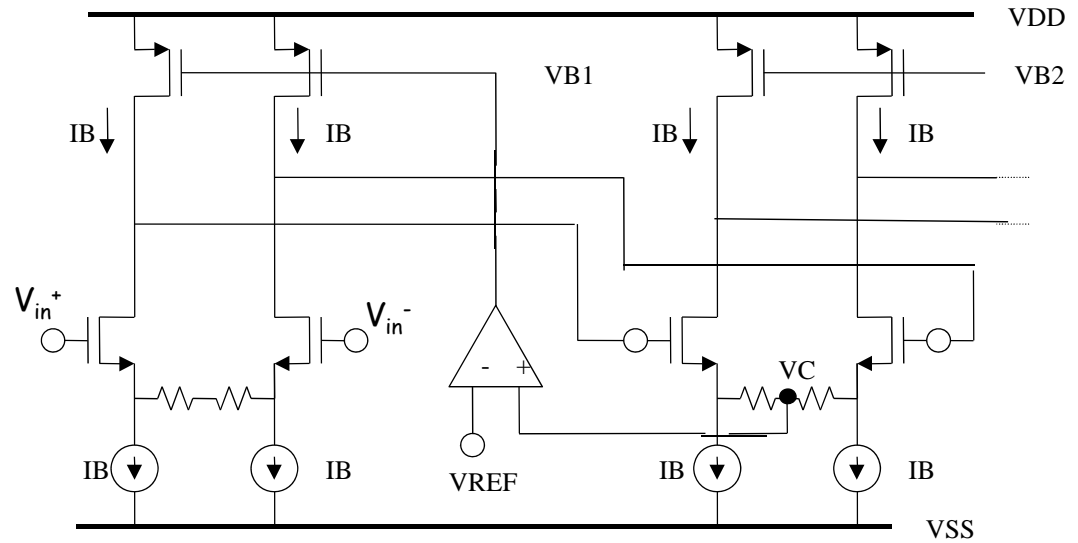
How to check stability of this loop?



# LV CMFB FOR OTAS

Typical OTA connection in fully differential OTA-C based circuits.

The common-mode voltage is obtained from the input of the following stage. Poor PSRR



**Pseudo-differential OTAs including the CMFB for the first one with good PSRR**

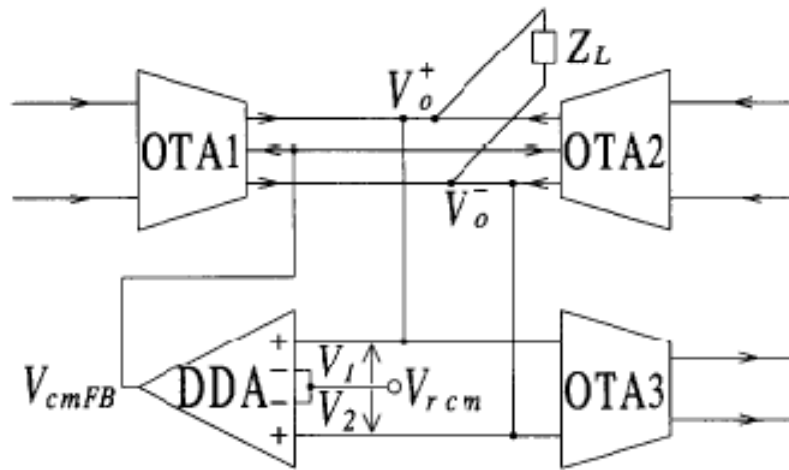
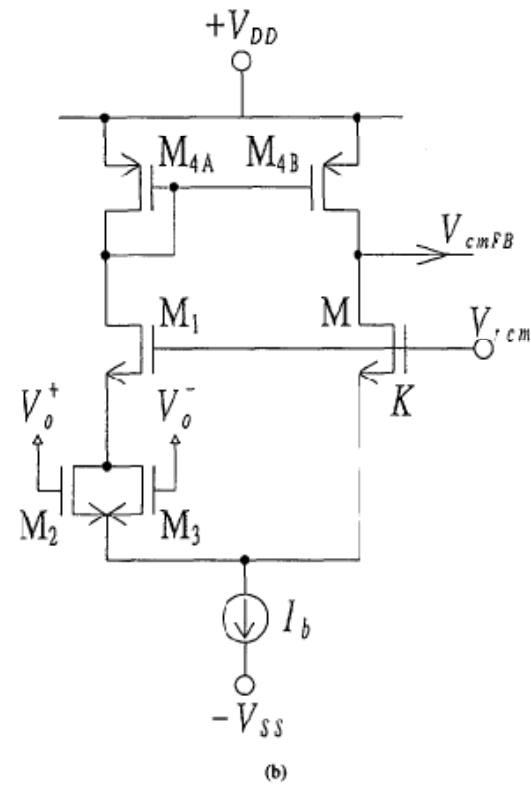


Fig. 1. Block diagram of CMFB with DDA.

**Common-Mode Feedback Circuit  
with Differential-Difference Amplifier**

Zdzislaw Czarnul, Shigetaka Takagi, and Nobuo Fujii



(b)

## Multipath common-mode feedback scheme suitable for high-frequency two-stage amplifiers

A.K. Gupta, V. Dhanasekaran, K. Soundarapandian and E. Sanchez-Sinencio

A method for stabilising the common-mode feedback (CMFB) loop in high-speed fully differential two-stage amplifiers is presented. Existing approaches may prove to be inadequate for high-speed designs. The problem becomes acute because of positive DC feedback by external network, which leads to 'latching states'. The proposed multipath approach avoids the latching states while maintaining the stability of the CMFB loop.

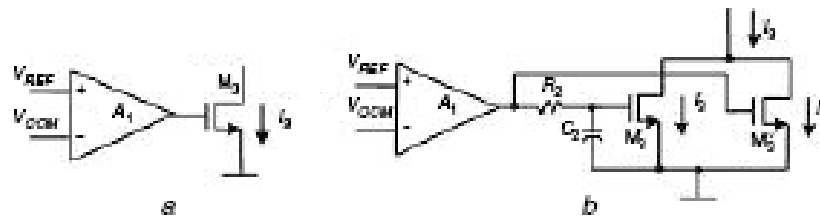


Fig. 2 Traditional CMFB and multipath CMFB schemes

a Traditional

b Multipath



## A CMOS 140-mW Fourth-Order Continuous-Time Low-Pass Filter Stabilized With a Class AB Common-Mode Feedback Operating at 550 MHz

Pankaj Pandey, Jose Silva-Martinez, and Xuemei Liu

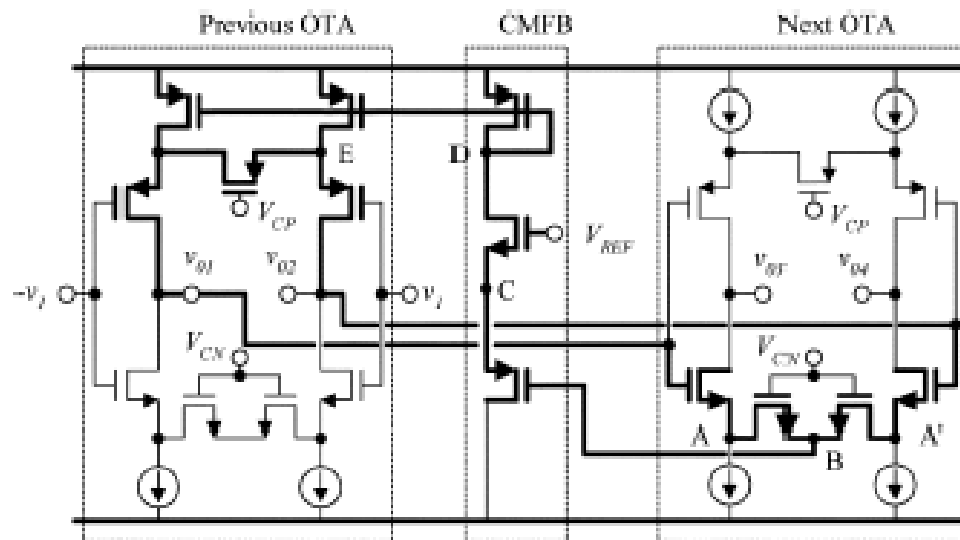
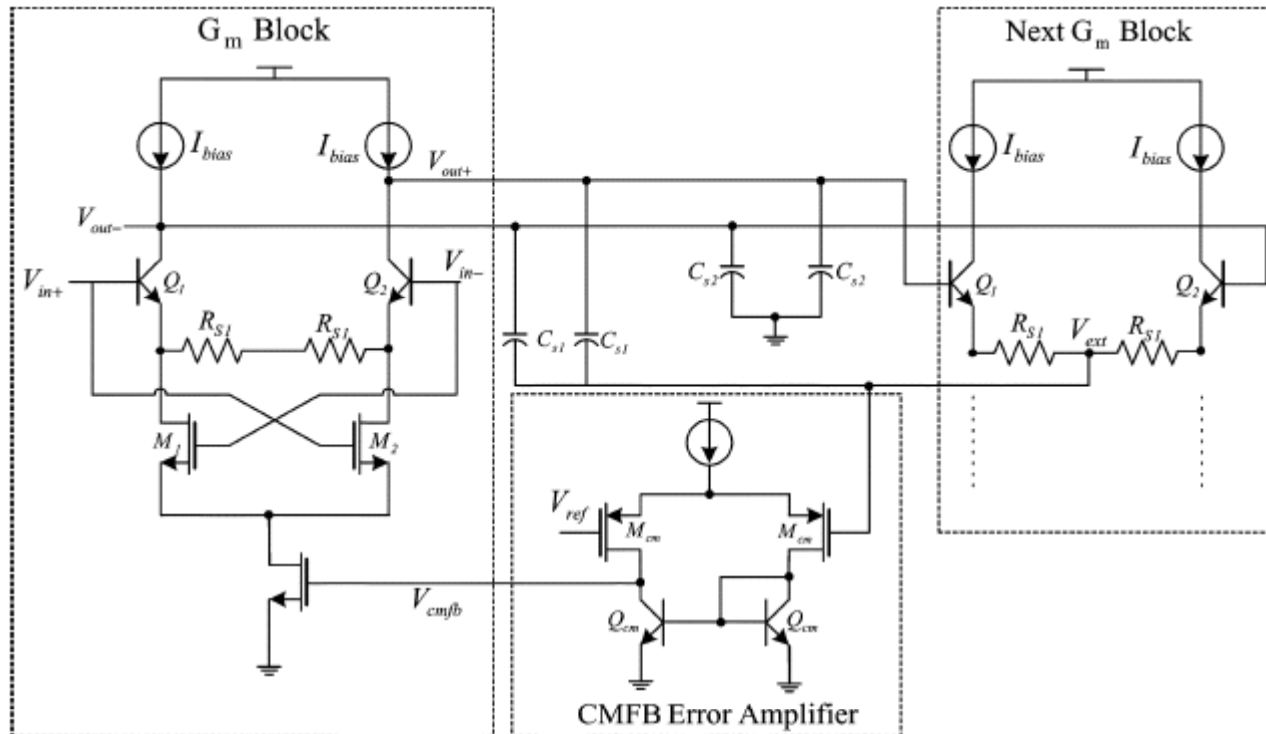


Fig. 3. CMFB scheme based on Class AB amplifier.

# An 11-Band 3–10 GHz Receiver in SiGe BiCMOS for Multiband OFDM UWB Communication

Alberto Valdes-Garcia, *Member, IEEE*, Chinmaya Mishra, *Student Member, IEEE*,  
 Faramarz Bahmani, *Member, IEEE*, Jose Silva-Martinez, *Senior Member, IEEE*, and  
 Edgar Sánchez-Sinencio, *Fellow, IEEE*



$G_m$  cell core and CMFB circuitry.

# Low-Power Architecture and Circuit Techniques for High-Boost Wide-Band $G_m$ - $C$ Filters

Manisha Gambhir, *Student Member, IEEE*, Vijay Dhanasekaran, *Student Member, IEEE*,  
Jose Silva-Martinez, *Senior Member, IEEE*, and Edgar Sánchez-Sinencio, *Fellow, IEEE*

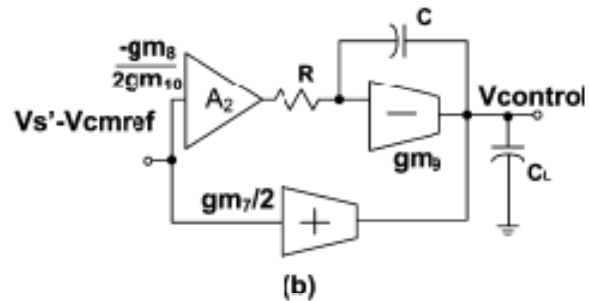
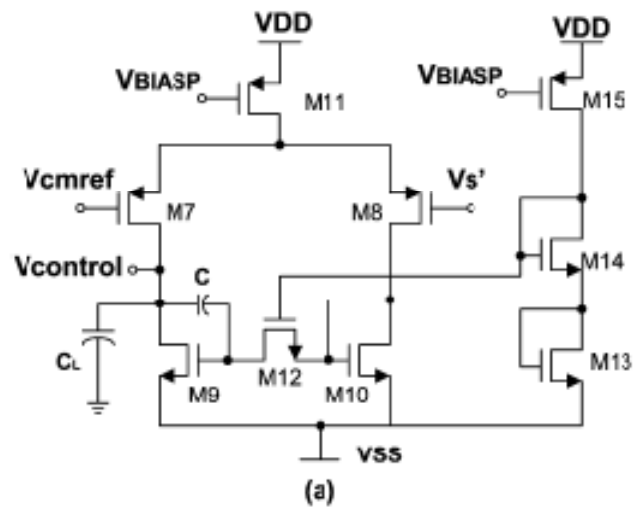


Fig. 10. (a) Circuit diagram for the proposed CMFB EA (b) Its equivalent representation.

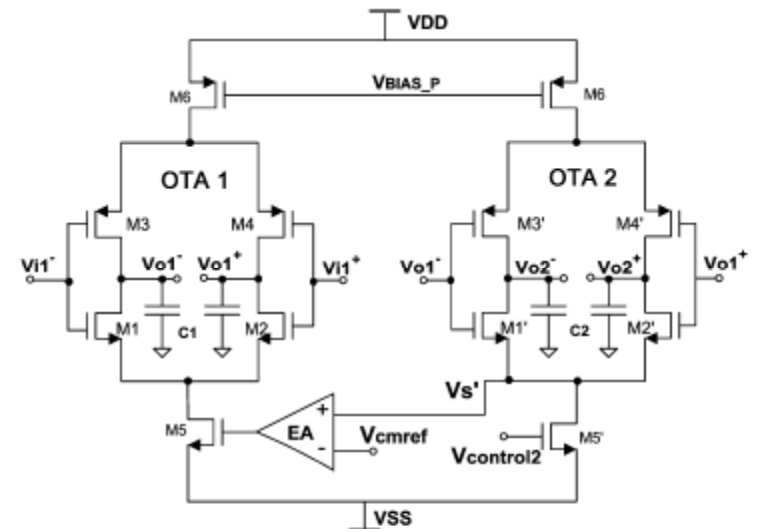


Fig. 9. CMFB loop involving two core OTAs and an CMFB amplifier.

# Final Remarks

- DC operating points for high impedances are difficult to fix
- Fully differential amplifiers with high output impedance nodes must use common-mode feedback circuits .
- Common mode circuits can fix the DC operating points as well as eliminate the common mode output component.
- Low voltage constraints impose optimal bias conditions at both the input and output ports of an amplifier.
- Common mode circuits for LV should be used both at the input and output