OP AMP CHARACTERISTICS

Static op amp limitations

REFERENCE: Chapter 5 textbook

ERRORS CAUSED BY THE INPUT BIAS CURRENT AND THE INPUT OFFSET CURRENT

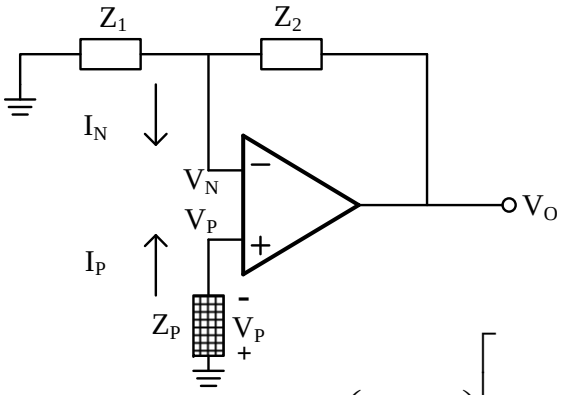
• Op Amp to function should have for the input terminals a DC path through which current can flow.

$$I_B = \frac{I_P + I_N}{2}$$ Input bias current

$$I_{OS} = I_P - I_N$$ Input offset vol tage , Ideally $I_{OS} = 0$ but due to mismatch $|I_{OS}| \neq 0$

i.e., for 741C

$$80nA \le I_B \le 500nA \quad \text{and} \quad 20nA \le |I_{OS}| \le 200nA$$



$$V_o = V_P\left(1 + \frac{Z_2}{Z_1}\right) + Z_2 I_N$$

also since $V_P = -Z_P I_P$

$$V_o = Z_2 I_N - \left(1 + \frac{Z_2}{Z_1}\right) Z_P I_P$$

$$E_o = \left(1 + \frac{Z_2}{Z_1}\right)\left[\frac{Z_2}{1 + \frac{Z_2}{Z_1}} I_N - Z_P I_P\right] = \left(1 + \frac{Z_2}{Z_1}\right)\left[\frac{Z_1 Z_2}{Z_1 + Z_2} I_N - Z_P I_P\right]$$

Note that I_N and I_P can be expressed as

$$I_P = \frac{2I_B + I_{OS}}{2}$$

$$I_N = \frac{2I_B - I_{OS}}{2}$$

Then the output offset voltage can be expressed as

$$E_O = \left(1 + \frac{Z_2}{Z_1}\right)\left[\left(\frac{Z_1 Z_2}{Z_1 + Z_2} - Z_P\right)I_B - \left(\frac{Z_1 Z_2}{Z_1 + Z_2} + Z_P\right)\frac{I_{OS}}{2}\right]$$

Note that if

$$Z_P = Z_1 // Z_2 = \frac{Z_1 Z_2}{Z_1 + Z_2}$$

Then E_O becomes

$$E_O \cong -\left(1 + \frac{Z_2}{Z_1}\right)\frac{Z_1 Z_2}{Z_1 + Z_2} I_{OS}$$

- Notice that one can keep the ratio Z_2/Z_1 constant but can reduce the values of Z_1 and Z_2 to minimize E_O.

Let us discuss another technique to reduce the input offset error.

For any configuration (inverting or non-inverting) one can write

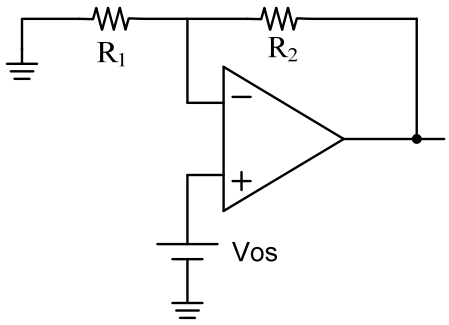
$$v_o = A_s V_i + E_o$$

$$\text{where } A_s = \begin{cases} -R_2/R_1 \\ 1 + R_2/R_1 \end{cases}$$

$$E_o = \left(1 + \frac{R_2}{R_1}\right)\left[V_{os} - (R_1 // R_2) I_{os}\right]$$

$$E_o \cong \frac{1}{\beta} E_I \qquad \text{where } \frac{1}{\beta} = 1 + \frac{R_2}{R_1}$$

The input offset voltage V_{os} can be modeled as shown next.



$$V_o = E_o = \left(1 + \frac{R_2}{R_1}\right) V_{os}$$

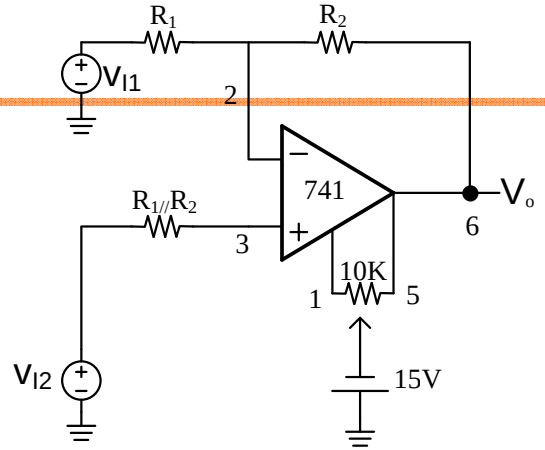
i.e. $\min V_{os} = \pm 2\text{mV}$ for a 741

$\max V_{os} = \pm 6\text{mV}$

For $\frac{R_2}{R_1} = 9$

Worst case is

$$E_o = 10 \times (\pm 6\text{mV}) = \pm 60\text{mV}.$$



Practical Internal Offset-Error-Nulling.

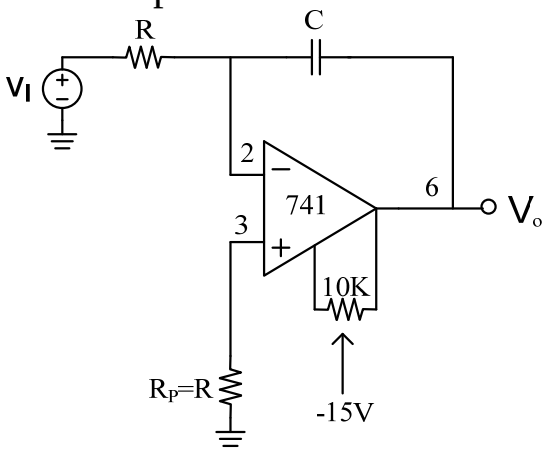
$$v_o = -\frac{R_2}{R_1}v_{I1} + \left(1+\frac{R_2}{R_1}\right)v_{I2} + E_o$$

$$E_o = \left(1+\frac{R_2}{R_1}\right)\left(V_{os} - (R_1 // R_2)I_{os}\right)$$

$$E_o = \frac{1}{\beta}E_I$$

- E_I is the total offset error referred to the output/

Example



$$v_o(t) = -\frac{1}{R_C}\int_o^t \left[V_I(\xi) + E_I\right]d\xi + V_o(0)$$

$$E_I = RI_{os} - V_{os}$$

Integrator with Internal Offset-Error Nulling.

Static op amp limitations

Low input bias current op amps

1. *Super-beta input op amps*: β_F ~ 1000 !, LM308 (I_B = 1nA)

2. *Input – bias –current cancellation*: Using internal circuitry, OP – 07 (I_B = 1 nA, I_{OS} =0.4 nA)

3. *JFET input op amps*: I_G in the order of tens of Pico amps. LF 356 BiFET (I_B = 30 pA, I_{OS} =3 pA), AD549, OPA129: Special JFET +Isolation techniques (I_B < 100 fA)

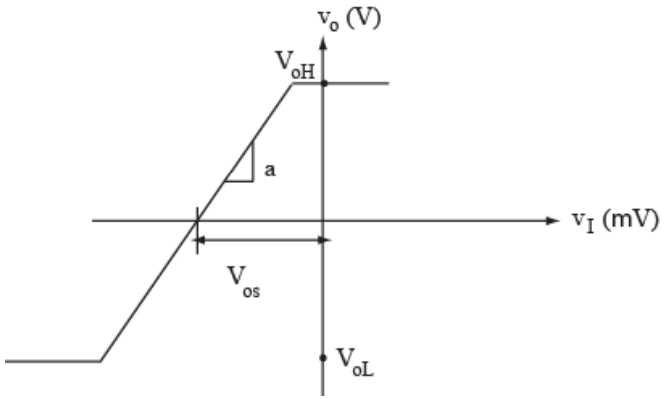
4. *MOSFET input op amps*: Input leakage current is around pA . TLC 279 CMOS (I_B = 0.7 pA, I_{OS} =0.1 pA),

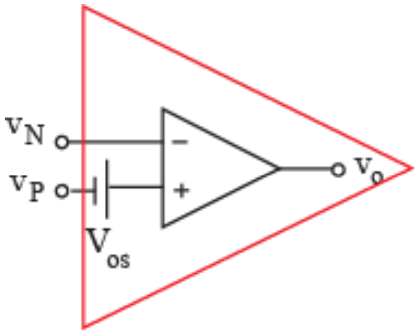
Input bias current drift

- **For Bipolar op amps increasing the temperature decreases I_B**
- **For p-n junction (Diode or JFET): $I_B(T) \sim I_B(T0) \cdot 2^{(T-T0)/10}$**
- **T0 : Ambient temperature (^oC)**
- **At high temperatures, there is no advantage in using FET op amps**

Static op amp limitations

2) Input offset voltage





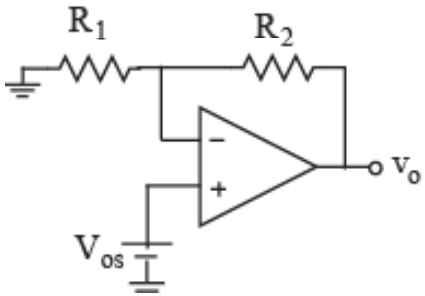
- $Vo = a . (v_P - v_N)$;
- By shorting v_P and v_N: $v_o = 0$,
- Due to inherent mismatches v_o is not zero

To force v_o to zero, a suitable correction voltage must be applied between the input ports.

$vo = a . (v_P + V_{os} - v_N) = 0$; $v_N = v_P + V_{os}$

Errors caused by V_{os} :

$$E_o = (1+(R_2 / R_1)). V_{os}$$



$R_2 >> R_1$: good for measuring V_{os}

Static op amp limitations

Thermal Drift

Temperature coefficient: $T_c (V_{os}) = d V_{os} / dT$ (mv/^oC)

$V_{os} (T) \sim V_{os} (25^oC) + Tc (V_{os}) . (T - 25^oC)$

Common Mode Rejection Ratio

We model this phenomena with a change in the input offset voltage due to v_{CM} variation
$1 / CMRR = d V_{os} / d v_{CM}$ (μV/V), In practice $v_{CM} \sim v_P$

Power Supply Rejection Ration

We model this phenomena with a change in the input offset voltage due to supply variation : $1 / PSRR = d V_{os} / d V_S$ (μV/V)

Changes of V_{os} with output swing

Δ Vos = Δ vo / a

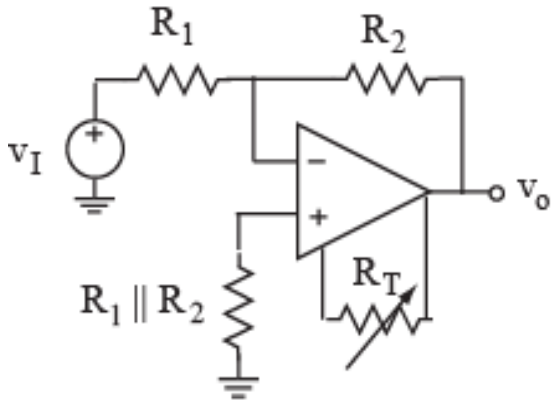
Static op amp limitations

Summary of effects which generate V_{os} :

$$V_{os} = V_{os0} + Tc\,(V_{os}) \cdot \Delta T + (\Delta V_p / CMRR) + (\Delta V_s / PSRR) + (\Delta v_o / a)$$

3) Input offset –error compensation

Internal offset nulling:



$$E_o = (1 + (R_2 / R_1)) \cdot [\, V_{os} - (R_1 \parallel R_2) I_{os} \,]$$

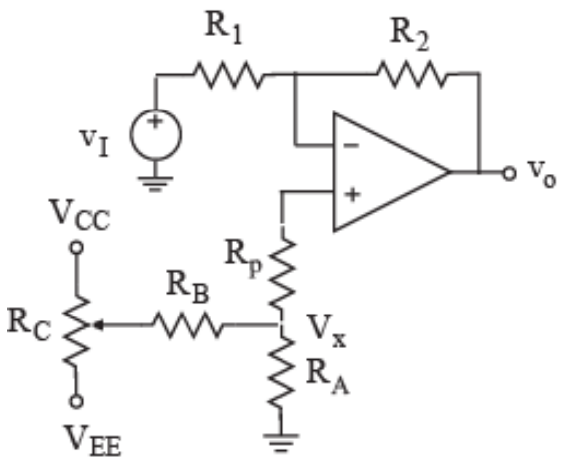
$$E_I = V_{os} - (R_1 \parallel R_2) I_{os}$$

E_I can be nulled by using a suitable trimmer, a smart designer tries to minimize E_I by a combination of circuit tricks (scaling, op amp selection, etc). The last choice would be trimming.

Static op amp limitations

External offset nulling:

Does not introduce any additional imbalance to the input stage, no degradation drift CMRR, PSRR



Input Error: $E_I + V_x$

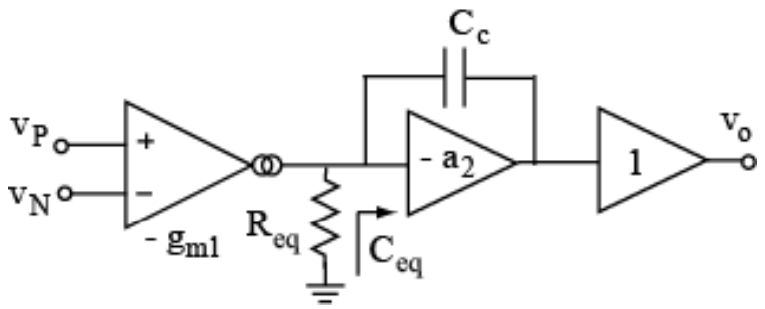
R_B >> R_C (Excessive loading of the wiper)

R_A << R_P (Avoid perturbing)

Dynamic op amp limitations Ref. Ch 6 textbook

1) Open-loop response

Dominant pole response:



Low frequencies: $v_o = g_{m1} R_{eq} a_2 (v_P - v_N)$

Higher frequencies: Low pass filter action

$$f_b = \frac{1}{2\pi R_{eq} C_{eq}} \quad \text{(dominant pole frequency)}$$

$C_{eq} \longrightarrow$ Very big for integration

$C_{eq} = (1 + a_2).\, C_c \longrightarrow$ Miller Effect

Expression for open-loop response:

$$a(jf) = \frac{a_0}{1 + j(f/f_b)}$$

a_0 : open-loop DC gain

$$|a(jf)| = \frac{a_0}{[1 + (f/f_b)^2]^{1/2}}$$

$$\angle a(jf) = -\tan^{-1}(f/f_b)$$

f_t : unity gain freq.

$f_t = a_0 f_b$

$(f_b \ll f_t)$

The open-loop response has higher order poles and zeroes, but the dominant pole frequency is chosen deliberately low to ensure that gain has dropped well below unity and the effect of higher order roots can be ignored

Dynamic op amp limitations

Dominant pole response:

$$a(jf) \longrightarrow -j\left(f_t / f\right) \quad ; \text{Integrator}$$

$$(f >> f_b)$$

$$GBP = f_t = \text{Const.}$$

- **For general –purpose type op amps: 500 kHz < GBP <20 MHz**
- **a_0 and f_b are ill-defined because of R_{eq} and a_2 due to manufacturing process variations. f_t is more practical parameter.**

$$v_o \sim \frac{1}{2\pi j f C_c} g_{m1}\left(v_P - v_N\right) \qquad f_t = \frac{g_{m1}}{2\pi C_c} = \frac{I_A}{8\pi V_T C_c}$$

Stable, predictable values of I_A and C_C

$$a(jf) = \frac{g_{m1}}{2\pi j f C_c} = -j\left(f_t / f\right)$$

Graphical visualization of loop-gain:

$$T(jf) = a(jf).(1/\beta)$$

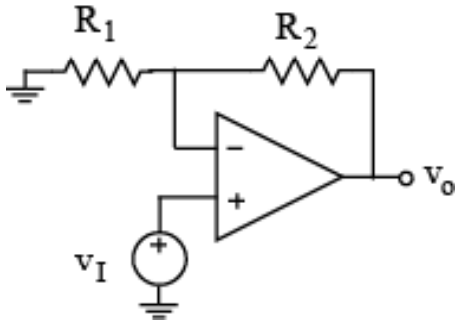
$$|T|_{dB} = |a|_{dB} - |1/\beta|_{dB}$$

$$\angle T = \angle a - \angle(1/\beta)$$

Dynamic op amp limitations

2) Closed-loop response

Non- inverting Amplifier:



$$A(jf) = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{1}{1 + \left[\left(1 + \frac{R_2}{R_1}\right) / a(jf)\right]} \qquad A(jf) = \frac{A_0}{1 + j\,(f / f_B)}$$

$$A_0 = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{1}{1 + \left[\left(1 + \frac{R_2}{R}\right) / a_0\right]} \sim \left(1 + \frac{R_2}{R_1}\right)$$

$f_B = f_b\,(1 + a_0\beta) \sim \beta \cdot f_t$; f_B : Closed loop bandwidth

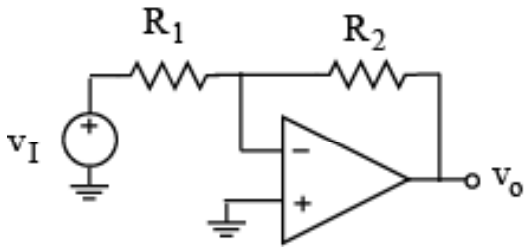
a) $|T| >> 1$, $A \sim A_{ideal}$
b) $|T| = 1$, phase $(T) = -90^o$, $A = A_{ideal} / (1 + j)$
c) $|T| << 1$, $A \sim A_{ideal} \cdot T = a$

Negative feedback reduces gain form a_0 to A_0 ($A_0 << a_0$), but widens the bandwidth from f_b to f_B ($f_b >> f_B$).

Gain – Bandwidth trade off:
GBP = $| A_0 | \cdot f_B = f_t$

Dynamic op amp limitations

Inverting Amplifier:



$$A(jf) = \frac{A_0}{1 + j(f/f_B)} \qquad A_0 \sim -\frac{R_2}{R_1} \qquad f_B \sim \beta \cdot f_t$$

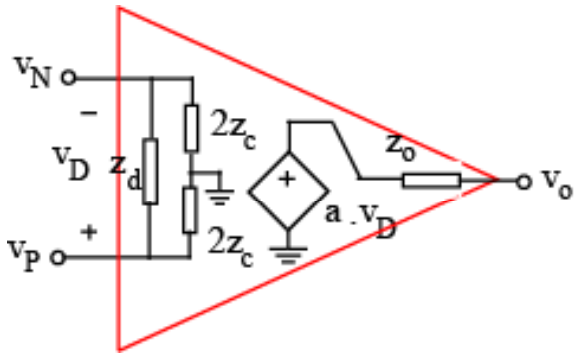
Gain – Bandwidth trade off:

GBP = $|A_0| \cdot f_B = (R_2 / R_1) \cdot f_t \cdot (R_1 / (R_1 + R_2)) = (1 - \beta) \cdot ft$

Non-inverting unity gain amplifier : GBP = f_t

Inverting unity gain amplifier : GBP = 0.5 f_t

3) Output and input impedances



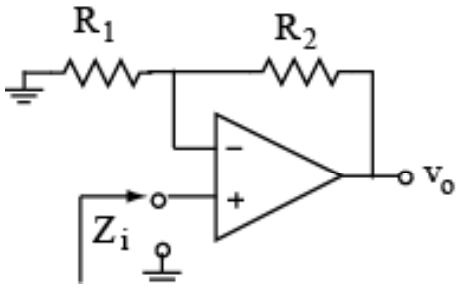
- **z_d, z_o are capacitive or inductive**
- **z_c, common mode input impednace**
- **Data sheets provide r_d, r_o, r_c**
- **Some times C_d, C_c information is provided**

Z ~ z (1 + T) (series) or Z ~ z (1 + T)$^{-1}$ (shunt)

By decreasing T at higher frequencies the series impedance is more capacitive and the shunt Impedance is more inductive

Dynamic op amp limitations

Input series impedance:



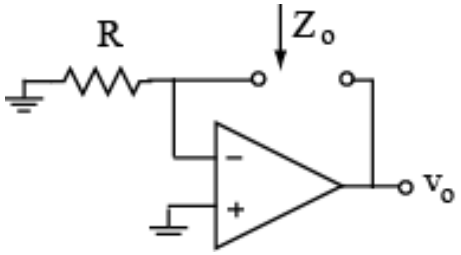
$$Z_d \sim z_d (1 + a\,\beta)$$

$$Z_d \sim r_d (1 + a_0\beta)\ \frac{1 + j\,(f / f_B)}{1 + j\,(f / f_b)}$$

$$|T| \gg 1,\ Z_d \sim r_d (1 + a_0\beta)$$

$$|T| = 0,\ Z_d \sim r_d$$

Output series impedance:



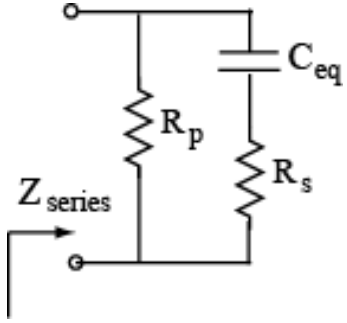
$$Z_o \sim R\,(1 + a)$$

$$Z_o \sim R\,(1 + a_0)\ \frac{1 + j\,(f / f_t)}{1 + j\,(f / f_b)}$$

$$|T| \gg 1,\ Z_o \sim R\,(1 + a)$$

$$|T| = 0,\ Z_o \sim R$$

Equivalent Circuit



Input

Low freq. $\longrightarrow$ $R_p = (2\,z_c) \parallel [r_d (1 + a_0\beta)]$

High freq. $\longrightarrow$ $R_p \parallel R_s = r_d$ OR $R_s \sim r_d$

$$|Z_{Ceq}(jf_B)| = r_d \longrightarrow C_{eq} = \frac{1}{2\pi f_B r_d}$$

Output

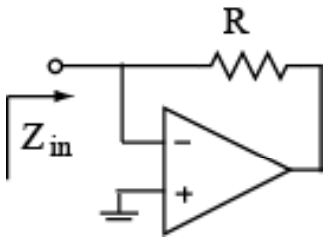
Low freq. $\longrightarrow$ $R_p \sim R\,(1 + a_0)$

High freq. $\longrightarrow$ $R_s \sim R$

$$C_{eq} = \frac{1}{2\pi f_t R}$$

Dynamic op amp limitations

Input shunt impedance:



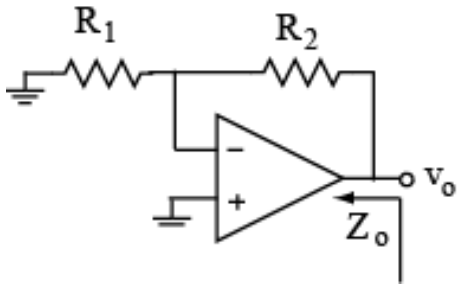
$$Z_i \sim R/(1+a)$$

$$Z_i \sim [R/(1+a_0)]\,\frac{1+j(f/f_b)}{1+j(f/f_t)}$$

$$|T| \gg 1,\ Z_i \sim R/(1+a_0)$$

$$|T| = 0,\ Z_o \sim R$$

Output shunt impedance:



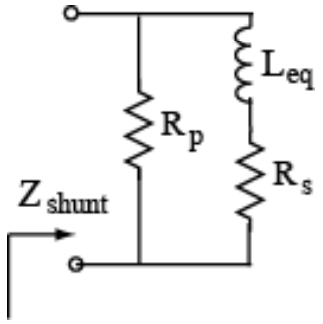
$$Z_o \sim r_o/(1+a\beta)$$

$$Z_o \sim [r_o/(1+a_0\beta)]\,\frac{1+j(f/f_b)}{1+j(f/f_B)}$$

$$|T| \gg 1,\ Z_o \sim r_o/(1+a_0\beta)$$

$$|T| = 0,\ Z_o \sim r_o$$

Equivalent Circuit



Output

Low freq. $\longrightarrow$ $R_p = r_o$

High freq. $\longrightarrow$ $R_p \| R_s \sim R_s = r_o/(1+a_0\beta)$

$$|Z_{Leq}(jf_B)| = r_o \longrightarrow L_{eq} = \frac{r_o}{2\pi f_B}$$

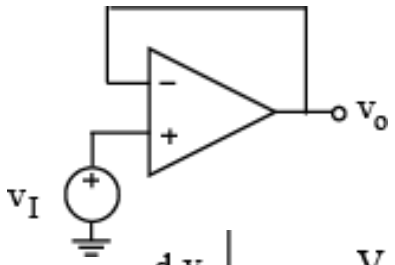
Dynamic op amp limitations

4) Transient response

Examining the transient response to a step signal

Rise Time (t_R)

$$A(jf) = \frac{A_0}{1 + j(f/f_t)} \longrightarrow \text{Voltage Follower}$$



$$v_I(t) = S(t) \longrightarrow v_o(t) = V_m(1 - \exp(-t/\tau))$$

$$\tau = 1/(2\pi f_t)$$

$$t_R = \tau(\ln(0.9) - \ln(0.1)) = 0.35/f_t$$

$$\left.\frac{dv_o}{dt}\right|_{t=0} = \frac{V_m}{\tau}$$

t_R : time for V_o to swing from 10% to 90% of V_m:

Slew –Rate limiting

- **Above a certain step – amplitude the output slope saturates at a constant value named slew-rate and the output waveform is a ramp**
- **Slew rate limiting is a nonlinear effect that stems from the limited ability by the internal circuitry to charge or discharge the frequency compensation capacitor C_c**

Dynamic op amp limitations

$$\frac{V_{om\,(crit.)}}{\tau} = S.R. \qquad V_{om\,(crit.)} = \frac{S.R.}{2\pi f_t}$$

Generalization for $\beta < 1$: $f_t \rightarrow \beta \cdot f_t$

Full - Power Bandwidth :

The maximum frequency at which the op amp will yield an undistorted AC output With the largest possible amplitude.

$$V_o(t) = V_{om} \cdot \sin(2\pi f t) \qquad \left.\frac{dV_o}{dt}\right|_{Max} = 2\pi f V_{om} = S.R.$$

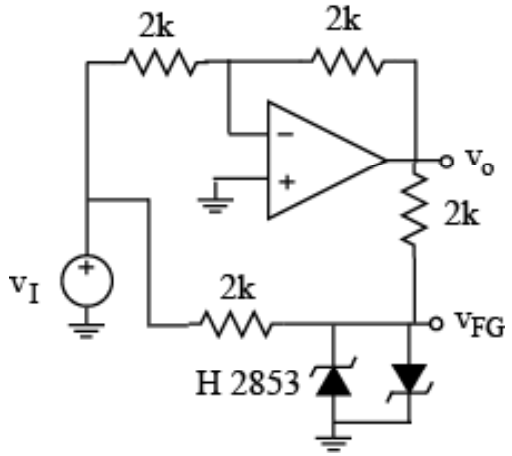
$$F.P.B = \frac{S.R.}{2\pi\ V_{sat}}$$

Settling time (t_s)

The time it takes for the response to a large input signal to settle and remain within Specified error band (0.1% and 0.01%nof a 10 V input step).

Test Circuit for t_s

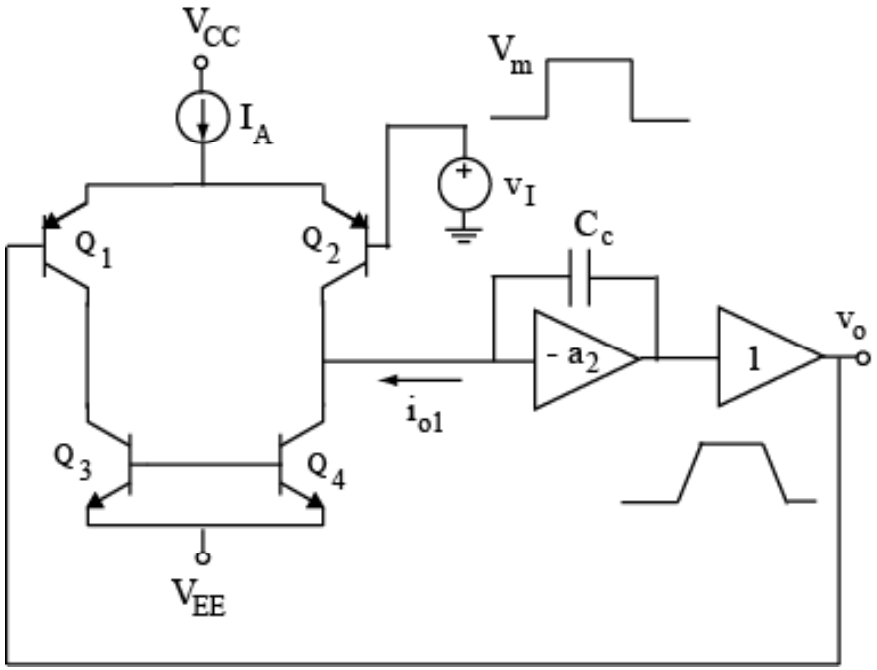
$$v_{FG} = (1/2)(v_I + v_o) = 0$$



Fast t_s is desirable in high speed, high accuracy D-A converters, S & H circuits and multiplexed amplifiers

Dynamic op amp limitations

Slew rate limiting – causes and cures



V_m small; input stage in linear region:

$$i_{o1} = g_{m1} V_m$$

$$\frac{dv_o}{dt} = \frac{g_{m1} V_m}{C_c}$$

By overdriving input stage i_{o1} saturates at I_A and C_c is current starved.

$$\left.\frac{dv_o}{dt}\right|_{Max} = \frac{I_A}{C_c} = S.R.$$

$$f_t = \frac{g_{m1}}{2\pi C_c} \longrightarrow S.R. = \frac{I_A (2\pi f_t)}{g_{m1}}$$

During slew-rate limiting, v_N may depart form v_P (input stage saturation).

Three different ways of improving S.R. :

(1) Increasing fT (reducing Cc)

(2) Reducing gm

(3) Increasing IA