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Control of the Common-Mode Component in CMOS Continuous-Time Fully Differential Signal Processing

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Abstract. A general description of fully differential (FD) amplifiers with common-mode feedback (CMFB) network is carried out in this article. The general requirements that any CMFB loop must satisfy allow us to deduce three suitable figures of merit (linear interaction or conversion gain, relative performances and nonlinear interaction between the common-mode and differential-mode loops) in order to compare the different approaches. The gain or transconductance, sensitivity to mismatching in the devices, and nonlinearity for every common-mode (CM) signal detector block have been derived. By identifying all the input-output signal paths in a generic FD amplifier with CMFB, the conversion signals are quantified. From the gain of the detector and the technique used for injecting back the CM correction signal, the performances provided by the CMFB loops in regard to the differential-mode counterpart are evaluated. From the CM signal detector nonlinearity, it is shown how the CM loop impacts on the distortion (nonlinear interaction) on the amplifier. Finally, all the considerations are verified by means of simulations, and the CMFB networks classified according to these figures of merit. A low-distortion CMBF loop based on the current steering principle of injection is proposed as well.

1. Introduction

Higher integration levels and speeds of operation, along with a decreased power consumption, are the most outstanding profits obtained by the digital design from the continued and fast scaling of CMOS VLSI technologies. However, it impacts on the performance of analog blocks in a very different way. A degradated output conductance, as well as a reduced dynamic range, are the most remarkable consequences of this scaling. The first one, which is due to channel length modulation in MOS transistors, causes low figures of small-signal output resistance and hence, very low dc gains. The latter one arises as a consequence of the more and more reduced total supply voltage that, dictated by fabrication processes, ICs can sustain. For that reason, analog blocks must now operate over a much higher portion of the total power supply voltage, to maintain the same signal-to-noise ratio as in technologies with higher channel lengths. In order to cancel the above effects, new techniques are being incorporated by analog designers. Thus, very recently [1] a feedback cascode biasing has been proposed which provides very high dc gain even in submicron technologies. In regard to the continued low supply voltage supported, one of the standard techniques to extend the dynamic range of analog blocks is to use FD signal processing. A cancellation of even harmonics, even under the presence of the unavoidable mismatching in the devices, as well as the suppression of all undesirable common-mode signals by the differential circuitry, improves over one order of magnitude the signal-to-noise in FD circuits with regard to the single-ended counterparts. These undesirable signals can be generated either by analog blocks or analog and digital blocks as in the case of mixed-mode circuits.

From a design point of view, the only conceptual difference between double- and single-ended signal processing resides, indeed, in the extra feedback required to control the output common-mode component in FD amplifiers. This need arises from the fact that feedback around the amplifier just provides stabilization for the output differential-mode (DM) component, while the common-mode (CM) is still operating in open-loop mode. The required control of the output amplifier CM component must be provided by an additional internal feedback network which is known as common-mode feedback (CMFB) network. For that reason, an FD

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amplifier may be considered as two merged amplifiers for all practical purposes. In general, a CMFB network must satisfy the following requirements:

1. To set the output CM component at a preset dc reference level (V_{ref}), which is usually where the DM gain reaches a maximum value and/or the maximum symmetric voltage (or current) swing is obtained
2. To process the CM component with a speed and accuracy similar to the ones which the DM component is processed by the FD amplifier
3. To minimize the interaction of the processing of the CM output component in the DM output component, and vice versa

Traditionally, not enough attention has been paid to the design of CMFB networks for FD amplifiers. In most textbooks and papers on analog IC design, DM feedback loops are studied much more deeply than their CM counterparts. In them, it is a very common practice only to point out the need of controlling the CM behavior in FD amplifiers and show one of the possible ways to do it, for which most of the time an identical CM loop structure is used and, of course, no practical design consideration is given in regard to its very limited performance. Thus, a general treatment on CMFB loops would be very useful to compensate this lack. Here, this task is tried. In particular, a general description of a linearized FD amplifier with CMFB is made in Section 2. There, nonidealities have had to be included in order to find out the different input-output signal paths, derive the expression of the effective gain associated to each of them and so, evaluate the *linear interaction* or conversion gains between the CM and DM loops. In Section 3, the gain or transconductance, sensitivity to mismatching in the components, and nonlinearity are determined for every CM signal detector in CMOS technology. Furthermore it is shown how the last parameter impacts on the total harmonic distortion (THD) of the system, and as a consequence, the excess of the distortion can be used to measure the *nonlinear interaction* between CM and DM amplifiers. All the possible ways of merging both amplifiers (loops), as well as the *relative performance* provided (gains and gain-bandwidths ratio) by each strategy, are described in Section 4. These three magnitudes constitute suitable figures of merit to compare the different approaches existing to control the CM component in FD amplifiers, because they indicate the degree of fulfillment of the requirements listed above for any CMFB network. In Section 5, all considerations are verified by means of simulations in a case study, a ranking of CMFB networks is established, and a low-distortion CM loop based on the current steering principle is proposed.

2. Signal Paths in Fully Differential Amplifiers

FD amplifiers are commonly considered as merged amplifiers. The signal to be processed, which consists of the DM component of two signals, is the input signal of one amplifier. The second amplifier, which is part of the CMFB network, must control the CM component of the output signals. In order to satisfy the requirement 2, both amplifiers are usually merged at the very front-end, in such a way that most of the signal paths are shared from the very beginning. Below, these amplifiers will be termed as *ampl* and *amp2* respectively.

Figure 1 illustrates a general block diagram of an FD amplifier with CM feedback [2]. The inputs *inl+* and *inl−* are the input terminals of the amplifier *ampl*. In the feedback path, a CM signal detector appears. Ideally, the detector provides a voltage or current proportional to the common-mode component of output signals V_o^+ and V_o^-. In this case, it is assumed that its output signal is a voltage V_s, yet, as we can observe below, no substantial modification is introduced in the context of this work if the output of CM detector were a current I_s. Following the feedback path (figure 1), the output voltage (V_s) of the CM signal detector is compared to the dc reference voltage V_{ref} to which the amplifier CM output component wants to be set. For that reason both signals are applied to the input terminals (*in2+* and *in2−* respectively) of the second amplifier *amp2*, which close the loop that provides the required stabilization in the output CM component. To avoid conversion signal from output DM component to CM component, and vice versa, besides the only linear

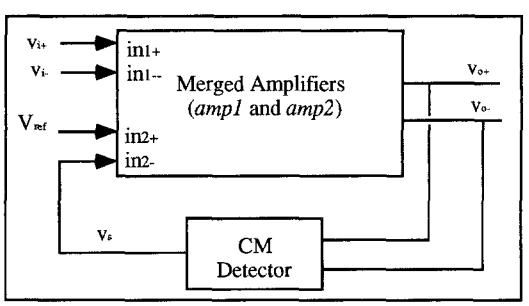


Fig. 1. Block diagram of an FD amplifier with CM feedback.

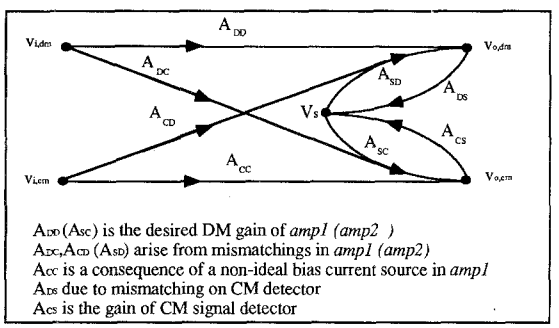
dependence of V_s with the CM component, the paths from the inputs *in2+* and *in2−* to the outputs V_o^+ and V_o^- must be identical. As can be observed below, the comparison with the reference voltage is usually carried out in its own detector in current output CM signal detectors. Then, the secondary inputs (*in2+* and *in2−*) are also input terminals of the CM detector block.

In order to visualize all different signal paths existing in any FD amplifier, nonidealities must be included. Thus, mismatchings in amplifiers *ampl* and *amp2* are next considered. These mismatchings cause different gains from the inputs to the outputs V_o^+ and V_o^- respectively. Moreover and from a general point of view, the small-signal output v_s of CM detector can be expressed as

$$v_s = \alpha_1 v_{o,cm} + \alpha_2 v_{o,dm} + \alpha_3 v_{o,dm}^2 \qquad (1)$$

where the first term, $\alpha_1 v_{o,cm}$, would be the only output if the CM signal detector were ideal, the term proportional to the DM output component, $\alpha_2 v_{o,dm}$, arises as a consequence of the unavoidable mismatches in the CM sense components, and the last and nonlinear term, $\alpha_3 v_{o,dm}^2$, appears due to nonlinear *I-V* characteristic of MOS transistors. Of course, other higher terms are involved but in general, they can be considered as second-order terms.

To facilitate the calculations, a perfect linear ($\alpha_3 = 0$) and nonmatched ($\alpha_2 \neq 0$) CM signal detector block will be firstly considered, and later, in the next section, the opposite case. The flow graph of figure 2 shows all the gain paths as well as the physical origin of them. We must realize that the coefficients α_1 and α_2 are renamed A_{CS} and A_{DS} respectively in this linearized system. Also, the input and output amplifier voltages have been represented by their respective CM and DM components. Two different feedback loops can be identified in figure 2. The loop between v_s and $v_{o,cm}$ is the CM loop and has a gain $LG_{CM} = A_{SC}A_{CS}$. The second loop affects the DM output component and of course it tends to reduce the differential gain A_{DD}. So, this loop can be called internal DM feedback loop, however its gain $LG_{DM} = A_{SD}A_{DS}$ is negligible with regard to LG_{CM}. Note that other DM feedback (external) may exist around the amplifier. Figure 2 also shows the gain paths which originate the conversion signal from CM to DM, and vice versa. Their gains are ($\Delta LG_{CM} = A_{CS}A_{SD}$) and ($\Delta LG_{DM} = A_{DS}A_{SC}$), respectively.



A_{DD} (A_{SC}) is the desired DM gain of *ampl (amp2)*
A_{DC}, A_{CD} (A_{SD}) arise from mismatchings in *ampl (amp2)*
A_{CC} is a consequence of a non-ideal bias current source in *ampl*
A_{DS} due to mismatching on CM detector
A_{CS} is the gain of CM signal detector

Fig. 2. Gain paths in FD amplifiers.

By means of Mason's rule, the effective gains, which are denoted by an upper asterisk, can be derived by inspection from the flow graph of figure 2, resulting in

$$A_{DD}^* = \frac{A_{DD}(1-\mathrm{LG_{CM}}) + A_{DC}\Delta LG_{CM}}{D} \cong A_{DD} \qquad (2a)$$

$$A_{CD}^* = \frac{A_{CD}(1-LG_{CM}) + A_{CC}\Delta LG_{CM}}{D} \cong A_{CD} \qquad (2b)$$

$$A_{DC}^* = \frac{A_{DC}(1-LG_{DM}) + A_{DD}\Delta LG_{DM}}{D} \cong -A_{DD}\frac{A_{DS}}{A_{CS}} \qquad (2c)$$

$$A_{CC}^* = \frac{A_{CC}(1-LG_{DM}) + A_{CD}\Delta LG_{DM}}{D} \cong -A_{CD}\frac{A_{DS}}{A_{CS}} \cong 0 \qquad (2d)$$

where $D = 1 - LG_{CM} - LG_{DM}$. The approximations have been done taking into account the order of magnitude of the gains as a consequence of their physical origin. Every loop in figure 2 has been assumed stable and the sign of the gains included in their symbols.

Some remarkable conclusions can be deduced from the above set of expressions:

The effective open-loop DM gain A_{DD}^* is nearly equal to A_{DD}.

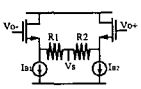
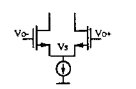
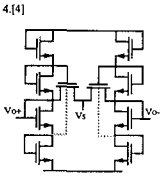
For typical values, the impact of CMFB loop on the amplifier CMRR is not significant since $CMRR^* = A_{DD}^*/A_{CD}^* \cong CMRR$.

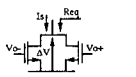
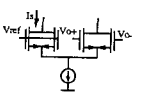
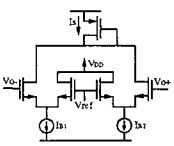
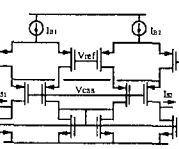
However, mismatching on the CM detector can lead to appreciable DM–CM conversion gain (A_{DC}^*), mainly for high α_2/α_1 and A_{DD} values. Hence, we denominate conversion-gain factor to the ratio α_2/α_1.

3. Common-Mode Signal Detectors in CMOS Technology

The CM signal detector most often used in CMOS technology are shown in Table 1. Their gain or transconductance ($\alpha_1 = A_{CS}$), conversion signal ($\alpha_2 = A_{DS}$),

Table 1. CM signal detectors in CMOS technology.

CM DETECTOR	PERFORMANCE	OBSERVATIONS
1. 	$\alpha_1 = 1$ $\alpha_2 = \frac{\Delta R}{4R}$ $\alpha_3 = 0$	• Linearity in itself • For practical IC resistor values, amplifier DM gain is greatly reduced • Amplifier need to be buffered
2. 	$\alpha_1 = 1$ $\alpha_2 = \frac{\Delta R}{4R} + \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\frac{\Delta R}{2R} + \frac{\Delta I_B}{4I_B} + \frac{\Delta\beta}{4\beta}}{2R + \sqrt{\frac{2}{\beta I_B}}} + \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{\Delta V_T + \frac{\Delta I_B}{2I_B}\sqrt{\frac{2I_B}{\beta}}}{I_B\left(2R + \sqrt{\frac{2}{\beta I_B}}\right)}$ $\alpha_3 = \frac{1}{2I_B} \cdot \frac{1}{\sqrt{8\beta I_B}} \cdot \frac{1}{\left(2R + \sqrt{\frac{2}{\beta I_B}}\right)^2}$	• High DC offset due to source followers • Other buffers can be used to reduce the DC offset • Mismatching between the passive resistors is the dominant error in α_2
3. 	$\alpha_1 = 1$ $\alpha_2 = \frac{\Delta\beta}{4\beta} + \frac{\Delta V_T}{4} \cdot \sqrt{\frac{\beta}{I_B}}$ $\alpha_3 = \frac{1}{8}\sqrt{\frac{\beta}{I_B}}$	• High DC offset • Highly non-linear CM signal detector
4.[4] 	$\alpha_1 = \frac{3}{4} + \frac{\Delta\beta}{8\beta}$ $\alpha_2 = \frac{\Delta\beta}{8\beta}$ $\alpha_3 \cong 0$	• Can reduce considerably the amplifier DM gain due to loading effects • Unless otherwise indicated, every transistor resides in its own well • Bulk modulation has not been considered in the calculations • Very linear structure

CM DETECTOR	PERFORMANCE	OBSERVATIONS
5.[5] 	$\alpha_1 = 2\beta \cdot \Delta V$ $\alpha_2 = \frac{\Delta\beta}{2} \cdot \Delta V$ $\alpha_3 = 0$	• Transistors act in linear region as voltage controlled resistors • R_{eq} is proportional to $V_{x,cm}$ • Mobility modulation effects cause a nonlinear coefficient α_3 [6]
6. 	$\alpha_1 = \sqrt{\frac{\beta I_B}{2}}$ $\alpha_2 \cong \frac{\Delta\beta}{4}\sqrt{\frac{I_B}{2\beta}} + \frac{\beta}{2} \cdot \Delta V_T$ $\alpha_3 \cong \frac{\beta}{16}$	• V_{ref} is the reference voltage for the output CM component • High non-linearity • Other important non-linear terms exist $\frac{3\beta}{16}(V_o^2 + V_o^2)$
7.[7] 	$\alpha_1 = \sqrt{\beta I_B} + \frac{\beta \cdot \Delta V_T}{4} + \frac{\Delta\beta}{2}\sqrt{\frac{I_B}{\beta}}$ $\alpha_2 \cong \frac{\Delta I_B}{8} \cdot \sqrt{\frac{\beta}{I_B}}$ $\alpha_3 \cong 0$	• Good transconductance • Linearity in regard to $v_{o,dm}$, but other non-linearities exist
8.[9] 	$\alpha_1 = \sqrt{\beta I_B}\left(1 + \frac{\Delta\beta}{2\beta}\right)$ $\alpha_2 = \frac{1}{2}\sqrt{\beta I_B} \cdot \frac{\Delta I_B}{4I_B}$ $\alpha_3 = 0$	• These coefficients are for the CM part of I_{o1} and I_{o2} • Check I_{o1}-I_{o2} as a function of $v_{o,dm}$

and nonlinearity (α_3) have been determined for each configuration under the presence of local variations (mismatches) between transistor magnitudes or components. Concretely, relative variations in threshold voltages (V_T) and transconductance parameters (β) are considered. Local V_T variations come from different charge quantities (oxide charge and depletion charge) and nonuniform gate oxide thickness and substrate doping. Local β variations account for variations in carrier mobility, aspect ratios (W/L), and gate oxide capacitance per unit area as well. For transistors operating in their triode region (high $V_{GS} - V_T$ values), mismatches in β may be more important than the threshold voltage counterparts, yet local V_T variations can be the dominant ones in transistors with low gate-source voltage (saturation zone). Usually, bias current mismatches are separately taken into account since they also depend on the dc point [3]. All these variations ($\Delta\beta$, ΔV_T, and ΔI_B) have been simultaneously considered in the derivation of coefficients α for each CM signal detector. Second-order effects in MOS transistors, such as mobility reduction and channel length modulation, have been neglected in the calculations.

As a figure of merit that provides some idea about the impact of CM signal detector nonlinearity on the performance of FD amplifiers, the THD of the differential output signals can be chosen. To simplify the calculations, now, a perfect matched ($\alpha_2 = 0$) and nonlinear ($\alpha_3 \neq 0$) CM signal detector, along with a purely linear DM feedback around the amplifier (figure 3), is studied. From these premises along with figure 3, the following set of equations can be written:

$$v_{o,dm} = A_{DD}gv_{i,dm} - A_{DD}fv_{o,dm} + A_{SD}v_S \tag{3a}$$

$$v_{o,cm} = A_{DC}gv_{i,dm} - A_{DC}fv_{o,dm} + A_{SC}v_S \tag{3b}$$

$$v_S = A_{CS}v_{o,cm} + \alpha_3 v_{o,dm}^2 \tag{3c}$$

where g and f are the feedforward and feedback factors respectively.

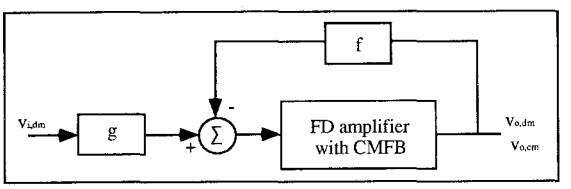


Fig. 3. Block diagram to determine the impact of α_3 on THD.

By solving the DM output signal $v_{o,dm}$ from the above set of equations (3), and carrying out an analysis of distortion on it [10], the following distortions on the second and third harmonic of $v_{o,dm}$ result:

$$HD_2 \cong \frac{1}{2}\frac{\alpha_3 A_{SD} A_{CL}}{LG_{CM} LG_{DM,ex}} V_i \quad (4a)$$

$$HD_3 \cong \frac{1}{2}\frac{\alpha_3^2 A_{SD}^2 A_{CL}^2}{LG_{CM}^2 LG_{DM,ex}^2} V_i^2 \quad (4b)$$

where $A_{CL} = g/f$ is the closed-loop gain, $LG_{DM,ex}$ is the gain of the DM feedback loop around the amplifier which equals to fA_{DD}, and V_i is the amplitude of the input signal ($v_{i,dm} = V_i \cos \omega t$). Needless to say, it is rather difficult to predict the harmonic distortions from (4) in an accurate way. However, as will be shown below, they are enough to provide a good idea about the relative impact on the amplifier distortion caused by the nonlinearity of different CMFB loops.

4. Injection of the Common-Mode Correction Signal

Relying on the output magnitude proportional to $v_{o,cm}$ provided by the CM detector, different ways exist for injecting the CM correction signal into the amplifier, or in other words, different ways of merging amplifiers *ampl* and *amp2* (figure 1). Each of them, along with a particular sense circuit of table 1, will provide a gain and gain-bandwidth with a determined order of magnitudes. Recall that for most of the applications, minimum design specifications for CM loops usually are

$$LG_{CM} \cong LG_{DM,ex} \quad (5a)$$

$$LGBW_{CM} \cong LGBW_{DM,ex} \quad (5b)$$

where LG_{CM} and $LG_{DM,ex}$ were defined above, and $LGBW_{CM}$ and $LGBW_{DM,ex} = fGBW_{DM,ex}$ are the loop gain-bandwidth products of CM and external DM loops respectively. Note that low values of feedback factor f relax the requirements a bit of CM loop in order to satisfy (5) since, as has been pointed out, this external feedback only affects the DM operation.

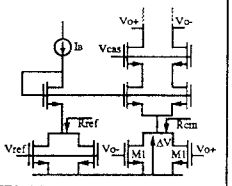
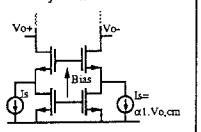
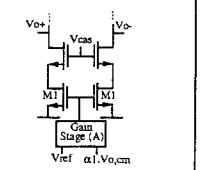
Table 2 illustrates the different possibilities of merging CM and DM amplifiers. Their relative performances (CM to DM behavior) are also shown for each strategy assuming that they are one-stage output compensated amplifiers. In regard to the resistive source degeneration technique shown in table 2, the symbols R_{ref} and R_{cm} indicate the equivalent resistance seen from the drain of common-drain transistors which degenerate the input and output branches of the current mirrors respectively. So, it can be easily demonstrated that they are given by the expressions:

$$R_{ref}^{-1} = 2\beta\, V_{ref} - 2\beta\, V_T \quad (6a)$$

$$R_{cm}^{-1} = 2\beta_1\, V_{o,cm} - 2\beta_1\, V_T \quad (6b)$$

which agrees with the coefficient α_1 of the CM signal detector 5 shown in table 1.

Table 2. Different modes to inject the CM correction signal in FD amplifiers.

STRUCTURE	PERFORMANCE $\frac{A_{CM}}{A_{DM}} = \frac{GBW_{CM}}{GBW_{DM}}$	OBSERVATIONS
1. Resistive source degeneration of current mirrors 	$\frac{\beta_1 \Delta V}{\beta_{in}(V_{GS}-V_T)_{in}}$	• $g_m=\beta_{in}(V_{GS}-V_T)_{in}$ is the transconductance of the DM amplifier • Low $g_{m1}=\beta_1 \Delta V$ due to operation of M_1 in their resistive mode • Very insufficient $A_{CM}(<<A_{DM})$ and $GBW_{CM}(<<GBW_{DM})$ • Configuration 5 (Table I) is used
2. Currents injection 	$\frac{\alpha_1}{\beta_{in}(V_{GS}-V_T)_{in}}$	• The same performance can easily be achieved in *CM* and *DM* loops • Configurations 6, 7, 8 (Table I) can be used
3. Current steering 	$\frac{\alpha_1 A g_{m1}}{\beta_{in}(V_{GS}-V_T)_{in}}$	• May cause instability in the *CM* loop. Check $\phi_{m,cm}$ • Configurations 1,2,3,4 (Table I) along with a gain stage are appropriate for it • Configurations 6, 7 (Table I) can be also appropriate with a suitable load

5. A Case Study

In order to verify the above design considerations and trade-offs, a practical case study follows. To carry it out, the CM output component of an FD amplifier has been successively controlled by each CMFB network here presented, and then their simulated performances compared with regard to the following figures of merit: effective conversion gain (A_{DC}^*) or linear interaction between DM and CM loops, relative performance CM-to-DM (A_{CM}/A_{DM}), and harmonic distortion (THD) or nonlinear interaction between DM and CM loops.

Figure 4 shows an FD high-performance folded-cascode amplifier without CMFB. This amplifier was designed to satisfy the following specifications: $\{A_o$, *GBW*, *SR*, $\phi_m\} \geq \{70$ dB, 5 MHz, 8 V/μs, 70 deg$\}$ with 6 pF and 5 V of load capacitances and total supply voltage respectively. Obviously, these specifications refer to amplifier DM behavior. According to (5) every CM loop has been also designed trying to provide a gain and gain-bandwidth product roughly equal to the DM counterparts.

In order to characterize the effective conversion gain A_{DC}^*, the mean value, standard deviation (σ), and worst-case (*WC*) value have been obtained from Monte Carlo analysis. Such analysis has been performed on

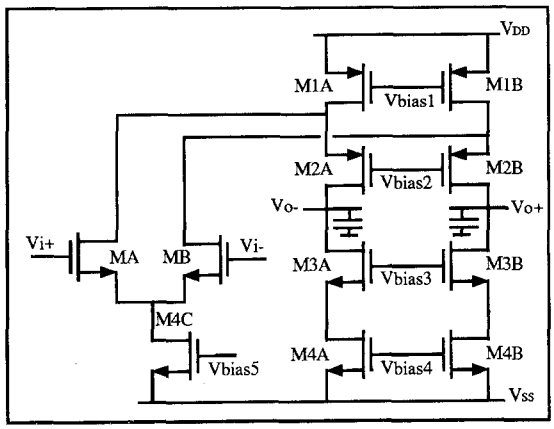


Fig. 4. An FD folded-cascode amplifier without CMFB.

75 trials with $\Delta\beta$ and ΔV_T spreads of 1% and 5 mV respectively. These parameters were randomly and uncorrelately varied in all the transistors. Other 1% relative variations between passive resistors were also included where required. Observe that mismatches between bias currents have not been specifically introduced, but they were automatically generated in the simulations from the other kinds of local variations. With regard to the figures of merits A_{CM}/A_{DM} and THD, perfect matched systems were assumed. All the simulated results have been obtained with SPICE in its level 2, by using the process parameters of a standard CMOS technology with 2 μm feature size. Below, these results are shown along with the particular structures of the CMFB loops, which were connected to the folded-cascode amplifier of figure 4.

5.1. CM Control by Resistive Source Degeneration Technique

Table 3 shows the folded-cascode amplifier performance when its output CM component is controlled by degeneration of current mirrors with active resistors. Indeed, the most remarkable lack of this very common technique resides on the low figures achieved for A_{CM} and GBW_{CM}. As a consequence of this slow and inaccurate CM control, a very asymmetrical output swing respect to the reference level V_{ref} will be obtained, which can lead to premature saturation of one of the output nodes in some applications. As indicated in (2c), the conversion-gain factor, in this case $\Delta\beta/4\beta$, along with the gain A_{DD} provides a theoretical worst-case A^*_{DC} value (WC_{theo}) of 17.9 dB. The discrepancy between WC_{theo} and the simulated WC value (23.6 dB) arises due to the loss of accuracy in the approximations done in (2c) as a consequence of the very low gain in this particular CMFB loop.

5.2. CM Control by Current Injection

The performance parameters of the amplifier when two injected currents act as controlling signal of the CM output component, are shown in table 4. To accomplish more realistic comparison among the impacts on the amplifier originated by CM loops, the dc currents in the folded-cascode amplifier were always kept constant. Thus, in CMFB networks based on the principle of the injection of currents, before the injection, dc currents were subtracted in order to maintain roughly the same $V_{GS} - V_T$ voltage in amplifier transistors as with CM loops based on different principles of operation. Comparing it with the performance provided by resistive source degeneration technique, it can be said that higher WC_{theo} values of DM loops with CM loops based on current injection are obtained. Concretely, for the CMFB structure 4.1, the resulting conversion-gain factor $\Delta\beta/4\beta + \Delta V_T/V_{DSat}$ accounts for the increase in the simulated WC and provides a WC_{theo} value of 32.7 dB. This factor for networks 4.2 and 4.3 can be approximately rewritten as

$$\frac{\Delta I_B}{8I_B} \cong \frac{\Delta\beta}{8\beta} + \frac{\Delta V_T}{4V_{DSat}} \tag{7}$$

which also demonstrates the higher sensitivity to mismatches in the components of these structures. However,

Table 3. Amplifier performance with CM control by source degeneration of current mirrors.

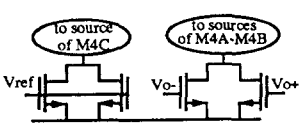
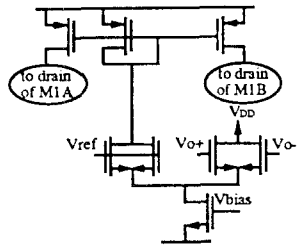
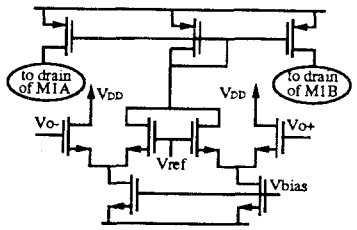
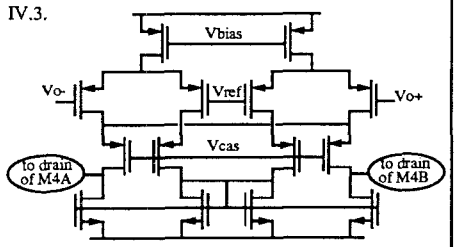
STRUCTURE	A^*_{DC}	$\frac{A_{CM}}{A_{DM}} = \frac{GBW_{CM}}{GBW_{DM}}$	THD ±1V$_{p-p}$ @100KHz
III.1. 	mean=11.5 dB σ=10.9 dB WC=23.6 dB	0.08	0.025 %

Table 4. Amplifier performance with CM control by current injection.

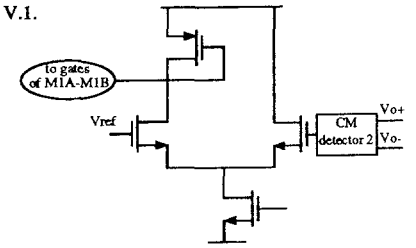
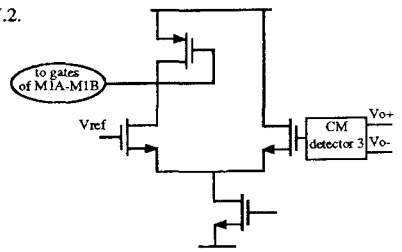
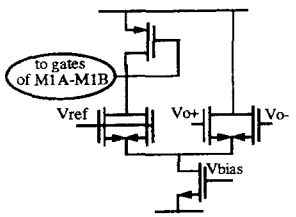
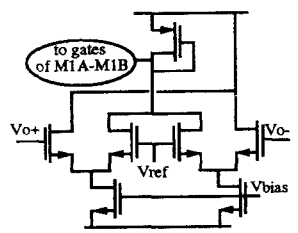
STRUCTURE	A^*_{DC}	$\frac{A_{CM}}{A_{DM}} = \frac{GBW_{CM}}{GBW_{DM}}$	THD $\pm 1V_{r-r}$ @100KHz
IV.1. 	mean=21.6 dB σ=8.9 dB WC=35.3 dB	0.82	0.09 %
IV.2. 	mean=7.2 dB σ=7.1 dB WC=21.7 dB	0.83	0.04 %
IV.3. 	mean=5.5 dB σ=7.8 dB WC=18.5 dB	0.95	0.01 %

much more significant than the characterization of the linear interaction A^*_{DC} between CM and DM loops in FD amplifiers in terms of worst-case values, results, indeed, in terms of their mean value and error distributions. As indicated by the Monte Carlo analysis, in spite of the larger spreads between the best-case and the theoretical worst-case A^*_{DC} values in CMFB loops based on current injection, in practice, these spreads are narrower than in resistive source degeneration loops. This fact is a consequence of the higher numbers of transistors involved in the first ones. Thus, each transistor has a minor impact on the performance of the whole circuit, and therefore, random parameter deviations are averaged out. Concerning the ratio between gains and gain-bandwidths of both loops, current injection technique provides a value close to one as expected from the considerations of table 2. Finally, the linearity of CMFB networks 4.2 and 4.3 ($\alpha_3 \cong 0$) originate a lower nonlinear interaction with the DM amplifier than structure 4.1. Loop 4.1 can improve its linearity by using input devices with lower (*W/L*) ratios, however, their minimum ratios are dictated by the CM requirements.

5.3. CM Control by Current Steering

Table 5 illustrates the amplifier behavior when its CM component is controlled by means of CMFB networks based on the current steering principle. Loops 5.1 and 5.2 incorporate the CM signal detector configuration 2 and 3 of Table 1 respectively. Just to avoid excessive dc shifts, complementary structures of these CM signal detectors were actually used in this particular case. As can be seen in Table 5, CM current steering loops provide similar behavior to DM loops in terms of speed and accuracy, while the nonlinear behavior varies widely from a structure to another. Thus, a high excess of harmonic distortion is generated by the CMFB network 5.2 due to its high nonlinear coefficient, which will be a common characteristic to every loop based

Table 5. Amplifier performance with CM control by current steering.

STRUCTURE	A^*_{DC}	$\frac{A_{CM}}{A_{DM}} = \frac{GBW_{CM}}{GBW_{DM}}$	THD $\pm 1V_{p-p}$ @100KHz
V.1. 	mean=8.2 dB σ=11.1 dB WC=21 dB	1.1	0.05 %
V.2. 	mean=20 dB σ=9.5 dB WC=33 dB	1.2	0.22 %
V.3. 	mean=22.1 dB σ=9.6 dB WC=36.2 dB	1.3	0.06 %
V.4. 	mean=9.4 dB σ=8.5 dB WC=23 dB	1.2	0.015 %

on the detection of the output CM component in the common-source node of a simple differential pair. The optimization of its linearity is limited by the amplifier output swing, A_{CM}, and GBW_{CM} required. CM loop 5.4, which uses the CM detector 7, shows a better nonlinear performance as could be expected from the result of its analysis (Table 1). Regarding the figure of merit A^*_{DC}, it must be noted the wider spread achieved with the configuration 5.1, which, in spite of having a high number of components in its CM detector, its sensitivity (α_2) to local variations is mainly determined by the matching between the passive resistors, and therefore, rather similar standard deviation values result when compared with the CMFB network 3.1. Again, very good agreements are achieved between the figures of theoretical and statistical worst cases in every CM current steering loop.

5.4. A Low-Distortion Current Steering CMFB Network

Sometimes, a current mirror can be seen loading the differential gain stage in current steering CMFB networks [8], [11]. In such a way, one could think in

investing the increase in the CM loop gain to improve the linearity and, therefore, to reduce the nonlinear interaction with the DM loop. However, the resulting configurations are very prone to cause instability in the CM feedback loop as a consequence of the additional low-frequency pole introduced at the output node of the current mirror load, and in general these CMFB networks should be avoided. Based on this idea but overcoming the above drawback, a low-distortion current steering loop is proposed in figure 5. Here, a diode-connected transistor loads the output node of the mirror, and the pole introduced is placed at a frequency given by $g_m/2C_{gs}$ where g_m and C_{gs} are its transconductance and gate-source capacitance respectively. Now, two secondary poles appear in the CM loop. Relying on the minimum CM phase margin, the position of the additional pole can be optimized. Thus, for a minimum CM phase margin equal to the folded-cascode amplifier counterpart, THD was kept below 0.007% for a 2-$V_{p\text{-}p}$ 100-kHz input signal. Of course, similar behavior in terms of gain and bandwidth are achieved with the CMFB loop of figure 5 with respect to the DM loop.

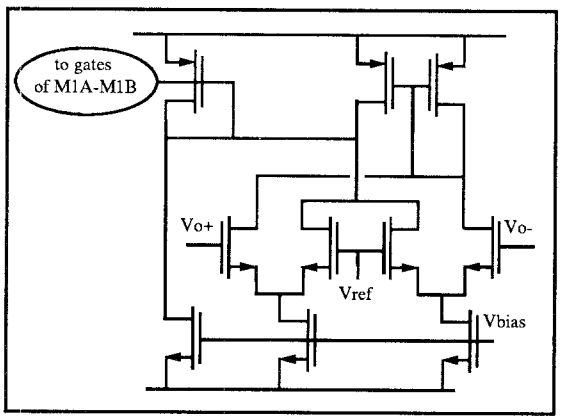


Fig. 5. Low-distortion CM current steering loop.

6. Conclusions

Fully differential signal processing is a more and more used topic. In it, an extra feedback loop (CMFB network), which must have necessarily a continuous-time nature for high frequency applications, is required to "tame" the output CM component of FD amplifiers. Here, an overall sight has been tried to provide the different existing approaches for such purpose. Suitable figures of merit to compare them have been given and used. As a result, CMFB networks illustrated in table 4 (configuration 4.3), and figure 5 showed superior performance. They are based on current injection and current steering principles and operate along with the CM signal detectors 8 and 7 (table 1) respectively. On the other hand, the more often used CM loops, which are based on either resistive degeneration of current mirrors or simple differential pair CM signal detector, provided very insufficient gain and bandwidth and high excess of distortion in the DM output component also respectively.

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References

1. E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuits," *IEEE J. Solid-State Circuits*, Vol. 25, pp. 289–298, 1990.
2. J.F. Duque-Carrillo and P. Van Peteghem, "A general description of common-mode feedback in fully-differential amplifiers," *Proc. IEEE Int. Symp. Circuits and Systems*, 1990, pp. 3209–3212.
3. K.R. Lakshmiknmar, R.A. Hadaway, and M.A. Copeland, "Characterization and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, Vol. 21, pp. 1057–1066, 1986.
4. M. Banu, "Common-mode signal detector," U.S. Patent 4 518 870, May 21, 1985.
5. T. Choi, R.T. Kaneshiro, R.W. Brodersen, P.R. Gray, W.B. Jett, and M. Wilcox, "High-frequency CMOS switched-capacitor filters for communications application," *IEEE J. Solid-State Circuits*, Vol. 18, pp. 652–664, 1983.
6. A. de la Plaza and P. Morlon, "Power-supply rejection in differential switched-capacitor filters," *IEEE J. Solid-State Circuits*, Vol. 19, pp. 912–918, 1984.
7. R.A. Whatly, "Fully differential operational amplifier with DC common-mode feedback," U.S. Patent 4 573 020, Feb. 25, 1986.
8. S.M. Mallya and J.H. Nevin, "Design procedures for a fully-differential folded-cascode CMOS operational amplifier," *IEEE J. Solid-State Circuits*, Vol. 24, pp. 1737–1740, 1989.
9. P.W. Li, M.J. Chin, P.R. Gray, and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, Vol. 19, pp. 828–836, 1984.
10. D.O. Pederson and K. Mayaram, *Analog Integrated Circuits for Communication*, chap. 2, Boston, MA: Kluwer, 1991.
11. E. Sackinger, J. Goette, and W. Guggenbuhl, "A general relationship between amplifier parameters and its application to PSRR improvement," *IEEE Trans. Circuits Systems*, Vol. 38, pp. 1173–1181, 1991.

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