FREQUENCY SYNTHESIZER FOR ON-CHIP TESTING AND AUTOMATED TUNING

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ABSTRACT

This paper presents a compact, phase-locked loop (PLL) based, frequency synthesizer suitable for built-in testing and automatic tuning applications operating in the 100MHz frequency range. Key features of this design include a differential charge pump with common mode feedback (CMFB) and a voltage controlled oscillator (VCO) based on a pseudo-differential OTA with a linear transconductance control and tuning invariant output resistance. Experimental results from an integrated prototype fabricated using standard 0.35µm CMOS technology are presented. The measured HD3 of the output signal is better than -39dB over 80% of the tuning range: 40-160MHz. The circuit occupies a silicon area of $200\times1000\mu m^2$ and operates from a 3.3V power supply.

1. INTRODUCTION

In recent years, the research on frequency synthesizer implementations has focused on wireless applications in the GHz range and clock generators for microprocessors. Various on-chip automatic tuning [1-2] and built-in testing [3] techniques require the generation of stable frequency tones in a range of tenths to few hundreds of MHz. Some recently reported design for testability techniques for analog filters [4] could also be implemented on-chip if a stimulus source in the mentioned frequency range is available. On-chip signal generators based on memory [5], sigma-delta [6] and switched-capacitor [7] techniques have been reported for built-in self test applications. Their frequency range is limited to a few MHz and even though some of them provide a very pure sinusoid [5, 6], not every application can afford the cost in area required by these solutions. The design of frequency synthesizers for the mentioned applications is an open problem addressed by this work. Section 2 describes the design of the proposed PLL and its main building blocks. Section 3 discusses the design of the VCO. Experimental results are presented in section 4.

2. FREQUENCY SYNTHESIZER

The frequency synthesizer is based on a type-II PLL. It is formed by a phase-frequency detector (PFD), a differential charge pump with CMFB, an external differential third order loop filter, a quadrature VCO and a programmable frequency divider, as shown in Figure 1.

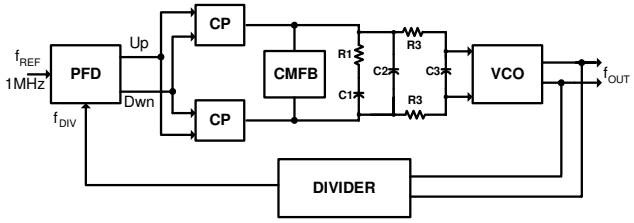

Figure 1. Frequency synthesizer block diagram.

2.1. Charge Pump

The frequency control voltage (V_{CF}) of the VCO is differential; therefore, the charge pump must be differential as well. In this design, two identical single ended charge pumps are used along with a CMFB circuit that fixes the appropriate common mode voltage (CMV) at the input of the VCO. Figure 2 shows the schematic diagram of the charge pump; it is formed by simple current mirrors (M9-M10, M3-M4) switched by differential pairs (M7-M8, M1-M2). The differential pairs are controlled by the Up-Down signals generated in the PFD. This structure has a very slow switching-off speed, since it depends on the time constant of transistor M3 (M1). A slow switching time introduces mismatch errors in the charge pump and degrades the spurious performance of the synthesizer [8].

A current mirror carrying a small current, I_{sm}, is added to nodes V1-V2 to discharge them and turn off the current mirror faster. In this design, the charge pump current I_{cp} = 20µA with I_q=30µA and I_{sm}=10µA. The extra current needed to speed-up the charge pump switching is justifiable due to the improved spurious performance. The small charge pump current provides a large output resistance that further improves the matching of the charge pump.

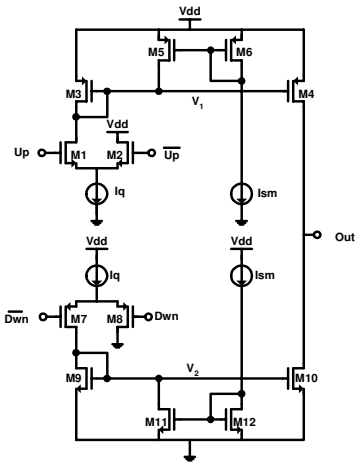

Figure 2. Charge pump schematic

2.2. CMFB

The CMV of the VCO control voltage is set by the CMFB circuit depicted in Figure 3. Differential pairs formed by M1-M4 sense the CMV of the output of the charge pumps (V_n and V_p) and compare it against voltage V_{CM}. A compensation current is injected to M8 and mirrored to M5 and M6. The difference between this current and the biasing current I_{biasCM} is injected back into nodes V_p and V_n to correct the CMV. The differential pairs M1-M4 are linearized by transistors Mn1 and Mn2, respectively to extend the linear range of the common mode detector and match the compliance voltage of the charge pump. The bias current of the common mode feedback I_{biasCM} is limited to 10% of the charge pump current to avoid large compensation currents that overwhelm the information provided by the charge pump to the loop filter.

One concern in the design of the CMFB circuit is the possible increase of the reference spurs due to the correction of the CMV of the VCO control voltage during the narrow current pulses generated by the charge pump at the reference frequency under the lock condition. In order to avoid this problem, switches SW1 and SW2 are used to disable the CMFB circuit once the desired CMV has been reached. Switches SW1 and SW2 are driven by a control circuit (Figure 4) that monitors the CMV. The control signal C_{off} opens the switches SW1-SW2 when the CMV falls within two predetermined limits V_{CMmin} and V_{CMmax} avoiding current injection from the CMFB into the loop filter. If the common mode level of the charge pump drifts and falls out of the limits V_{CMmin} and V_{CMmax}, then switches SW1 and SW2 are closed and the CMFB circuit is enabled. The limits V_{CMmin} and V_{Cmmax} are set by the ratio of the transconductance of M6-M8 and M_b10, approximately 100 mV below and above V_{CM}, respectively.

Two rectifiers formed by transistors M1-M8 constitute the core of the control. The output currents of the common mode detector M9-M10, M11-M12 are rectified in transistors M5-M7 and added. The sum is compared against a reference current provided by M_b10. If the common mode voltage is larger than the specified limits, the current in transistors M6-M8 is larger than the reference and the C_{off} goes to '0' turning SW1-SW2 off.

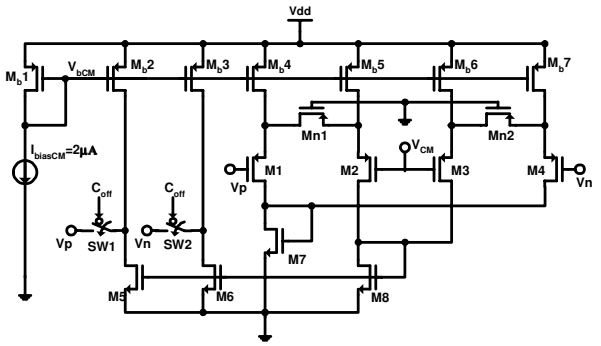

Figure 3. Charge pump common mode feedback schematic.

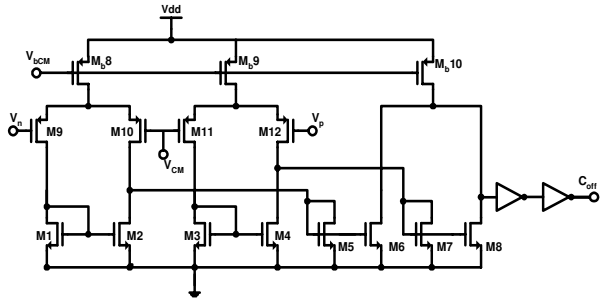

Figure 4. Common mode feedback control.

3. VCO DESIGN

Ring oscillators are preferred in PLLs for clock signal generation due to their simplicity and low power consumption. However, their harmonic distortion is high and their amplitude is fixed; both characteristics are undesirable for the target applications of this PLL. LC-based oscillators have a superior linearity and phase noise performance but their required area can become prohibitively large for frequencies below 1GHz. For signal generation in the range of tenths to few hundreds of MHz, a transconductance-capacitance (OTA-C) oscillator structure [9] offers amplitude control and low distortion in a compact implementation, and hence is chosen for this design. Figure 5 shows a block diagram of the designed differential quadrature oscillator. The oscillation frequency is determined by the ratio $g_m\omega/C$. For this implementation C=400fF.

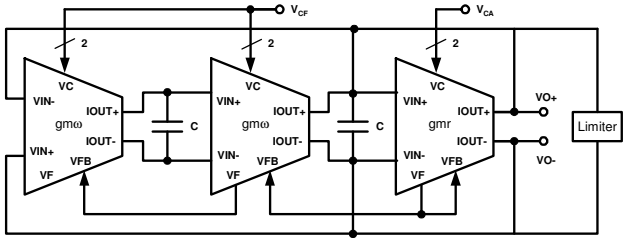

Figure 5. VCO block diagram.

The employed limiting mechanism is simple and assures a low-distortion output; it consists of diode connected transistors. The amplitude of the output signal can be controlled by the negative resistance (1/gmr) through V_{CA}. A linear oscillation frequency (f_{OSC}) Vs. frequency control voltage (V_{CF}) is convenient for the overall PLL performance and attained through the use of OTAs with linear transconductance control. The circuit schematic of the employed OTA is shown in Figure 6. The transconductance operation is carried out by transistors M1 which operate in the linear region. The drain to source voltage (V_{DS}) of these transistors is determined by the differential voltage VC through transistors M2; in this way the effective transconductance is a linear function of VC.

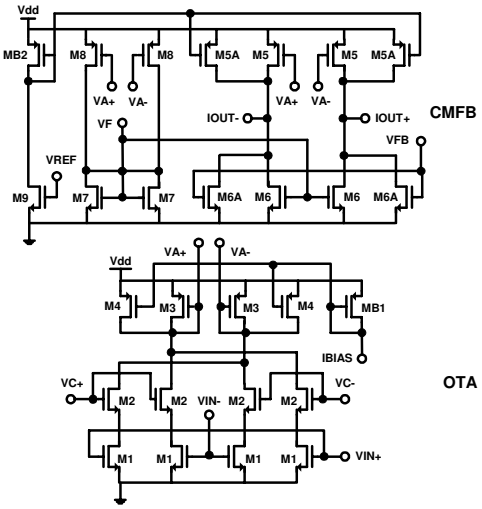

Figure 6. Voltage controlled transconductor schematic.

An inherent CMFB detection mechanism [10] is employed to control the DC level of the output nodes. This mechanism takes advantage of the fact that cascaded OTAs are used in the oscillator architecture. The DC level of the previous OTA is sensed by transistors M1. This DC level will impact the current flowing through transistors M3 and M8. Since transistors M7 are diode connected and their gate terminals attached, only the common mode variations will have an impact on the node VF; this voltage is fed back to the previous OTA. In turn, the following OTA will detect the common mode DC level at the output nodes and will feedback this information through the node VFB. The current flowing through transistors M6A is compared with the current provided by transistors M5A. This current comparison forces VFB (and hence the DC level at the output nodes) to be very close to VREF.

For an OTA-C oscillator, a relatively high output resistance (R_{OUT}) is desired from the OTA. An important disadvantage of the inherent CMFB detection mechanism proposed in [10] is that the addition of transistors M5A and M6A degrades R_{OUT} significantly since they must have the same aspect ratio as the transistors to which they are connected in parallel. This effect worsens when two or more OTAs are be connected to the same node. This R_{OUT} issue is addressed in this design in the following way: First, it should be noted that in the differential current mirror formed by transistors M3 and M5 we are interested in transferring the AC information only. To optimize the frequency response, a multiplying factor of 2 is desired for these current mirrors, which would imply to double the DC current, further degrading R_{OUT}. To avoid this problem, transistors M5A are added. They provide most of the DC current required by the input stage. Transistors M3 are biased by only a small portion of the DC current and, since they are diode connected, copy the AC variations to transistors M5. In this way, the transistors at the output branch are biased with a relatively small DC current that does not depend on the transconductance magnitude. An OTA with a sufficiently high and tuning invariant R_{OUT} is obtained, improving the linearity and tuning range of the VCO.

4. EXPERIMENTAL RESULTS

The proposed frequency synthesizer was fabricated using the TSMC 0.35µm standard CMOS technology. The microphotograph is presented in Figure 7. The synthesizer output spectrum for a frequency of 59MHz is shown in Figure 8. The second harmonic is mainly due to mismatch in the buffers that drive the output pads. As expected, the V_{CF} Vs. F_{OSC} characteristic of the VCO is linear for most of the tuning range as it can be observed in Figure 9. Figure 10 shows the output signal at frequencies in the limits of the operating range. The experimental results are summarized in Table 1.

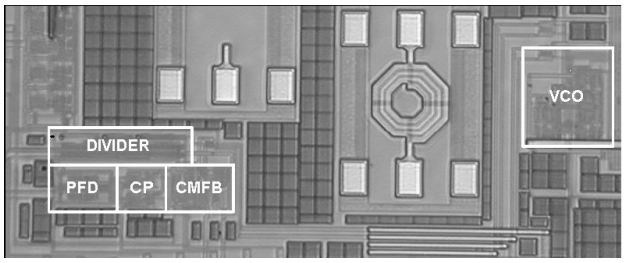

Figure 7. Frequency synthesizer microphotograph.

Synthesizer frequency step	1MHz
HD3 (from 40 to 150MHz)	<-39dB
Tuning range	38 to 167 MHz
Phase noise @1MHz offset	-80dBc/Hz
Current consumption	22mA
Voltage supply	3.3V
Active area	200×1000 μm^2

Table 1. Summary of experimental results

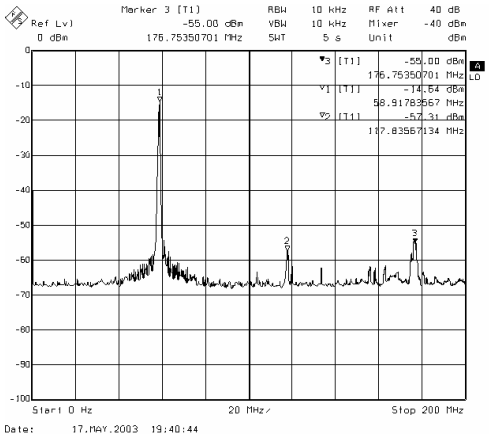

Figure 8. Output spectrum.

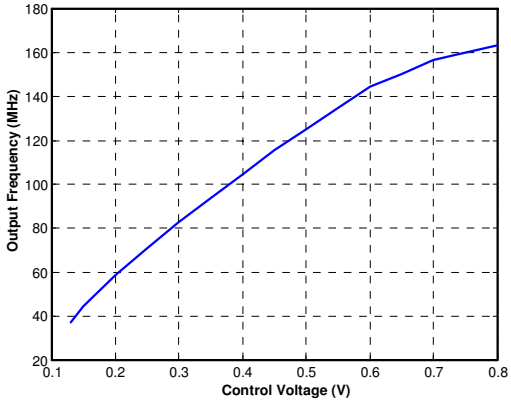

Figure 9. Measured VCO tuning range.

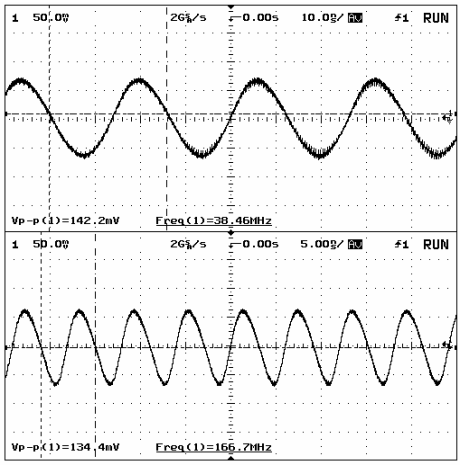

Figure 10. Transient output of quadrature oscillator.

5. CONCLUSION

A frequency synthesizer that is suitable for a variety of automated tuning and built-in testing techniques has been successfully implemented in standard CMOS 0.35µm technology. Experimental results support the feasibility of the proposed design. Various circuit-level design features, such as a CMFB for a differential charge pump and a pseudo differential OTA with linear transconductance control and tuning invariant output resistance have been developed to yield a low distortion and wide tuning range on-chip signal generator.

6. ACKNOWLEDGMENTS

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11. REFERENCES

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