ECEN 665 (ESS)

Radio Frequency Filters

Material courtesy of Fikret Dülger,

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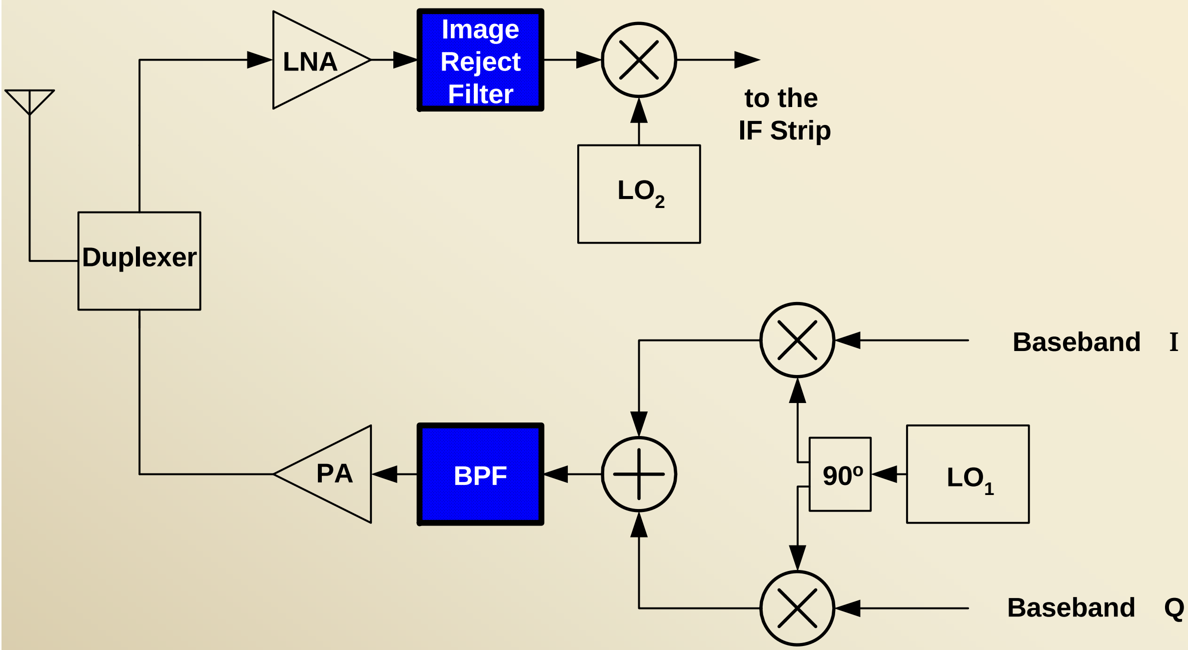
Outline

- Problem Definition, Motivations and Research Goal
- A Fully-Integrated Q-Enhancement LC Bandpass Filter
  - Noise Analysis
  - Nonlinearity Analysis
  - IC Measurements of the Filter in 0.35μm CMOS
- Comparison with previous reported filters and Conclusions

Problem Definition and Motivations

- Wireless Communication systems have become an important part of our daily lives.
- The demand towards lower cost makes the task of circuit designers more and more challenging.
- This translates into the circuit specifications with lower power consumption, smaller die area but without any compromise from higher performance .

Problem Definition and Motivations

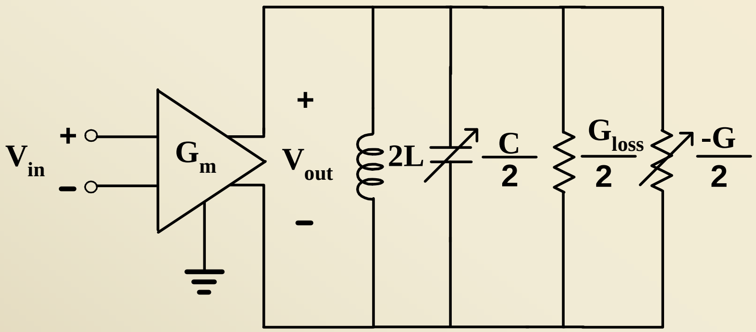


- Transceiver front-ends are the sections next to the antenna.
- Frequency range of interest is from 900 MHz to 2.4 GHz.
- In state-of-the-art solutions, the bandpass filters are off-chip.
- MOTIVATION FOR INTEGRATION!

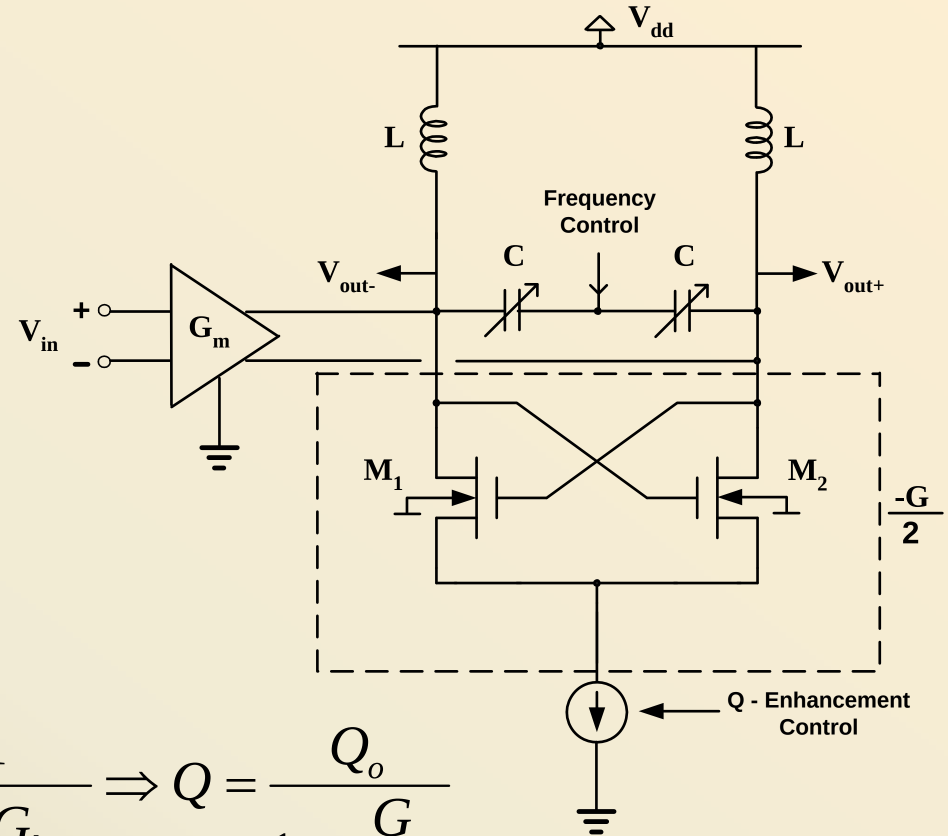
Research Goal

- The feasibility of a Q-enhanced bandpass filter designed with a standard (low cost) CMOS technology at 2 GHz is investigated.
  - The issue is addressed through the simulations, analyses, and the experimental verification of a prototype designed and fabricated in a 0.35μm CMOS technology.

Q-Enhancement Bandpass Filters



(a)



(b)

$$Q_o \equiv \frac{1}{\omega_o L G_{loss}} \Rightarrow Q = \frac{Q_o}{1 - \dfrac{G}{G_{loss}}}$$

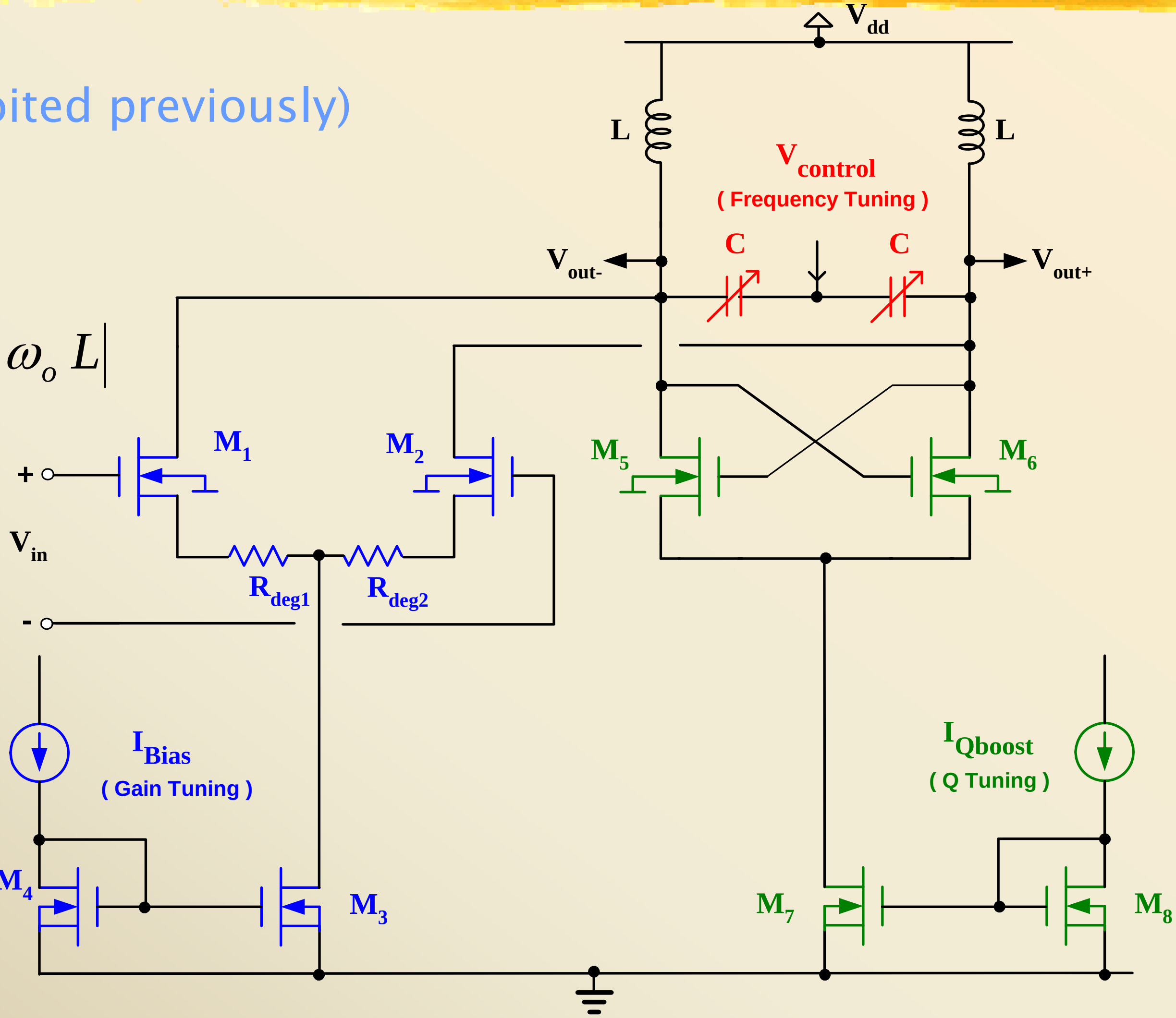
$$(G_{loss} > G \quad for\ stability)$$

A CMOS Programmable RF Bandpass Filter

Programmable in:
- Peak Gain (not exploited previously)
- Filter Q
- Center Frequency

$$|H(j\omega_o)| \cong |G_m(j\omega_o)Q\omega_o L|$$

$$\omega_o \cong \frac{1}{\sqrt{LC}}$$



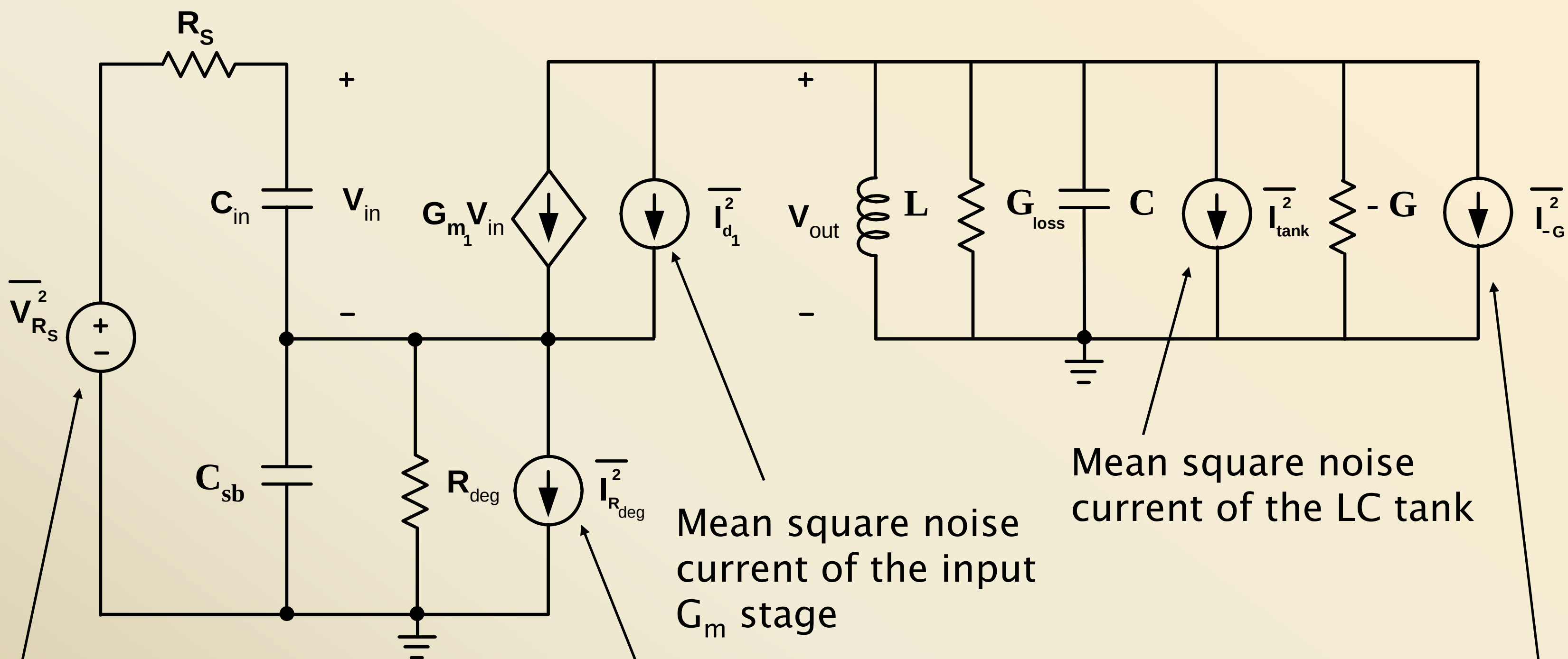
A CMOS Programmable Bandpass Filter

- The peak gain programmability through the input G_m stage.

$$\left|H(j\omega_o)\right| \cong \left|\frac{G_m(j\omega_o)}{G_{loss}-G}\right| = \left|G_m(j\omega_o)Q\,\omega_o\,L\right|$$

- Increasing Q also increases the peak gain.
- If ω_o and Q are fixed, the peak gain can be modified through G_m.

Noise Analysis



Mean square noise current of the input G_m stage

Mean square noise current of the LC tank

Mean square noise voltage of the source resistance

Mean square noise current of the source degeneration resistor

Mean square noise current of the negative conductance generator

Noise Analysis (contd.)

- The noise factor at ω_o is obtained as

$$F = 1 + \frac{\boxed{8kTG_{loss} + 2\overline{I^2_{-G}}} + 2\overline{I^2_{R_{\deg}}}\, G^2_{m1} \left| Z_{S_{in}}(j\omega_o) \right|^2}{4kTR_S G_m^2} + \frac{2\overline{I^2_{d_{in}}}}{4kTR_S G^2_{m1}}$$

- The calculations yield the following percentage contributions from the components:

  LC Tank: 44.5%, –G: 38%, Input G_m: 13.5%, R_{deg}: 2.7%

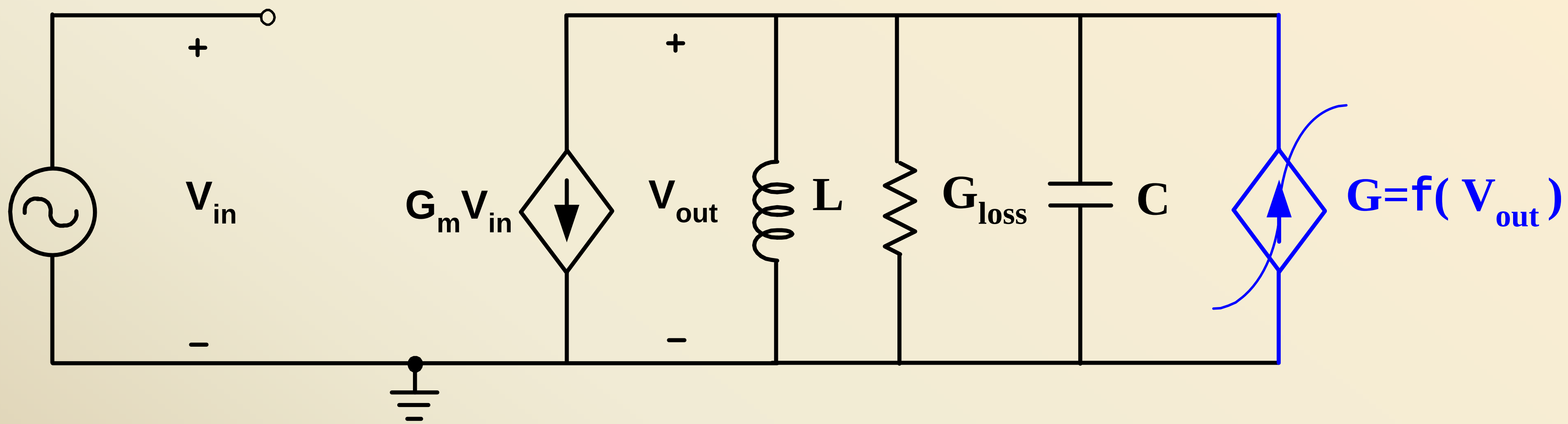
- Increasing G_m reduces the contribution of -G and the LC tank

Nonlinearity Analysis

- There are three main nonlinearity contributors:
  - the negative conductance generator
  - the varactor
  - the input G_m stage
- The analyses consider each contributor separately!
- Isolating each contributor allows us to identify the design trade-offs involved.

Nonlinearity Analysis (contd.)

Contribution of the Negative Conductance Generator



- The nonlinear behavior of the Negative Conductance is isolated first.

- We use the method proposed by Wambacq/Sansen in “Distortion Analysis of Analog Integrated Circuits”.

Noise-linearity, Q-selectivity-linearity trade-offs !

- The 1dB compression point is approximated as:

$$V_{1dB} \cong \sqrt{\frac{2.32 \times g_{m_5}}{\left(2K_2^2 + \dfrac{K_2 \theta_5 g_{m_5}}{1+\theta_5\left(V_{GS5} - V_{T5}\right)}\right)} \left(\boxed{\frac{1}{G_m^2 Q^3 \omega_o^3 L^3}}\right)}$$

$$K_2 \cong \frac{\mu_o C_{OX}}{2}\left(\frac{W_5}{L_5}\right)\left(\frac{1}{\left(1+\theta\left(V_{GS5} - V_{T5}\right)\right)^3}\right)$$

- The effective bias of the negative conductance should be maximized
- With a higher Q_o, a lower g_{m5} is required: higher eff. bias with given I_{ss}.
- The higher the peak gain, $G_m Q \omega_o L$, the worse the linearity.

Nonlinearity Contribution of the Varactor

$$V_{1dB} \cong \sqrt{\frac{1.55}{\boxed{G_m^2 Q^3 \omega_o^3 L^3}} \times \frac{\left| \frac{1}{j2\omega_o L} + G_{loss} + j2\omega_o (C + C_{Vo}) \right|}{\left| -\frac{K_{3_{C_V}}}{L} - j\omega_o 2K_{3_{C_V}} G_{loss} + 4\omega_o^2 \left((C + C_{Vo}) K_{3_{C_V}} - 2K_{2_{C_V}}^2 \right) \right|}}$$

- Higher peak voltage gain, $G_m Q \omega_o L$, degrades linearity
- Trade-offs between noise-linearity and selectivity-linearity!

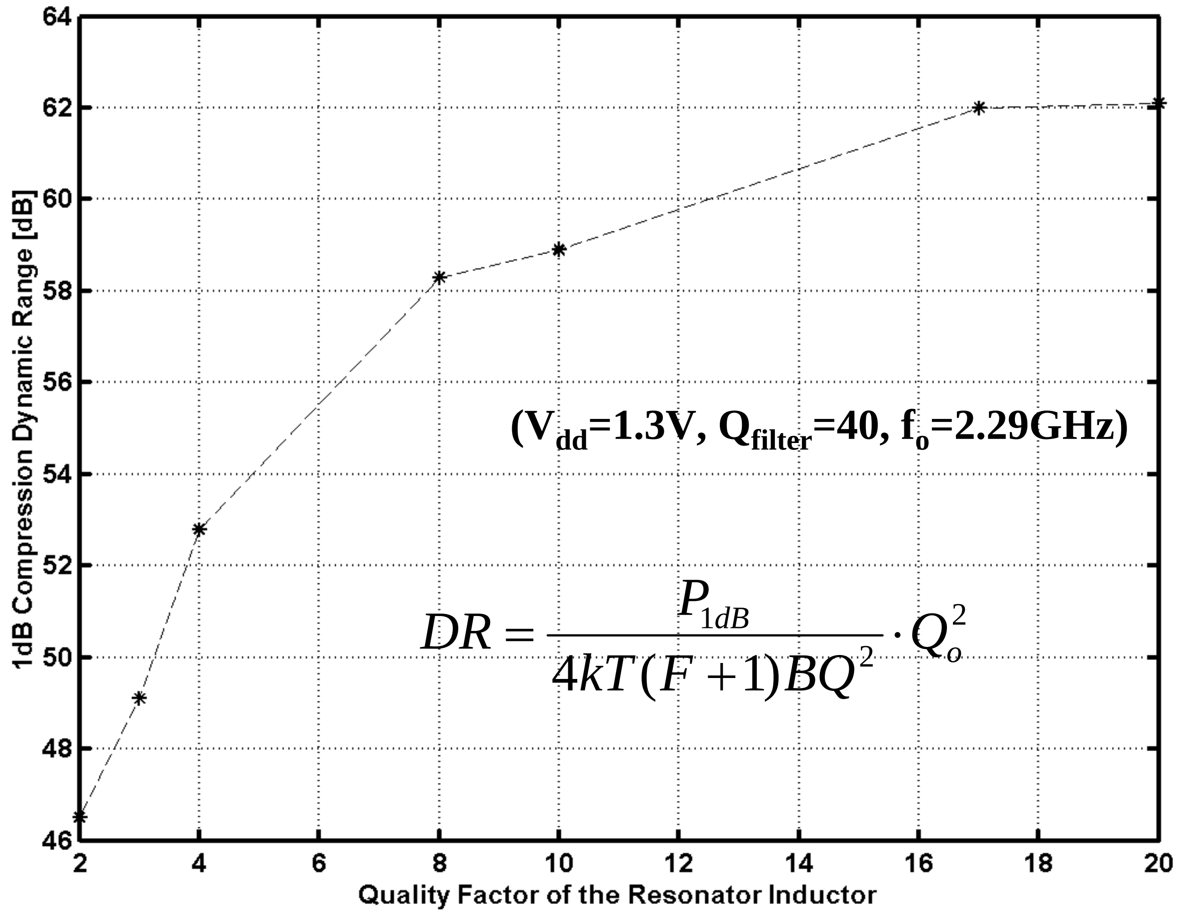
Nonlinearity Contribution of the Input G_m stage

$$V_{1dB} \cong \sqrt{2.32 \times \frac{G_{m1}^2 (1 + G_{m1} R_{\deg})^3}{\left(2K_{2_{G_{m1}}}^2 + \dfrac{K_{2_{G_{m1}}} \theta_1 G_{m1}}{1 + \theta_1 (V_{GS1} - V_{T1})} \right)}}$$

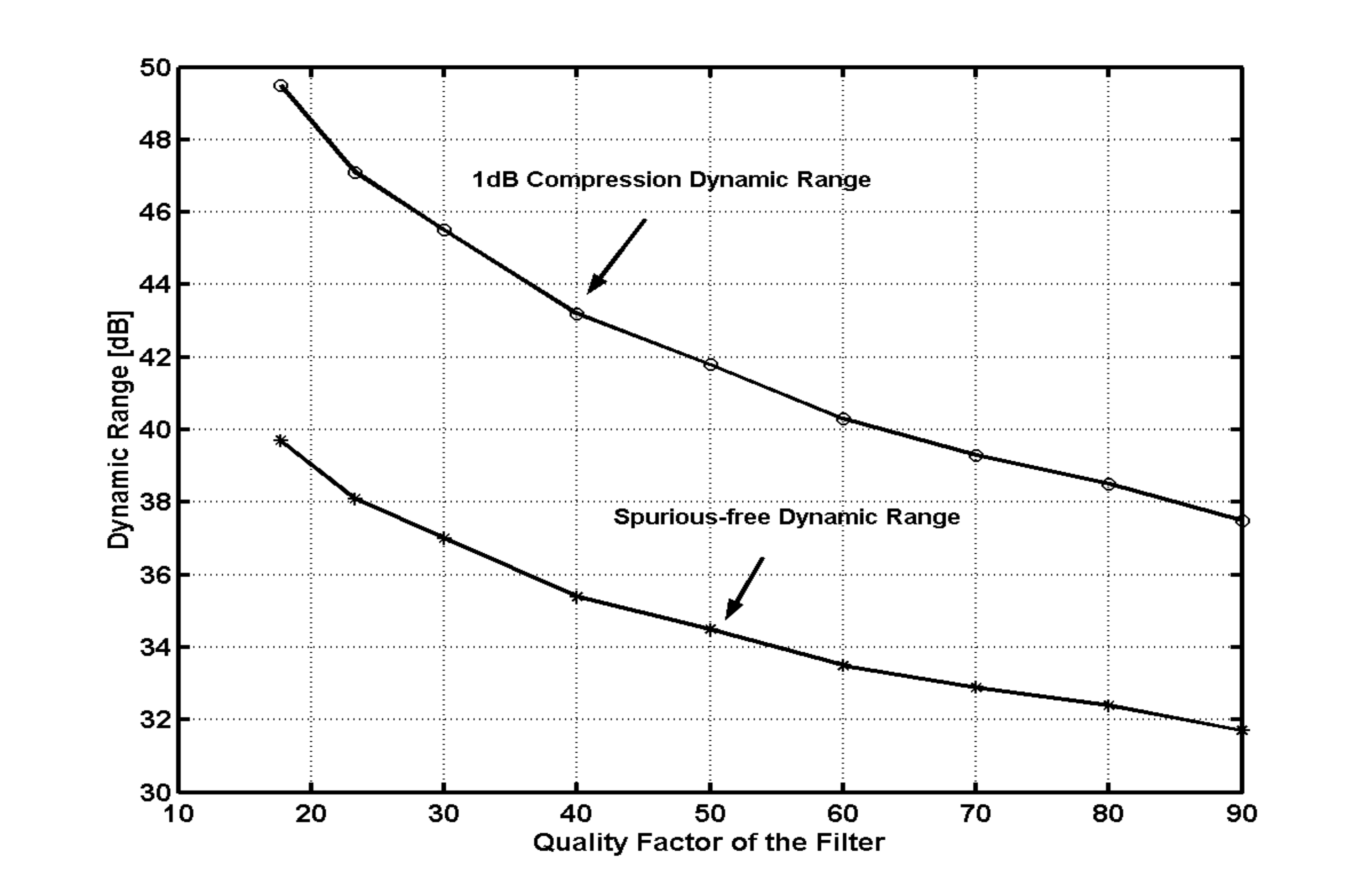
- The effective bias of the transistors should be maximized!
- Increasing R_{deg} improves the linearity with a penalty in power consumption for the same input G_m.
- The same applies to adding R_{deg} to the cross-coupled pair

linearity-power trade-off

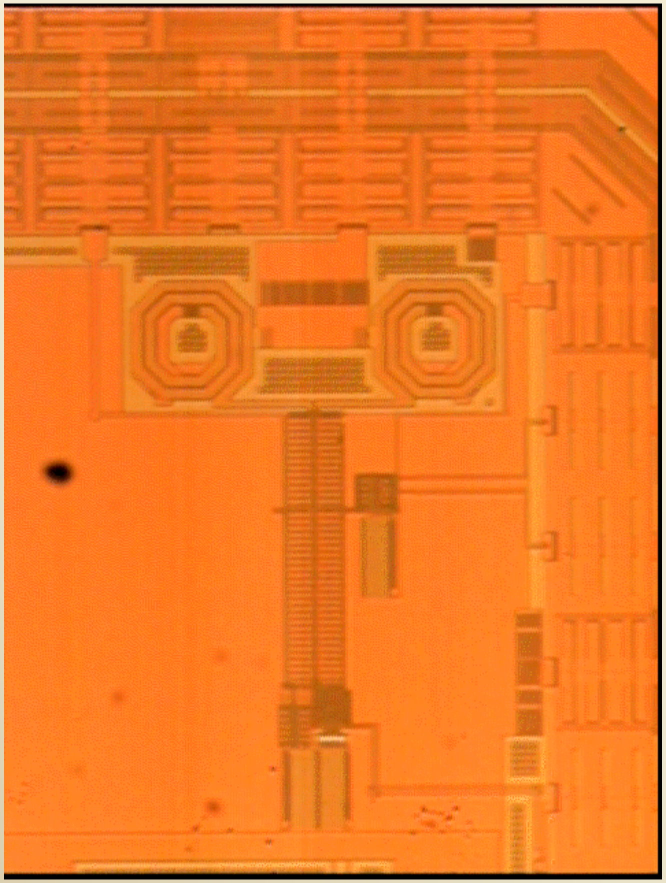
Simulated DR vs. Q of the Resonator Inductor



Dynamic Range Simulations



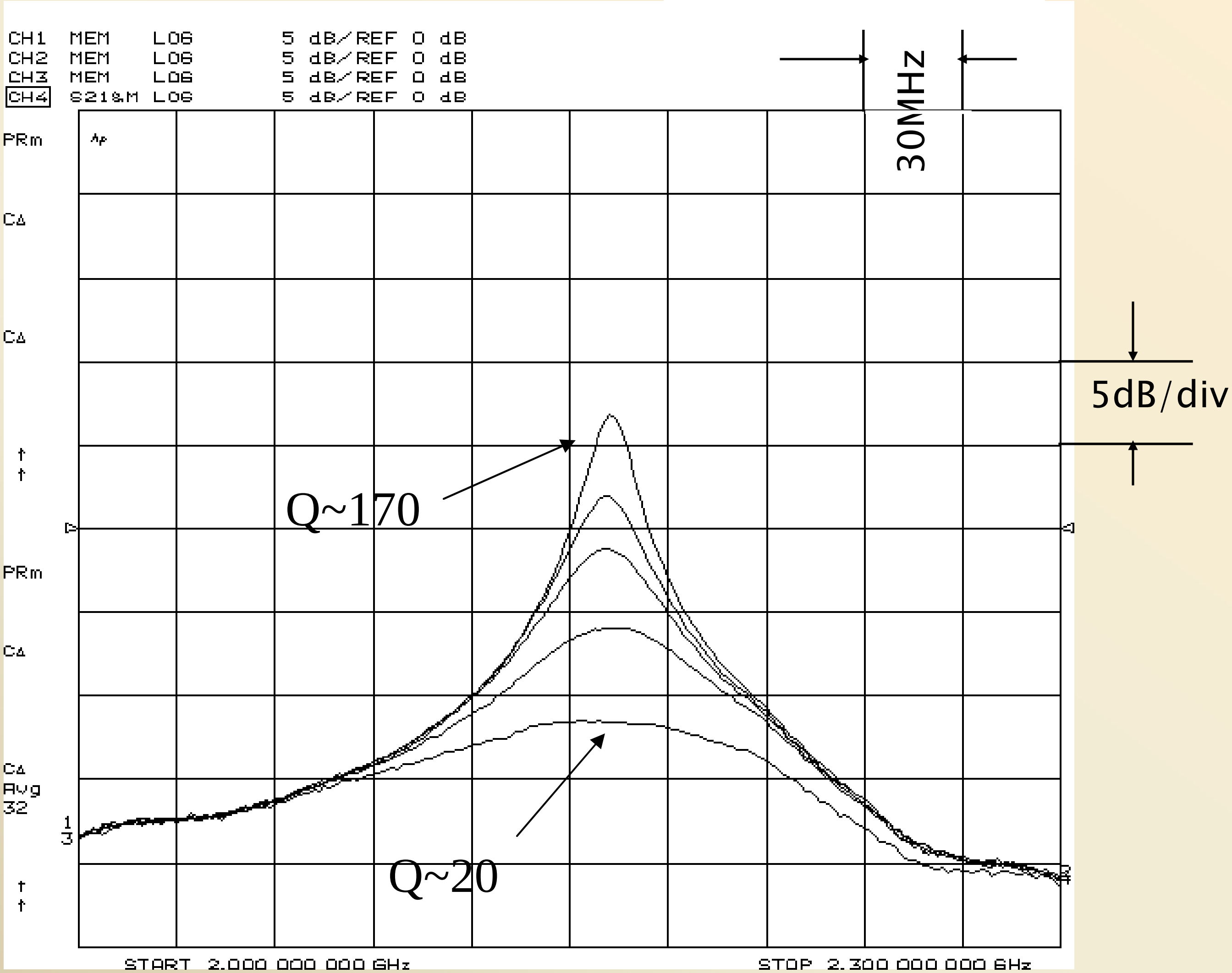
Integrated Circuit Measurements



- TSMC 0.35μm CMOS technology
- The second poly was not used. Compatibility with a standard Digital CMOS
- The filter operates with a supply voltage of 1.3V, and 4mA for a Q= 40 at 2.19GHz
- Chip area+buffers~ 0.1mm^2.

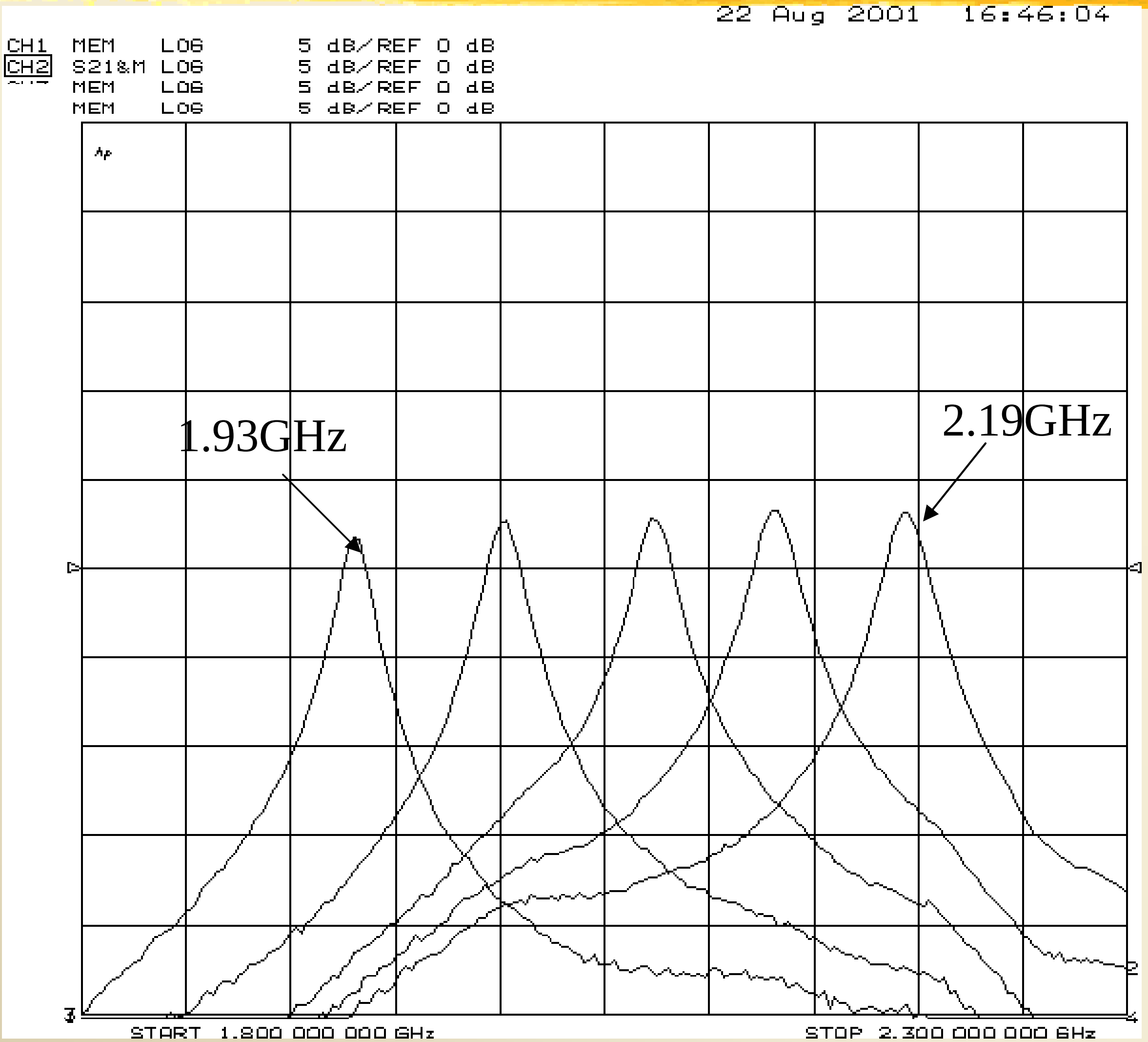
Measured Q-Tuning

More than 3 octaves at f_o=2.16GHz



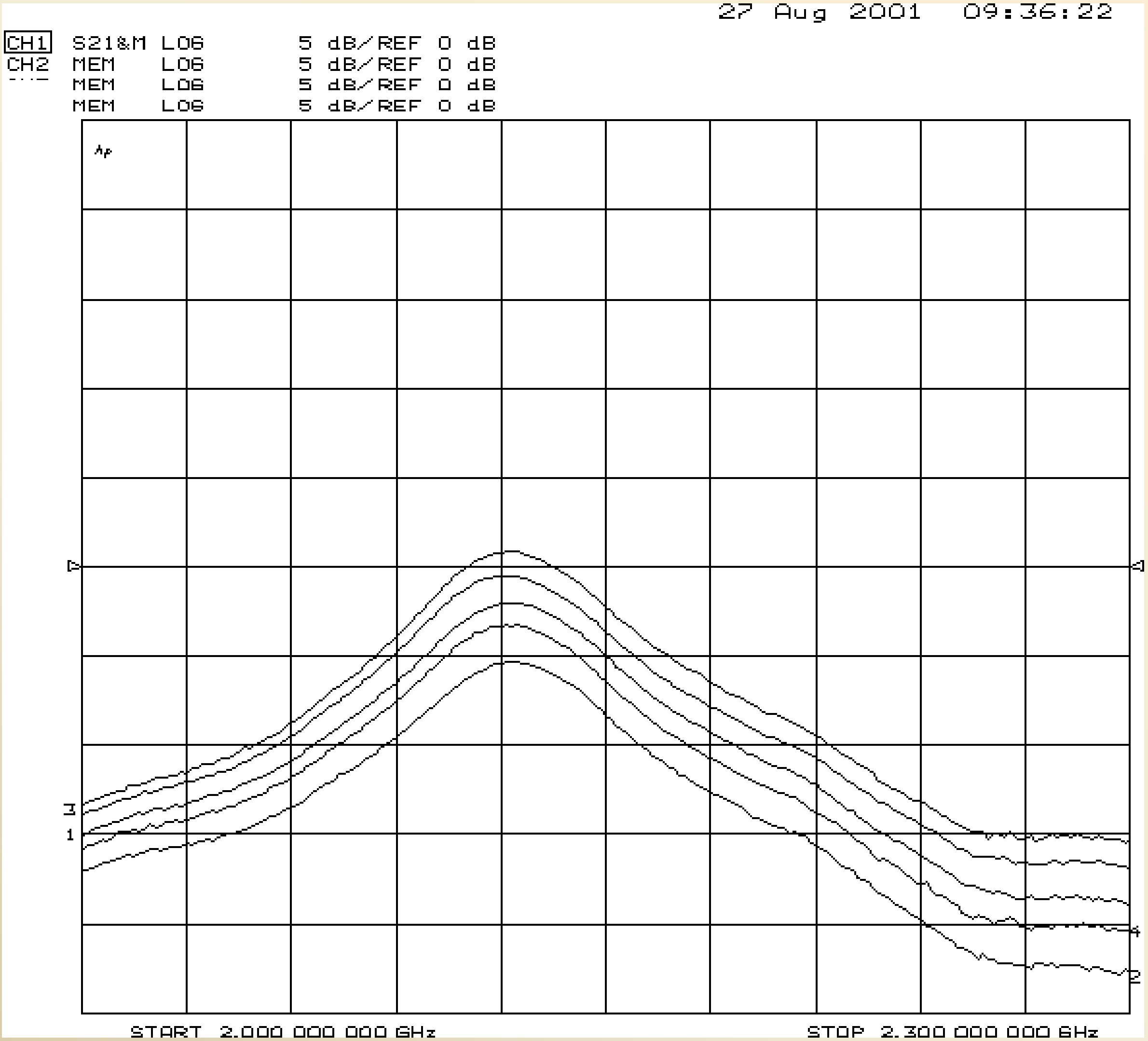
Measured Frequency Tuning

13% around 2.1GHz with Q~100



Measured Peak Gain Tuning

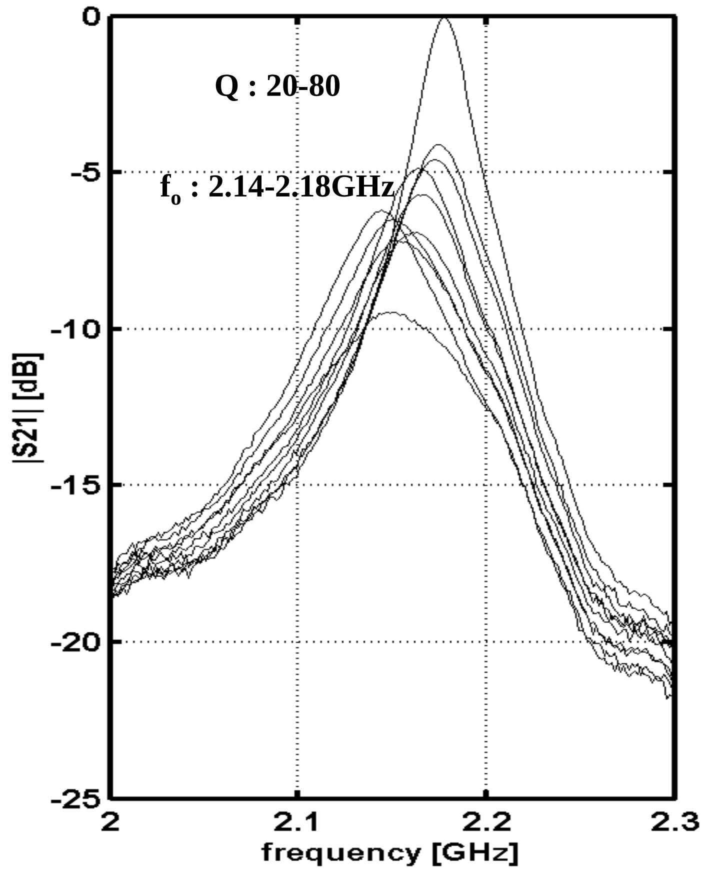
Around
2 octaves with
f_o=2.12GHz
and Q=40



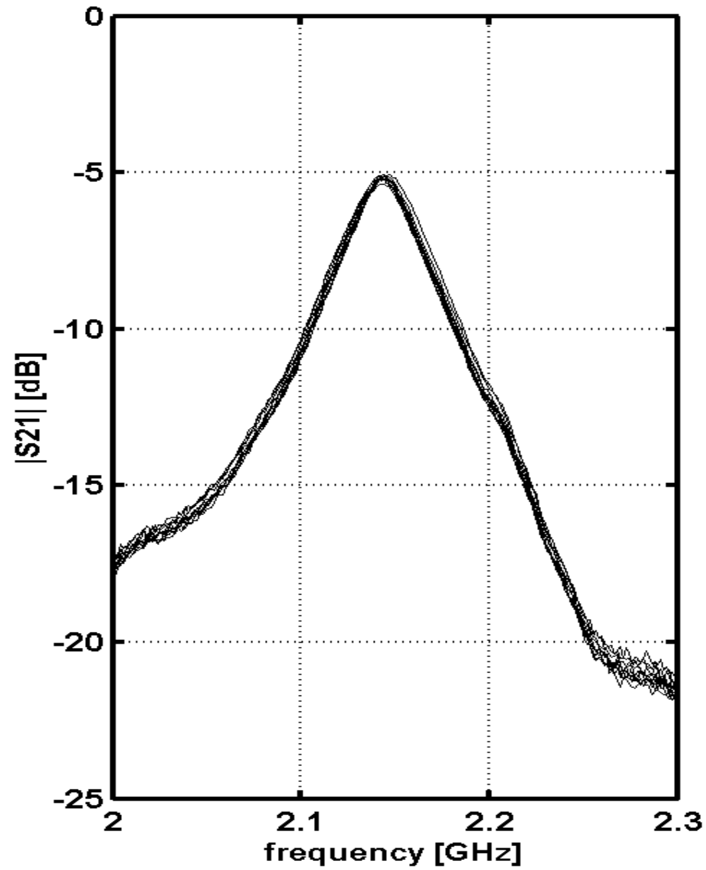
Providing gain at the ω_o of an image-reject filter is useful in a receiver front-end after the LNA, to relax the NF spec of the mixer.

Overlaid Measurements of 10 different ICs

(a)
with the same bias settings



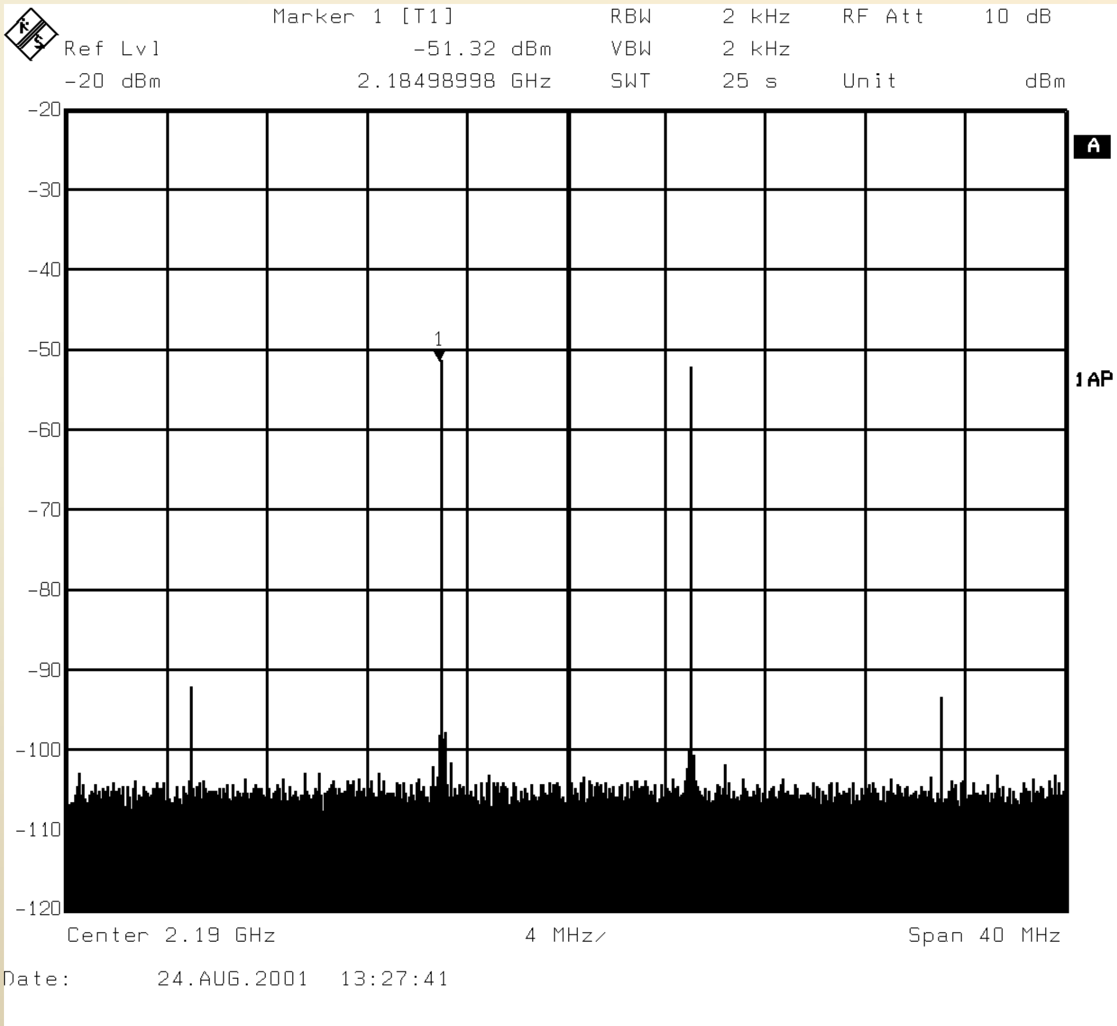
(b)
programmed for the same f_o, gain and Q=40



Two-tone IM3 Measurement

*V_{dd}=1.3V, f_o=2.19GHz, Q=40

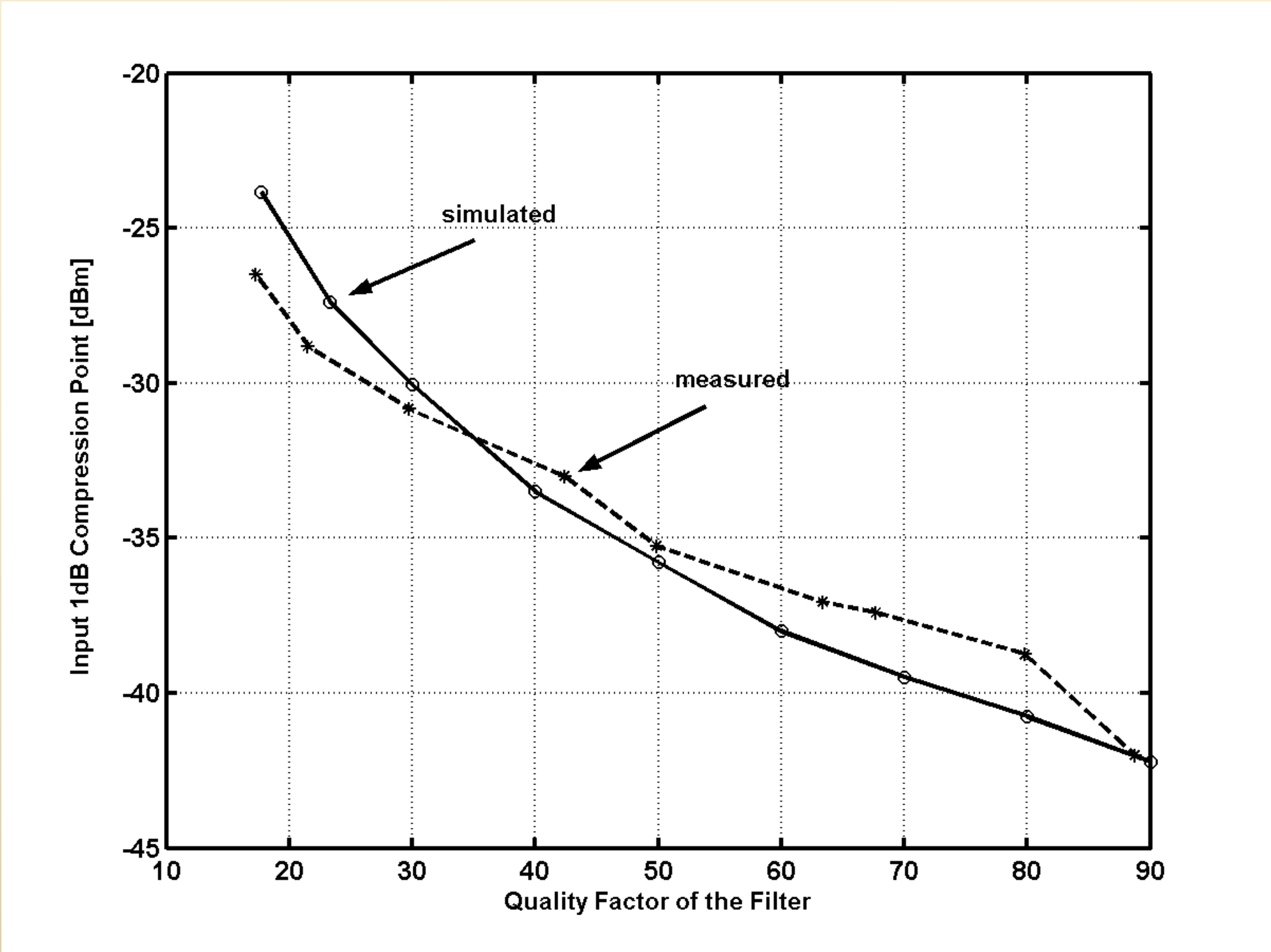
P_{in}= -38dBm
f_{in1}=2.185GHz
f_{in2}=2.195GHz



$P_{in,1dB}$= -30dBm
IIP_3=-17.5dBm

1 dB Compression Comparison

*V_{dd}=1.5V, f_o=2.17GHz



A Comparison with State-of-the-art

Reference	Tech.	f_o	Bandwidth	V_{dd}	P_D/Pole	Area/Pole	SFDR
[1]	Bipolar	1.8GHz	51.4MHz	2.8V	12.2mW	0.2mm^2	30dB
[3]	Bipolar	1GHz	25MHz	5V	34mW	0.3 mm^2	36dB
[4]	BiCMOS	750MHz	37.5MHz	5V	40mW	0.3 mm^2	25dB
[5]	BiCMOS	1.9GHz	150MHz	2.7V	12.15mW	1.79 mm^2	49dB

A Comparison with State-of-the-art (contd.)

Reference	Tech.	f_o	Bandwidth	V_{dd}	P_D/Pole	Area/Pole	SFDR
[2]	CMOS	850MHz	18MHz	2.7V	52mW	0.5mm^2	55dB
[6]	CMOS	850MHz	28.3MHz	2V	22.9mW	0.32mm^2	28dB
[7]	CMOS	2.14GHz	60MHz	2.5V	2.9mW	0.59mm^2	55dB
This work	**CMOS**	**2.19GHz**	**53.8MHz**	**1.3V**	**2.6mW**	**0.05mm^2**	**31dB**

Remarks

- Low voltage, low power, compact fully-integrated programmable bandpass filter in mainstream CMOS at frequencies higher than 2GHz.

  - Comparison shows that the proposed RF filter uses the lowest power supply voltage, lowest power consumption per pole and occupies at least four times less silicon area per pole
  - Programmability in the peak gain
  - Noise and Nonlinearity analyses of the structure provide simplified approximate expressions to clarify design trade-offs

Reference:

• Fikret Dulger, E. Sanchez-Sinencio, J. Silva-Martinez,
"A 1.3-V 5-mW fully integrated tunable bandpass filter at 2.1 GHz in 0.35 um CMOS,"

IEEE Journal of Solid-State Circuits, Volume :38 Issue:6, June 2003, Page(s): 918- 928

• F. Dulger and E. Sanchez-Sinencio, "Integrated RF Building Blocks for Wireless Communication"

book, details will follow later.