Introduction to RF VCO Design

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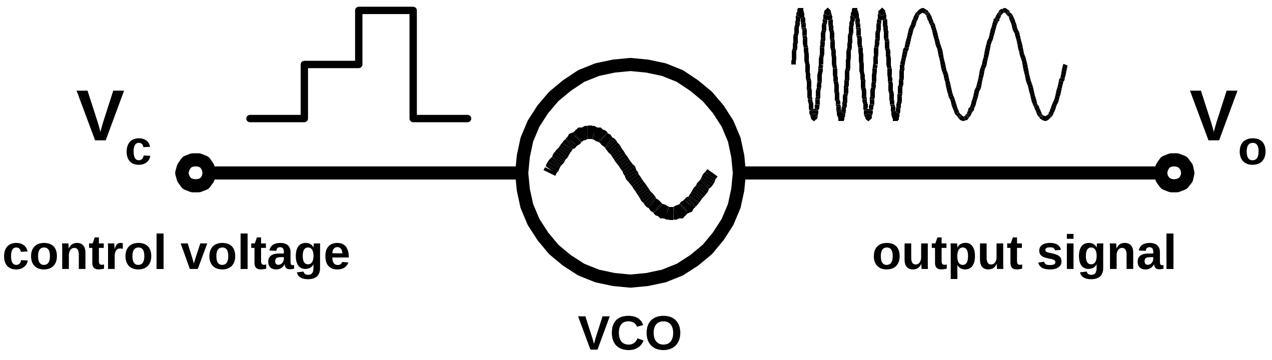
- Introduction
- VCO design procedure
- Quadrature generators
- Measurement
- Inductor measurement using microprobe

Introduction to VCO

- VCO stands for Voltage Controlled Oscillator.
- VCO is an Oscillator of which frequency can be Controlled by external Voltage stimulus.

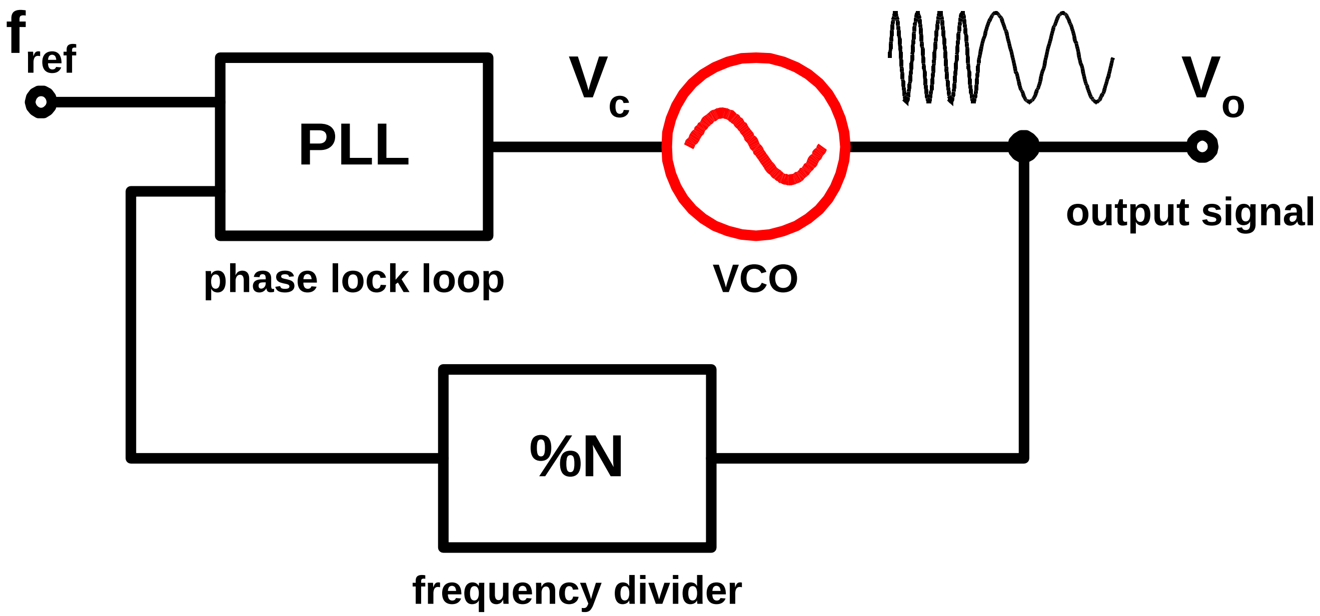


VCO in Frequency Synthesizer

- One of major applications for VCO is a frequency synthesizer.
- Frequency synthesizer provides sinusoidal/pulse signals at predetermined frequencies that is precisely controllable by digital words.
- Frequency synthesizer is a core building block of any system that has to work at multiple frequencies such as wireless communication transceivers.

VCO in Frequency Synthesizer cont.

- Frequency synthesizer usually consists of a VCO, a PLL and a frequency divider.



Requirements for VCO Design

- Frequency tuning range
  - Tuning range must cover the entire band of operation.
- Phase noise
  - Close to the oscillation frequency due to spontaneous jitter.
- Harmonic distortion
  - Spectral impurity of the signal
- Signal power
  - Must be high enough to drive the load.
- Power consumption

VCO for Bluetooth transceiver

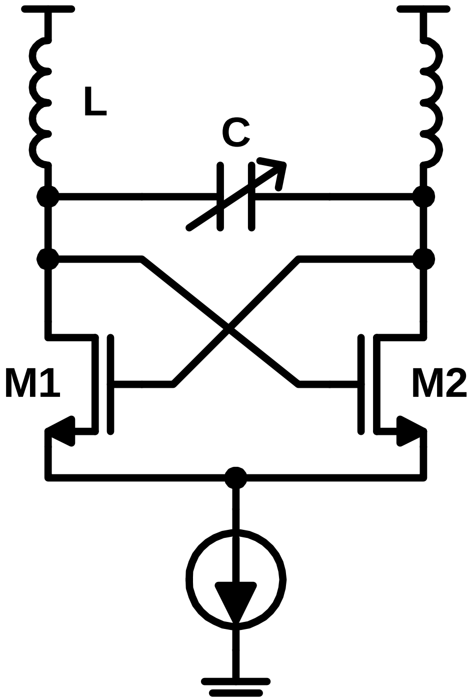
- Frequency tuning range : 2.402 ~ 2.479GHz
- Phase noise : -128dBc/Hz@3MHz
- Harmonic distortion : less than 20dB
- Signal power : more 0dBm
- Power consumption : less than 8mA

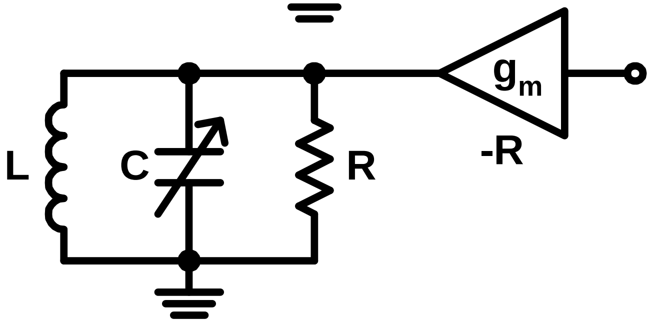
Procedure 1. Specification Study

- Relatively low tuning range : 3.3%
- High frequency of oscillation : >2.4GHz
- Very high phase noise requirement

→ LC tuned oscillator is most suitable

Procedure 2. LC Tuned Oscillator





- Oscillation frequency is tuned by resonant frequency of LC tank.

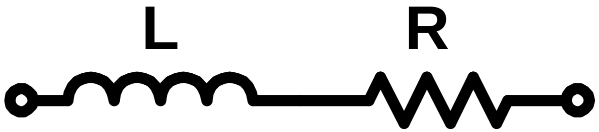
$$\boxed{w_o \approx \frac{1}{\sqrt{LC}}}$$

- Cross-coupled transistors work as a negative resistance that sustains oscillation by compensating loss in the LC tank.
- Frequency is controlled by varying the capacitance of the tank.

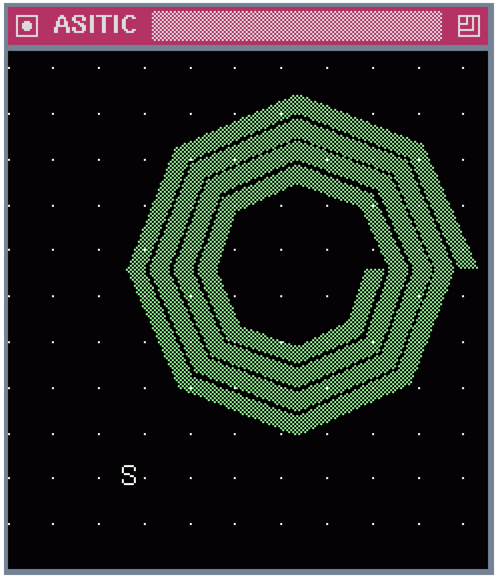
Procedure 3. On-chip Inductor

$$\boxed{Q \approx \frac{wL}{R}}$$

- Specifications
  - L = 2nH
  - Q > 5



- On-chip spiral inductor must be simulated with EM(Electro-Magnetic) simulator such as ASITIC.



← ASITIC EM simulator

Inductance and Q

$$L \propto \text{Metal area}/\text{Total area}$$

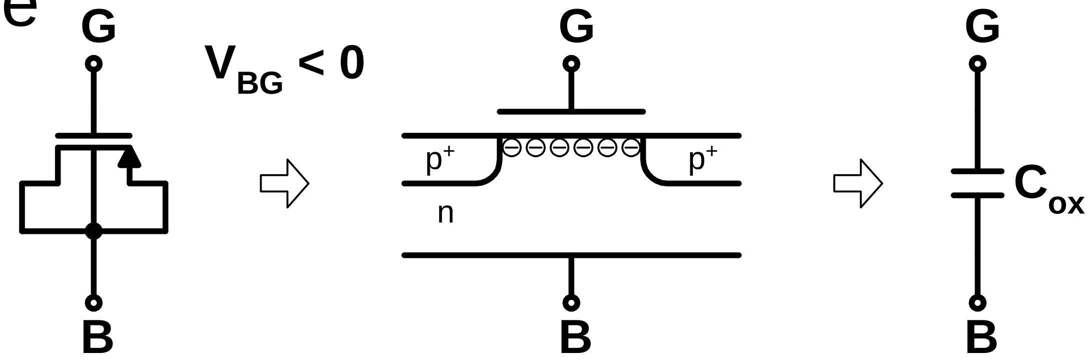
$$Q \propto \text{Metal width}$$

$$f_{self\_resonant} \propto 1/\text{Metal area}$$

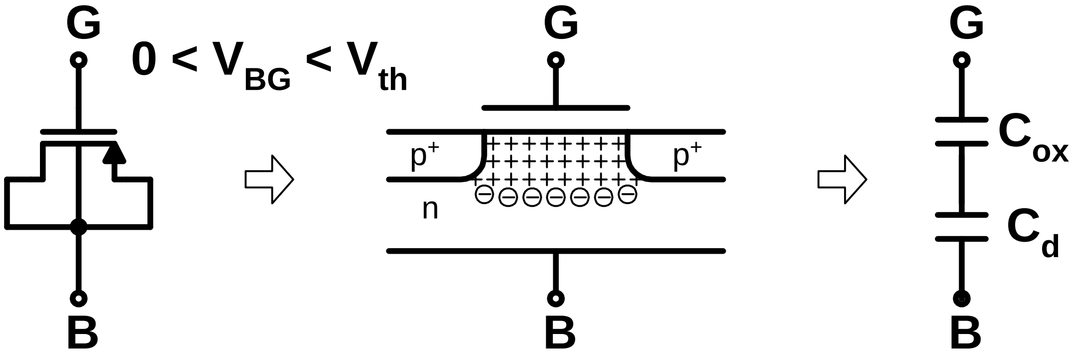
- Q can be improved by increasing metal width.
- To keep L same, total area has to be increased.
- Increased metal area reduces self resonant frequency

Procedure 4. MOSFET Varactor

- Back gate controlled PMOS varactor
- Accumulation mode

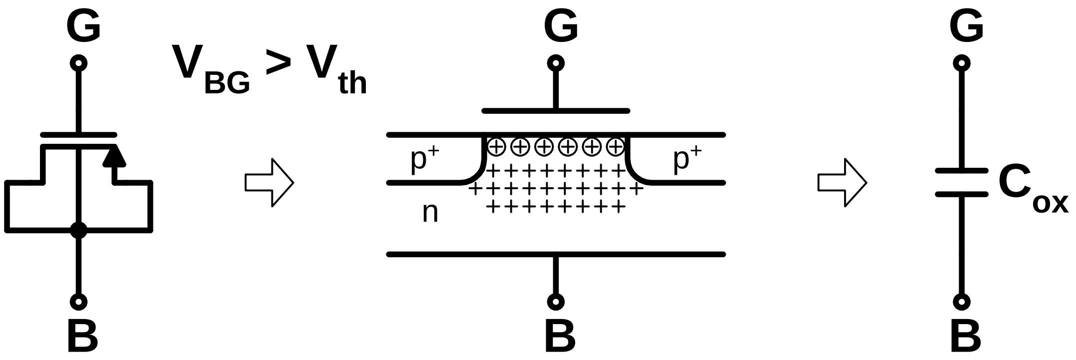


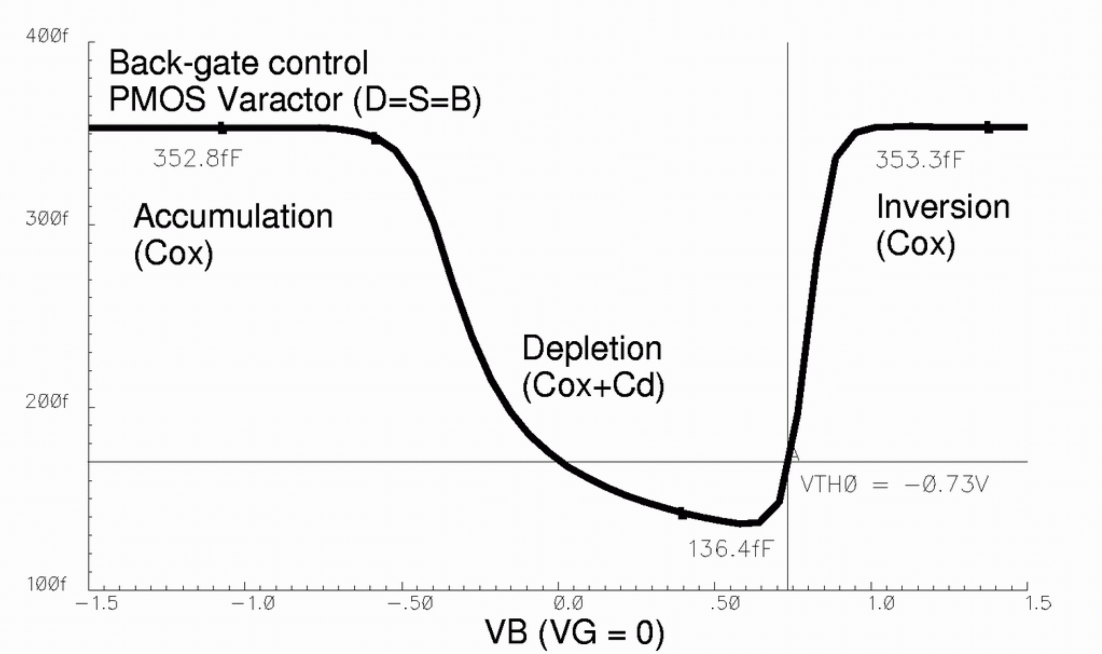
- Depletion mode



Procedure 4. MOSFET Varactor (cont.)

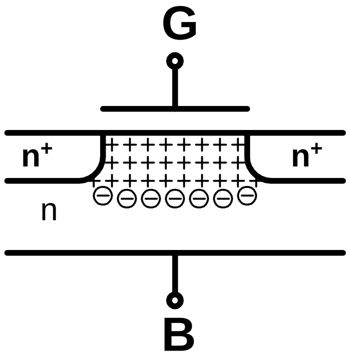
- Inversion mode



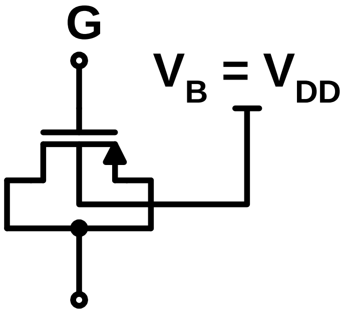


Procedure 4. MOSFET Varactor (cont.)

- Accumulation/Depletion only varactor



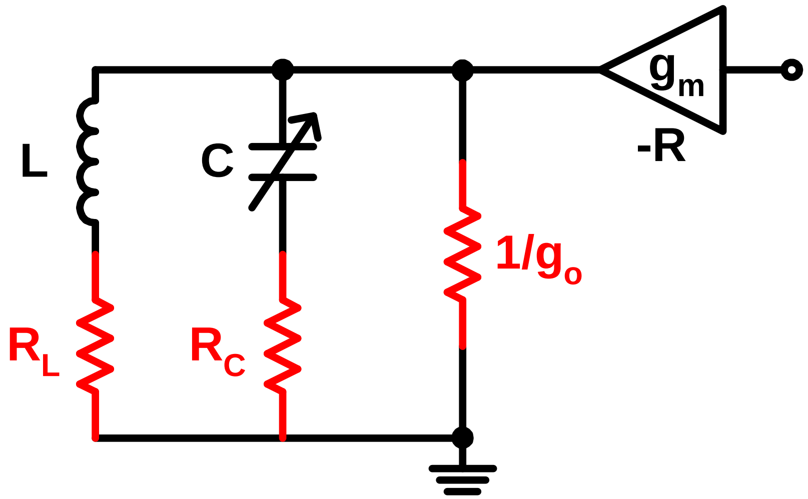
- Inversion only varactor



Procedure 5. Active Elements

- g_m of the cross-coupled MOS pairs must be high enough to compensate the loss of the tank.
- It is a good idea to have plenty of margin in design.
- The length of the transistors must be minimum in order to minimize parasitics.

Procedure 5. Active Elements (cont.)



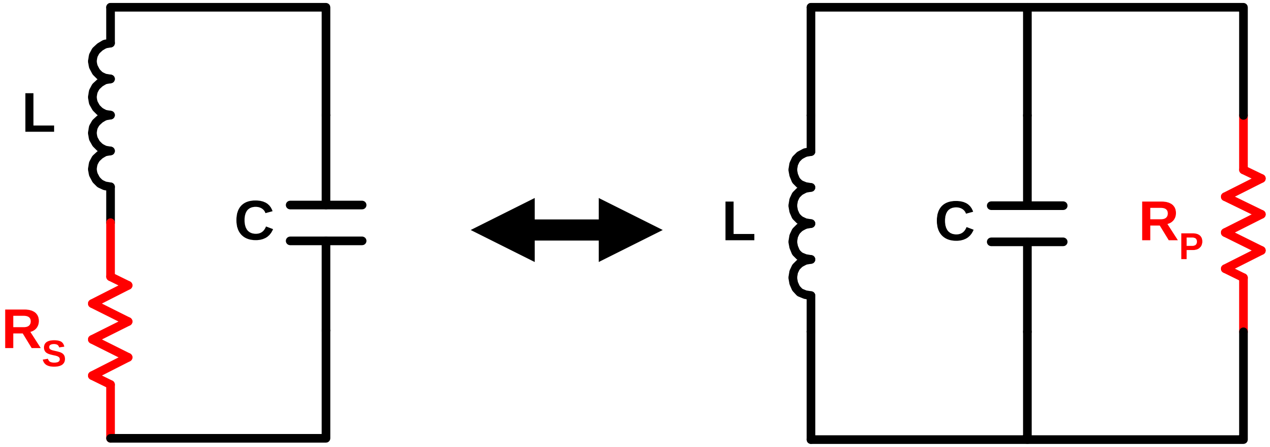
$$g_m > a\left\{g_o + \frac{1}{Q_L w_o L} + \frac{w_o C}{Q_C}\right\}$$

$$Q_L = \frac{w_o L}{R_L},\quad Q_C = \frac{1}{w_o C R_C}$$

$$a > 3$$

- Sources of the loss
  - Quality of L (Q_L)
  - Quality of C (Q_C)
  - Output impedance of the transistor. (g_o)
- Gm of the transistor must be larger than total loss.
- α is safety margin for starting oscillation.

Series-parallel conversion



$$R_S = \frac{(w_o L)^2}{R_P} = \frac{R_P}{Q_L{}^2} \qquad R_P = \frac{(w_o L)^2}{R_S} = Q_L{}^2 R_S$$

- Only valid close to resonant frequency

Phase Noise

- Phase noise is uncertainty of center frequency of VCO output
- The spectrum looks as if it has finite power in certain frequency offset away from the center frequency
- In time domain, phase noise is also referred to as timing jitter

Phase Noise (cont.)

- Signal amplitude

$$V_A = I_{tail} R_P = \frac{I_{tail}(w_o L)^2}{R_S} = I_{tail} Q_L{}^2 R_S$$

- Noise power

$$v_n{}^2 = \frac{4kT\gamma g_m R_P{}^2}{4Q_L{}^2}\left(\frac{w_o}{\Delta w}\right)^2 = kT\gamma g_m Q_L R_S{}^2\left(\frac{w_o}{\Delta w}\right)^2$$

- Phase noise

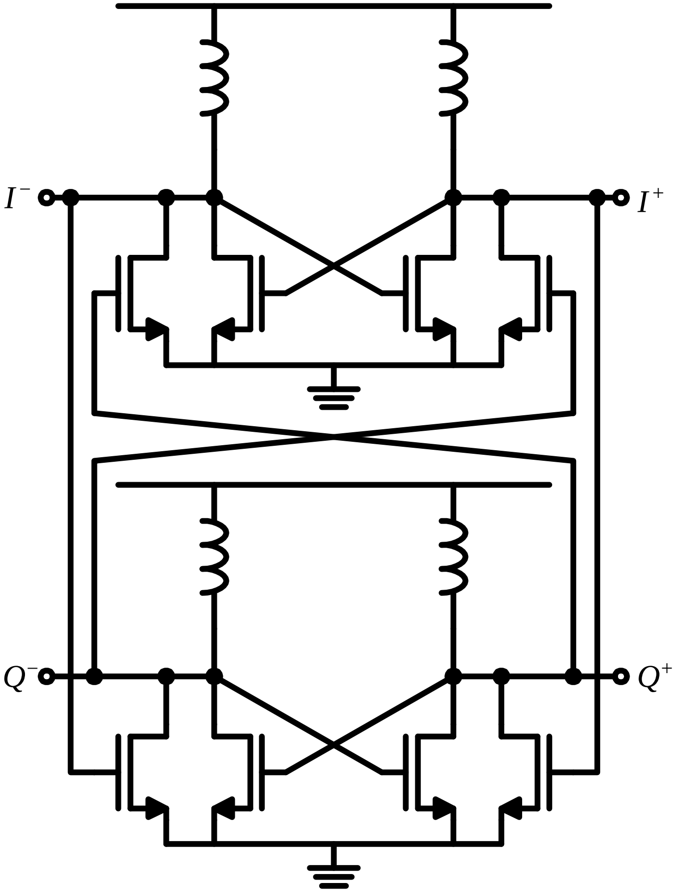
$$PN = \frac{8v_n{}^2}{V_A{}^2} = \frac{8kT\gamma g_m}{I_{tail}{}^2 Q_L{}^2}\left(\frac{w_o}{\Delta w}\right)^2$$

Phase Noise (cont.)

- Signal power can be increased either by higher Q or by higher L
- Only high Q improves phase noise
- High power dissipation also improves phase noise

Quadrature Signal Generation 1

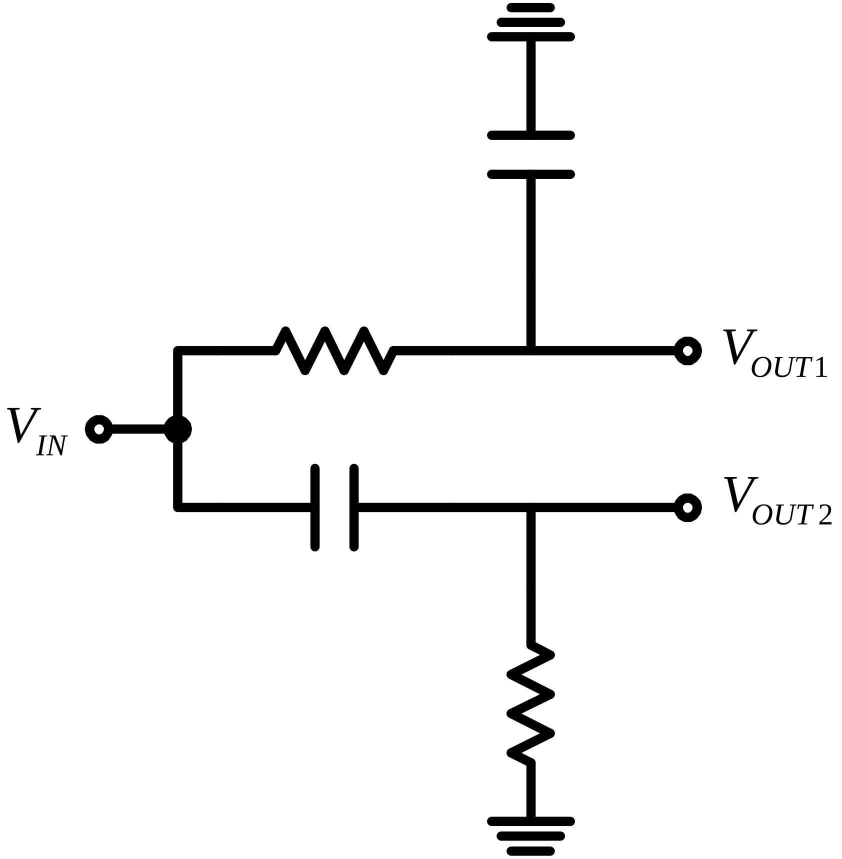
- Two identical coupled oscillators
  - Immune to mismatch - the coupled oscillators synchronize to exactly the same frequency
  - Large area and power dissipation



- Lam, C.; Razavi, B. “A 2.6 GHz/5.2 GHz CMOS voltage-controlled oscillator”, ISSCC, 1999, pp. 402-403

Quadrature Signal Generation 2

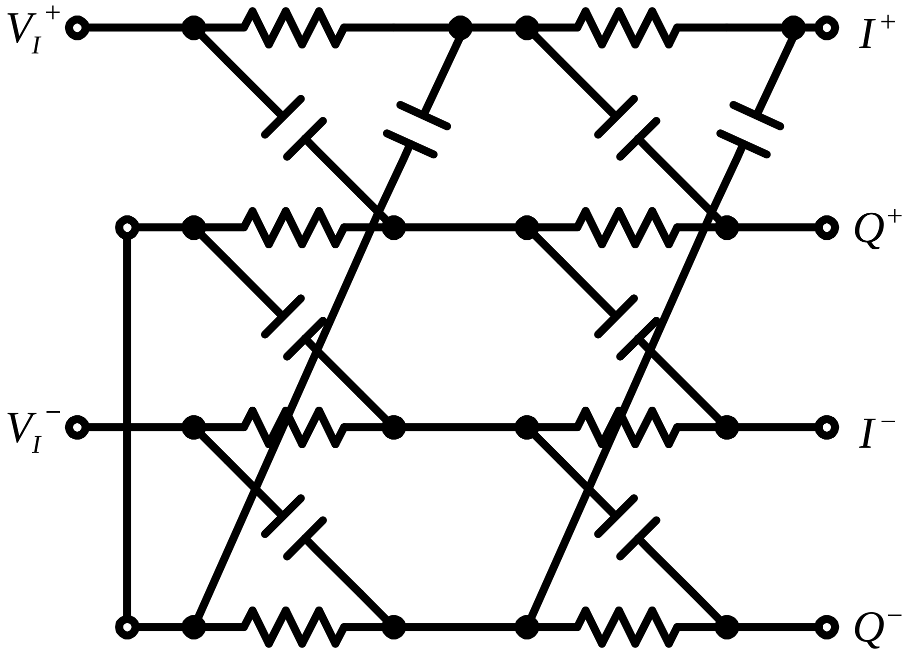
- RC-CR network
  - Low power : passive element only
  - Sensitive to mismatch
  - Amplitude mismatch



- Orsatti, P.; Piazza, F.; Huang, Q., “A 20-mA-receive, 55-mA-transmit, single-chip GSM transceiver in 0.25 CMOS”, JSSC, vol 34, Dec. 1999 , pp. 1869-880

Quadrature Signal Generation 3

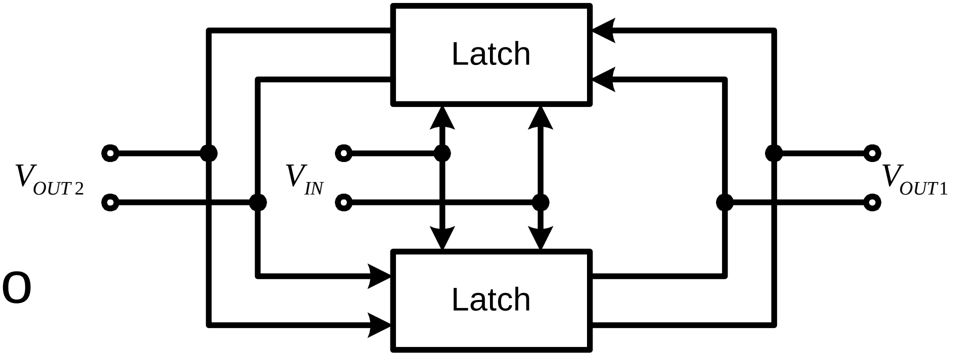
- Polyphase network
  - Low power
  - Amplitude matching
  - Insertion loss



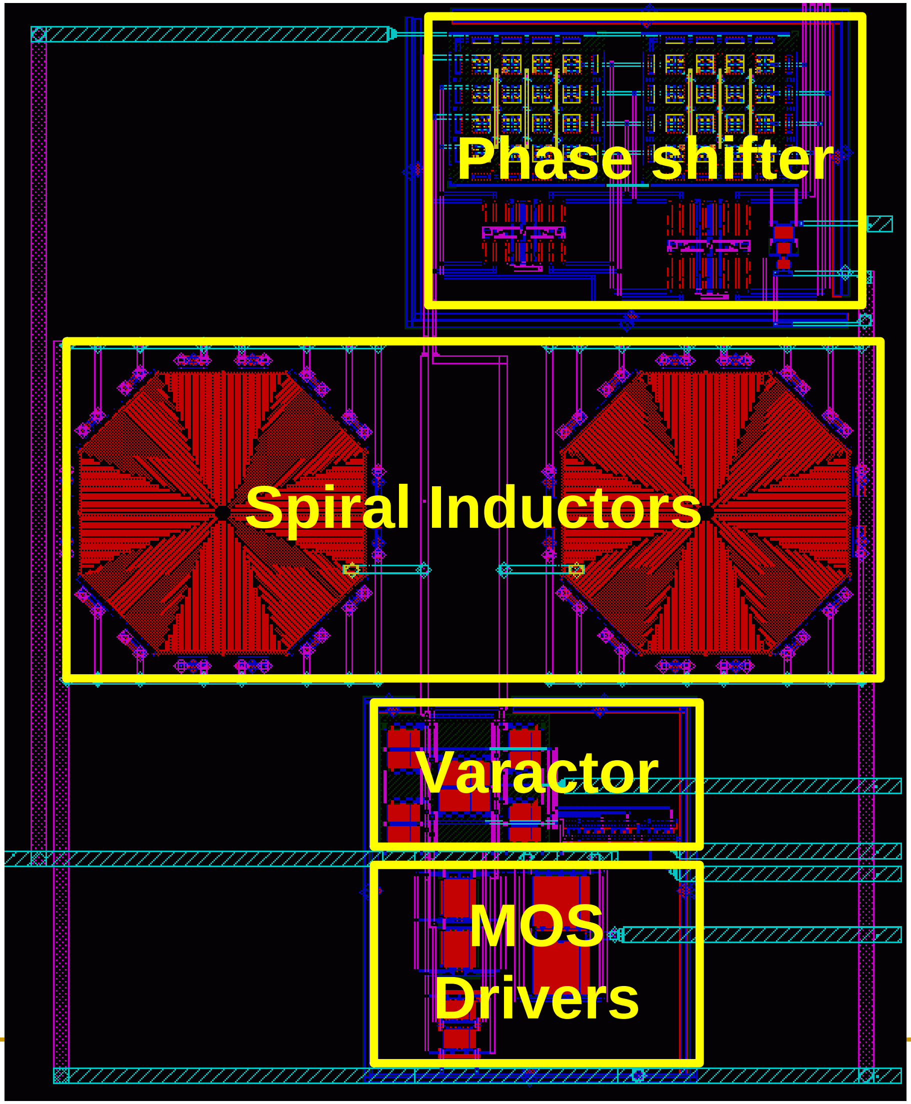
- Parssinen, A.; Jussila, J.; Ryynanen, J.; Sumanen, L.; Halonen, K.A.I., “A 2-GHz wide-band direct conversion receiver for WCDMA applications,” JSSC, vol. 34, Dec. 1999, pp. 1893-903

Quadrature Signal Generation 4

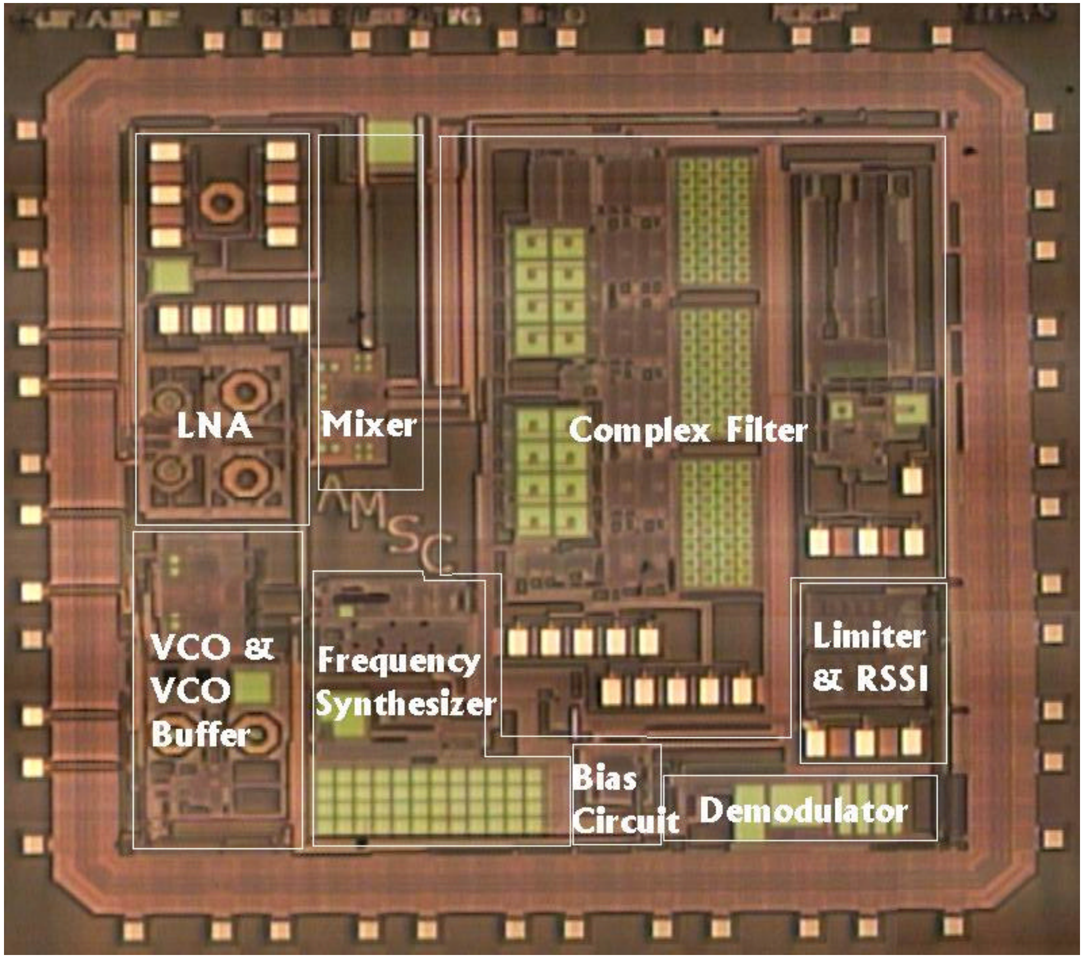
- Divide-by-two circuit
  - Relatively immune to mismatch
  - Requires 2x frequency oscillation which leads to high power dissipation



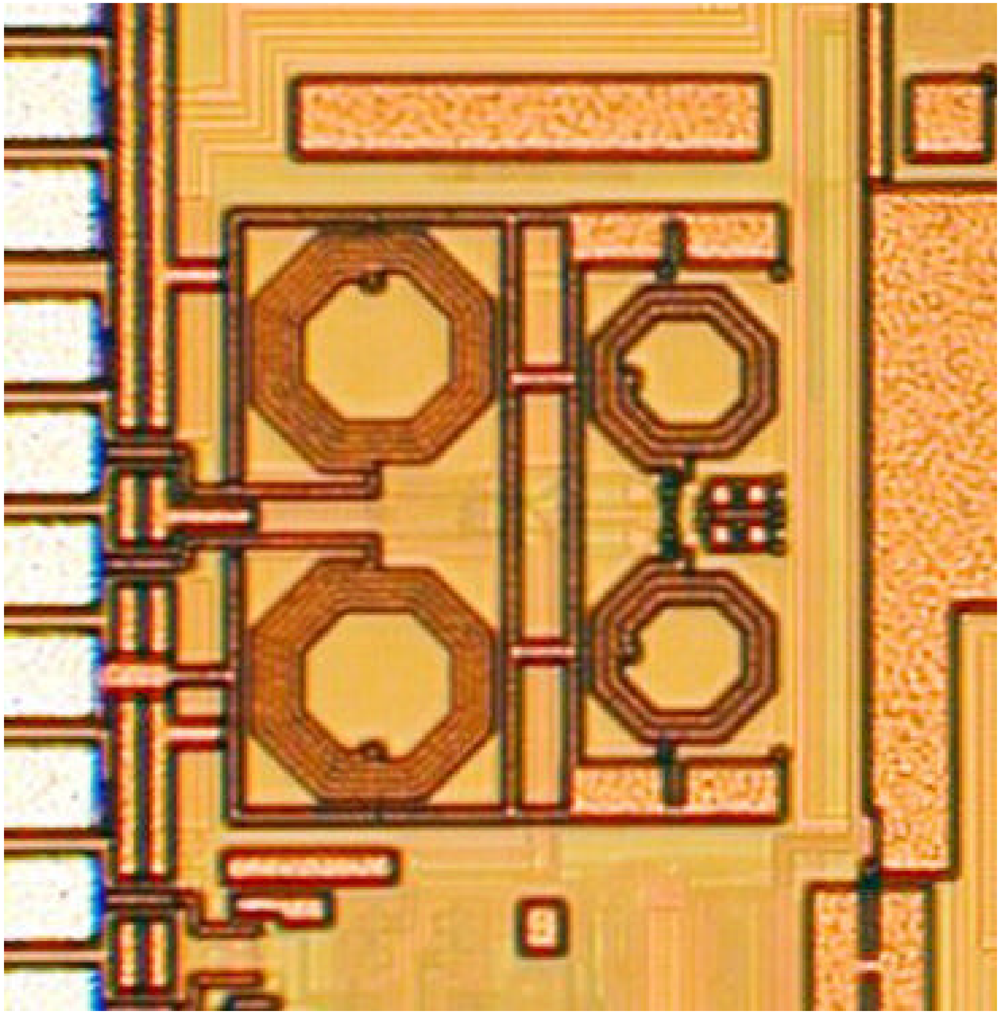
Layout of Bluetooth VCO



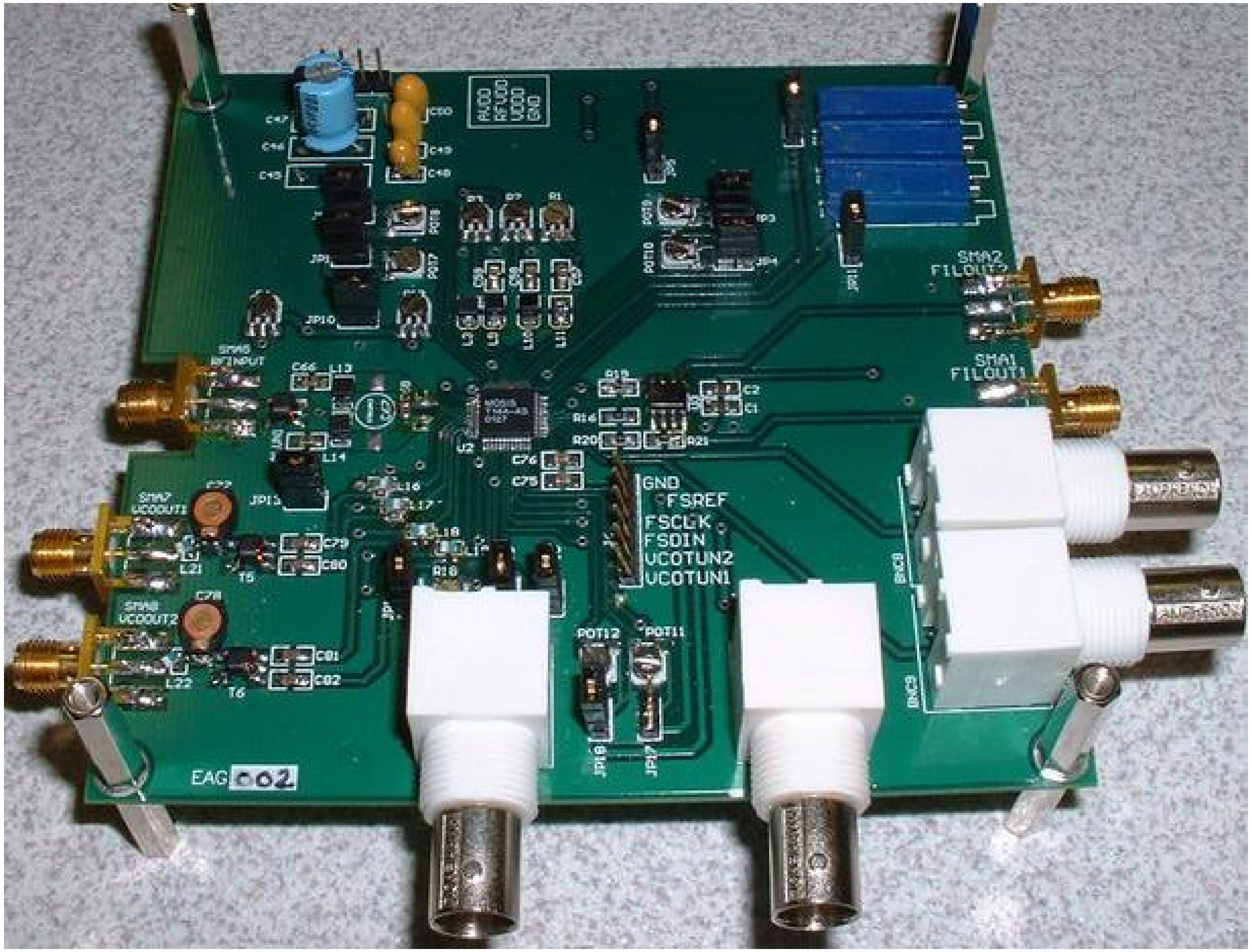
Chip Microphotograph



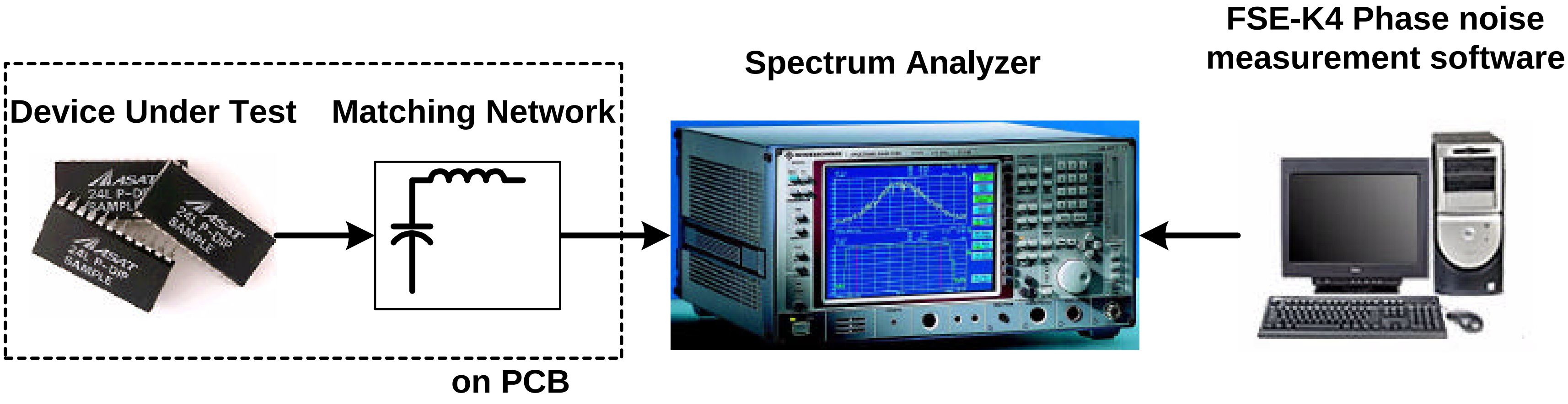
Another Layout (for 802.11b+BT)



PC Board


SMA2
FILOUT2
SMA1
FILOUT1
SMA6
RFINPUT
SMA7
VCOOUT1
SMA8
VCOOUT2
GND
FSREF
FSCLK
FSDIN
VCOTUN2
VCOTUN1
POT12
POT11
JP16
JP17
BNC8
BNC9
EAG 002

Using Spectrum Analyzer



- A matching network to make the output impedance of the VCO to match 50Ω is recommended
- The phase noise measurement can be automated by using FSE-K4 software

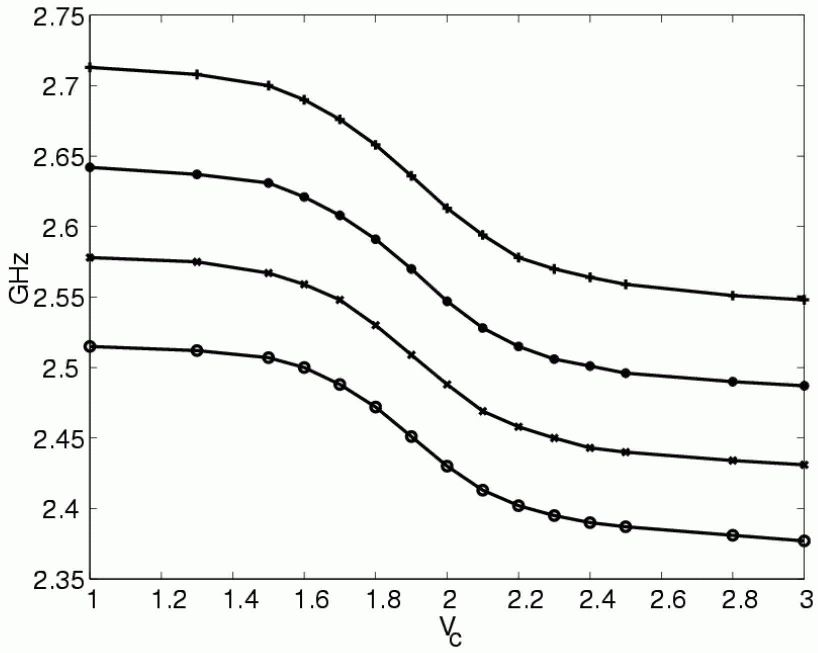
Testing Results

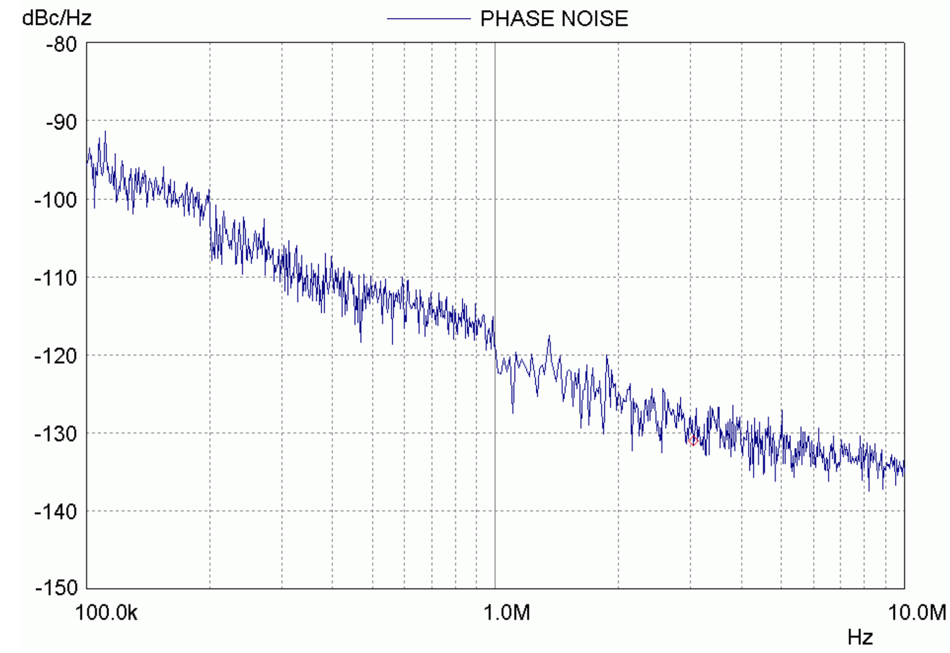
- Since the frequency of oscillation is too high for any oscilloscope available in the lab, the spectrum analyzer is the only option for testing the circuit.
- Measured parameters:

❑ Frequency tuning range	: 2.37 ~ 2.72GHz
❑ Signal power	: -12dBm
❑ Phase noise	: -130dBc/Hz @ 3MHz

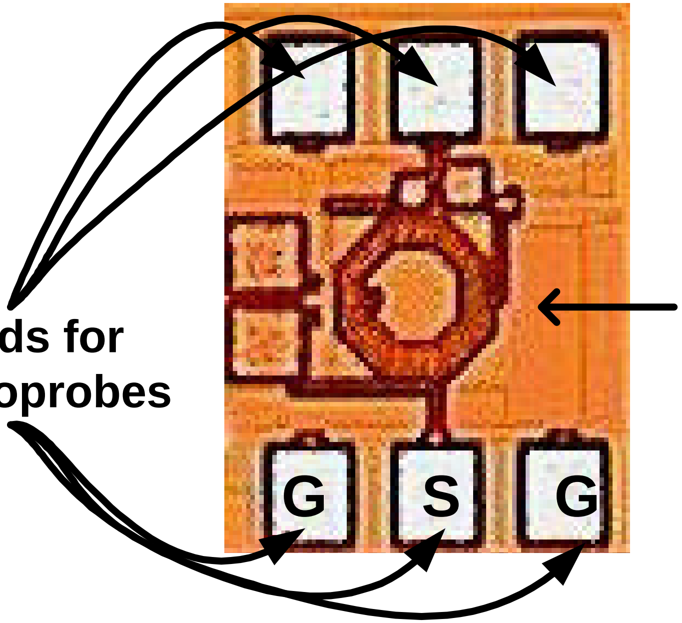
Testing Results

- Tuning Range
  - 2.37 ~ 2.72GHz
- Phase noise
  - -130dBc/Hz @ 3MHz offset





Inductor Measurement using Microprobe

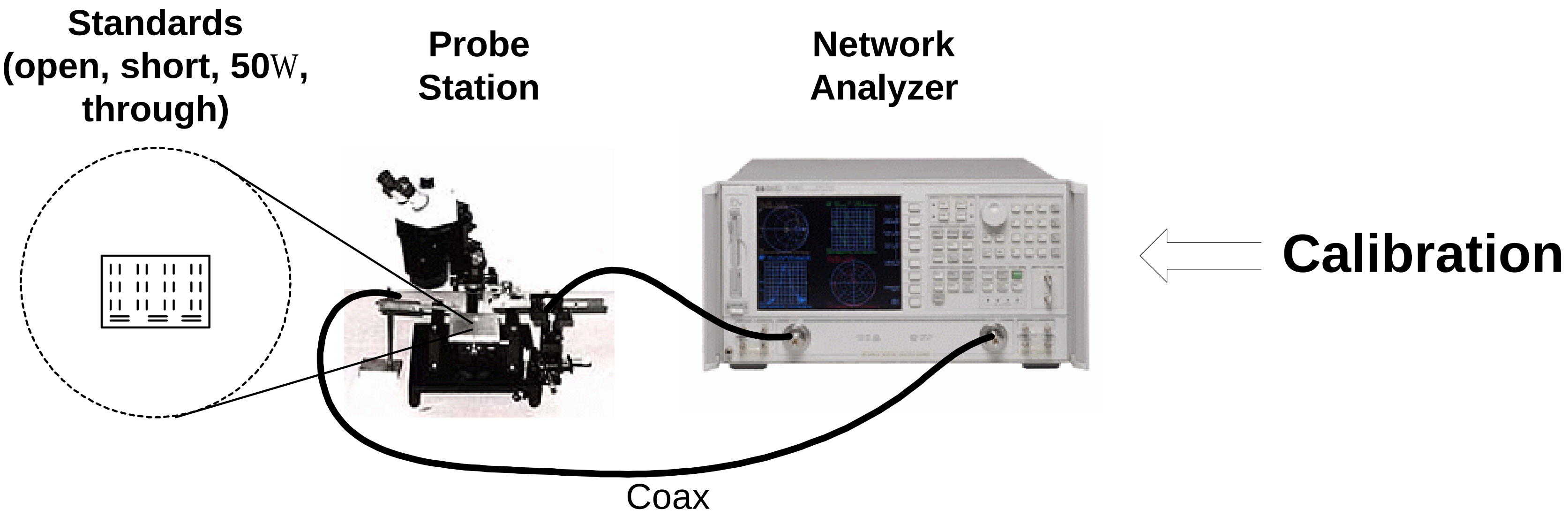


Pads for microprobes

Spiral Inductor

- Measurement instruments
  - Probe Mount Station
  - Microprobe (150μm pitch)
  - Network Analyzer (HP 8719ET)
  - SMA Coaxial cable

Calibrating Network Analyzer



Standards (open, short, 50W, through)

Probe Station

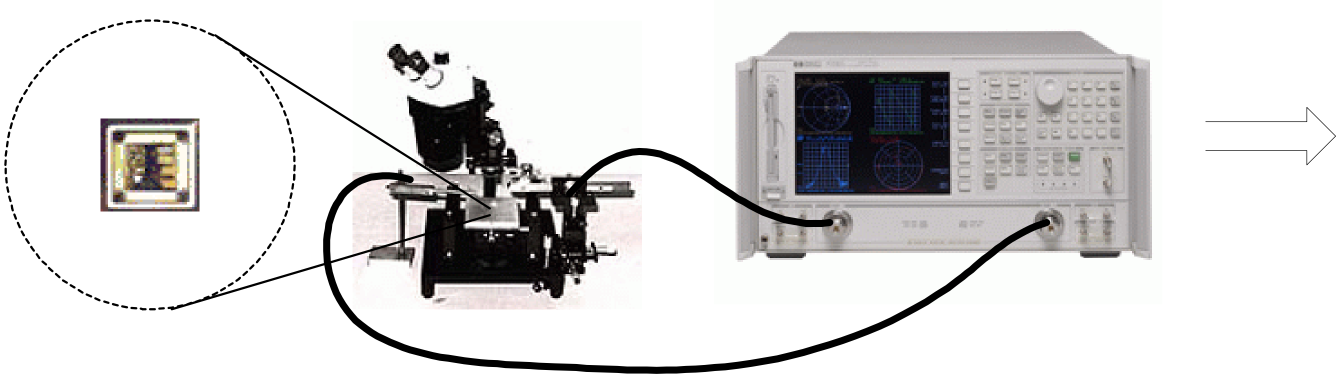
Network Analyzer

Calibration

Coax

- Calibration is required to compensate the effect of microprobes, coaxial cables and network analyzer itself.
- The effect of pads for microprobe landing *cannot* be calibrated out. De-embedding after measurement is required.

Measurement Setup



Chip
(TSMC 0.35u
Spiral inductor)

Probe
Station

Network
Analyzer

s-parameters

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

Coax

- The device under test is measured after calibration
- Network analyzer extracts the s-parameters

s-parameter to y-parameter Conversion

$$y_{11} = \frac{(1 - s_{11})(1 + s_{22}) + s_{12}s_{21}}{Z_o\Delta}$$

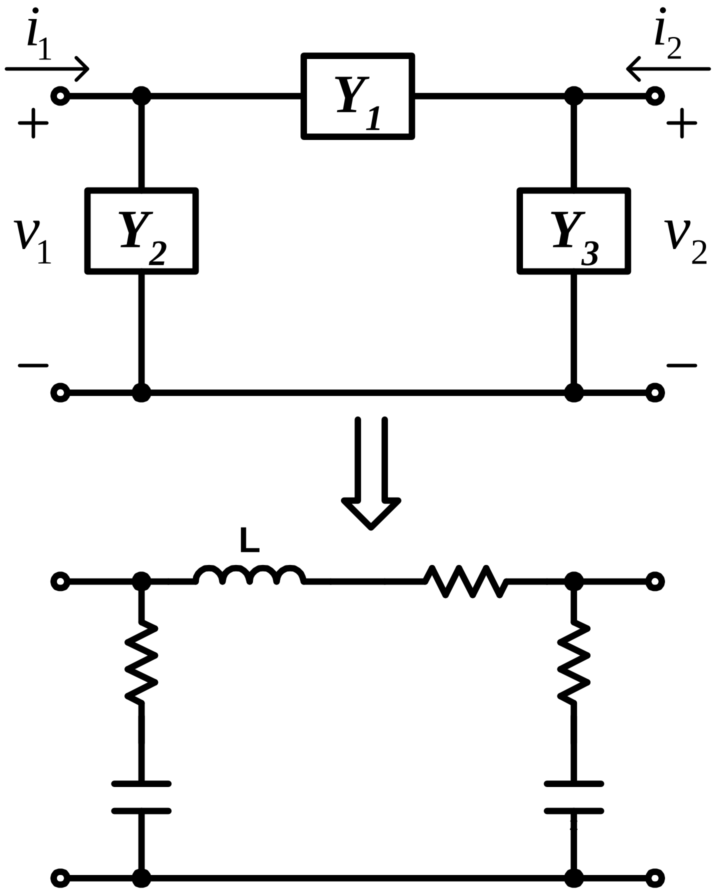
$$y_{12} = \frac{-2s_{12}}{Z_o\Delta}$$

$$y_{21} = \frac{-2s_{21}}{Z_o\Delta}$$

$$y_{22} = \frac{(1 + s_{11})(1 - s_{22}) + s_{12}s_{21}}{Z_o\Delta}$$

$$\Delta = (1 + s_{11})(1 + s_{22}) - s_{12}s_{21}$$

Modeling Inductor from y-parameter



$$y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = Y_1 + Y_2$$

$$y_{12} = \left.\frac{i_1}{v_2}\right|_{v_1=0} = -Y_1$$

$$y_{21} = \left.\frac{i_2}{v_1}\right|_{v_2=0} = -Y_1$$

$$y_{22} = \left.\frac{i_2}{v_2}\right|_{v_1=0} = Y_1 + Y_3$$

Conclusion

- Basic concept of VCO is discussed.
- Design procedure of a 2.4GHz VCO for Bluetooth application is presented.
- Testing result of the circuit is provided.