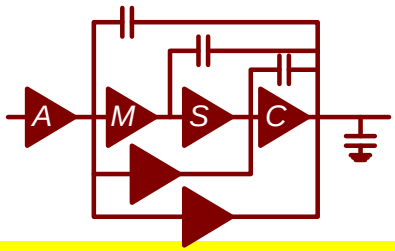


Analog and Mixed-Signal Center

Frequency Synthesizers for Communication Systems

Part of this material came from courtesy of Ari Valero

Outline

- Introduction
- Linear model
- Charge Pump PLL
- Performance Metrics
- Design Methodology

What is a PLL?

- From a communications point of view, a phase-locked loop is an optimum phase estimator
- For an input $r(t)=A\sin(\omega t + \phi)$, the PLL provides an estimate $A\sin(\omega t + \phi_{ML})$

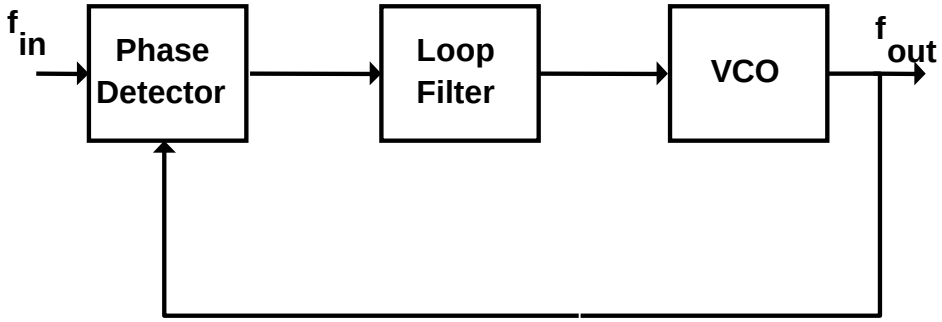
How does it work?

- Inject sinusoidal signal into the reference input
- The internal oscillator locks to the reference
- Frequency and phase differences between the reference and internal sinusoid = *k* or 0
- Internal sinusoid then represents a filtered version of the reference sinusoid

Where is it used?

- Frequency Synthesis
  - Reference frequency for modulation and demodulation
  - Clock reference
  - Radio, Television
- Clock Recovery
  - Serial interfaces (Computers, optical networks)
- FM demodulation
  - Radio

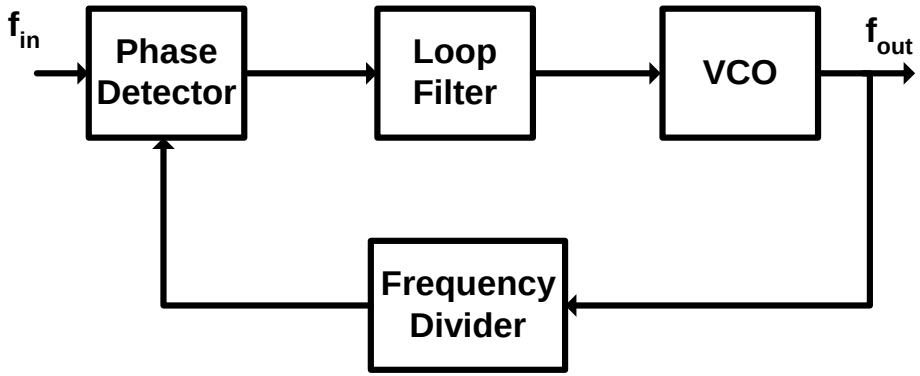
What does it look like?



- Phase Detector (PD). Nonlinear block that provides the phase difference between the input and oscillating signal
- Loop Filter (LPF). Eliminates high order harmonics of PD output and helps to stabilize the loop
- Voltage Controlled Oscillator (VCO). Nonlinear device that generates a sinusoidal signal whose frequency is controlled by its DC input.
- Feedback interconnection. The output of the VCO is fed to the Phase Detector to generate a phase error signal. This phase error signal controls the oscillation frequency of the VCO.

How can we implement a Frequency Synthesizer with a PLL?

If a frequency divider is introduced in the feedback interconnection, the frequency of the reference input is multiplied by the feedback factor at the output of the PLL



From a fixed reference frequency (f_{in}) a large set of output frequencies (f_{out}) can be generated

$$f_{out} = N \cdot f_{in}$$

N Integer -> Integer-N Frequency Synthesizer
N Fractional -> Fractional-N Frequency Synthesizer

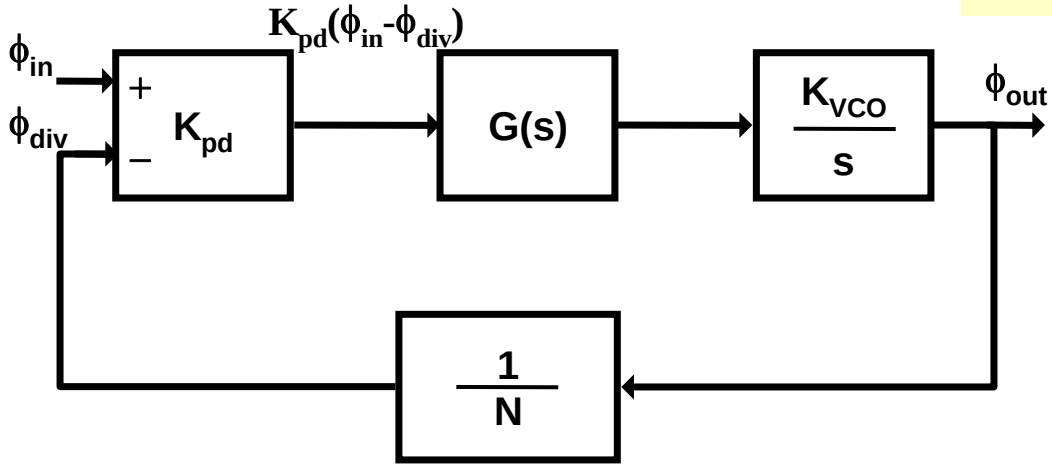
Linear Model

A PLL depends on nonlinear operations to work properly

To analyze its behavior we need to limit the analysis to the locked state

The following phase domain model provides a way to study the characteristics of operation of the loop

The loop is considered locked when the phase and frequency of the feedback (divided VCO output) is exactly equal to the average phase and frequency of the input



The output of the phase detector is:

$$V_{PFD} = K_{PD}\Delta\phi$$

Where the phase difference is:

$$\Delta\phi = \phi_{in} - \phi_{div}$$

The output of the VCO is:

$$f_{VCO}(t) = K_{VCO}V_{ctrl}(t)$$

Integrating both sides

$$\phi_{VCO}(t) = K_{VCO}\int_0^t V_{ctrl}(t)dt$$

In s-domain the VCO transfer function becomes:

$$G_{VCO}(s) = \frac{\Phi_{VCO}(s)}{V_{ctrl}(s)} = \frac{K_{VCO}}{s}$$

The Loop Filter transfer function:

$$G(s)$$

PLL Transfer Function

The closed loop transfer function:

$$H_{out}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = N\frac{K_{PD}K_{VCO}G(s)}{Ns + K_{PD}K_{VCO}G(s)}$$

The transfer function from phase error to output:

$$H_{\Delta\phi}(s) = \frac{\Phi_{out}(s)}{\Phi_{\Delta\phi}(s)} = N\frac{K_{VCO}G(s)}{Ns + K_{PD}K_{VCO}G(s)}$$

The order of a PLL is defined by the number of poles in the open and closed loop transfer functions and the type of a PLL indicates the number of perfect (lossless) integrators in the loop

Hold Range: the frequency range over which the PLL is able to statically maintain phase tracking: $\Delta\omega_H = K_{PD}K_{VCO}G(0)$.

Lock Range: the frequency range within which the PLL locks within one single-beat note between the reference frequency and output frequency: $\Delta\omega_L \approx \pm K_{PD}K_{VCO}G(\infty)$.

The Pull-In and Pull-Out Range: The pull-in range, $\Delta\omega_P$, is defined as the frequency range in which the PLL will always become locked. The pull-out range, $\Delta\omega P_O$, is defined as the limit of dynamic stability for the PLL. No simple relationships for these.

Type – I PLL

For a Type-I PLL with different Loop Filters G(s) we have the following responses

$$G(s) = G_1(s) = 1$$

$$H_{out1}(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = N\frac{K_{PD}K_{VCO}}{Ns + K_{PD}K_{VCO}}$$

$$G(s) = G_2(s) = \frac{1}{s\tau + 1}$$

$$H_{out2}(s) = \frac{K_{PD}K_{VCO}/\tau}{s^2 + s/\tau + K_{PD}K_{VCO}/N\tau}$$

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N\tau}}$$

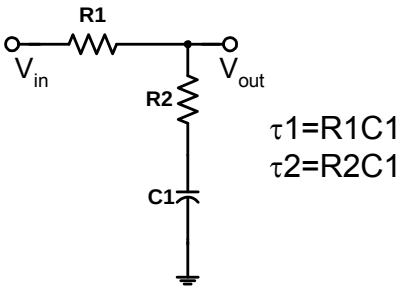
$$\xi = \frac{1}{2}\sqrt{\frac{N}{\tau K_{PD}K_{VCO}}}$$

$$G(s) = G_3(s) = \frac{s\tau_2 + 1}{s(\tau_1 + \tau_2) + 1}$$

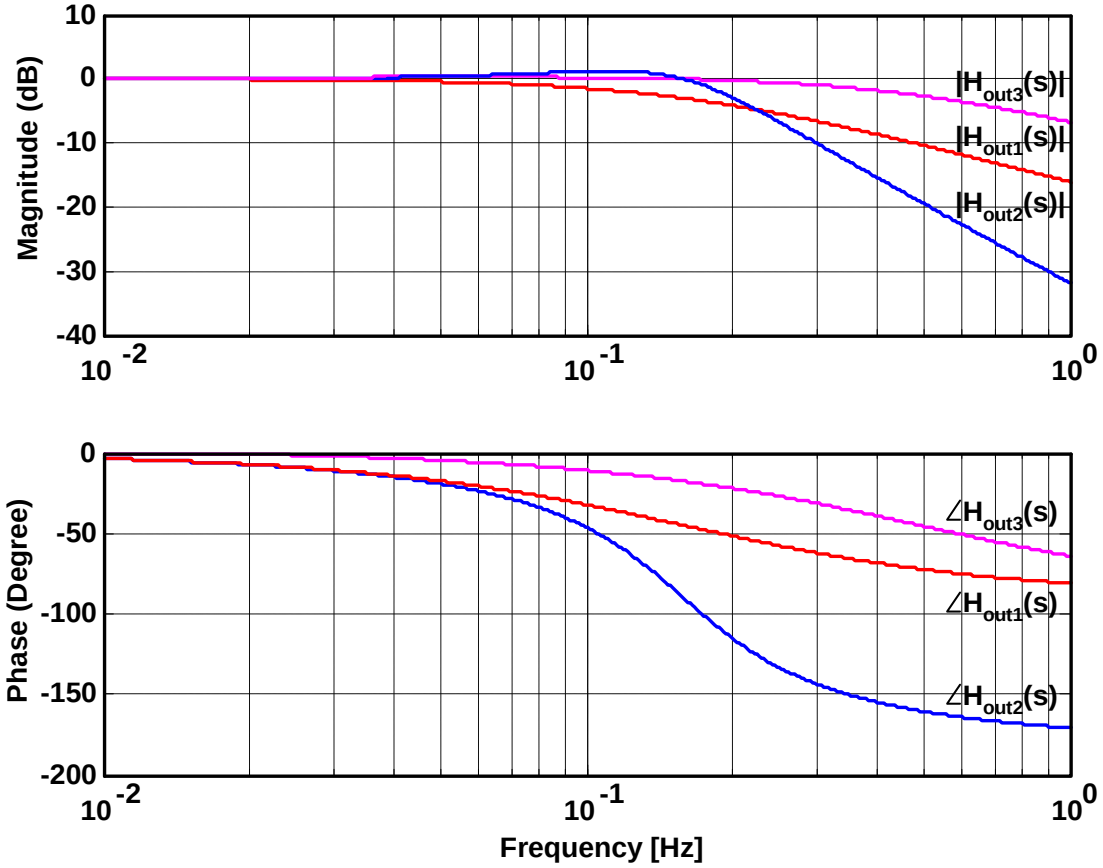
$$H_{out3}(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1 + \tau_2)}}$$

$$\xi = \frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1 + \tau_2)}} + \left(\tau_2 + \frac{N}{K_{PD}K_{VCO}}\right)$$



Type – I PLL

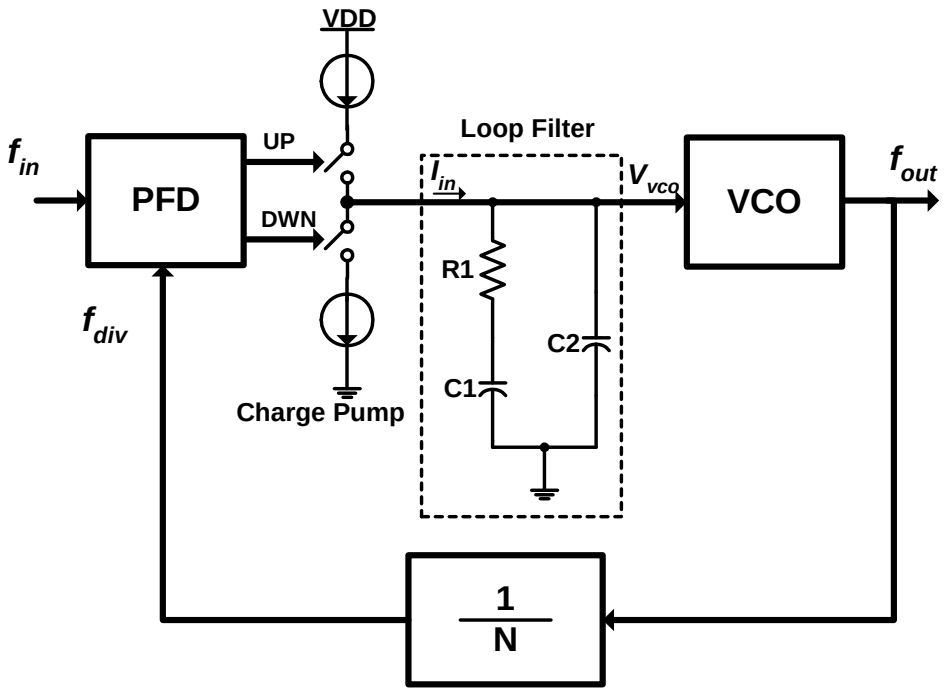


A drawback of type-I phase-locked loops is that it is not possible to set independently the loop bandwidth ω_n, the damping factor ξ and the loop gain $K_{PD}K_{VCO}$

Comparison of the closed loop transfer function of the PLL for the three previous loop filters

Charge Pump PLL (Type-II)

A type-II PLL is the most commonly used for frequency synthesizer applications, it is also known as charge-pump PLL



Advantages:

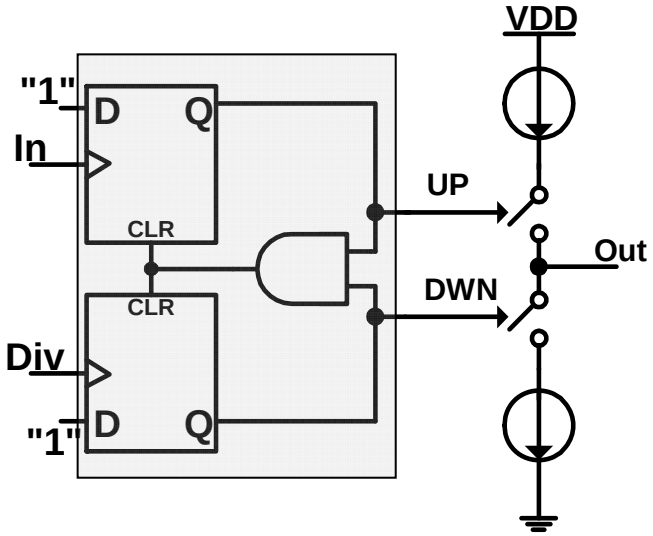
- Increased locking range
- Speed up in capture process
- Phase Frequency Detector (PFD) – Charge Pump (CP) combination creates extra pole at zero frequency
- This pole provides infinite gain at DC, which results in zero phase error in ideal locked state

Disadvantages:

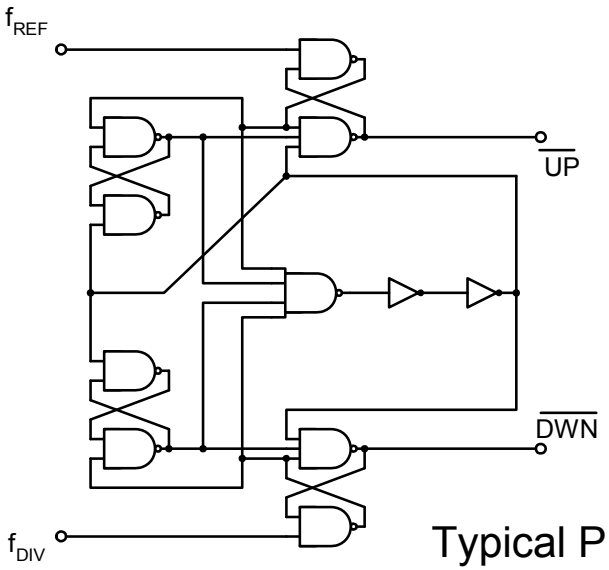
- Sampled operation introduces spurious tones at the VCO output
- Loop bandwidth limited by stability considerations

Note: This PLL is also known as Digital PLL since the phase comparison and frequency division are performed digitally

Phase-Frequency Detector



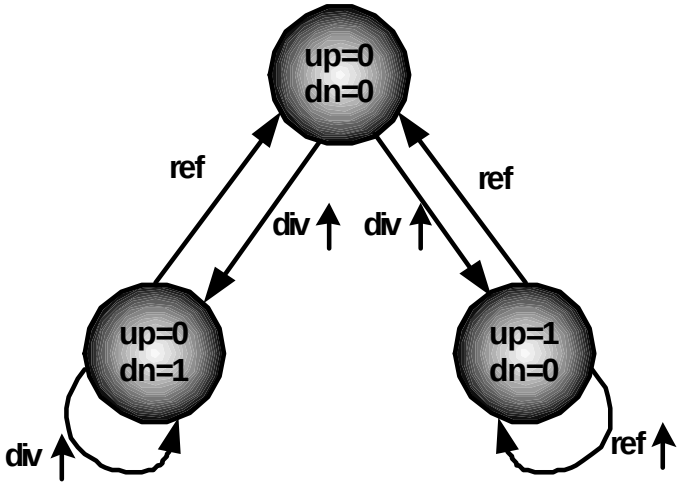
Conceptual PFD-CP



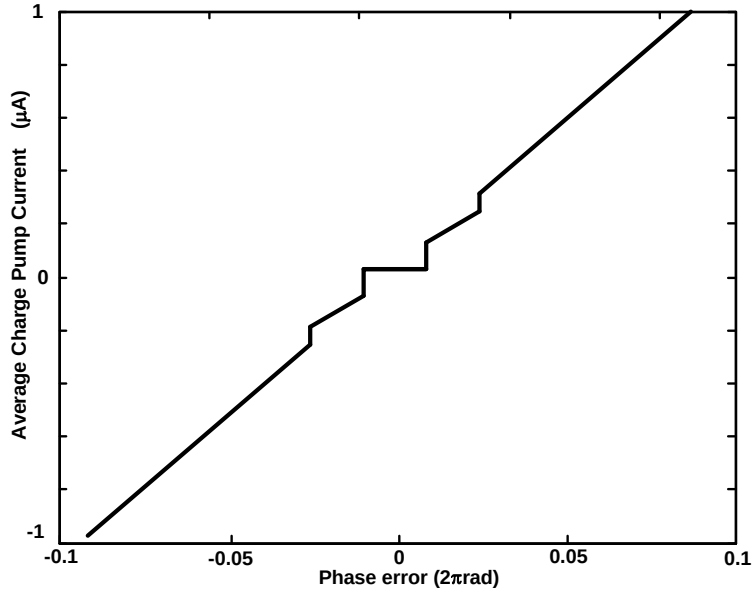
Typical PFD implementation

- Compares edges of reference and divided clocks.
- If reference clock leads the divided clock, the UP signal is asserted.
- If the divided clock leads the reference clock , the DWN signal is asserted.
- In an ideal PFD no pulses are present at the output in the locked state.
- Duty cycle of inputs is not relevant to the circuit operation.
- The width of the UP/DWN pulses is proportional to the phase difference between the clock inputs.

- In practical PFD the delay of the gates creates non-idealities in the phase input/output characteristic.
- The PFD can no longer resolve very small phase errors, and a dead zone is created.
- To solve this problem, extra delay is introduced in the feedback path of reset signal.

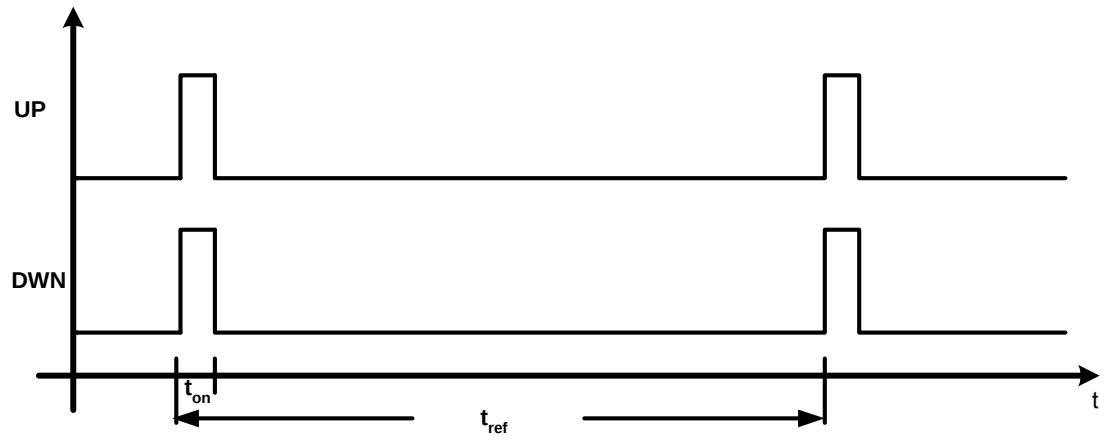


State machine of PFD



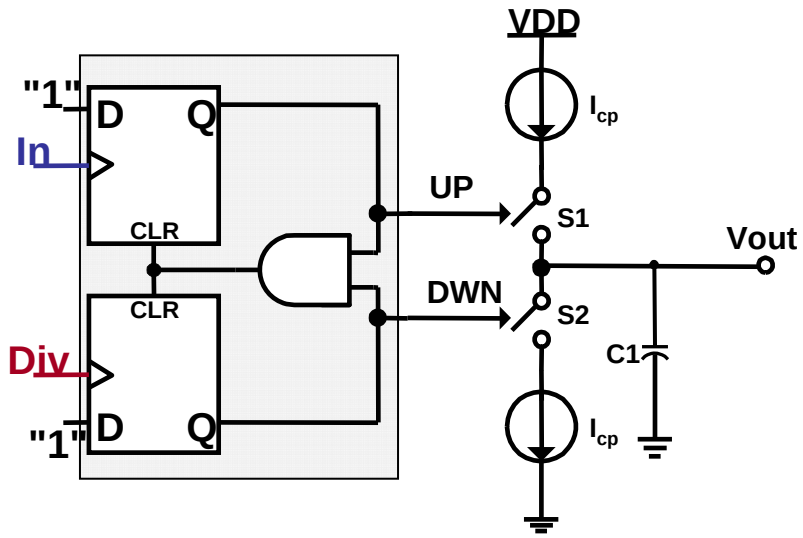
Phase response of PFD with dead zone

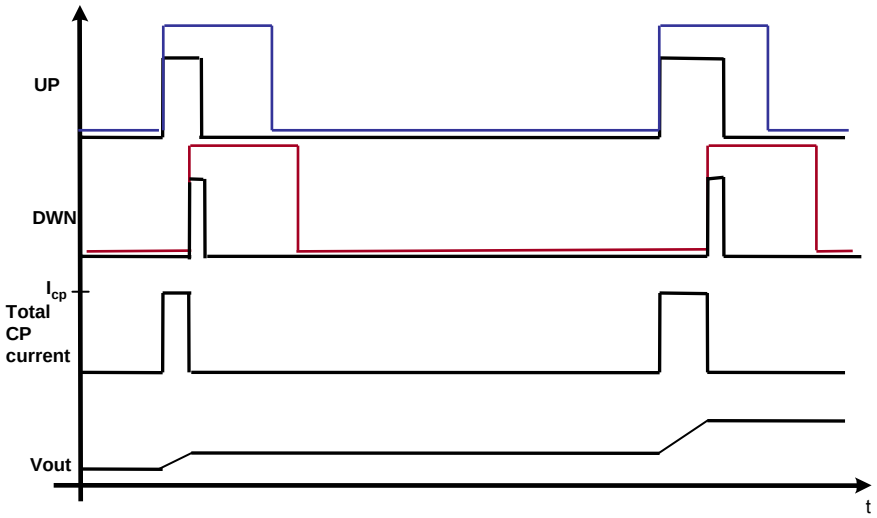
- In locked state, narrow pulses are generated in both UP/DWN outputs.
- The width of these pulses determines the amount of noise introduced to the VCO output by the charge-pump.
- Timing mismatch between the UP/DWN pulses is a source of spurious tones.



Output of PFD for locked state

Charge Pump





- The Charge-Pump converts the phase error information provided by the PFD into a voltage that controls the VCO frequency.
- If the UP input is asserted, S1 is closed and charge is injected into capacitor C1, increasing voltage Vout
- If the DWN input is asserted, S2 is closed and charge is extracted from capacitor C1,decreasing voltage Vout

Charge Pump

Calculating the Detector Gain:

The time the UP/DWN signals are asserted is:

$$t_{up} = \frac{\Delta\phi \cdot T}{2\pi}$$

Where T is the reference period and $\Delta\phi$ is the phase difference measured by the PFD.

The average current provided by the charge pump for a given $\Delta\phi$ is:

$$\bar{I}_{pd} = I_{cp} \frac{t_{up}}{T} = \frac{I_{cp}}{2\pi} \Delta\phi$$

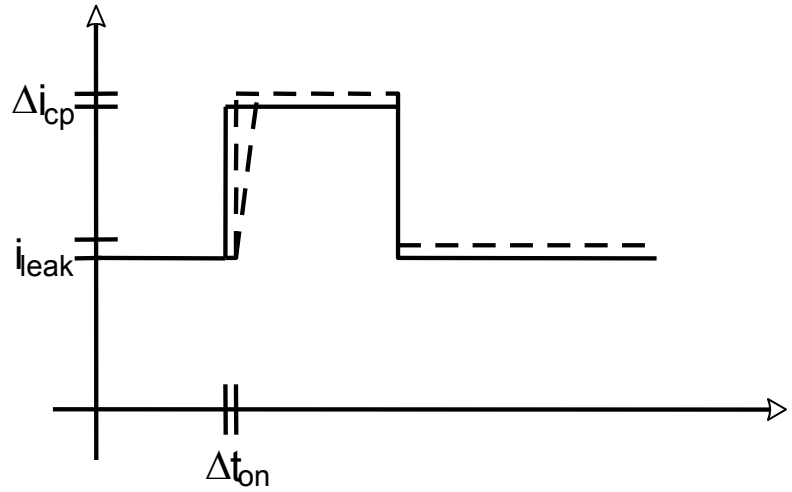
Which gives an overall phase detector gain K_{pd} of:

$$K_{pd} = \frac{I_{cp}}{2\pi}$$

Capacitor *C1* is the main integrating capacitor; it generates the pole at zero frequency. Resistor *R1* introduces a stabilizing zero. Capacitor *C2* is added to the loop filter to reduce the glitches on the VCO control voltage

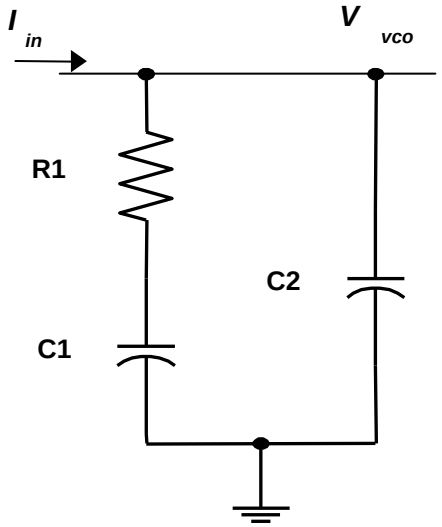
Non-ideal effects of charge pumps

- Current mismatch
  - Mismatch between source and sink currents in the charge pump introduces a finite phase error.
- Current leakage
  - When the source/sink currents are off, leakage currents can flow and modify the VCO control voltage of the VCO by charging/discharging the loop filter. Spurs are introduced.
- Charge sharing
  - Parasitic capacitances from the switches share charge with the loop filter when the nodes they are connected to have a large change in their voltage.
- Charge injection
  - Occurs when switches are turned off and the charge in their channels is injected/extracted to the loop filter. Spurs are introduced



Loop Filter Characteristics

- The PFD-CP and C1 combination introduces a pole at zero frequency.
- This pole, along with the zero generated by the VCO generates -40dB/decade loop gain at low frequency.
- If the loop gain crosses 0dB with a slope of -40dB, then the circuit is unstable.
- In order to stabilize the circuit, resistor R1 is introduced in series with C1 to create a zero.
- The zero at ω_z reduces the slope of the loop gain to -20dB/decade and stabilizes the circuit.
- Capacitor C2 is added to reduce ripples in the VCO control voltage. Adds a second pole ω_{p2} to the loop filter.
- An extra (third) pole can be added to further eliminate VCO ripple, at the expense of phase margin degradation (stability)



$$\omega_z = \frac{1}{R_1 C_1}$$

$$\omega_{p2} = \frac{1}{R_1 \dfrac{C_1 C_2}{C_1 + C_2}} \approx \frac{1}{R_1 C_2}$$

Loop Filter

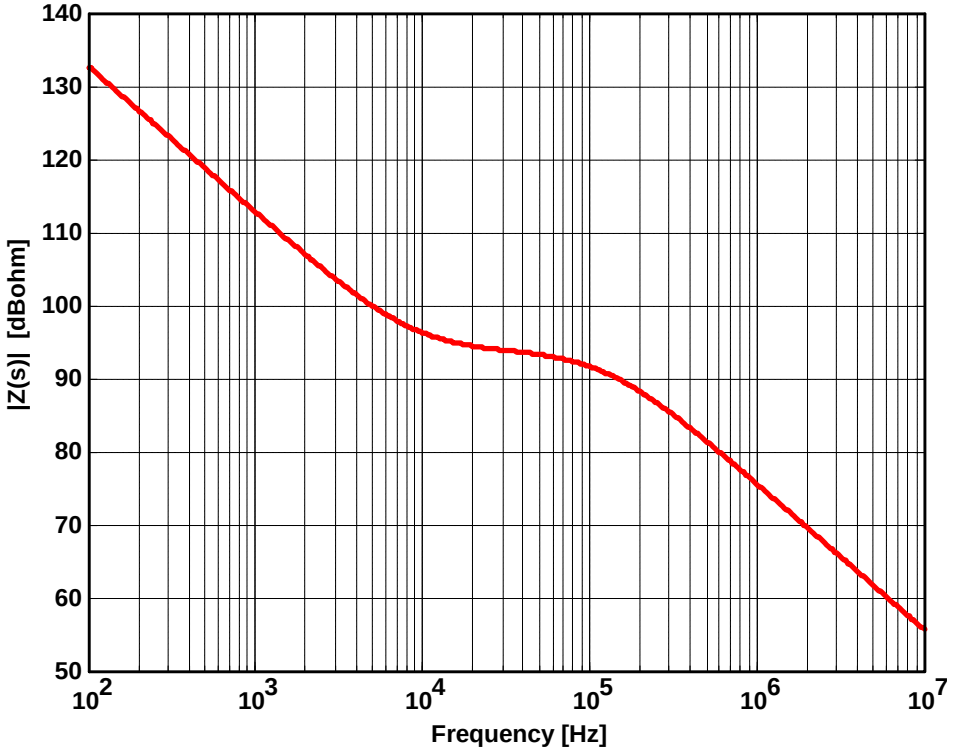
The transimpedance of loop filter is:

$$Z(s) = \frac{V_{VCO}}{I_{in}} = R_1 \frac{1 + sR_1C_1}{s\left[R_1C_1R_1C_2s + R_1(C_1 + C_2)\right]}$$

And the open loop transfer function of the PLL

$$H_{ol}(s) = \frac{\phi_{div}}{\phi_{in}} = \frac{K_{PD}K_{VCO}Z(s)}{N}$$

$$= \frac{K_{VCO}I_{cp}}{2\pi N} R_1 \frac{1 + sR_1C_1}{s\left[R_1C_1R_1C_2s + R_1(C_1 + C_2)\right]}$$



Transimpedance of loop filter

The crossover frequency (0dB gain in the $H_{ol}(s)$)

$$\omega_c = \sqrt{\omega_z \cdot \omega_{p2}} = \omega_z \sqrt{\frac{C_1}{C_2} + 1}$$

The phase margin

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right)$$

The phase margin, zero and pole frequency can be written as a function of the capacitor ratio C1/C2

$$\phi_m = \tan^{-1}\left(\sqrt{\frac{\omega_{p2}}{\omega_z}}\right) - \tan^{-1}\left(\sqrt{\frac{\omega_z}{\omega_{p2}}}\right)$$

$$\phi_m = \tan^{-1}\left(\sqrt{\frac{C_1}{C_2}+1}\right) - \tan^{-1}\left(\frac{1}{\sqrt{\frac{C_1}{C_2}+1}}\right)$$

$$\omega_z = \frac{\omega_c}{\sqrt{1+\frac{C_1}{C_2}}}$$

$$\omega_{p2} = \omega_c\sqrt{1+\frac{C_1}{C_2}}$$

With these values, the crossover frequency as a function of PLL parameters can be obtained.

This form of the equation assumes the crossover frequency is aligned with the maximum of the phase margin

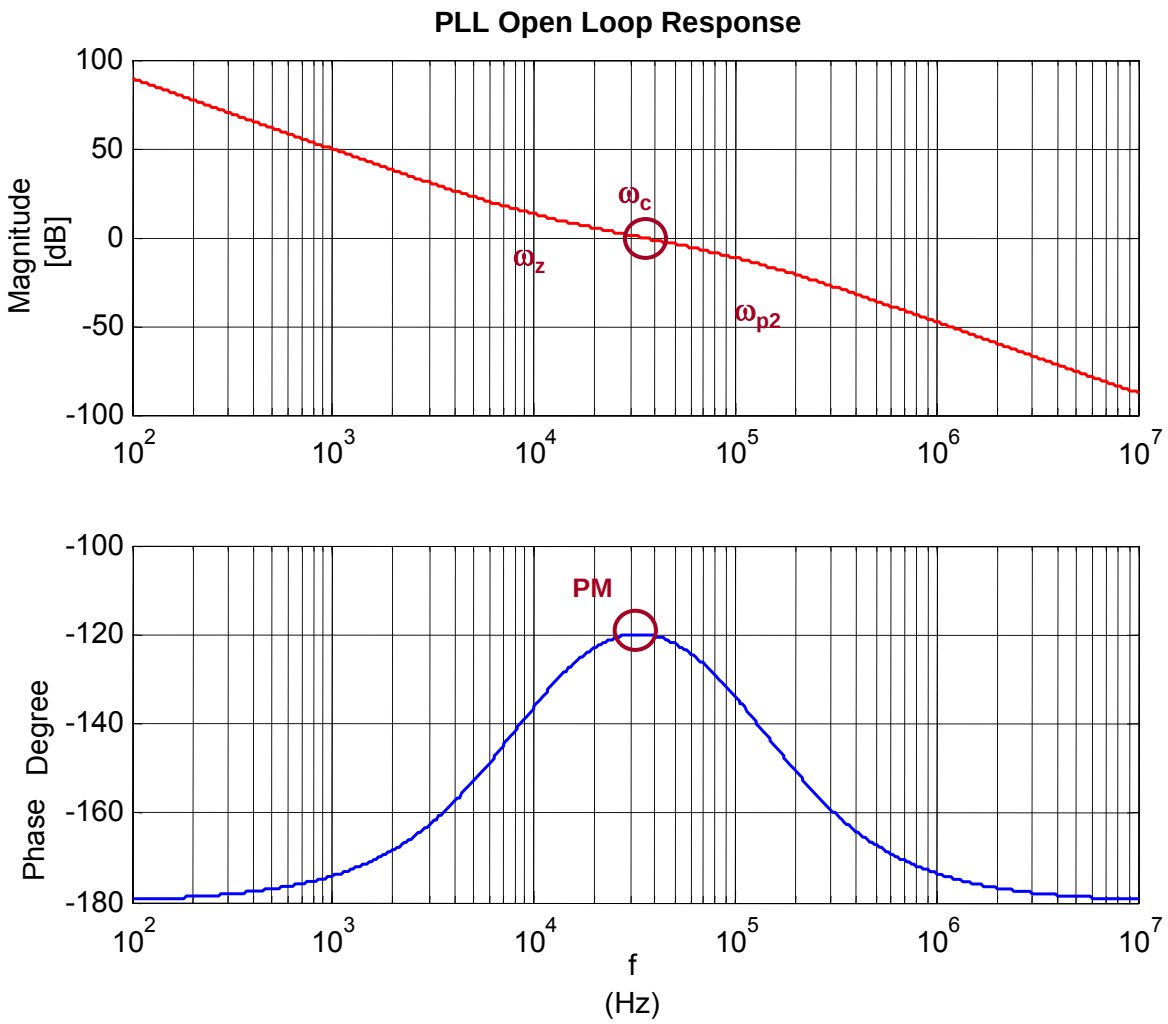
$$\omega_c = \frac{I_{cp}K_{vco}}{N}R_1\frac{C_1}{C_1+C_2} \approx \frac{I_{cp}K_{vco}R_1}{N}$$

This equation shows that the loop bandwidth is not a function of C1, but a function of R1, K_{vco}, I_{cp} and N.

In general, the crossover frequency Wc is equal to the loop bandwidth of the PLL.

The ratios between ω_c/ω_z and ω_{p2}/ω_c determine the phase margin and damping factor of the PLL.

Thus, the transient characteristics of the loop are set by them.



Plotting the open loop response of the PLL helps to determine graphically the crossover frequency and phase margin

Performance Metrics

The design of frequency synthesizers for RF systems involves complying to a large set of specifications, such as:

- Tuning Range and Frequency Resolution
- Phase Noise
- Spurious Signals
- Settling Time

Communication standards usually do not include particular block specifications. It is up to the system/circuit designer to obtain the proper circuit specifications for each building block

Frequency Resolution and Accuracy

The *frequency resolution* of the synthesizer is set by the required channel spacing of the intended application

The *frequency accuracy* is related with the maximum offset that the synthesized frequency can have, with respect to the desired center frequency

Standard	Tuning range (GHz)	Frequency Resolution	Frequency Accuracy
Bluetooth	2.400 – 2.479	1 MHz	± 75 kHz
IEEE 802.11a	5.150 – 5.350 5.750 – 5.850	20 MHz	± 60 kHz
IEEE 802.11b	2.400 – 2.479	5 MHz	± 60 kHz
IEEE 802.11g	2.400 – 2.479	20 MHz	± 60 kHz
DCS1800	1.710 – 1.785 1.805 – 1.880	200 kHz	± 5 kHz

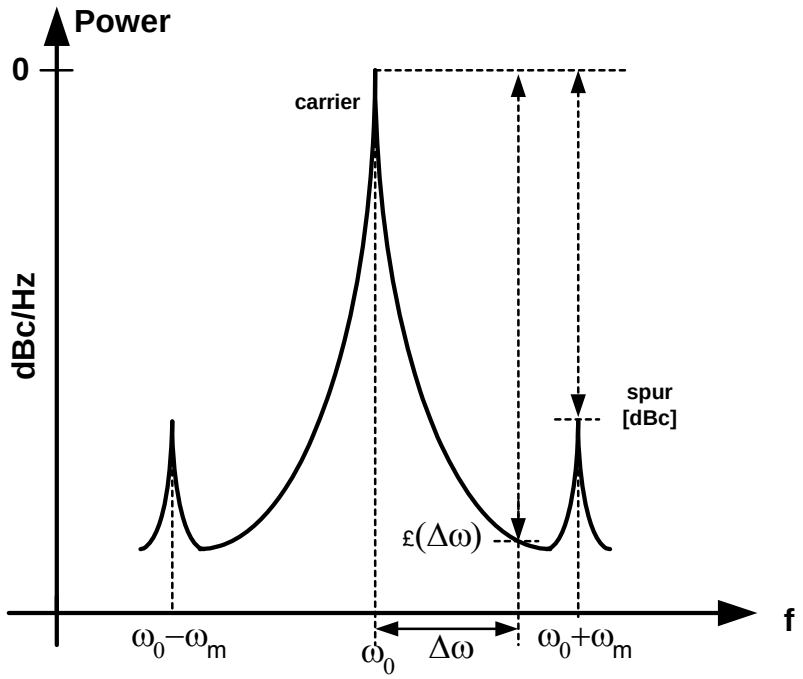
The *frequency resolution* affects the selection of synthesizer architecture (Integer / Fractional)

The *frequency accuracy* defines a boundary for settling time calculation

Phase Noise

Phase noise is a measure of the spectral purity of a signal and is one of the most important parameters for characterization of the synthesizer

Phase noise degrades the quality of the data in a communication system



Assume the PLL output is a sinusoidal tone at ω_0

$$v(t) = \left(1 + a(t)\right) \cdot \sin\left(\omega_0 t + \theta(t)\right)$$

with amplitude and phase variation *a(t)* and θ(t) respectively

θ(t) has a random part and a deterministic part

$$\theta(t) = \theta_r(t) + \theta_d \cdot \sin(\omega_d t)$$

The random part, $\theta_r(t)$, accounts for phase noise and the deterministic part, $\theta_d \cdot \sin(\omega_d t)$, for spurious tones

Phase Noise (continued..)

Assuming the phase variations are a single tone in the phase, $\theta(t) = \theta_m \cdot \sin(\omega_m t)$, and the root mean square (rms) value of $\theta(t)$ is much smaller than 1 radian, the output of the oscillator becomes:

$$v_{osc}(t) \approx A \cdot \sin(\omega_0 t) + A\frac{\theta_m}{2}\left[\sin\left((\omega_0 + \omega_m)t\right) + \sin\left((\omega_0 - \omega_m)t\right)\right]$$

the output spectrum of the oscillator contains a narrowband FM signal with a modulation index θm and a strong component at the fundamental frequency $\omega 0$

The oscillator output voltage power spectral density (PSD) is related to the phase noise PSD

$$S_V(\omega) = \frac{A^2}{2}\left[\delta(\omega - \omega_0) + \frac{1}{2}S_\theta(\omega - \omega_0) + \frac{1}{2}S_\theta(\omega_0 - \omega)\right]$$

$$S_\theta(\omega) = \frac{\theta_m^2}{2}\delta(\omega - \omega_m)$$

The phase noise skirt is directly translated to noise side lobes at both sides of the carrier frequency

Phase Noise (continued..)

Phase noise $£\{\Delta\omega\}$ is defined as the ratio of the noise power, in a bandwidth of 1 Hz at a certain offset frequency $\Delta\omega$ from ω_0, to the carrier power $P_{carrier}$

$$£\{\Delta\omega\} = 10\log\frac{P_{noise}(\text{1Hz band at } \Delta\omega)}{P_{carrier}}$$

The actual phase noise at an offset ω_m is:

$$£\{\Delta\omega\} = 10\log\left(\frac{S_V(\omega_0+\omega_m)}{A^2/2}\right) = 10\log\left(\frac{S_\theta(\omega_m)}{2}\right) \quad [dBc]$$

The units dBc/Hz refer to the ratio between the noise and the carrier in dB in a bandwidth of 1 Hz.

Phase Noise (continued..)

The phase noise at the output of the VCO comes from

- Reference clock
- Phase-Frequency Detector
- Charge Pump
- Loop Filter
- Frequency Divider
- VCO Active Devices Noise

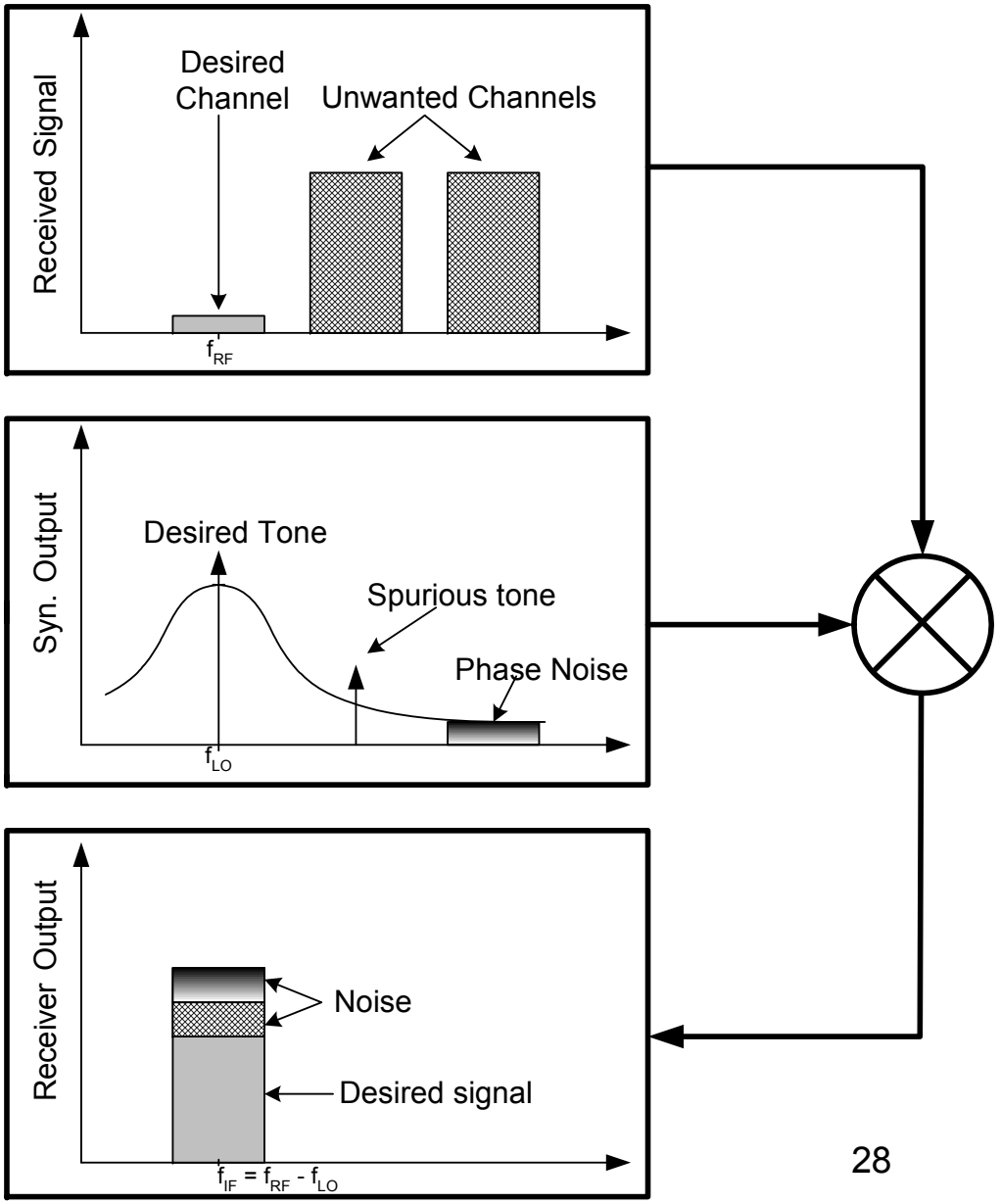
Due to this noise, the output of the VCO is no longer a single frequency tone, but a smeared version

Sometimes the energy is concentrated at frequencies other than the desired frequency, appearing as a spike above the skirt. This energy is due to a spurious tone.

Effect of Phase Noise in Received Signal

Phase Noise and Spurious Tones are mixed with adjacent channels and degrade the desired downconverted signal.

The unwanted channels may be much larger than the desired channel (as much as 40dB for Bluetooth), setting stringent requirements for phase noise and spurious signals.



Phase Noise Specification

The total noise, P_{noise}, in a channel with bandwidth f_{BW}, blocker power P_{blk} at an offset frequency $\Delta\omega$ from the desired channel and a phase noise $\pounds\{\Delta\omega\}$ *is*

The equation assumes that the phase noise is constant (white) in the channel bandwidth

$$P_{noise}(\text{dBm}) = P_{blk}(\text{dBm}) + f_{BW}(\text{dBHz}) + \pounds\{\Delta\omega\}(\text{dBc/Hz})$$

The signal-to-noise ratio (SNR) of the downconverted signal is:

$$\text{SNR(dB)} = P_{IF}(\text{dBm}) - P_{noise}(\text{dBm})$$

$$\text{SNR(dB)} = P_{sig}(\text{dBm}) - \left[P_{blk}(\text{dBm}) + \pounds\{\Delta\omega\}(\text{dBc/Hz}) + f_{BW}(\text{dBHz})\right]$$

For a minimum received signal P_{sig_min}, maximum blocker signal P_{blk_max} and minimum required *SNR*, the phase noise specification can be determined as:

$$\pounds\{\Delta\omega\}(\text{dBc/Hz}) < P_{sig\_\min}(\text{dBm}) - P_{blk\_\max}(\text{dBm}) - f_{BW}(\text{dBHz}) - \text{SNR(dB)}$$

Phase Noise Numerical Example

For Bluetooth the carrier-to-interferer ratio at a 3MHz offset is 40dB, the SNR is 16dB, the channel bandwidth is 1MHz. With these values the phase noise can be calculated

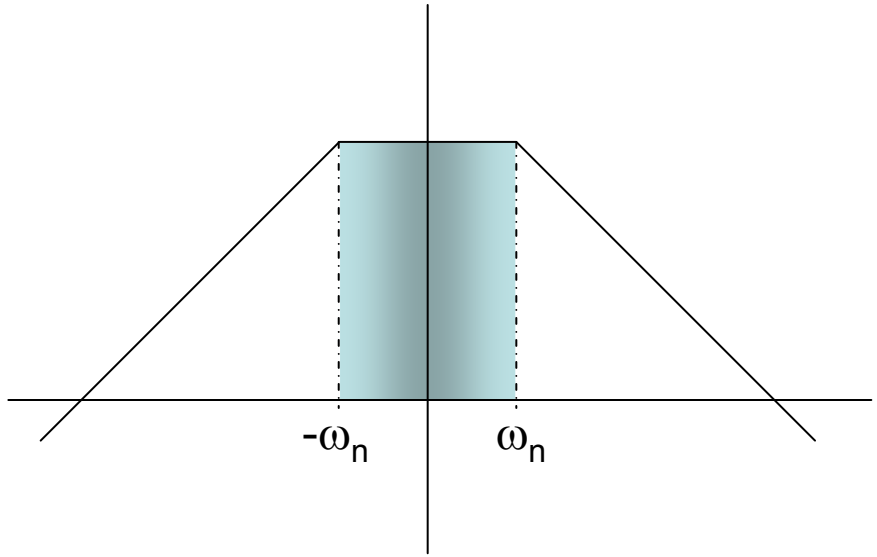
$$£\{3MHz\}(\text{dBc/Hz}) < -40dB - 10\log(1e6Hz) - 16dB$$
$$£\{3MHz\} < -116dBc/Hz$$

A margin has to be added to the obtained value since there are more contributions to the degradation of the signal to noise ratio (SNR), generally this margin is related to the overall noise figure of the system and can be as large as 4dB

Close-in Phase Noise

The close-in phase noise is the portion of the phase noise located very close to the oscillator center frequency

It is usually dominated by the noise of the reference signal and is typically constant over the loop bandwidth (ω_n)



$$£_i(\text{dBc/Hz}) < -10\log(4\omega_n)(\text{dBHz}) - \text{SNR(dB)}$$

The term $4\omega_n$ accounts for the double sided noise around the fundamental tone of the oscillator and the contribution to the phase noise of the reference at frequencies higher than the loop bandwidth

Spurious Signals

The periodic phase variation at the output of the oscillator generates spurious tones (also named spurs)

Spurs are generated due to the sampled nature of the charge-pump PLL.

The spur specification is calculated in a similar fashion as the phase noise, but now the noise is concentrated in a single frequency, instead of being smeared in the channel bandwidth.

$$\mathrm{spur}(\Delta\omega)(\mathrm{dBc}) < P_{sig\_\min}(\mathrm{dBm}) - P_{blk\_\max}(\mathrm{dBm}) - \mathrm{SNR}(\mathrm{dB})$$

For Bluetooth the carrier-to-interferer ratio at a 2MHz offset is 30dB, the SNR is 16dB and the spur results in:

$$\mathrm{spur}(2MHz)(\mathrm{dBc}) < -30(\mathrm{dBm}) - 16(\mathrm{dB})$$
$$\mathrm{spur}(2MHz) < -46dBc$$

Effect of non-idealities on spurious signals

Recall that the oscillator output modulated by a sinewave of baseband frequency f_m generates a pair of frequency components – the spurious signals, at a distance $\pm f_m$ from the carrier frequency f_0

$$v_{osc}(t) \approx A \cdot \sin(\omega_0 t) + A_{sp} \frac{\theta_m}{2} \left[\sin\left((\omega_0 + \omega_m)t\right) + \sin\left((\omega_0 - \omega_m)t\right) \right]$$

The previous equation also shows that the amplitude of the spurious signals A_{sp} is related to the amplitude of the carrier signal A and to the peak phase deviation θ_m by

$$A_{sp} = A \frac{\theta_m}{2}$$

To calculate the magnitude of the spurious tones we need to determine the maximum phase variation as a function of the amplitude at the tuning line of the VCO, A_m

spurious signals continued . .

$$\theta_m = \left| K_{vco} \int_0^{\tau} A_m \cos(\omega_{ref}\tau) d\tau \right|_{\max} = \frac{K_{vco} A_m}{\omega_{ref}}$$

The amplitude of the undesired spurious tone in decibel with respect to the magnitude of the carrier can be obtained

$$\left[\frac{A_{sp}}{A} \right]_{dBc} = 20 \log\left(\frac{\theta_m}{2} \right)$$

$$= 20 \log\left(\frac{K_{vco} A_m}{2\omega_{ref}} \right)$$

The maximum tuning line ripple A_m for a given spurious specification $[A_{sp}/A]$ dBc is:

$$\mathrm{A_m} = \frac{2\omega_{ref}}{K_{vco}} 10^{\frac{\left[\frac{A_{sp}}{A} \right]_{dBc}}{20}}$$

There are two main effects which can generate reference spurious:

1. **Leakage current in loop filter and charge-pump**

If the charge-pump current I_{out} is considered as a periodic pulse train, the Fourier series representation is

$$I_{out}(t) = I_{leak} + 2I_{leak}\sum_{n=1}^{\infty}\cos(2\pi n f_{ref} t)$$

The amplitude of the ripple signal generated by the leakage current at the reference frequency Am is

$$A_m = 2I_{leak}\left|Z(j\omega_{ref})\right| \longrightarrow \left[\frac{A_{sp}}{A}\right]_{dBc} = 20\log\left(\frac{I_{leak}\left|Z(j2\pi f_{ref})\right|K_{vco}}{2\pi f_{ref}}\right)$$

The relative amplitude of the spurious signals does not depend on the absolute bandwidth of the loop filter or on the charge-pump current *Icp*.

It is only a function of the transimpedance of the loop filter Z(s), the VCO gain *Kvco* and the absolute magnitude of the leakage current I_{leak}.

2. Mismatch in the charge-pump Up and Down current sources

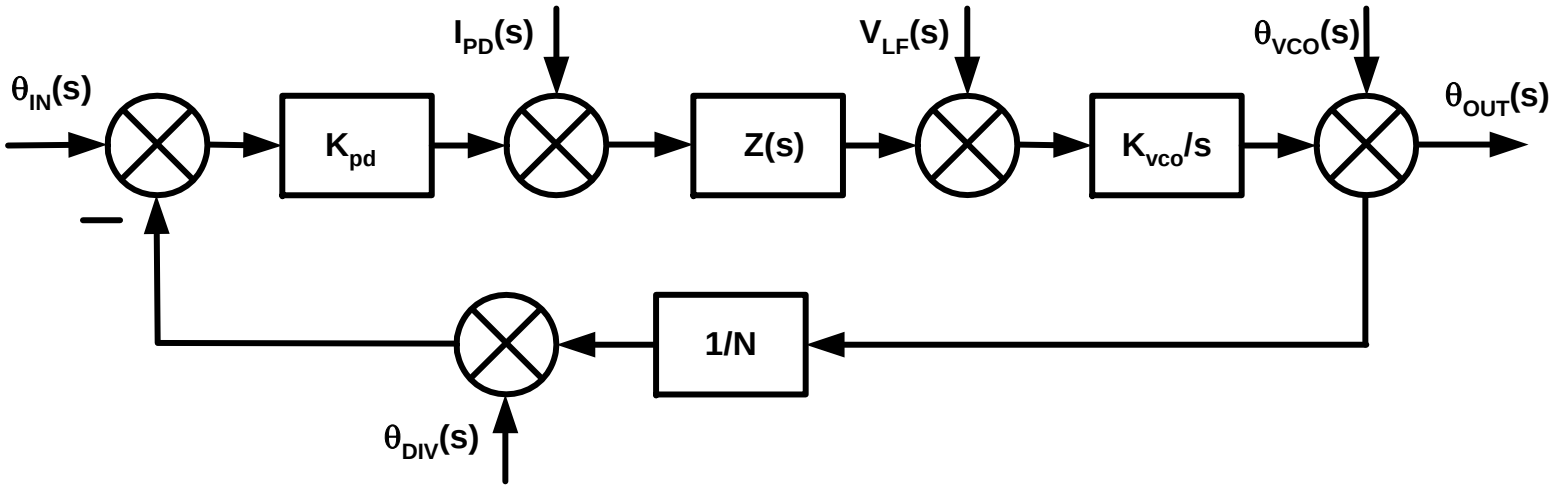
Similar calculations can be performed to obtain the magnitude of the spurious tone as a function of the mismatch of charge-pump currents

The Fourier series of the current waveform must be obtained and the fundamental tone of I_{out} obtained.

$$\left[\frac{A_{sp}}{A}\right]_{dBc} = 20\log\left(\frac{I_{out}\left|Z(j2\pi f_{ref})\right|K_{vco}}{4\pi f_{ref}}\right)$$

The previous results are very important, since they allow the designer to estimate the spurious tone magnitude during the initial design of the charge-pump and without the need of close loop simulations

Phase Noise in a PLL



$$H_{LP}(s) = \frac{\theta_{OUT}(s)}{\theta_{IN}(s)} = \frac{N \cdot K_{pd} K_{vco} Z(s)}{N \cdot s + K_{pd} K_{vco} Z(s)}$$

At very low frequencies $N \cdot s << KpdKvcoZ(s)$ and $H_{LP}(s) \approx N$

$$H_{VCO}(s) = \frac{\theta_{OUT}(s)}{\theta_{VCO}(s)} = \frac{N \cdot s}{N \cdot s + K_{pd} K_{vco} Z(s)}$$

For frequencies above the loop bandwidth, $N \cdot s << KpdKvcoZ(s)$ and $\lim_{s \to \infty} HVCO(s) = N$

$$H_{LF}(s) = \frac{\theta_{OUT}(s)}{V_{LF}(s)} = \frac{N \cdot K_{vco}}{N \cdot s + K_{pd} K_{vco} Z(s)}$$

bandpass characteristic and presents peaking at frequencies around the loop bandwidth

- VCO highpass
- REF lowpass

Settling time

DEFINITION: The time required for the PLL to change its output frequency from fout(0) to fout(∞) within a frequency error smaller or equal to ε

$$\varepsilon \geq \left| f_{out}(t) - f_{out}(\infty) \right|$$

Applying a change in the reference frequency from *fref* to and leaving the divider ratio N unchanged also provides the same VCO output frequency *(N+ΔN)fref*

The output frequency of the VCO

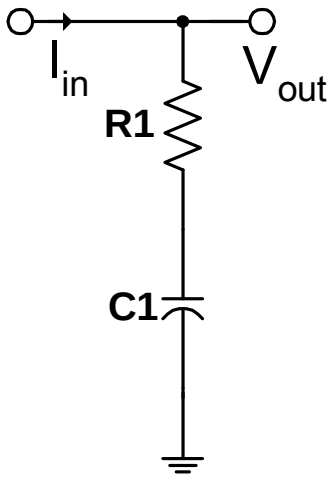
$$f_{out} = (N + \Delta N) f_{ref} = N\left\{\left(1 + \frac{\Delta N}{N}\right) f_{ref}\right\}$$

The closed loop transfer function is:

$$H(s) = \frac{N\left(2\zeta\omega_n s + \omega_n^2\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

The filter used for the analysis contains one pole at the origin and one zero that stabilizes the loop

$$G(s) = K_f \frac{1 + \tau s}{s}$$



Settling time (continued . . .)

where

$$\zeta = \frac{\tau}{2}\sqrt{\frac{K_{pd}K_f K_{vco}}{N}} = \frac{\sin(\phi_m)}{2\sqrt{\cos(\phi_m)}}$$

$$\omega_n = \sqrt{\frac{K_{pd}K_f K_{vco}}{N}} = \omega_c\sqrt{\cos(\phi_m)}$$

The steady state frequency can be found using the final value theorem

$$\Delta f_{out}(\infty) = f_{out}(\infty) - f_{ref} = \lim_{s\to 0} s\left[\frac{\Delta N f_{ref}}{N\cdot s}H(s)\right] = \Delta N f_{ref}$$

The PLL responds to the input frequency step as

$$\Delta f_{out}(s) = f_{out}(s) - f_{ref} = \frac{\Delta N f_{ref}}{N\cdot s}H(s)$$

$$\Delta f_{out}(s) = \Delta N f_{ref}\frac{\left(2\zeta\omega_n s + \omega_n^2\right)}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)}$$

and the lock time can be calculated as:

$$t_{lock} = \left|L^{-1}\{\Delta f_{out}(s)\} - \Delta f_{out}(\infty)\right| < \varepsilon$$

$$t_{lock} = \left|L^{-1}\left\{\frac{\Delta N f_{ref}}{N\cdot s}H(s)\right\} - \Delta f_{out}(\infty)\right| < \varepsilon$$

Settling time (continued . . .)

Depending on the value of the damping factor ξ, there are three different cases

$0 < \xi < 1$	Underdamped
$\xi = 1$	Critically Damped
$\xi > 1$	Overdamped

The poles of the transfer function for each case are

$$\omega_{1,2} = \begin{cases} -\omega_n\left(\zeta \pm j\sqrt{1-\zeta^2}\right) & \zeta < 1 \\ -\zeta\omega_n & \zeta = 1 \\ -\omega_n\left(\zeta \pm j\sqrt{-\omega_n\left(\zeta \pm \sqrt{\zeta^2-1}\right)}\right) & \zeta > 1 \end{cases}$$

Decomposing the transfer function of *Δfout(s)* in partial fractions we obtain the general form

$$\Delta f_{out}(s) = \begin{cases} \dfrac{\Delta N f_{ref}}{s} + \dfrac{\dfrac{\Delta N f_{ref}\omega_1}{j2\sqrt{1-\zeta^2}\omega_n}}{s-\omega_1} + \dfrac{-\dfrac{\Delta N f_{ref}\omega_2}{j2\sqrt{1-\zeta^2}\omega_n}}{s-\omega_2} & \zeta < 1 \\ \dfrac{\Delta N f_{ref}}{s} + \dfrac{-\Delta N f_{ref}}{s+\omega_n} + \dfrac{\Delta N f_{ref}\omega_n}{(s-\omega_n)^2} & \zeta = 0 \\ \dfrac{\Delta N f_{ref}}{s} + \dfrac{\dfrac{\Delta N f_{ref}\omega_1}{j2\sqrt{\zeta^2-1}\omega_n}}{s-\omega_1} + \dfrac{-\dfrac{\Delta N f_{ref}\omega_2}{j2\sqrt{\zeta^2-1}\omega_n}}{s-\omega_2} & \zeta > 1 \end{cases}$$

Settling time (continued . . .)

Applying the inverse Laplace transformation

$$\Delta f_{out}(t) = \begin{cases} \Delta N f_{ref}\left(1+\dfrac{\omega_1 e^{-\omega_1 t}-\omega_2 e^{-\omega_2 t}}{j2\sqrt{1-\zeta^2}\,\omega_n}\right) & \zeta<1 \\ \Delta N f_{ref}\left(1-e^{-\omega_n t}(1-\omega_n t)\right) & \zeta=0 \\ \Delta N f_{ref}\left(1+\dfrac{-\omega_1 e^{-\omega_1 t}+\omega_2 e^{-\omega_2 t}}{2\sqrt{\zeta^2-1}\omega_n}\right) & \zeta>1 \end{cases}$$

Substituting in the equation for t_{lock} (page40), the frequency error ε becomes:

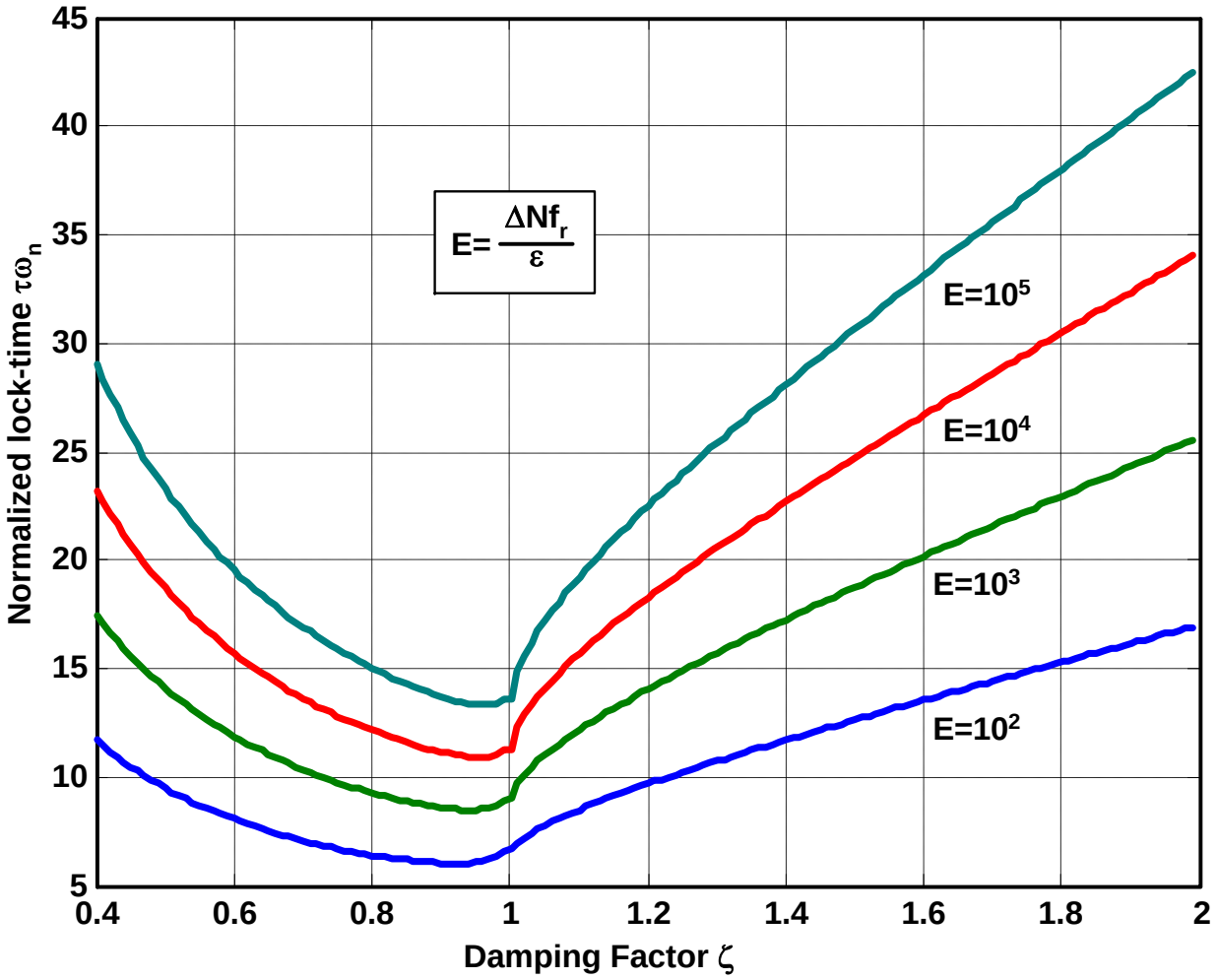
$$\varepsilon = \begin{cases} \Delta N f_{ref}\dfrac{e^{-\omega_n\zeta t}}{\sqrt{1-\zeta^2}}\sin\left(\omega_n\sqrt{1-\zeta^2}\,t-\tan^{-1}\dfrac{\sqrt{1-\zeta^2}}{\zeta}\right) & \zeta<1 \\ \Delta N f_{ref}e^{-\omega_n t}(1-\omega_n t) & \zeta=0 \\ \Delta N f_{ref}e^{-\omega_n\zeta t}\left(\cosh(\omega_n\sqrt{\zeta^2-1}t)+\dfrac{-\zeta}{\sqrt{\zeta^2-1}}\sinh(\omega_n\sqrt{\zeta^2-1}t)\right) & \zeta>1 \end{cases}$$

Settling time (concluded . . .)

Solving for t_{lock} we obtain expresions for the settling time for a given frequency step and error

$$t_{lock} = \begin{cases} \dfrac{\ln\left(\dfrac{\Delta N f_{ref}}{\varepsilon\sqrt{1-\zeta^2}}\right)}{\omega_n \zeta} & \zeta < 1 \\ \text{Solved numerically} & \zeta = 0 \\ \dfrac{1}{\left(\xi - \sqrt{\xi^2 - 1}\right)\omega_n} \ln \dfrac{\left(\Delta N f_{ref}\sqrt{\xi^2 - 1} + \xi\right)}{\varepsilon 2\sqrt{1-\xi^2}} & \zeta > 1 \end{cases}$$

Plot of the normalized lock-time $\tau\omega_n$ as a function of the damping factor ξ for several values of $\frac{\Delta N f_r}{\varepsilon}$

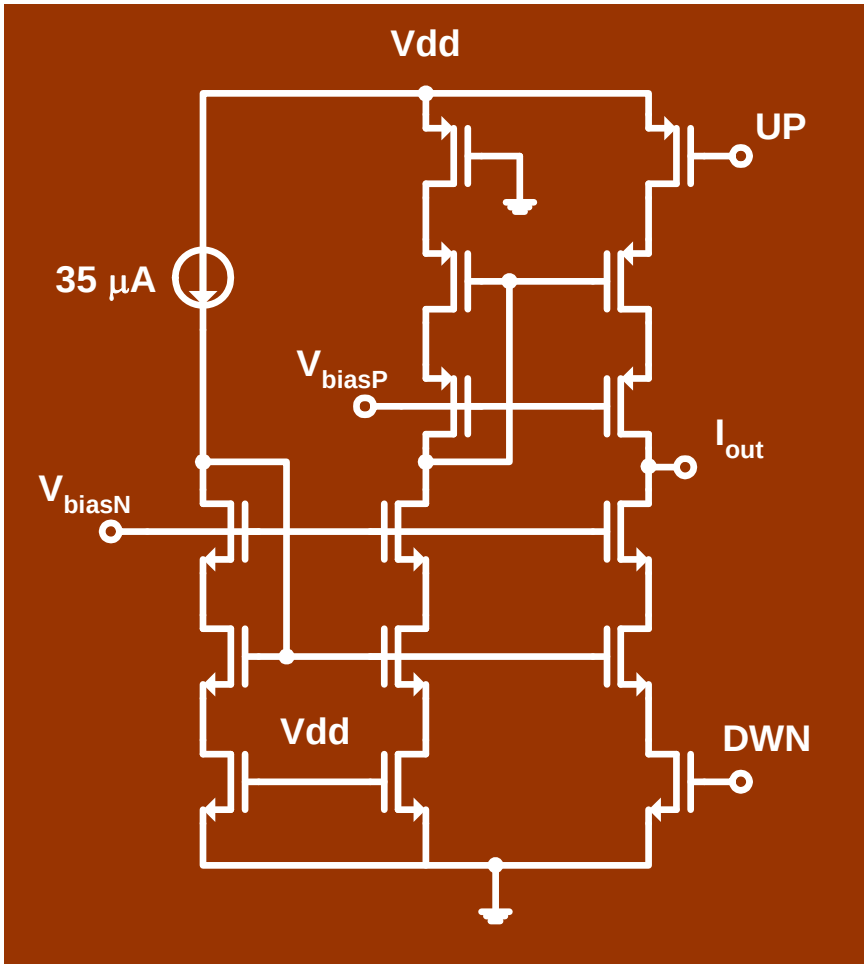


Design Procedure

- Choose a phase margin
- Calculate the damping factor required to obtain the desired phase margin (Fig. 2.19a)
- Based on the damping factor, settling time and settling accuracy determine the minimum loop bandwidth $\omega_{c,min}$
- Determine C1/C2 ratio based on the phase margin
- Calculate C2,min based on leakage current *Ileak* (1nA), charge pump mismatch *Iout* (2nA) and spurious suppression
- Calculate C1,min
- Compute the position of the zero ω_z
- Calculate the value of resistor R1
- Determine the charge pump current

Examples of circuit implementations

Charge Pump



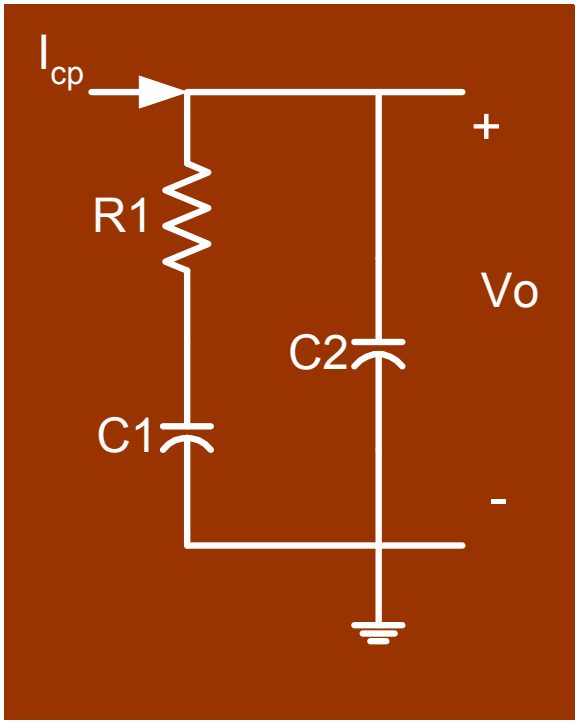
Cascode current mirrors minimize the current mismatch.

But reduce linear range of output voltage.

Design Considerations:

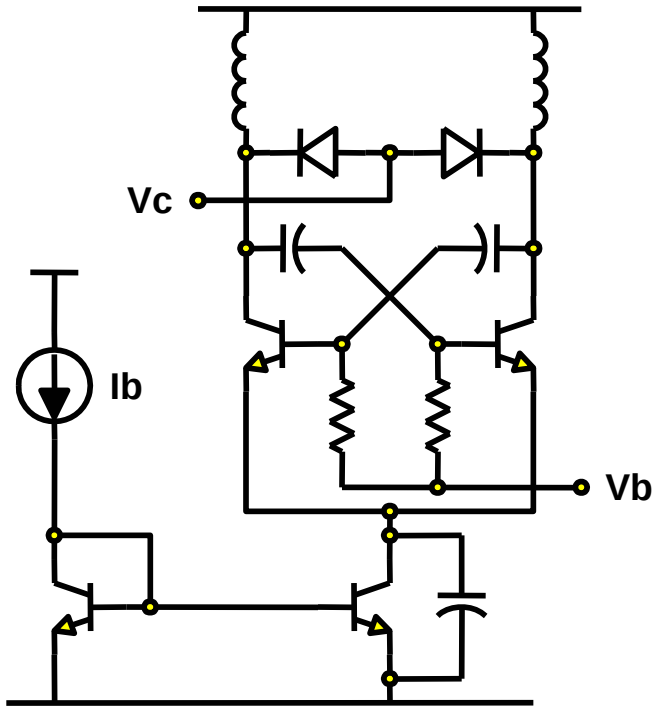
- Source and sink current matching.
- Source and sink speed matching.
- Leakage current minimization.
- Reference Spurs.
- Compliance voltage.

Loop Filter



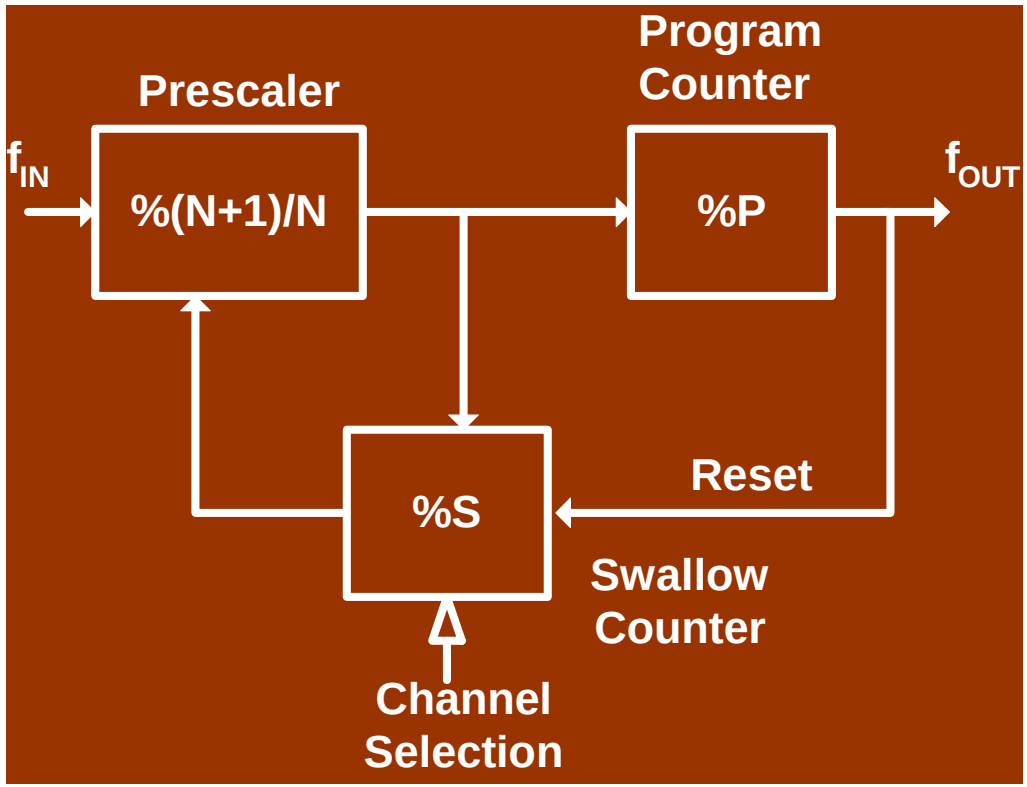
- Trade offs
  - Settling Time
  - Close-in Phase Noise
  - Total Capacitance (area)
  - Charge Pump Current
  - Phase Noise Contribution of R1

Voltage Controlled Oscillator



- Trade offs
  - Phase Noise
  - Tuning Range
  - Power Consumption

Programmable Divider



- Popular scheme for integer-N FS
- Program Counter can be also programmed
- Fast response of Swallow Counter

$$(N+1)S+(P-S)N$$

$$f_{out}=(NP+S)f_{in}$$

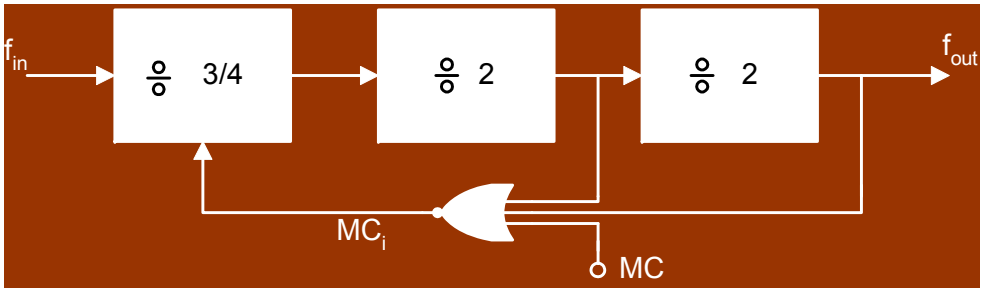
$$P>S$$

Prescaler

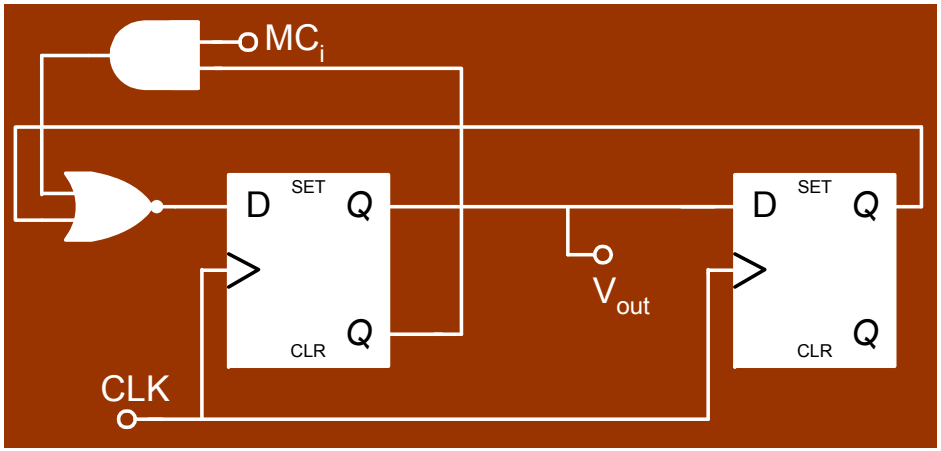
- Critical block in design of FS along with VCO (High frequency of operation)
- Usually consumes a lot of power
- Two main architectures
  - Synchronous
  - Asynchronous
- Frequency dividers
  - Digital
    - Pure digital (TSPC logic)
    - Quasi – digital (Current Mode Flip - Flops)
  - Analog
    - Injection – locked frequency dividers

Synchronous Prescaler

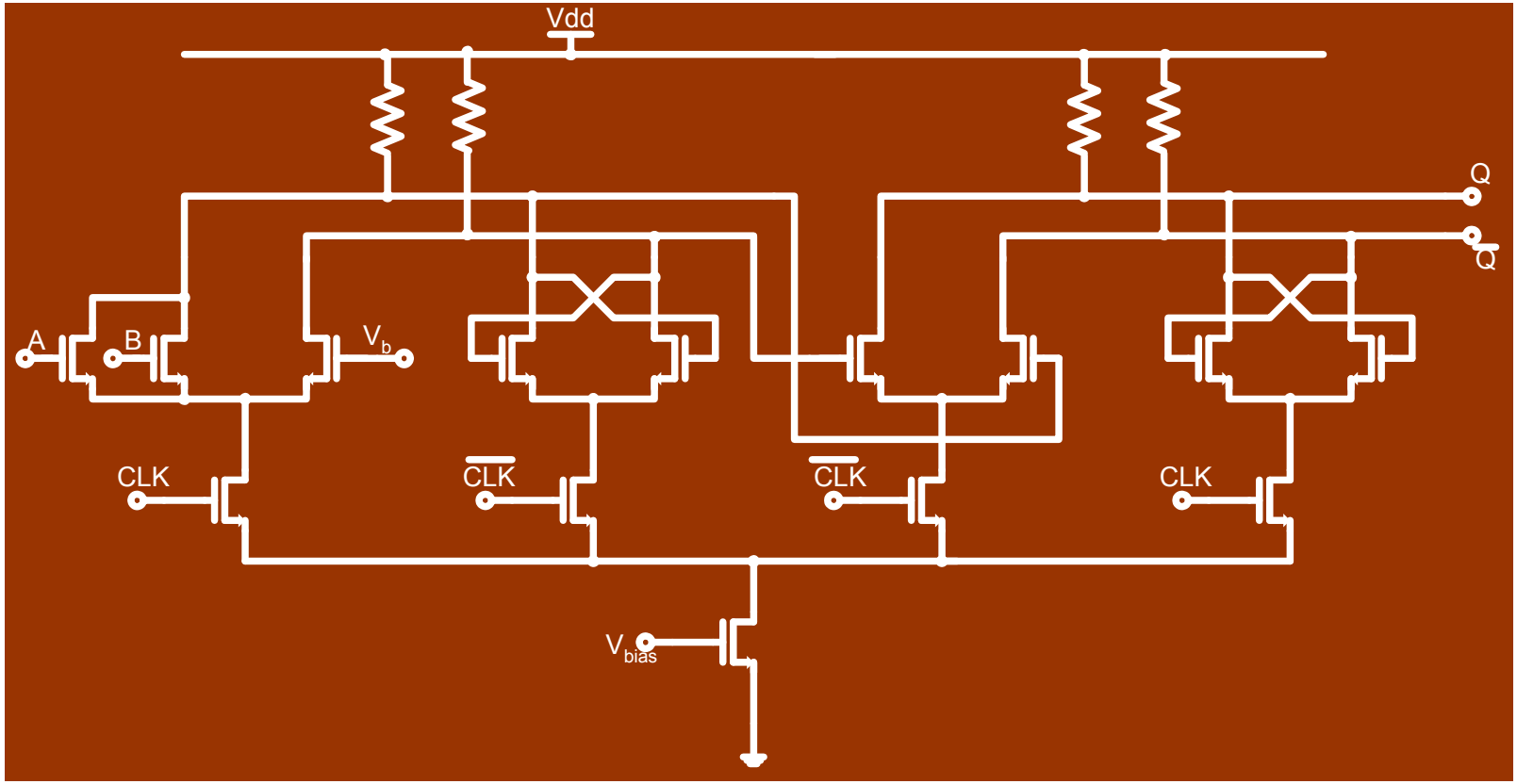
- Input Flip – Flops run at maximum speed



- Feedback gates need minimum delay
- Feedback reduces speed by aprox. 30%

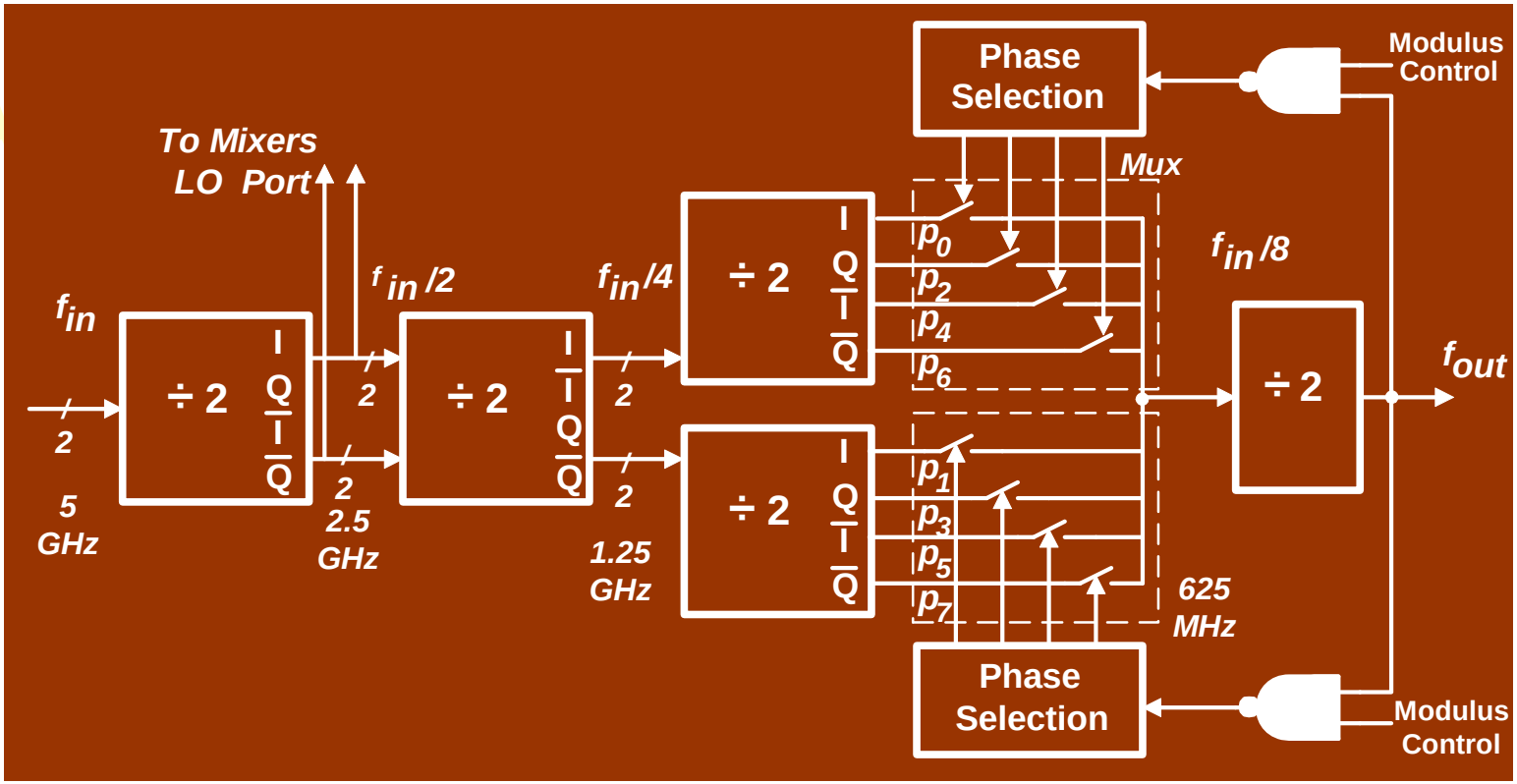


CMOS Flip - Flop



- Current Mode Logic (CML). Low voltage swing
- Input differential pair followed by latch
- Speed limited by RC product of output nodes

Phase Switching Prescaler



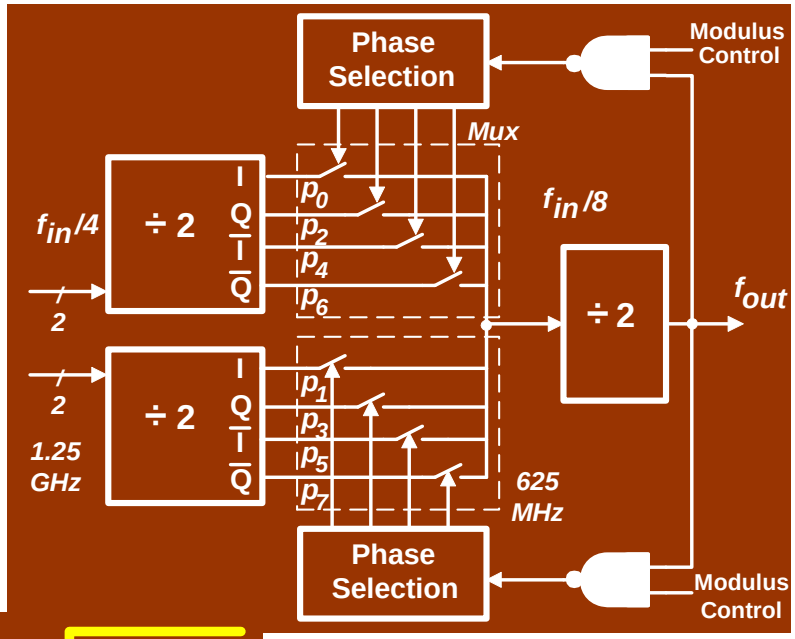
Phase switching prescaler for reduced power consumption compared with traditional architectures.

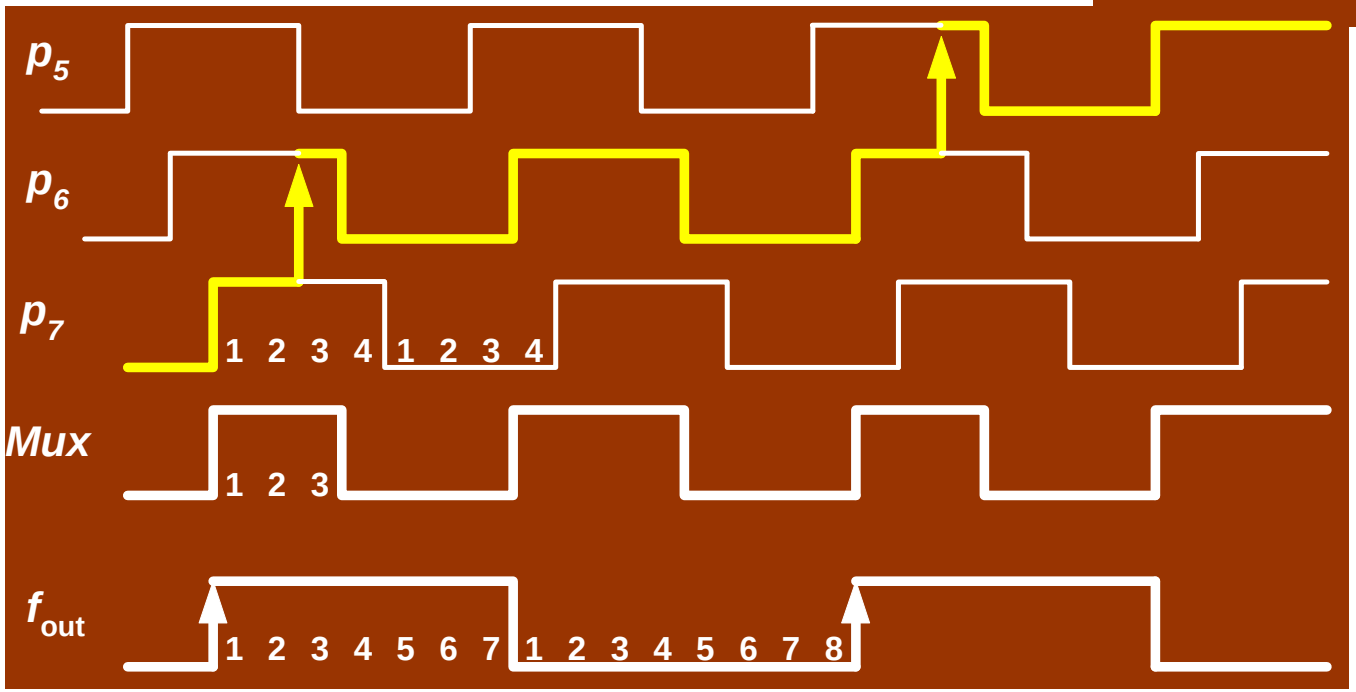
15/16 Dual Modulus

Phase Switching Prescaler

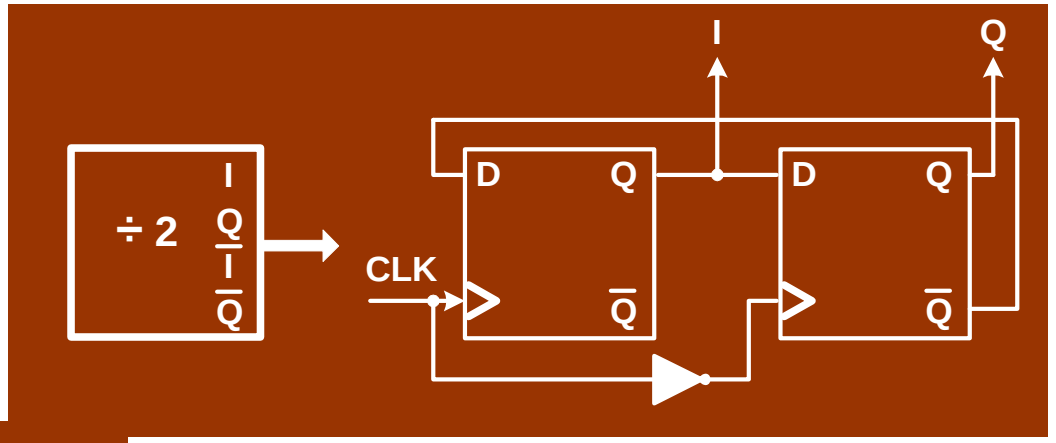
Phase switching principle

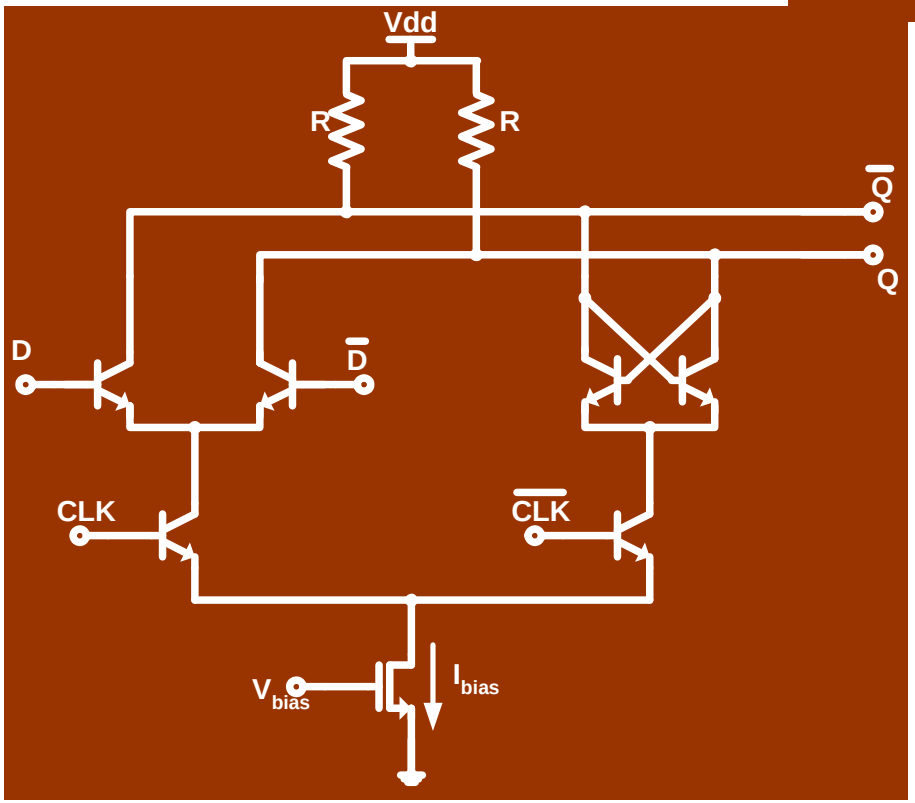
Every rising edge of f_{out} the multiplexer selects a phase that lags 45° the current phase, effectively swallowing an input pulse (dividing by N+1)





Implementation: High Frequency
D Flip-flop in bipolar technology



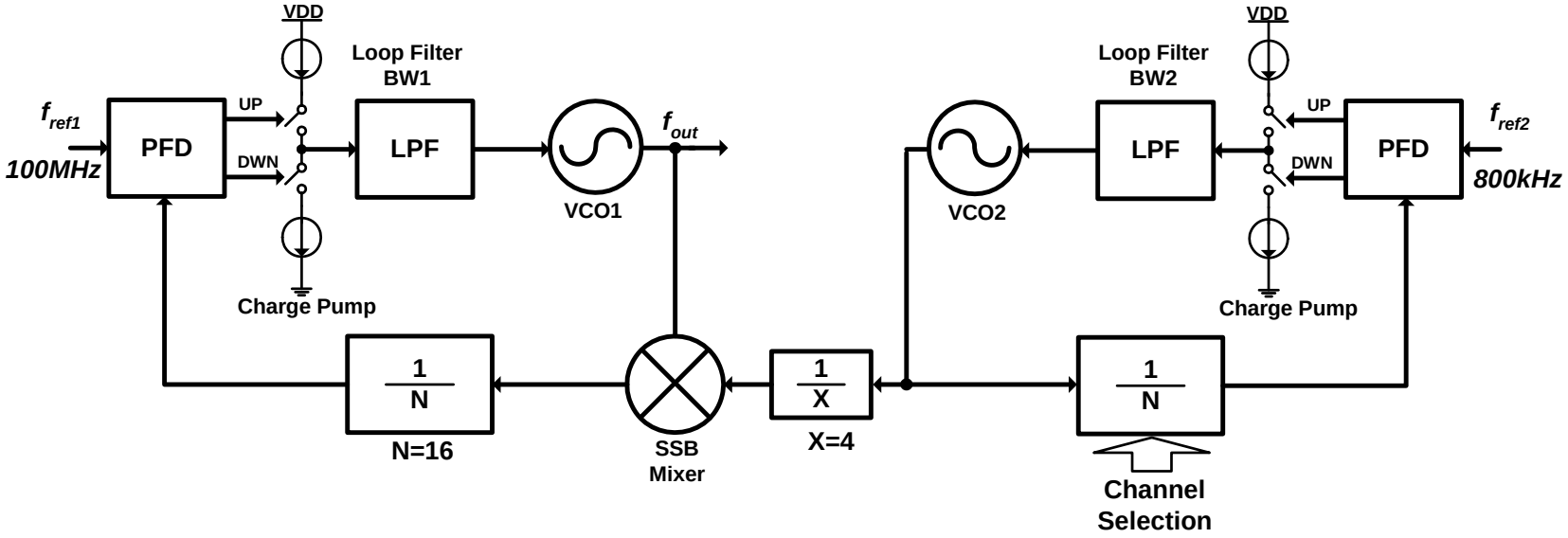


Recent Advances in Frequency Synthesizers Design

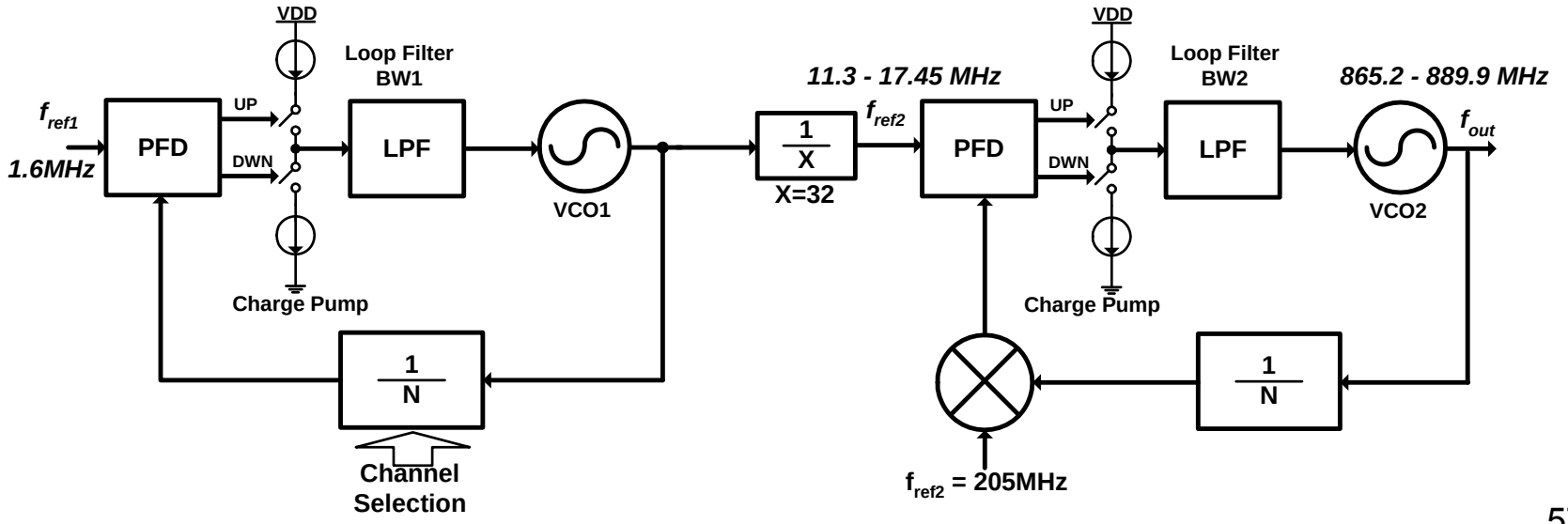
- The research focuses in:
  - New Architectures
  - Linearization techniques (spur reduction)
  - Digital PLL
  - Fast Settling
  - New and improved VCO
  - Reduced power frequency dividers
  - Low voltage – low power PLLs

a)

Dual Loop Architectures

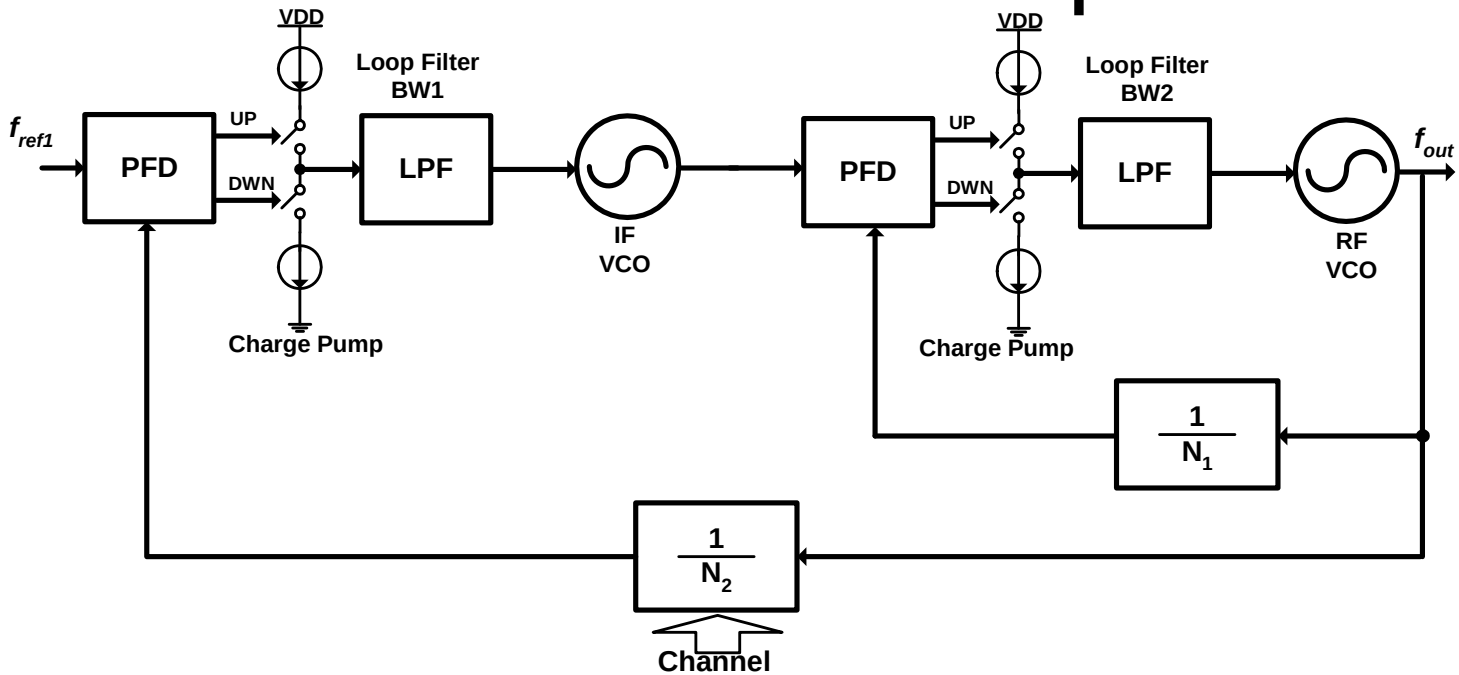


T. Kan and H. C. Luong, "A 2-V 1.8-GHz Fully Integrated CMOS Frequency Synthesizer for DCS-1800 Wireless Systems", *VLSI Circuits*, pp: 234 - 237, 2000.

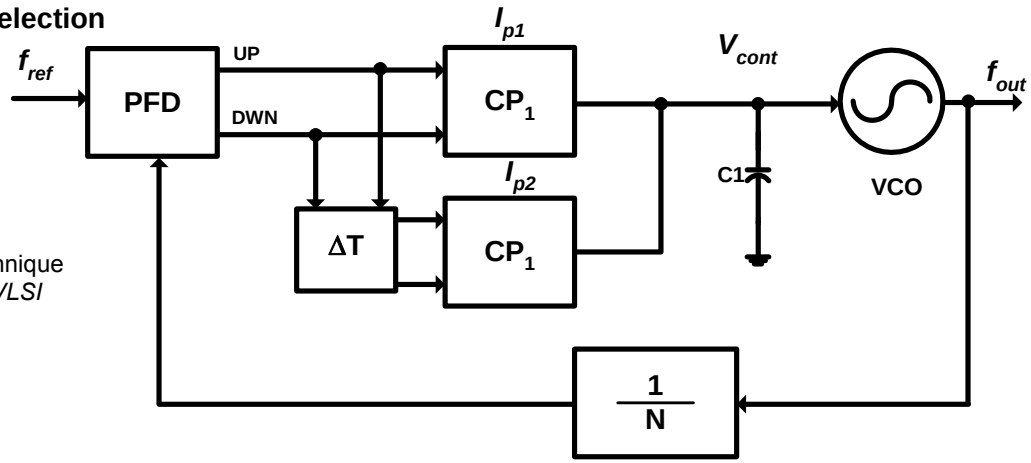


W. Yan and H. C. Luong, "A 2-V 900-MHz monolithic CMOS dual-loop frequency synthesizer for GSM wireless receivers", *IEEE JSSC*, vol. 36, pp: 204-216, February 2001.

Nested Loop PLL and Stabilization Technique



A.N. Hafez and M.I. Elmasry, "A Fully-Integrated Low Phase-Noise Nested-Loop PLL for Frequency Synthesis", *CICC*, pp: 589 – 592, 2000.



T. C. Lee and B. Razavi, "A Stabilization Technique for Phase-Locked Frequency Synthesizers", *VLSI Symposium*, pp: 39 - 42, 2001