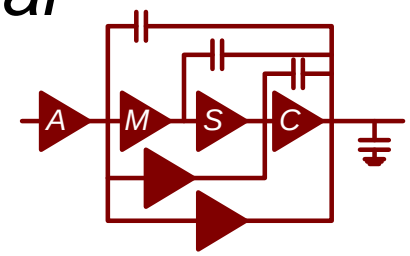
INTRODUCTION TO PLL DESIGN FOR FREQUENCY SYNTHESIZER

Thanks Sung Tae Moon and Ari Valero for part of this material

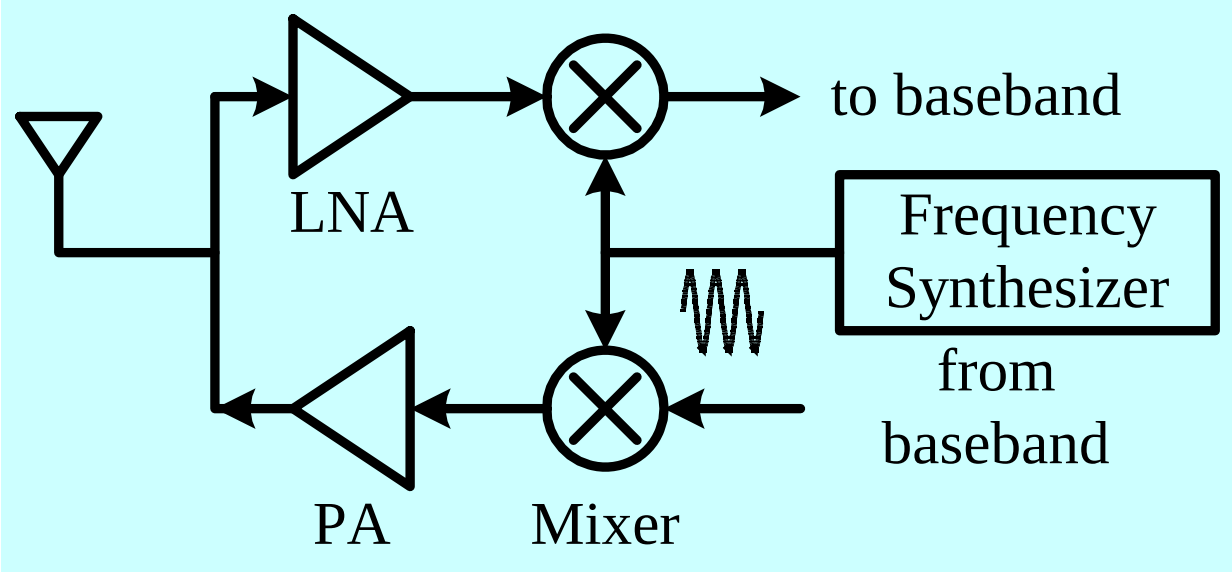


Analog and Mixed-Signal Center

Contents

- Introduction to Frequency Synthesizer
- Specification Study
- PLL Design
- Testing Examples

Frequency Synthesizer in Transceiver



- FS provides LO signal for up/down conversion
- Frequency accuracy is in the order of tens of ppm
- High spectral purity in terms of phase noise and spurious signal
- Settling time requirement when switching channels

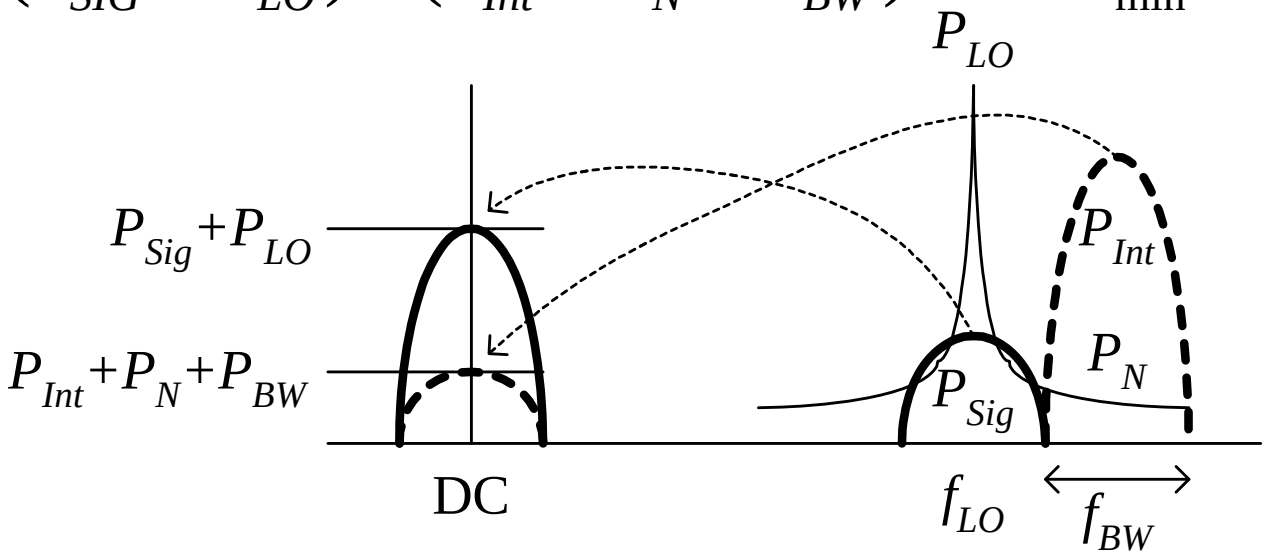
Communication Standards

	Bluetooth	802.11a	802.11b	802.11g
Bit rate	1 Mbps	54 Mbps	11 Mbps	54 Mbps
Sensitivity	-70 dBm	-82 dBm	-76 dBm	-76 dBm
FER	10^{-3} (BER)	10^{-5}	8×10^{-2}	8×10^{-2}
Band (MHz)	2400–2479	5180–5805	2412–2472	2412–2472
Channel Spacing	1 MHz	20 MHz	5 MHz	20 MHz
Accuracy	±75 kHz	±20 ppm	±25 ppm	±25 ppm
Settling	$< 259\ \mu s$	$224\ \mu s$	$224\ \mu s$	$224\ \mu s$
Interference	+40 dB at 3 MHz	+32 dB at 40 MHz	+35 dB at 25 MHz	+35 dB at 25 MHz

$$T_{down} = T_{slot} - T_{pkt} = 625\mu s - 366\mu s = 259\mu s$$

Phase Noise Requirement

$$SNR = (P_{SIG} + P_{LO}) - (P_{Int} + P_N + P_{BW}) > SNR_{\min}$$



$$P_N - P_{LO} = PN < (P_{Sig} - P_{Int}) - P_{BW} - SNR_{\min}$$

- Calculated from adjacent channel interference rejection requirement
- SNR due to interference down conversion has to be better then minimum required SNR

$$P_N - P_{LO} = PN < (P_{Sig} - P_{Int}) - P_{BW} - SNR_{\min}$$

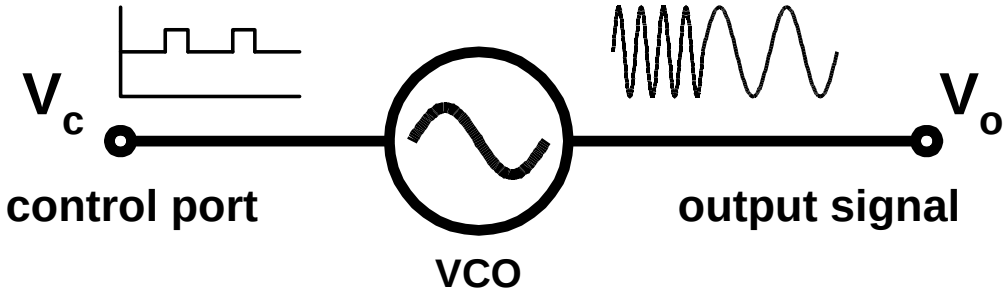
For illustration consider the Table in page 4 , the Bluetooth standard specifies an interferer of +40dB at 3MHz away from the desired signal.

SNRmin from a BER of 0.001 is 18dB.

$P_{BW} = 10\log 10^6 = 60dB$.

Thus PN= -118DBc at 3MHz from carrier. The computation assumes phase white noise within the channel bandwidth

Spurious Signal



$$v_o(t) = V_o \cos(\omega_o t + K' \int v_c(t) dt)$$

$$= V_o \cos(\omega_o t + K \sin \omega_m t)$$

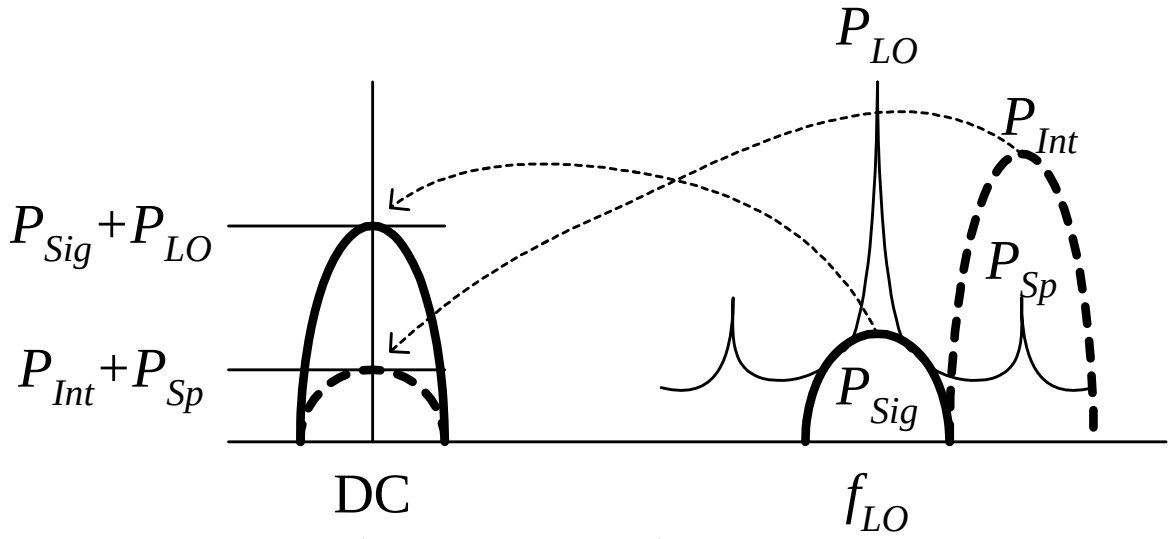
$$\approx V_o (\cos \omega_o t - \sin \omega_o t \cdot K \sin \omega_m t)$$

$$= V_o \left(\cos \omega_o t - \frac{K}{2} \cos(\omega_o - \omega_m)t + \frac{K}{2} \cos(\omega_o + \omega_m)t \right)$$

- VCO output is modulated by coupled signal on control port.
- Two sideband tones at $\pm\omega_m$ away from the center frequency

Spur Requirement:

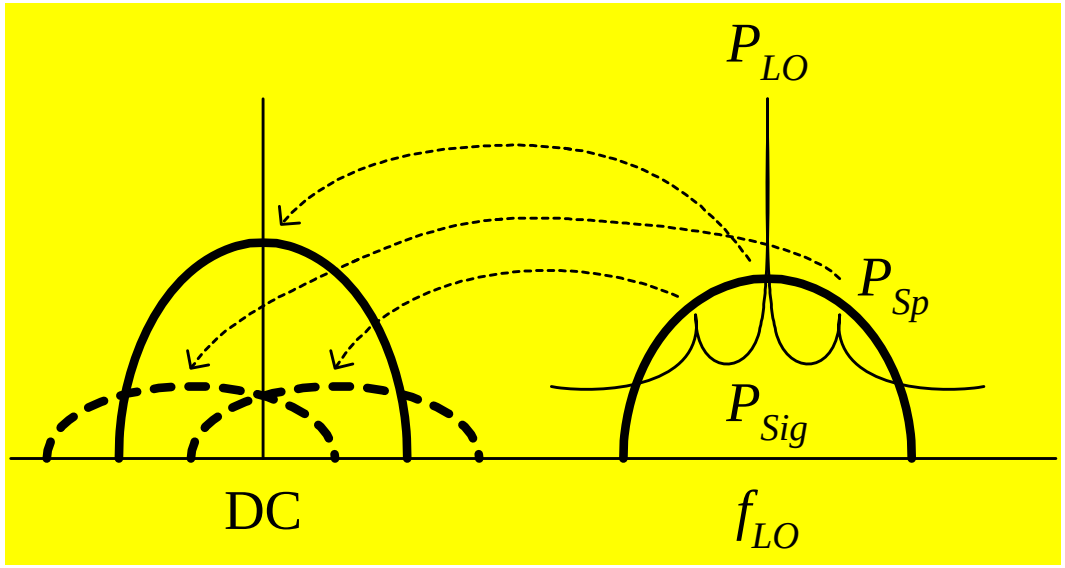
Reference spur can be a serious problem if the system uses narrow channel spacing and the spur coincides with the adjacent channels . This might occur for BT transceivers with an integer-N frequency synthesizer.



$$P_{Sp} - P_{LO} < (P_{Sig} - P_{Int}) - SNR_{\min}$$

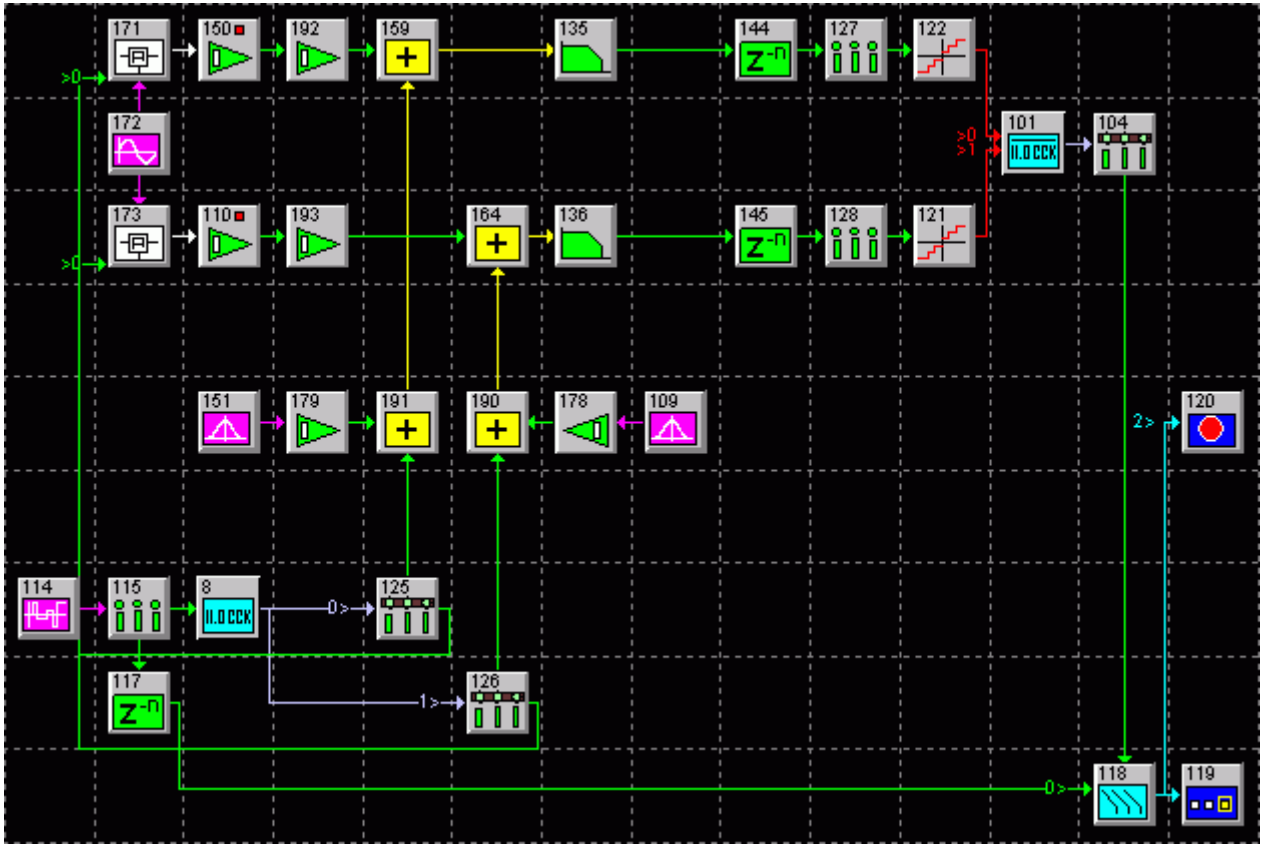
- Calculated from adjacent channel interference rejection requirement
- Since spur is not noise, P_{BW} is out of equation

Spur Requirement for 802.11b



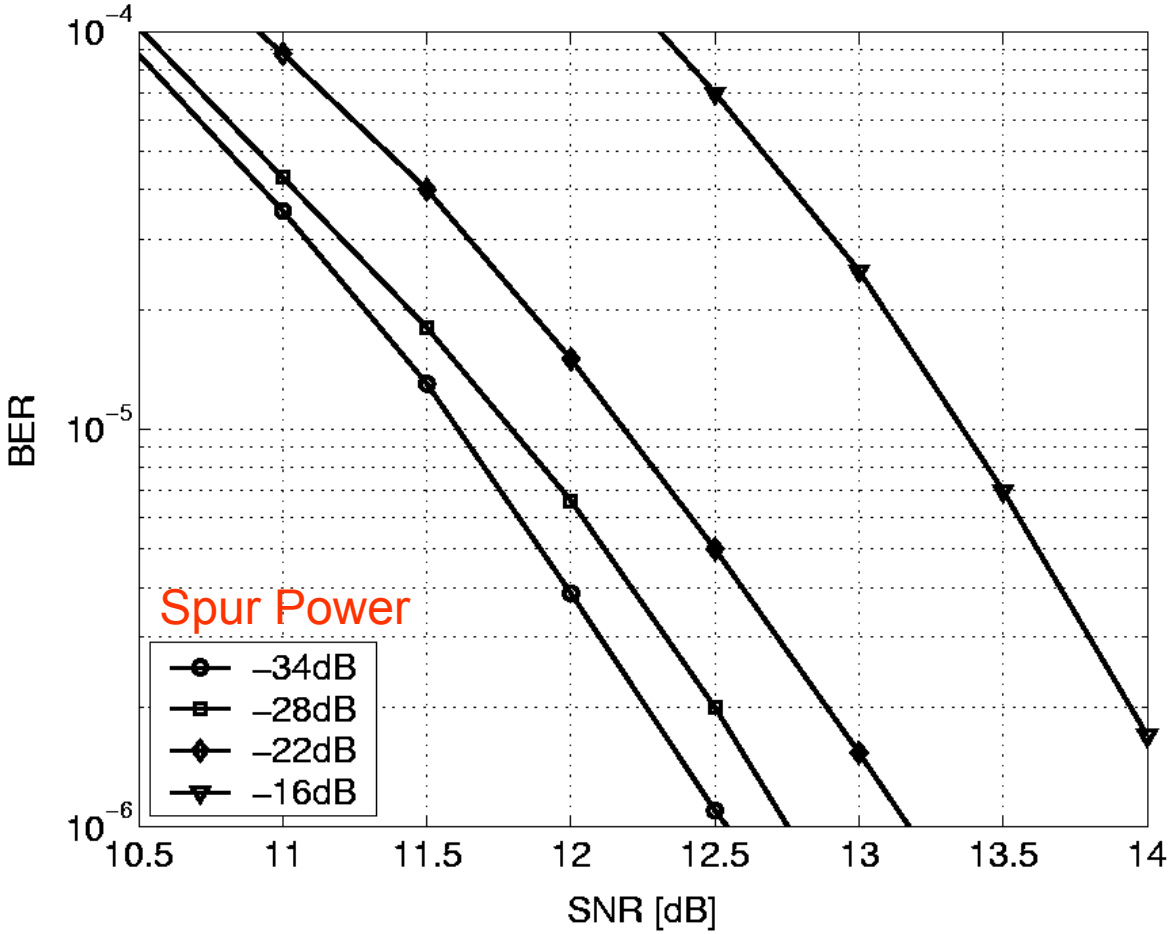
- Channel is wider then spur offset
- System level simulation is required to estimate the degradation of the signal
- The reference spur must be at least 25dB below the carrier signal to keep a BER better than 10^{-5} when the input SNR is 12dB

Spur Simulation in Systemview

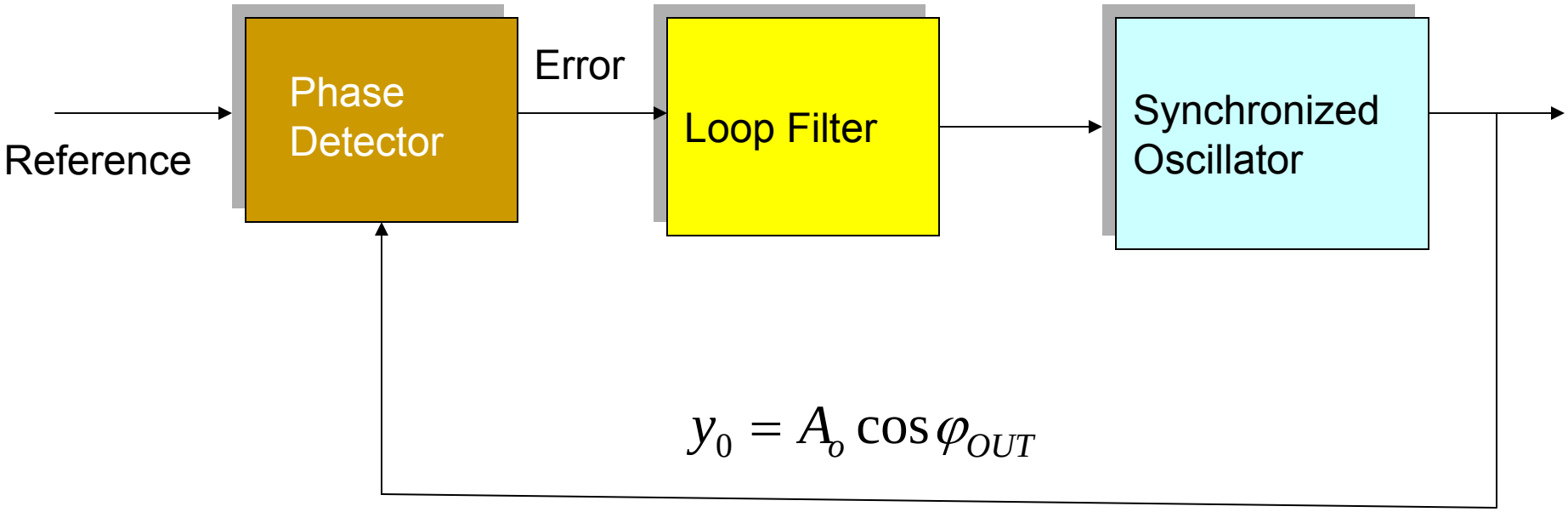


Spur Simulation Result

The effect of reference spur at 2M Hz in 802.11b system



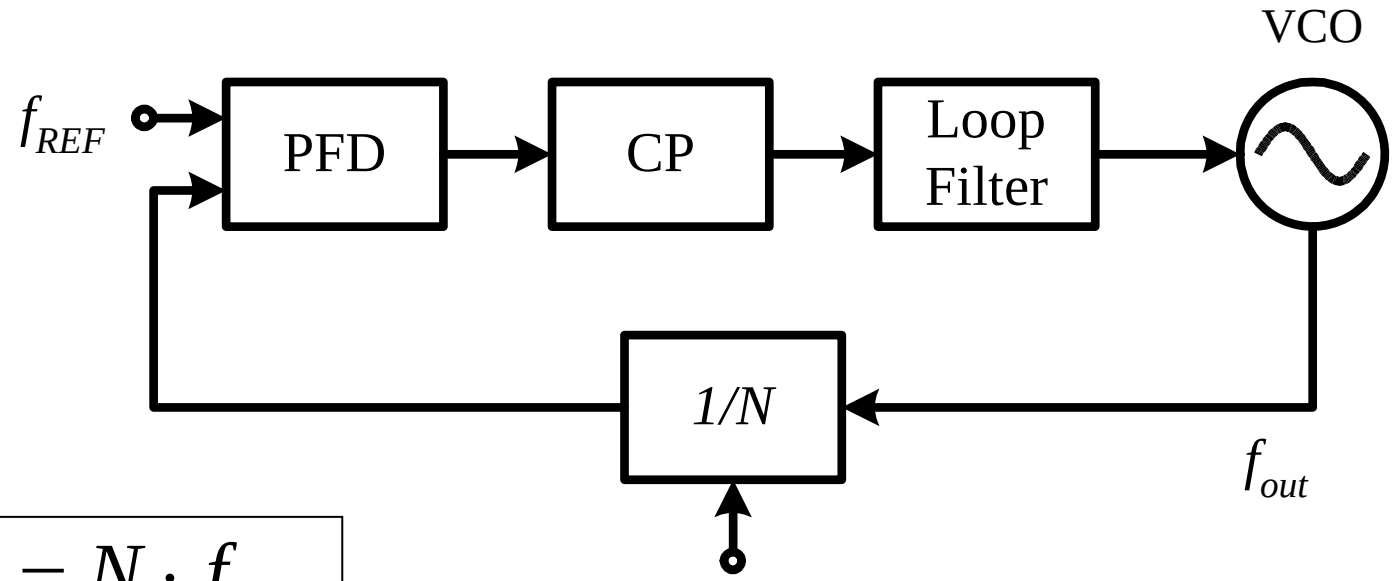
A basic phase locked-loop architecture



$$\text{Re}\,ference = y_i = A_i \cos\varphi_{IN}$$

$$Error = K_P(\varphi_{IN} - \varphi_{OUT} - \theta)$$

Integer-N Synthesizer



$$f_{out} = N \cdot f_{REF}$$

- Only integer multiple of f_{REF} is allowed for output
- f_{REF} is not necessarily equal to channel spacing
- $f_{REF\_max}=GCD(f_{Channel},f_{Spacing})$

A numerical example.-

- *For Wireless LAN 802.11b the standard specifies channels from 2412 MHz to 2472 MHz in steps of 5 MHz.*
- *Thus the maximum f_{REF} is GCD(2412 MHz, 5MHz) = 1M Hz*

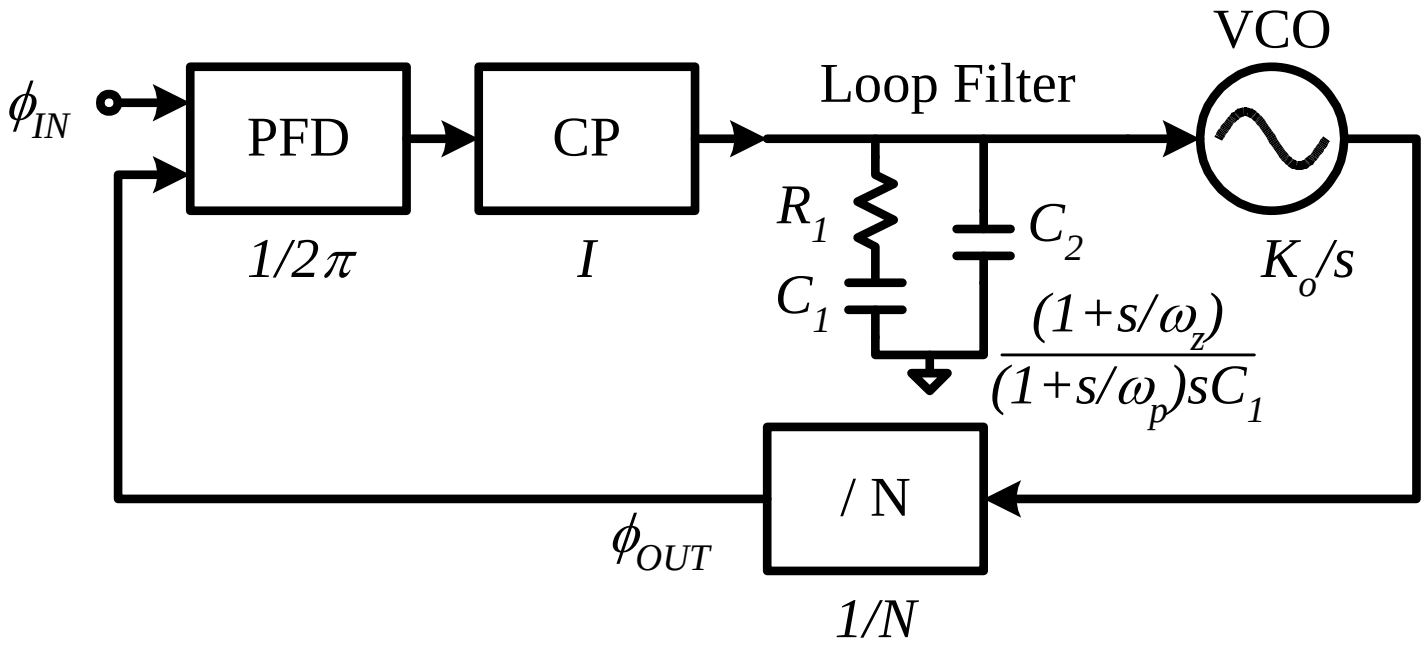
Process of Operation

- PFD compares the phase difference between the reference and the divided VCO output.
- PFD output is a series of pulses with duty cycle proportional to the phase difference.
- CP converts the voltage pulses into current pulses
- Loop filter converts current pulses into filtered voltage level.
- With negative feedback, the phase difference between the reference and the VCO become smaller and smaller until they are exactly in-phase.
- Once locked, the frequency of the VCO is equal to N times the reference frequency.

Charge-pump PLL

- Phase frequency detector (PFD) extends acquisition range to full VCO tuning range, not limited by loop bandwidth
- Charge-pump and capacitive filter introduce a pole at the origin. Infinite DC gain leads to zero static phase error

Charge-pump PLL Linear Model



- Transfer function of *phase*
- PFD and CP is modeled as constant gain
- VCO is modeled as integrator
- Frequency divider is modeled as constant loss

Linear Model Equations

- Open-loop transfer function
  - To check phase margin for stability
  - Important parameters : ω_n (natural frequency), ω_c (crossover frequency), ω_z (zero), ω_p (additional pole)
- Closed-loop transfer function
  - To check transient behavior, including settling time, overshoot and stability
  - Important parameters : ω_n (natural frequency), ζ (damping factor)

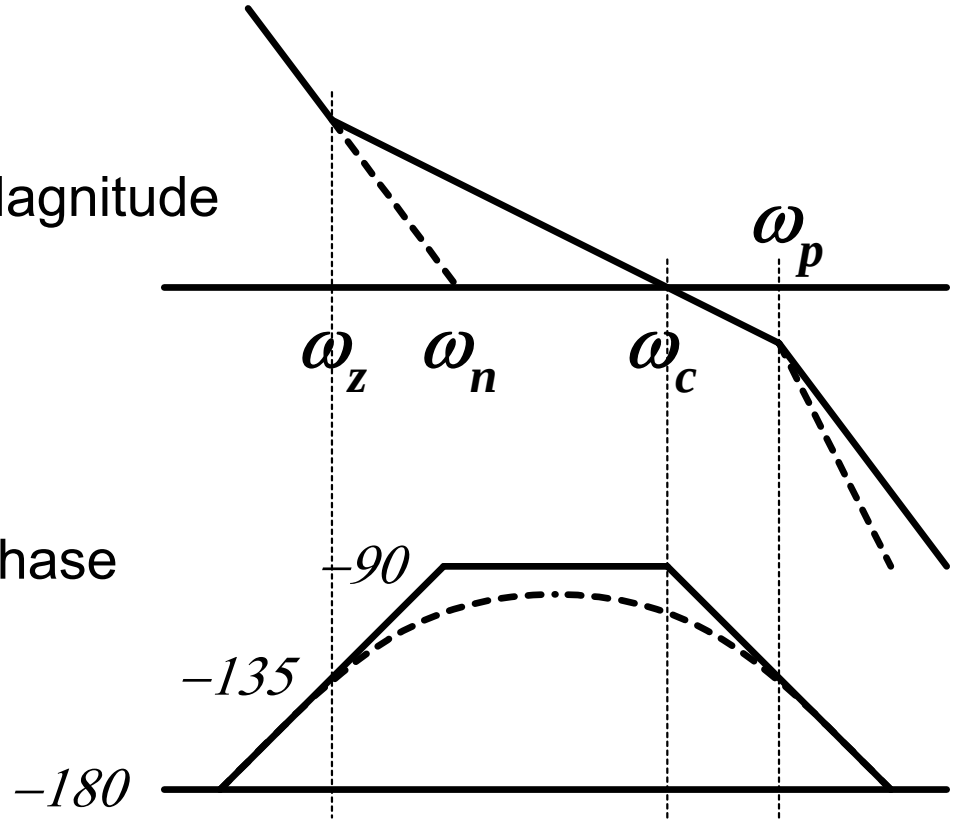
Open-loop Transfer Function

$$H_{open}(s) = \frac{IK_o}{2\pi C_1 N} \frac{(1 + s/\omega_z)}{s^2 (1 + s/\omega_p)}$$

- Two poles at the origin make the loop potentially unstable
- Stabilizing zero at ω_z makes the loop stable
- Additional pole at ω_p improves rejection of undesirable signal

Open-loop Transfer Function (cont.)

- Magnitude
- Phase



- Natural frequency

$$\omega_n = \sqrt{\frac{IK_o}{2\pi C_1 N}}$$

- Crossover frequency

$$\omega_c \approx \frac{\omega_n^{\ 2}}{\omega_z}$$

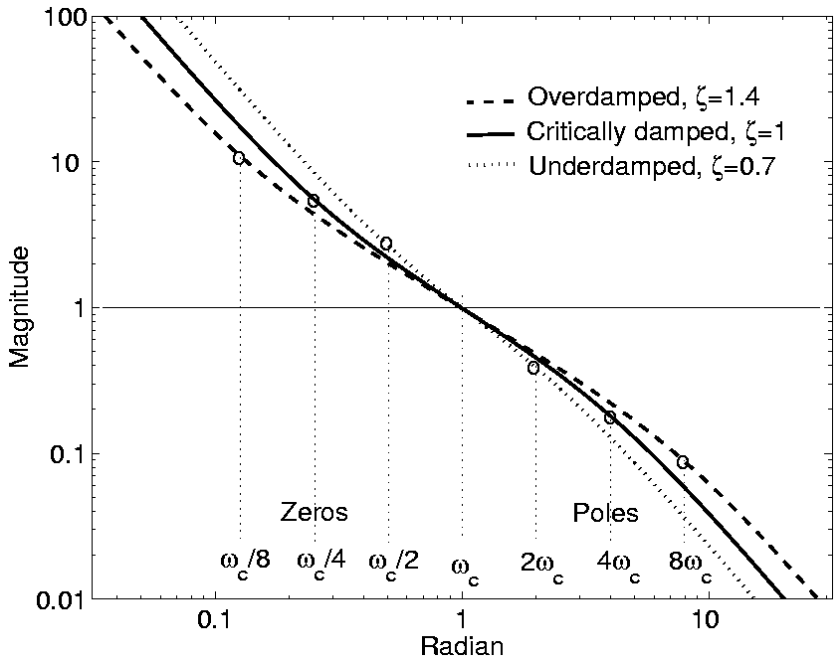
- Zero frequency

$$\omega_z = \frac{1}{R_1 C_1}$$

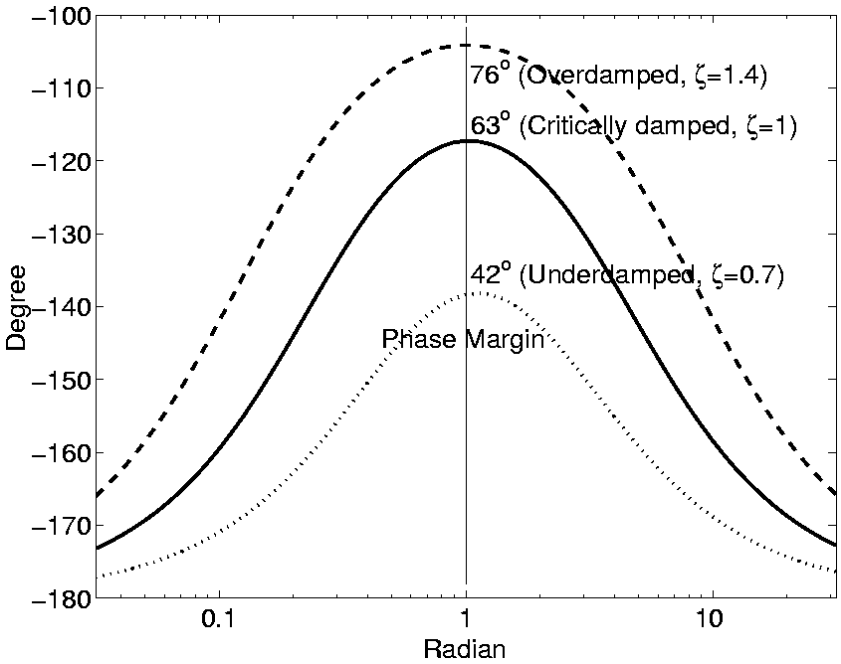
- Pole frequency

$$\omega_p \approx \frac{1}{R_1 C_2}$$

Stability due to Phase Margin



Magnitude



Phase

- Phase margin changes depend on placement of zero and poles
- Crossover frequency is approximately same as loop bandwidth

Gardner's Stability Limit

- Since PFD and CP works in discrete time domain, linear approximation fails when the loop bandwidth gets close to sampling frequency
- Gardner's stability limit states

$$\omega_c < \frac{\omega_{REF}}{\pi(1+\pi\omega_z / \omega_{REF})}$$

- Loop bandwidth should be considerably lower then reference frequency

Closed-loop Transfer Function

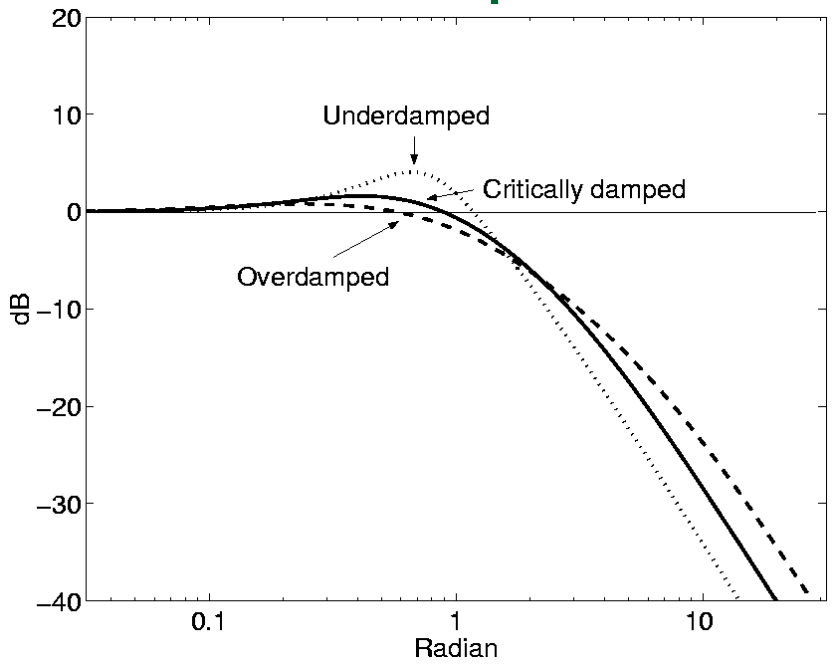
$$H_{closed}(s) = \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_o) + s^3/(\omega_p K_D K_o)}$$

$$\approx \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(K_D K_o)}$$

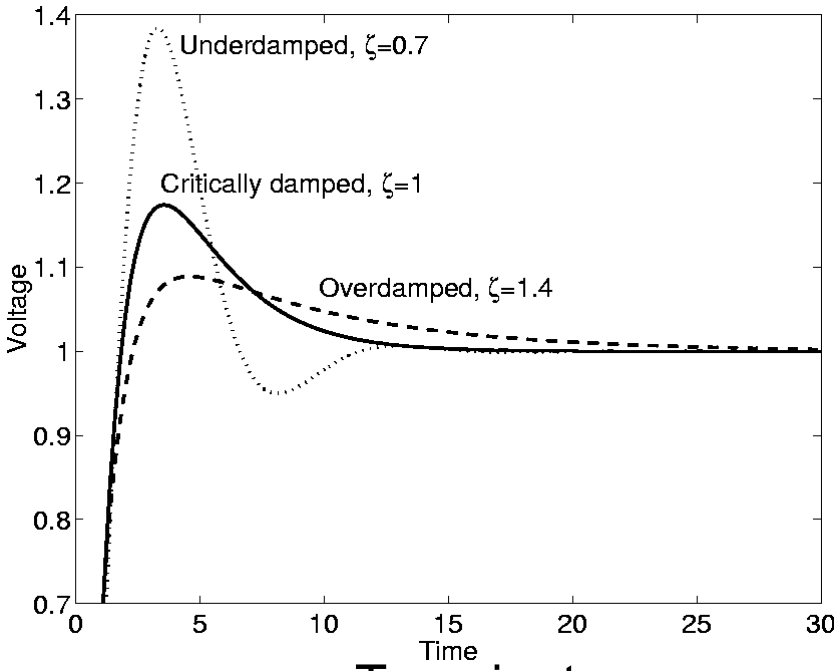
- Second-order transfer function with a zero
- Important parameters are ω_n (natural frequency) and ζ (damping factor)

$$\omega_n = \sqrt{K_D K_o} = \sqrt{\frac{I K_o}{2\pi C_1 N}} \qquad \zeta = \frac{\omega_n}{2\omega_z}$$

Closed-loop Behavior



Magnitude

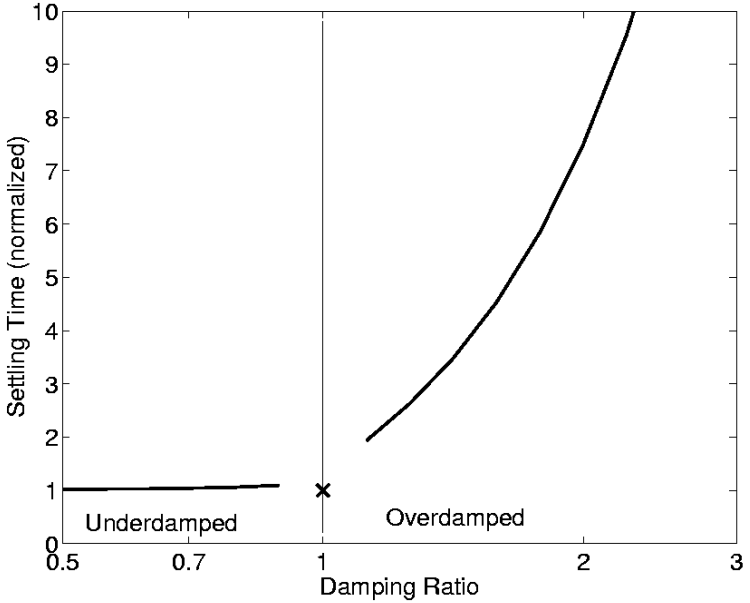


Transient

- In magnitude response, peaking occurs due to zero in forward path.
- In transient response, overshoot occurs when underdamped.

Settling Time Estimation

$$t_s = \begin{cases} \dfrac{1}{\zeta\omega_n}\ln\dfrac{\Delta f}{\alpha f_o\sqrt{1-\zeta^2}} \\ \dfrac{1}{\zeta\omega_n}\ln\dfrac{\Delta f}{\alpha f_o} \\ \dfrac{1}{(\zeta-\sqrt{\zeta^2-1})\omega_n}\ln\dfrac{\Delta f\,(\sqrt{\zeta^2-1}+\zeta)}{2\alpha f_o\sqrt{\zeta^2-1}} \end{cases}$$

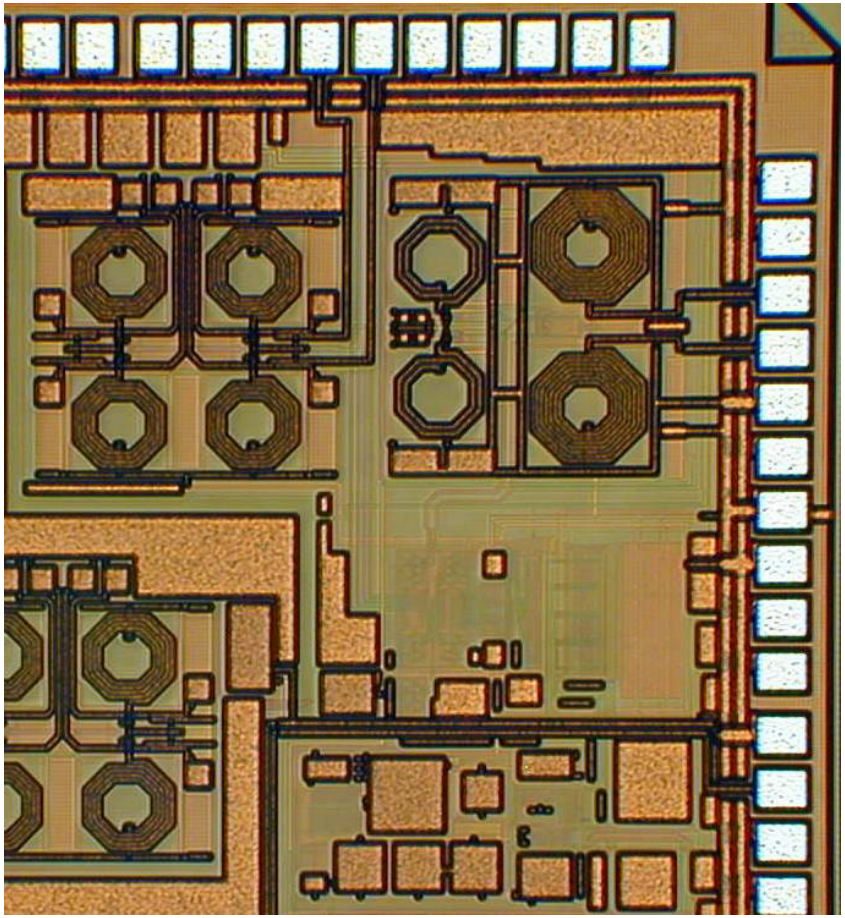


- f_o is starting frequency, Δf is amount of frequency jump, α is settling accuracy
- The larger the bandwidth, the faster the settling time
- Overdamping slows down settling time

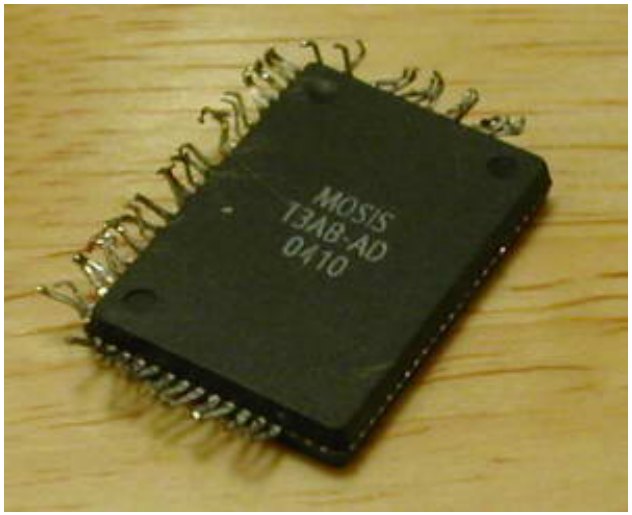
Design Procedure

1. Determine reference frequency from requirements $f_{REF}=GCD(f_{Channel},f_{Spacing})$
2. From Gardner's stability limit, determine the loop bandwidth $\omega_c < \omega_{REF}/10$
3. Choose damping ratio ζ
4. Calculate natural frequency $\omega_n = \omega_c/2\zeta$
5. Check if settling time is good enough
6. Calculate zero and pole frequency $\omega_z = \omega_n/2\zeta$, $\omega_p = \omega_n x 2\zeta$

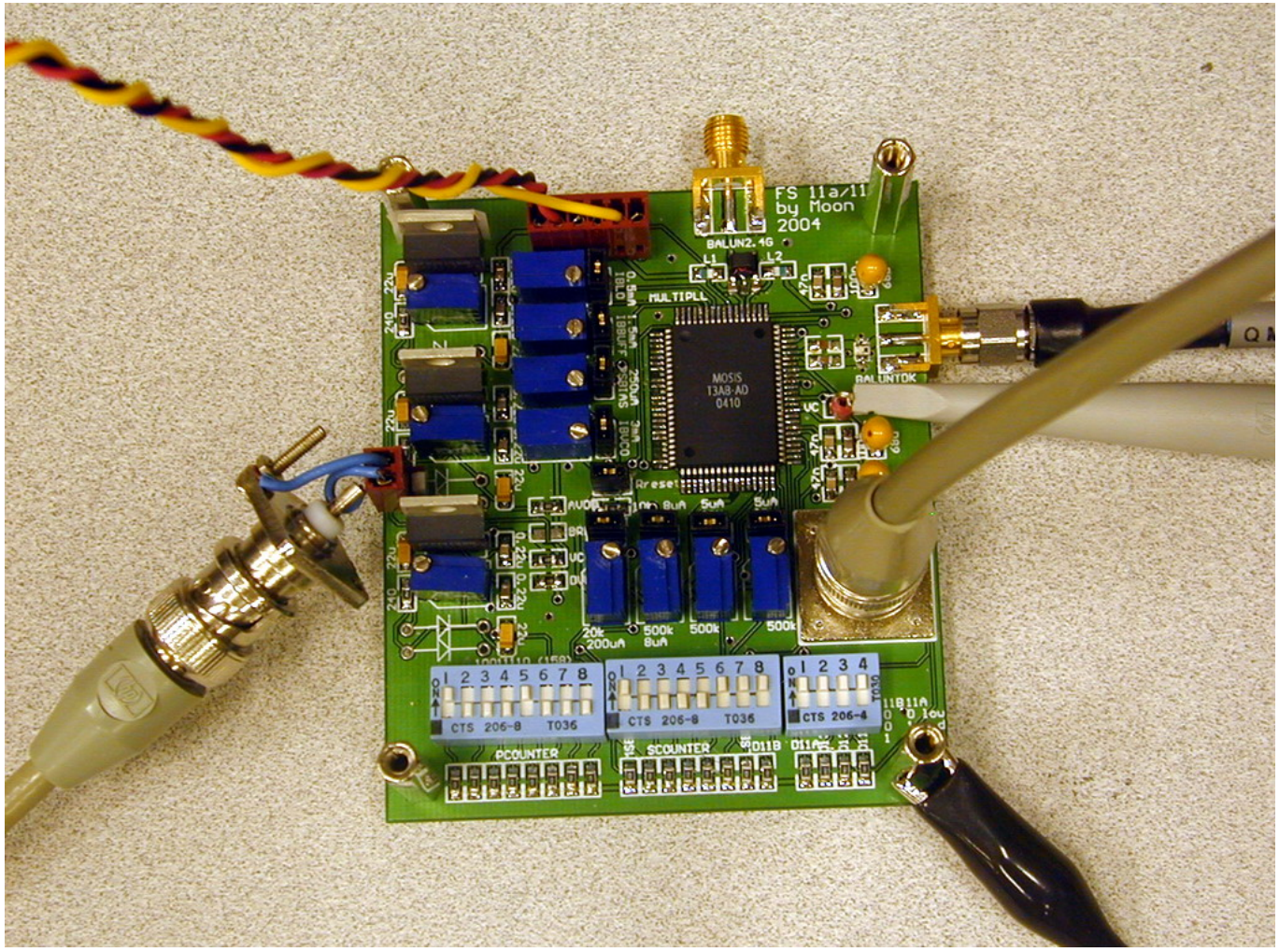
Testing : Chip Microphoto



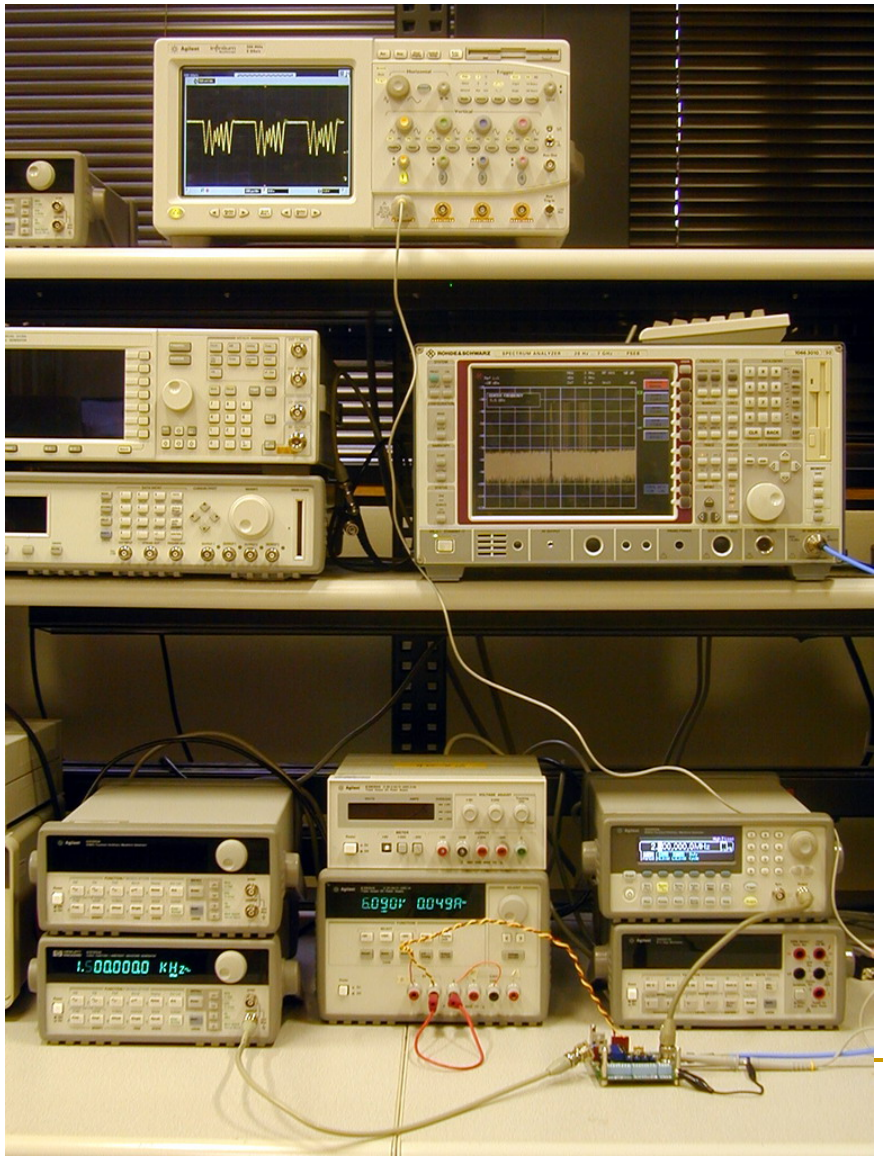
Testing : Failed Chip



Testing : PC Board

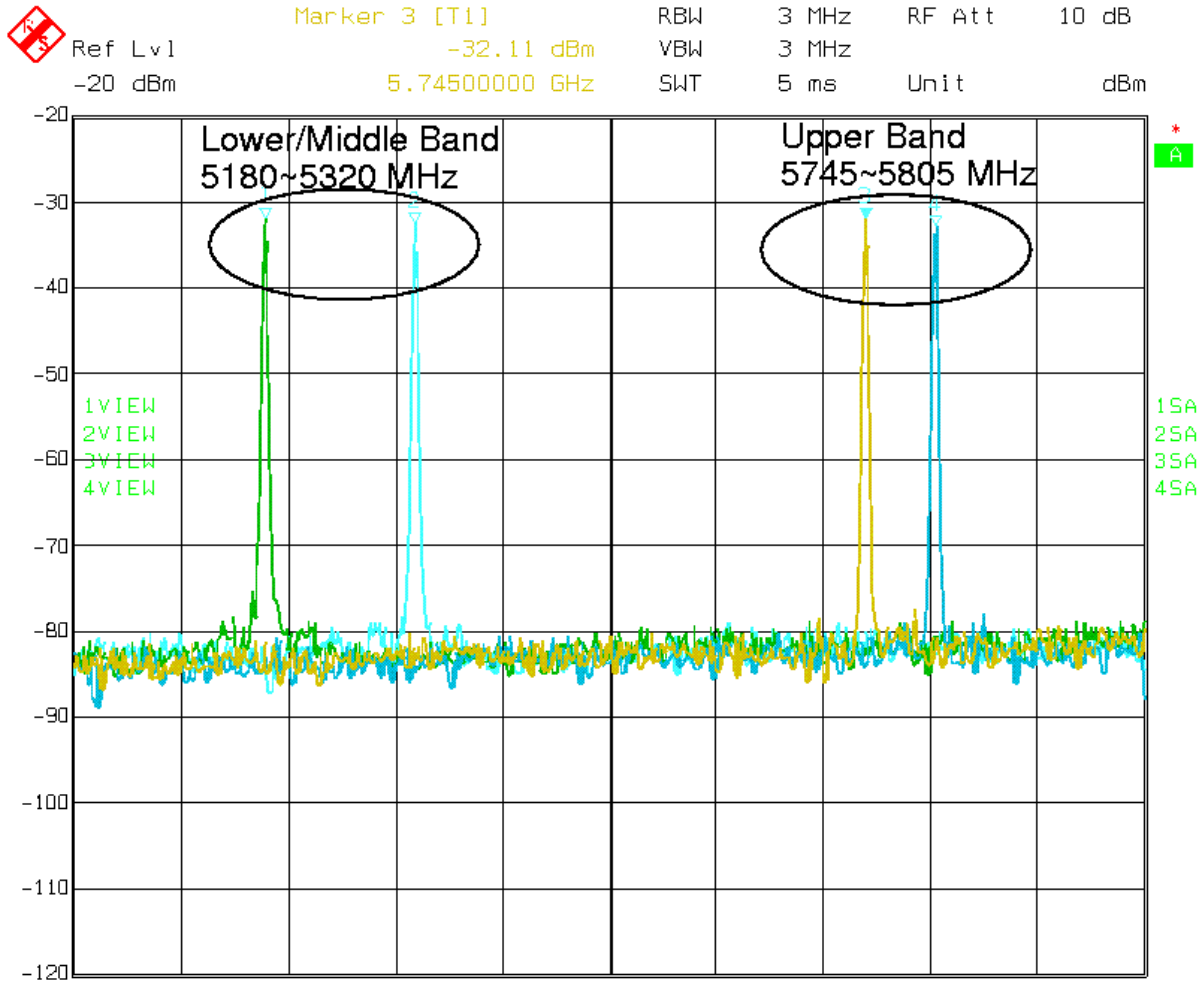


Testing : Equipments

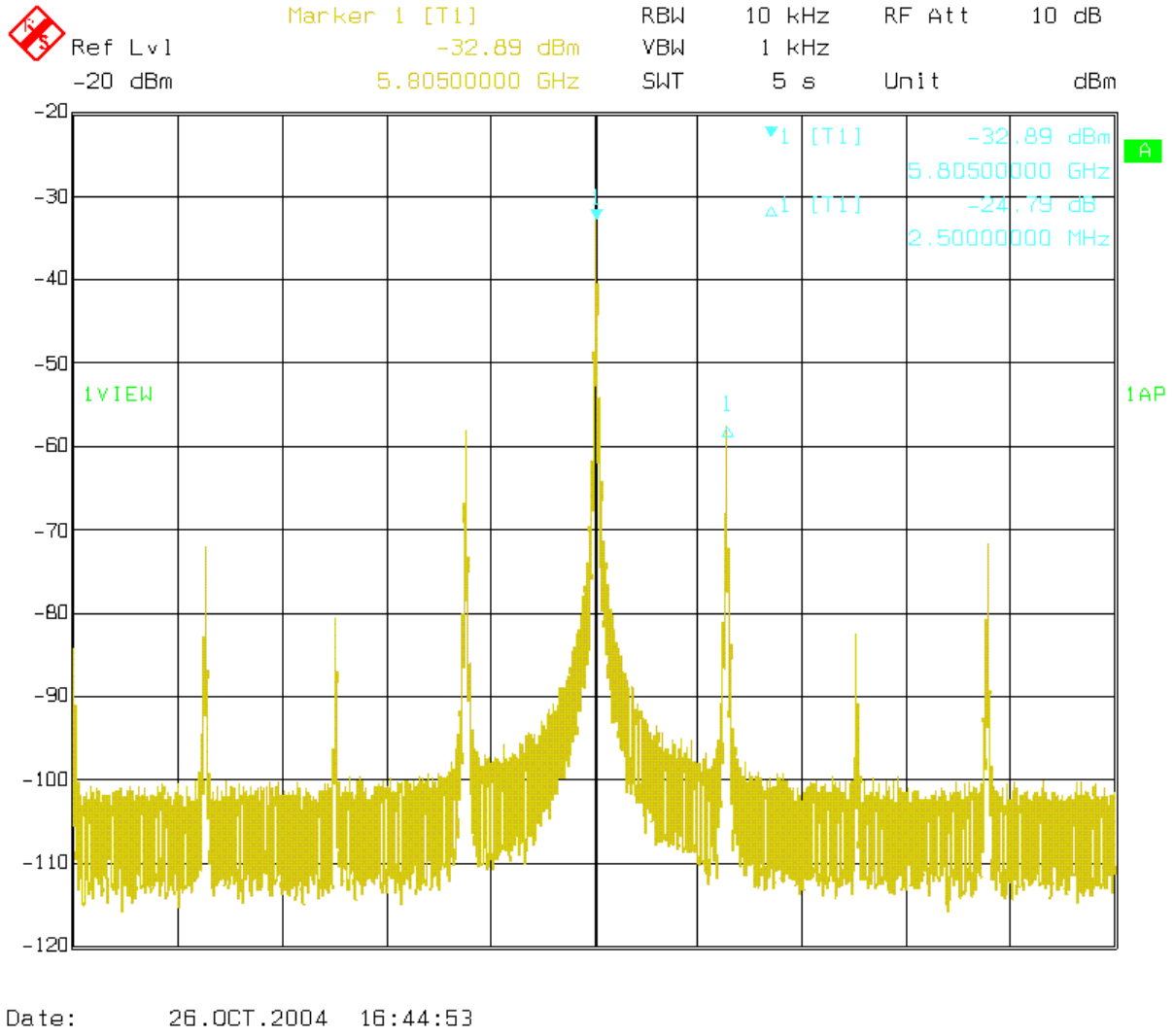


- Agilent infiniium Oscilloscope
- R&S FSEB Spectrum analyzer
- Agilent 33250A Function Generator
- HP 33120A Function Generator
- Agilent E3631A Power Supply

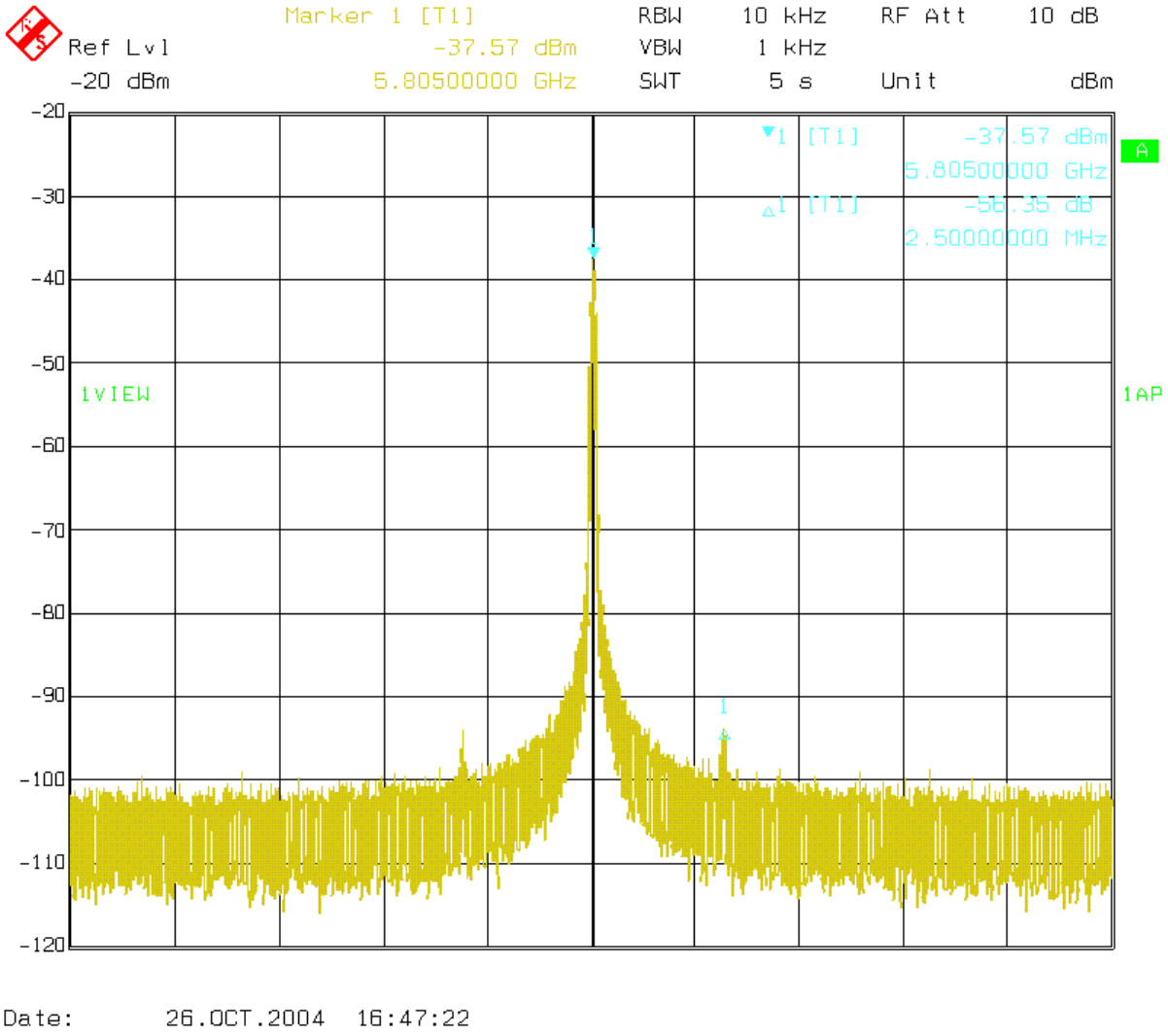
Testing Results : Tuning Range



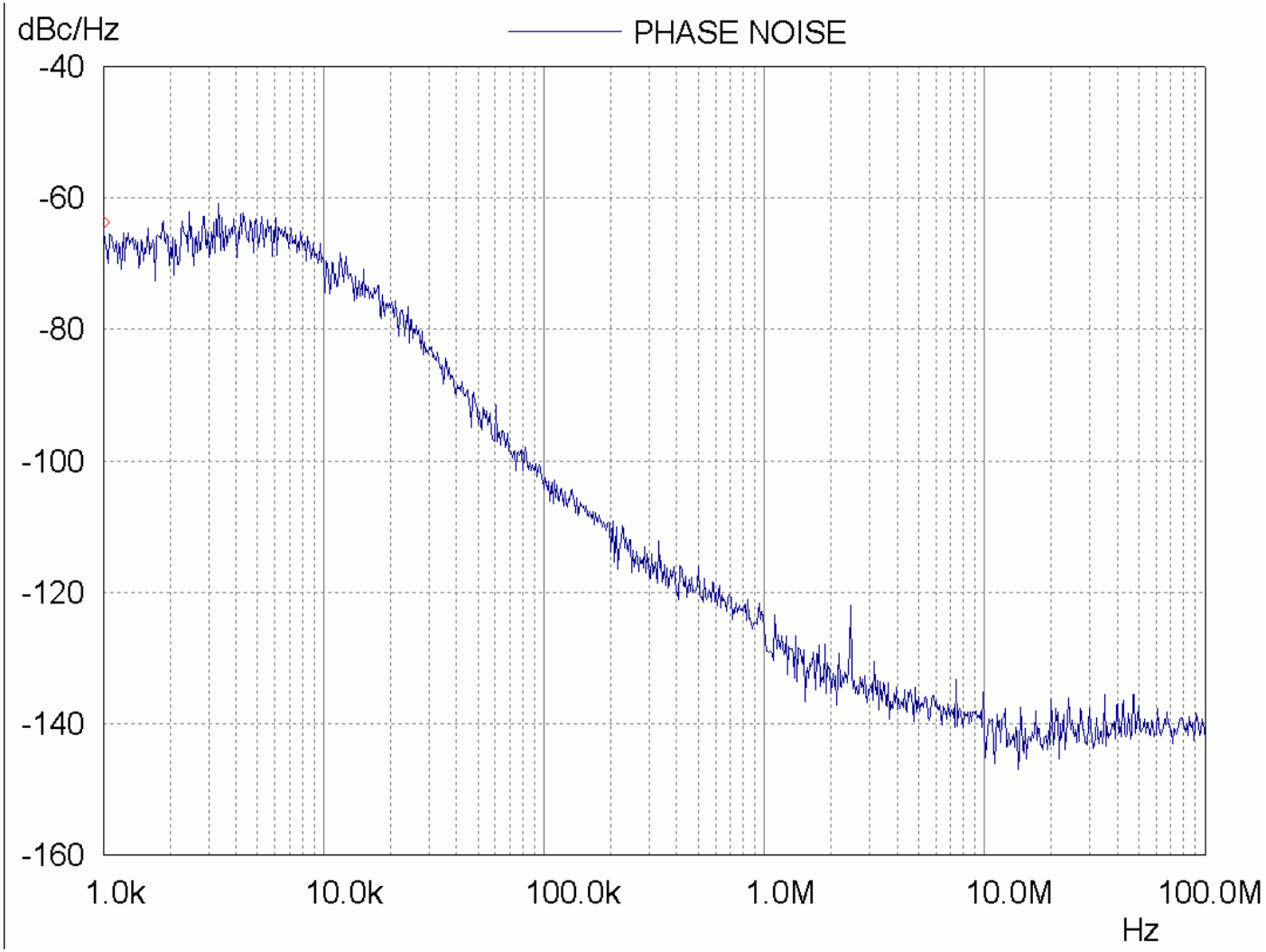
Testing Results : High Spur



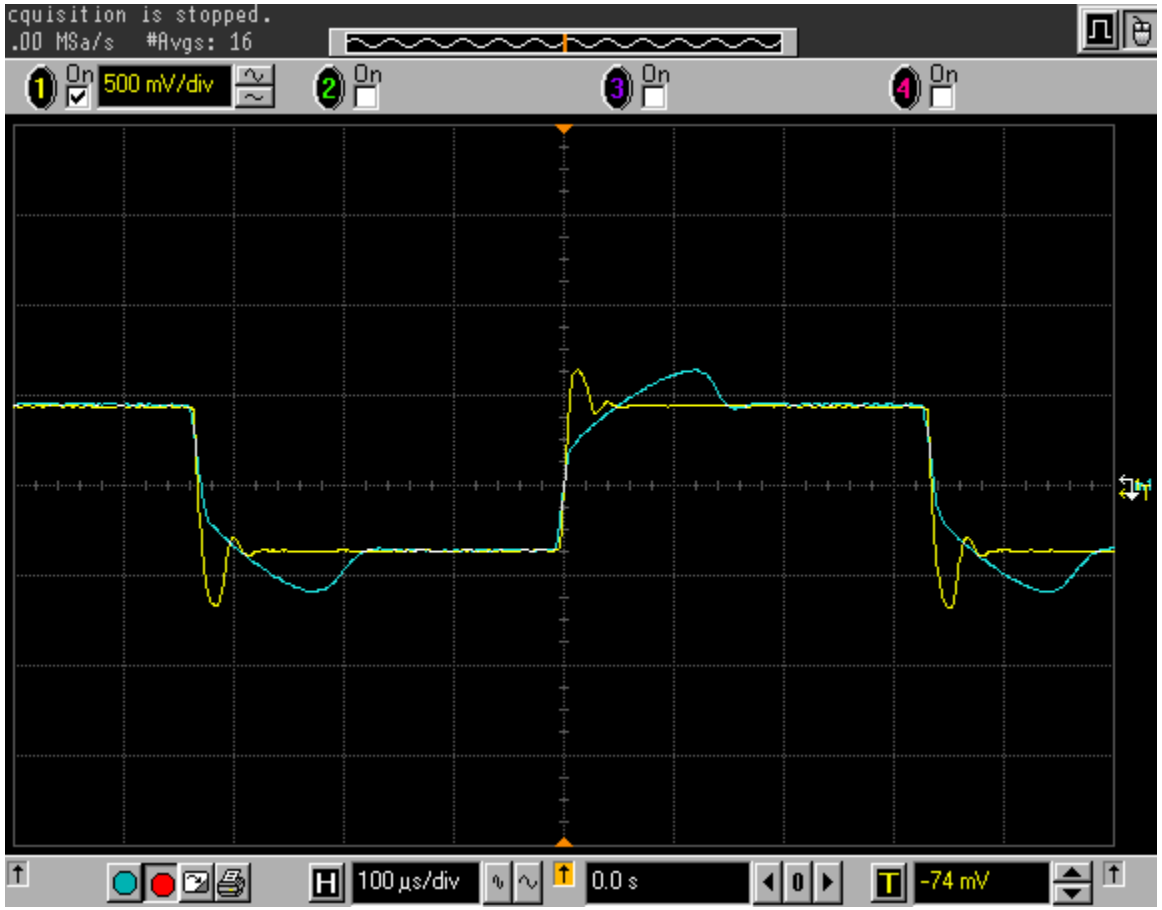
Testing Results : Low Spur



Testing Results : Phase Noise



Testing Results : Settling Time



Testing Results : Unstable Settling