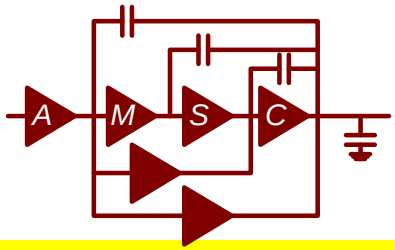
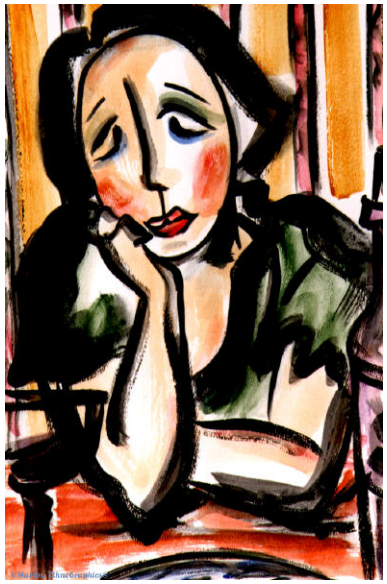


Analog and Mixed-Signal Center

Receiver Architectures:

Fundamentals and Properties

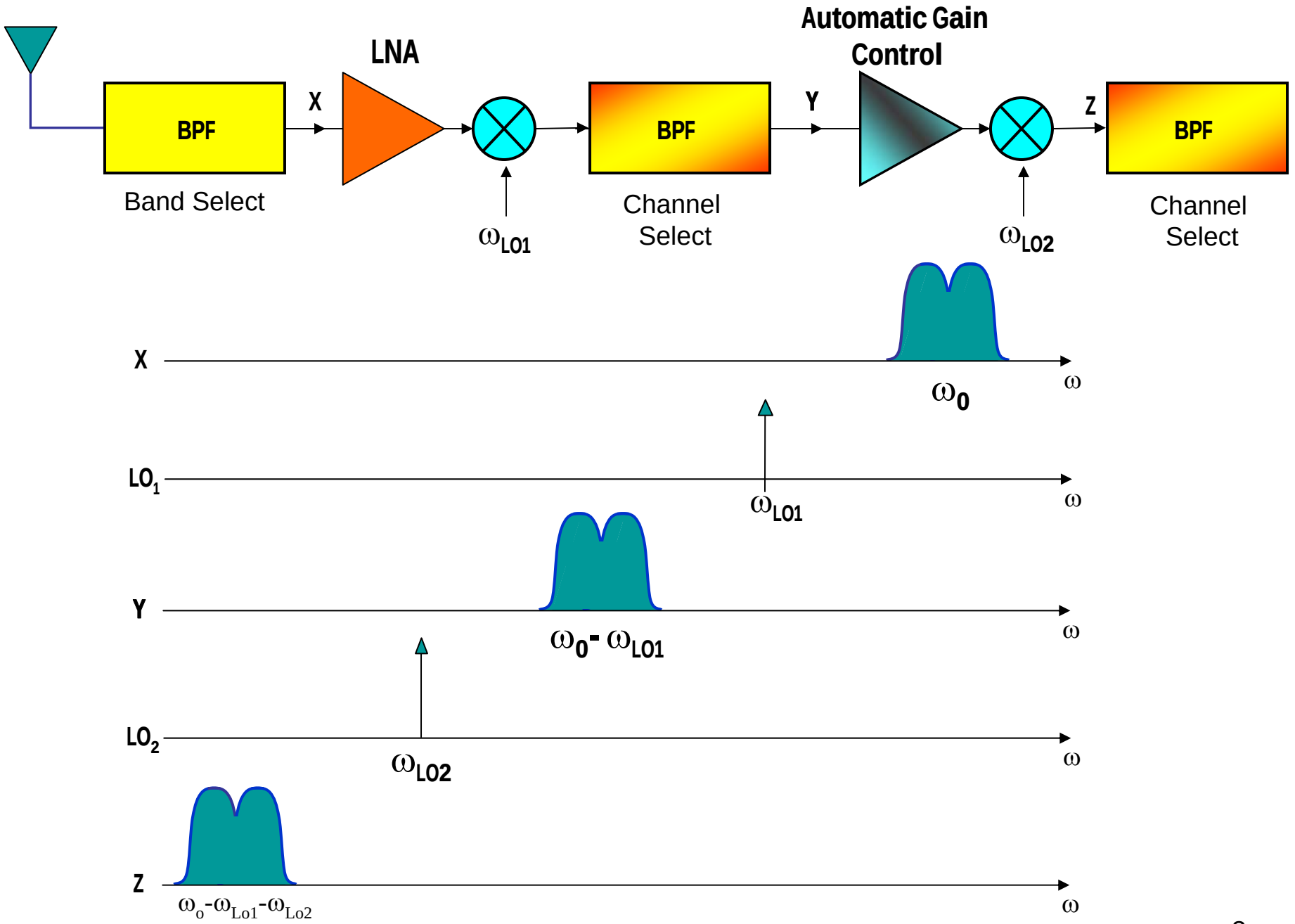


How can we relax or solve this image rejection problem ?

A possible solution is the use of more than one IF stage. This can relax the specs of the filters and other building blocks. How many IF stages are required ?

This depends on the design specs, a rule of thumb is to keep the ratio between the operating frequency before and after a downcoversion should be lower than 10. Say for a signal at 900 MHz can be first downconverted to an IF of 250 MHz, then filter out unwanted signal and second downconverted to 50 MHz and in a third downconversion the IF is 10 MHz.

How complex will be the filtering, power consumption and cost?



Double Superheterodyne Architecture

Multi-Stage IF Receivers

- From stage to stage the desired signal is further and further downconverted until the desired final IF is obtained.

- The ratio between the operating frequency before and after downconversion is usually kept lower than 10, say 4. For instance a 1800 MHz signal is first downconverted to a first IF of 450 MHz, then consecutively to 90 MHz and finally to 18 MHz.
- Note that each downconvertion stage has the same mirror frequency trouble than the single-stage IF receiver.
- Significant filtering between stages is required. This filtering is done with off chip filters to further complicate the sensitivity to parasitic components, also the power consumption will be high.

How are the ω_{LO} and ω_{IF} selected?

– Key consideration is the so-called image frequency.

– Ideally ω_{IF} should be high enough such that ω_{IMA} never falls in band.

– There are two possible choices for ω_{LO}

$\omega_{LO} = \omega_{RF} + \omega_{IF}$ High side injection

or

$\omega_{LO} = \omega_{RF} - \omega_{IF}$ Not a good choice

- Regarding ω_{IF} , one has to consider the VCO tuning range.

  Assume the AM case {530 to 1,610} KHz = BW

$$\omega_{IF} = \frac{BW}{2}$$

$$\omega_{IF} = \frac{(1{,}610 - 530)}{2} KHz = 540 KHz \neq 455 KHz$$

Case 1. $\{75 \text{ to } 1{,}155\} KHz$

$75\text{KHz} = (530 - 455)\ \text{KHz}$

$1{,}155\text{KHz} = (1{,}610 - 455)\ \text{KHz}$

ω_{LO} frequency span 15.4

Case 2. $\{985 \text{ to } 2{,}065)\ \text{KHz}$ High side injection

$985\text{KHz} = 530\text{KHz} + 455\ \text{KHz}$

$2{,}065\text{KHz} = (1{,}610 + 455)\ \text{KHz}$

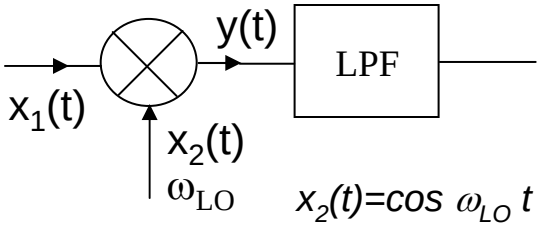
ω_{LO} frequency span 2.01

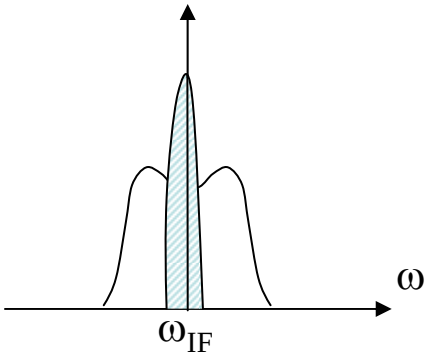
For VCO tuning reason, Case 2 is more attractive.

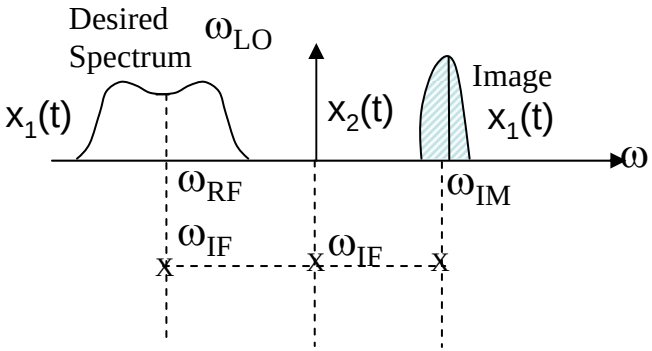
-Explore the case of FM VCO range.

Aside, there is a trade-off in IF selection; low IF improves the selectivity due to a Lower Q requirement of the SAW filter, while a high IF enhances the sensitivity due to higher attenuation that can be offered by the image-rejection filter.

IMAGE FREQUENCY PROBLEM

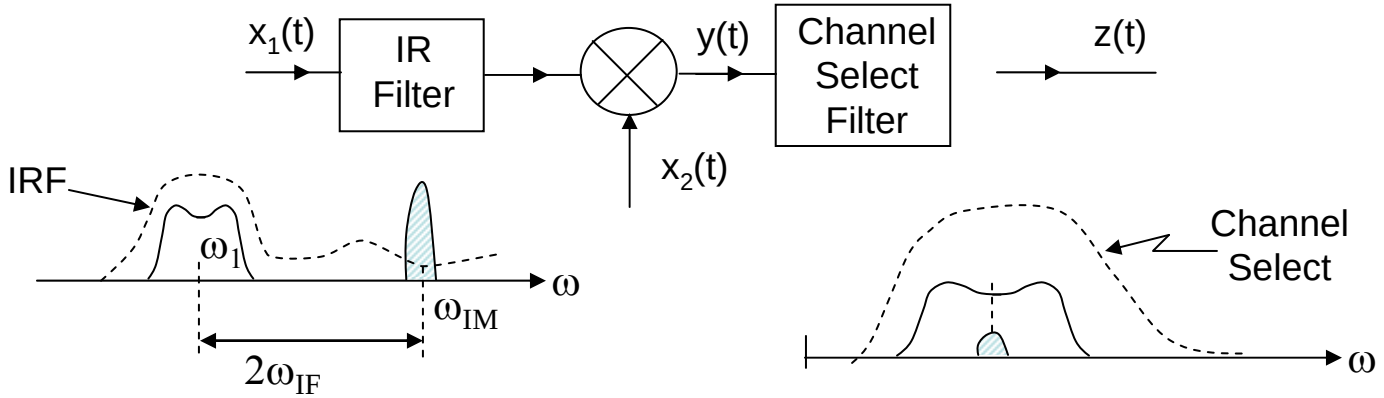






How to tackle this image frequency problem?

- Add a filter before and after



The conventional receiver (RX) Architectures are:

1. **Superheterodyne**

2. **Image Reject RX: Hartley and Weaver**

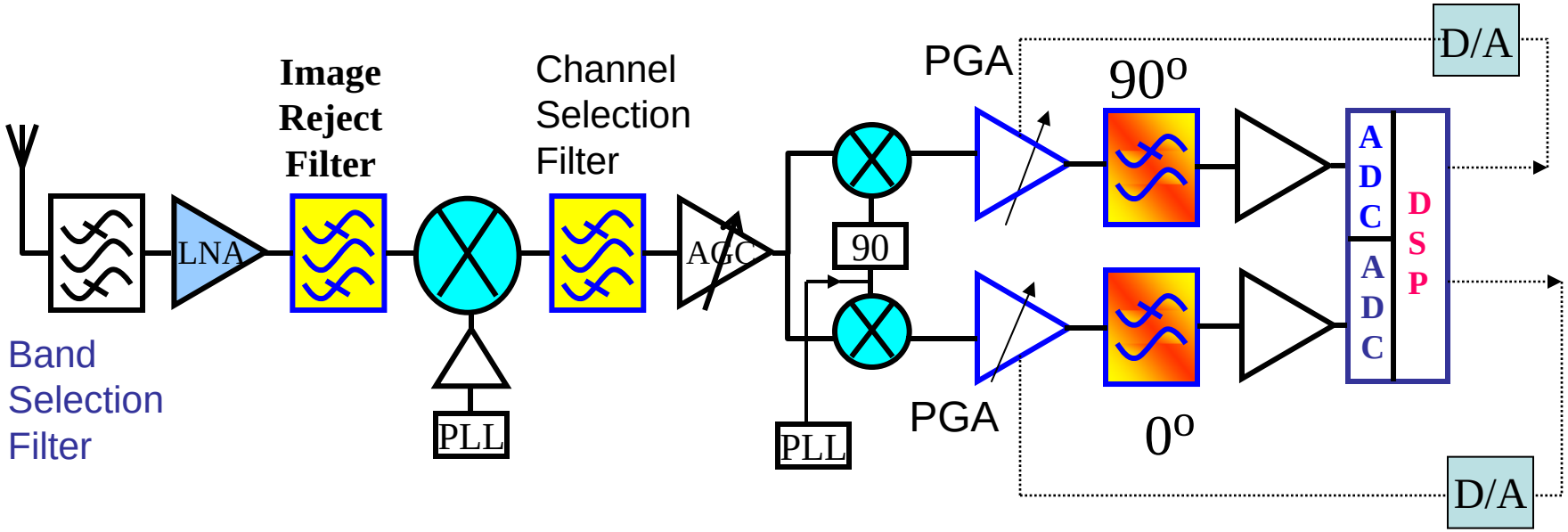
3. **Zero-Intermediate Frequency (IF)**

4. **Low –Intermediate Frequency (IF)**

These are the most used architectures in CMOS Receivers reported in the literature. The selection of the architecture is partially dependent on the standards. However some standard such as the GSM/DCS/PCS/EDGE have been designed using options 1, 3 and 4. Others such as Bluetooth have been dominated by low-IF Architecture. In other cases for multi-standards for instance the 802.11a/b/g the Zero-IF has been the dominant architecture for their implementations.

Next we discuss these architectures and their pros and cons.

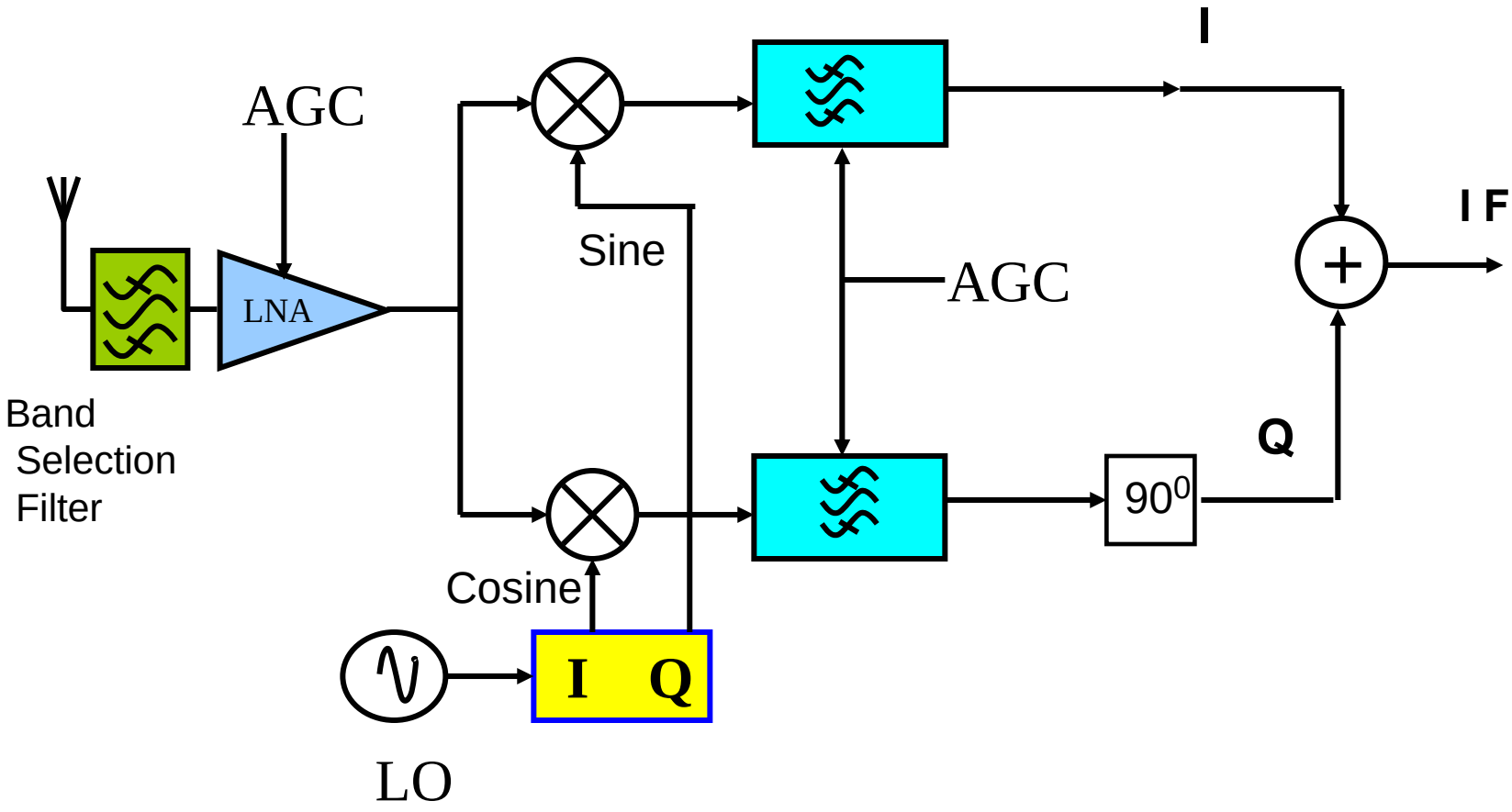
Super Heterodyne Receiver with Quadrature Down-conversion



- **Good performance in terms of image and spurious suppression.**
- **A *complex mixer* is required.**
- ***In the DSP a complex non-linear algorithm control the DC-level dynamically*.**
- **Low integration due to the use of SAW filters.**
- **Limited multi-standard ability.**

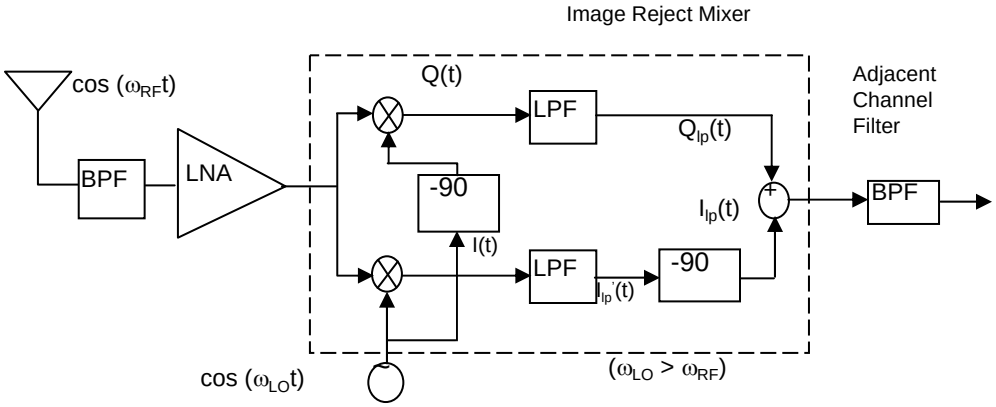
Due to the difficulty to design broadband I/Q phase shifters an alternative solution (*Weaver)* solution is next discussed.

HARTLEY Image Rejection RX



• Ideally the image is rejected, in practice the static gain/phase mismatches are 0.2 to 0.6 db/1^0 to 5^0, corresponding to an image rejection of roughly 30 to 40dB.

Image Rejection Mixer Analysis



$$I(t) = cos(\omega_{LO}t)\cdot cos(\omega_{RF}t)$$
$$= 0.5\{cos[(\omega_{LO} - \omega_{RF}t)] + cos[(\omega_{LO} + \omega_{RF})t]\}$$
$$Q(t) = sin(\omega_{LO}t)\cdot cos(\omega_{RF}t)$$
$$= 0.5\{sin[(\omega_{LO} - \omega_{RF})t] + sin[(\omega_{LO} + \omega_{RF})t]\}$$

$$I_{lp}`(t) = 0.5cos[(\omega_{LO} - \omega_{RF})t] = 0.5cos(\omega_{IF}t)$$
$$Q_{lp}(t) = 0.5sin[(\omega_{LO} - \omega_{RF})t] = 0.5sin(\omega_{IF}t)$$
$$I_{lp}(t) = 0.5cos(\omega_{IF} - 90^o) = 0.5sin(\omega_{IF}t)$$

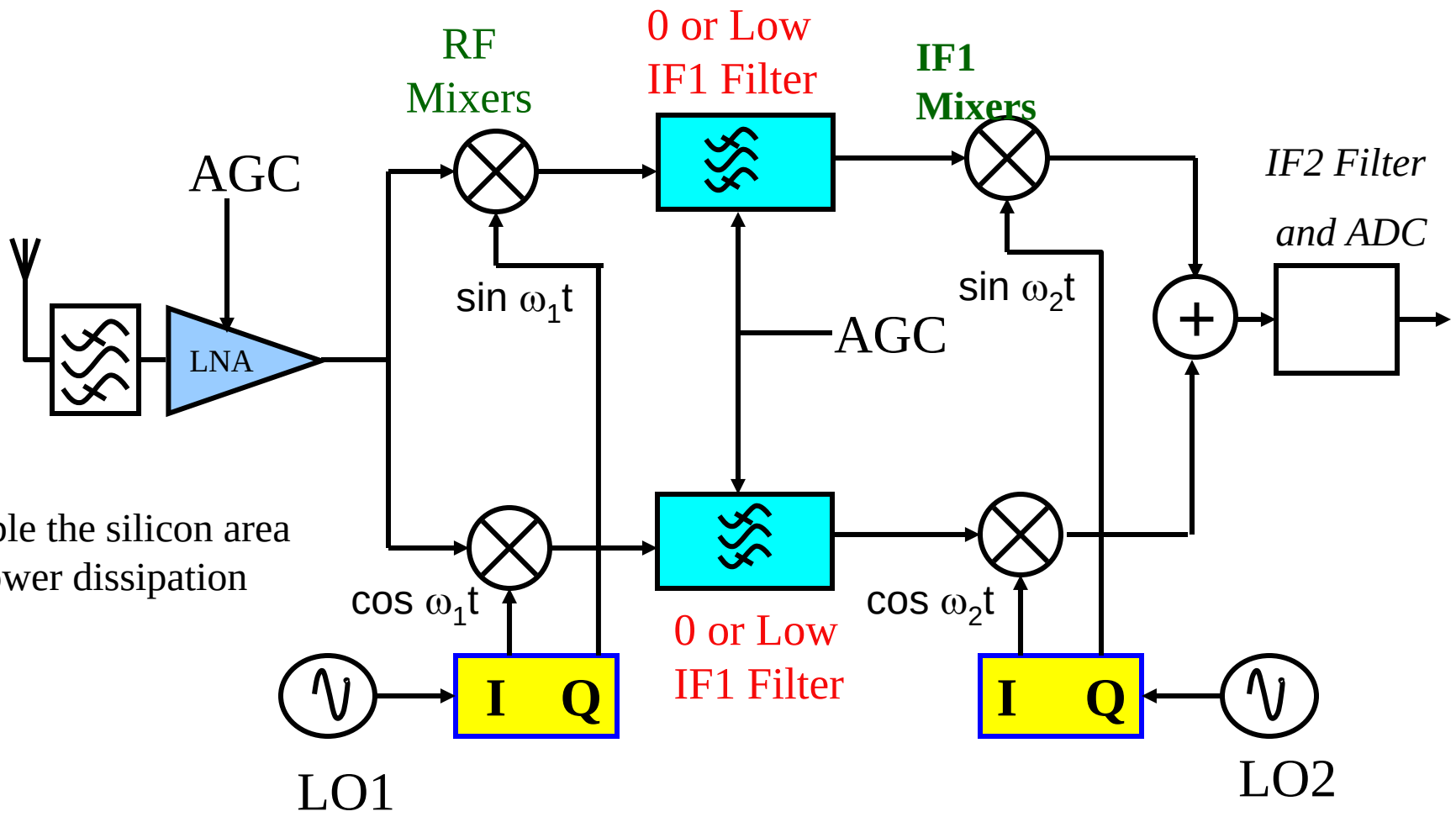
$$\Rightarrow \quad v_o(t) = I_{lp}(t) + Q_{lp}(t) = sin(\omega_{IF}t).$$

The **image input** signal, *for high-side injection* of the LO, is $v_{I,Im}(t)=cos[(\omega_{LO} + \omega_{IF})t]$.

$$I(t) = cos[(\omega_{LO} + \omega_{IF})t]\cdot cos(\omega_{LO}t) = 0.5\{cos(\omega_{IF}t) + cos[(2\omega_{LO} + \omega_{IF})t]\}$$
$$I_{lp}`(t) = 0.5cos(\omega_{IF}t)$$
$$I_{lp}(t) = 0.5sin(\omega_{IF}t)$$
$$Q(t) = sin(\omega_{LO}t)\cdot cos[(\omega_{LO} + \omega_{IF})t] = 0.5sin(-\omega_{IF}t) + 0.5sin[(2\omega_{LO} + \omega_{IF})t]$$
$$Q_{lp}(t) = -0.5sin(\omega_{IF}t)$$

$\Rightarrow$ $v_{o,Im}(t) = I_{lp}(t) + Q_{lp}(t) = 0;$ Image response can be completely suppressed.

The Barber-Weaver Receiver

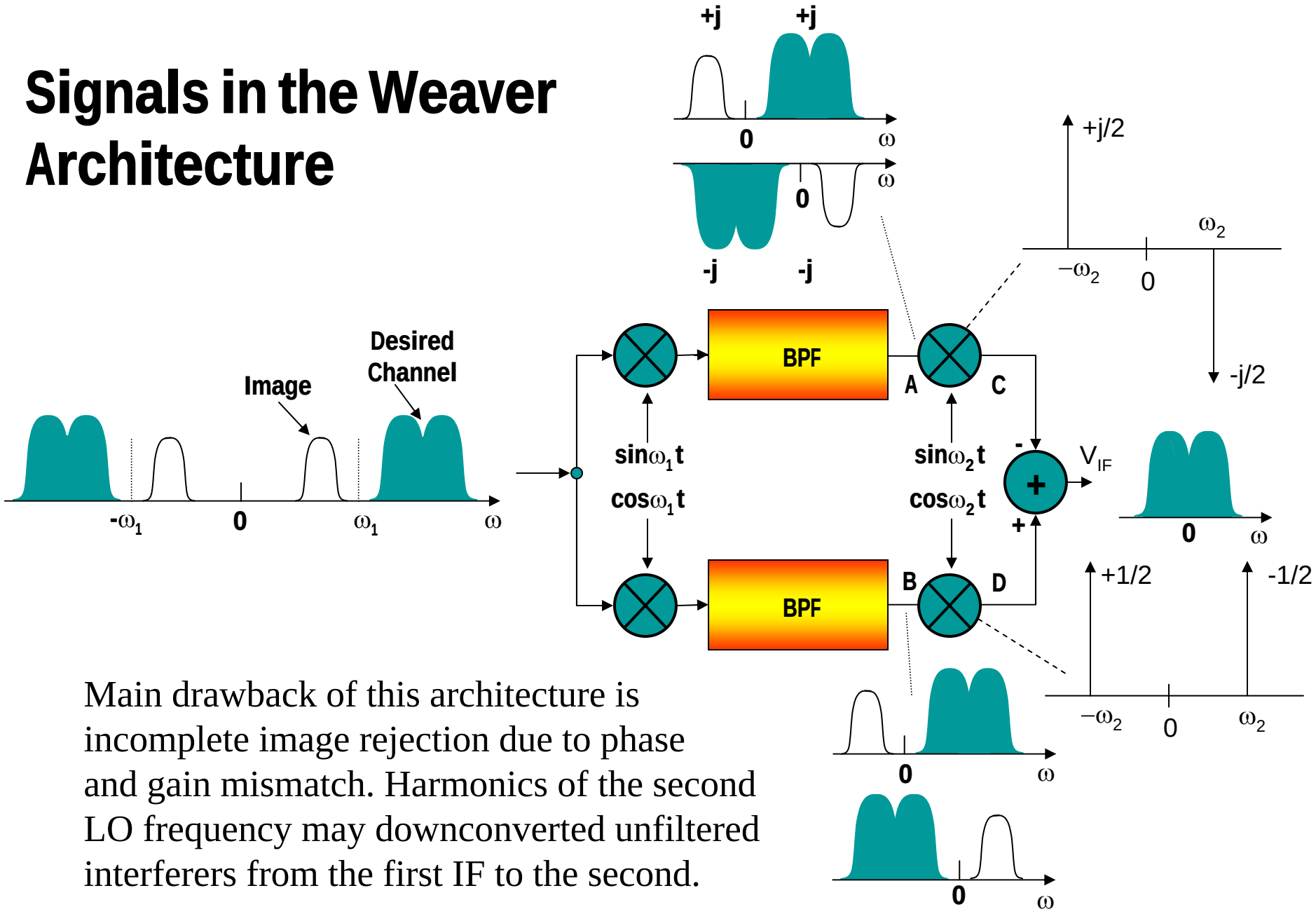


• Double the silicon area and power dissipation

• Difficult Matching of I & Q Paths ; - No phase shifter (90^0) needed

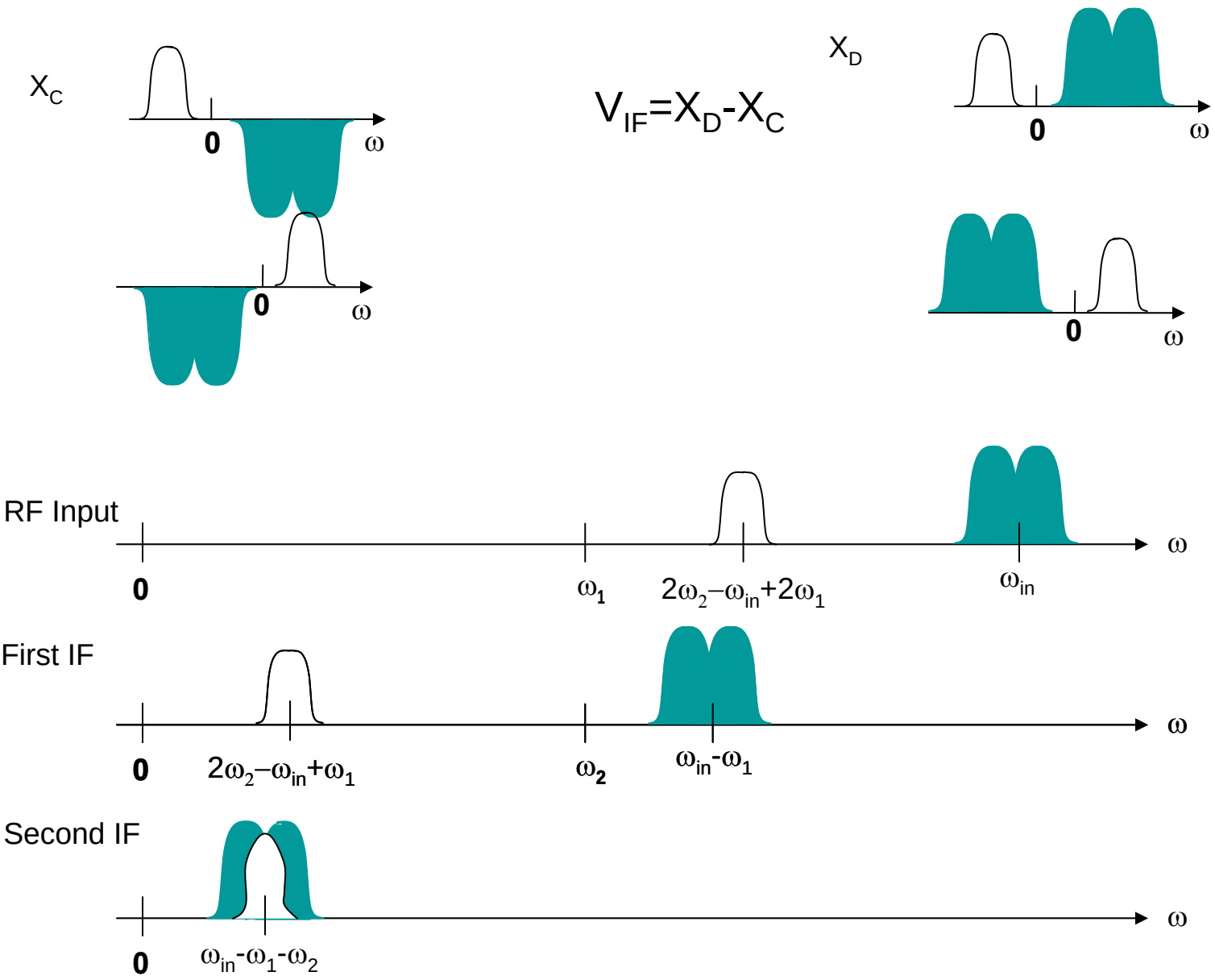
• Operates with low IF1 and IF2 ; - overhead in area for LO2, mixers.

Signals in the Weaver Architecture

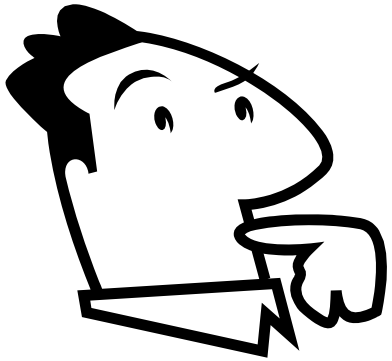


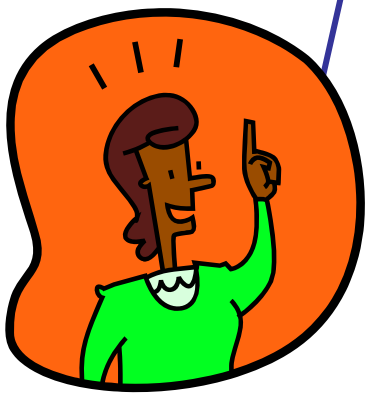
Main drawback of this architecture is incomplete image rejection due to phase and gain mismatch. Harmonics of the second LO frequency may downconverted unfiltered interferers from the first IF to the second.

Problem of Secondary Image



What other receiver structures alternatives can be considered and with what properties ?



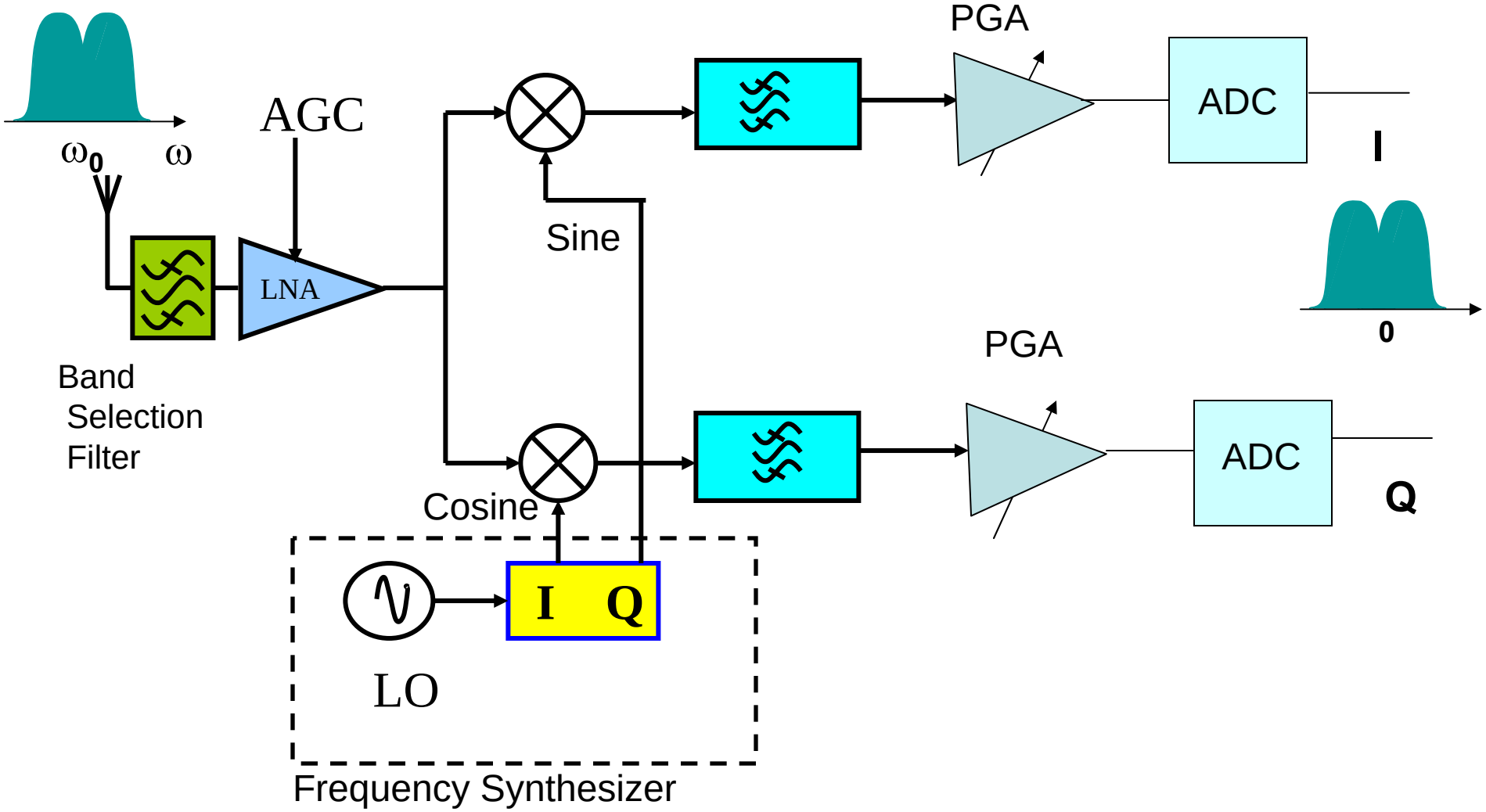


Can we make the IF very low, say to DC ?

How and at what price ?

Direct Conversion (IF=0)

Direct Conversion or Zero-IF front end Receiver



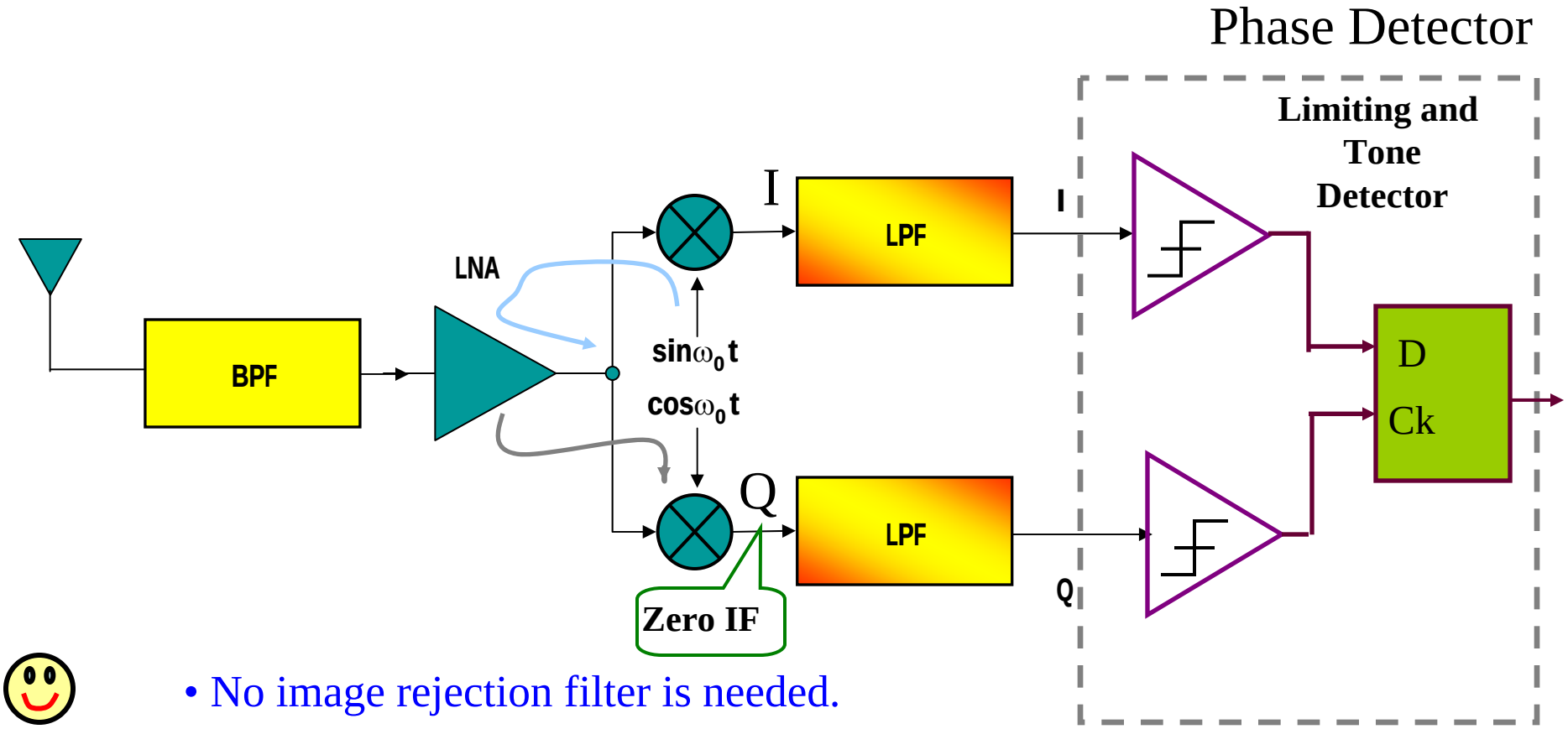
Direct Conversion or Zero-IF front end Receiver

- The LPF can be integrated. No image signal exists
- The RF spectrum is translated to the baseband in the first downconversion.
- The LO is equal to the input carrier frequency.

- This architecture operates only with double-sideband AM signals because it overlaps negative and positive parts of the input spectrum.

- For frequency and phase-modulated signals, the downconversion needs quadrature outputs. *Two sides of FSK (or QPSK) carry different information.*

Direct Conversion Front End Receiver With Quadrature Down-Conversion for FSK (digital) Demodulation



- No image rejection filter is needed.

- Offset voltages can degrade the S/N and saturate the following stages. Isolation between ports is not ideal.
- I/Q mismatch degrades the downconversion constellation

FSK Direct Conversion Receiver.-

The frequency shift keyed signals appear with opposed relative phase at the phase detector, giving a binary mark or space output according to weather the input signal is lower or higher than the local oscillator frequency. Let assume these inputs (mark and space) signals are:

$$S_M = \cos(\omega + \omega_D)t$$

$$S_S = \cos(\omega - \omega_D)t$$

The quadrature oscillator signals to the mixers are:

$$LO_I = \cos \omega t$$

$$LO_Q = \sin \omega t$$

The mixer outputs when a **mark** is sent are:

$$I_M = S_M \cdot LO_I = \cos(\omega + \omega_D)t \cdot \cos \omega t$$

$$I_M = 0.5[\cos(\omega + \omega_D) + \cos \omega_D t]$$

$$Q_M = S_M \cdot LO_Q = \cos(\omega + \omega_D)t \cdot \sin \omega t$$

$$Q_M = 0.5[\sin(2\omega + \omega_D)t - \sin \omega_D t]$$

Similarly when a **space** is sent:

$$I_S = 0.5[\cos \omega_D t + \cos(2\omega + \omega_D)t$$

$$Q_S = 0.5[\sin(2\omega - \omega_D)t + \sin \omega_D t]$$

The double frequency components of I and Q are removed in the LPF of each channel, yielding:

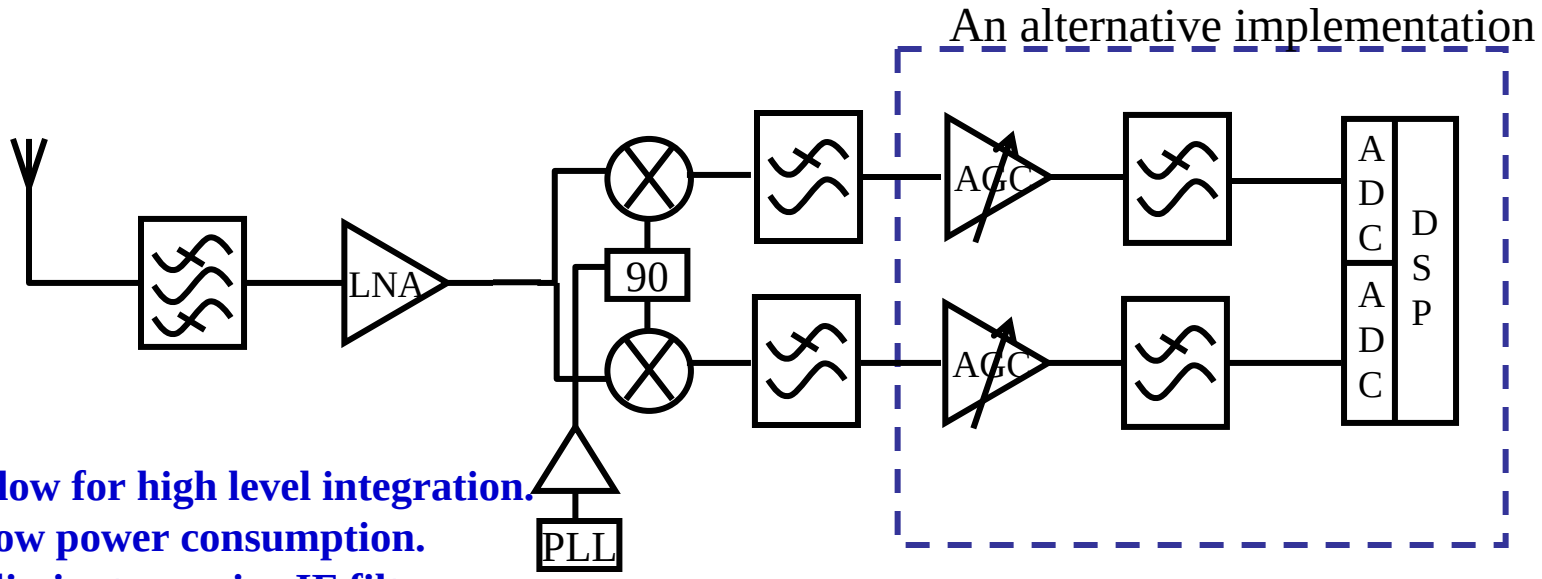
$$I_M = +0.5 \cos \omega_D t$$

$$Q_M = -0.5 \sin \omega_D t$$

$$I_S = +0.5 \cos \omega_D t$$

$$Q_S = +0.5 \sin \omega_D t$$

Direct-Conversion Receiver (continues)



- ✓ **Allow for high level integration.**
- ✓ **Low power consumption.**
- ✓ **Eliminate passive IF filters**
- ✓ **Good for SSB digital modulation**
- ✓ **Good Multi-standard ability.**
- ➢ **DC offset problem.**
- ➢ **Increased ADC dynamic range. Because of limited filtering**
- ➢ **Need of a high-Q VCO.**

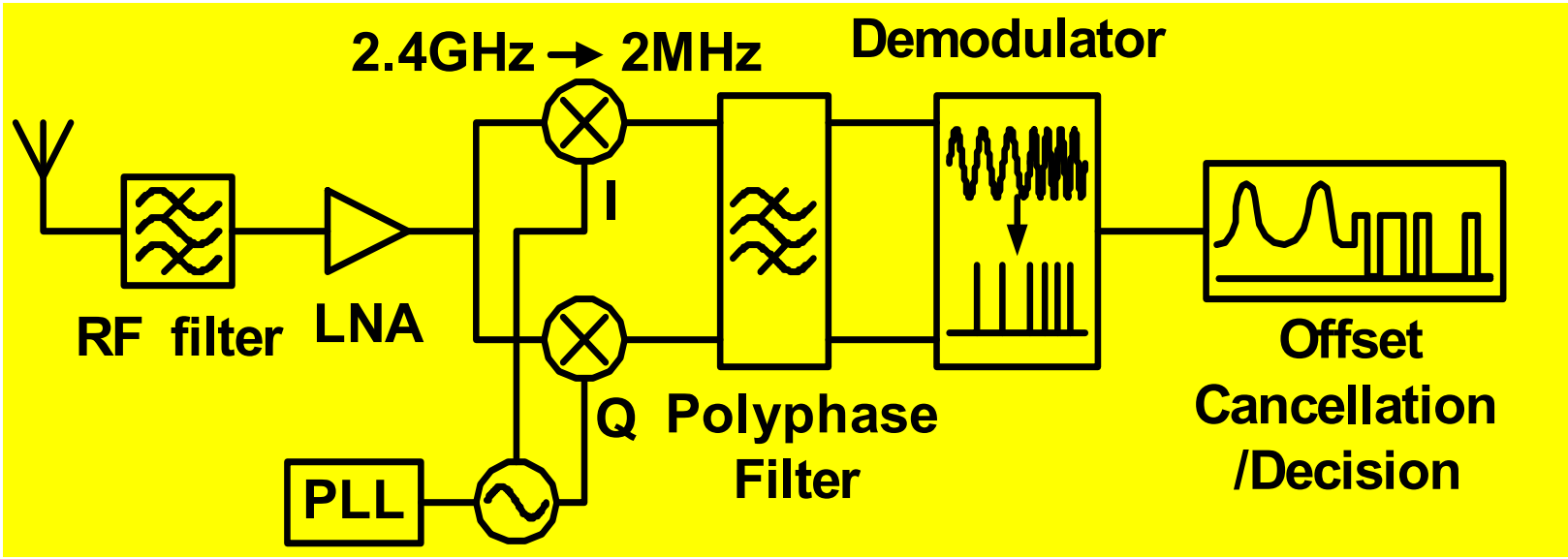
- Moves design efforts to baseband.
- Unprotected LO leakage into antenna.
- I/Q match required over high gain range

Low IF Receiver Architecture

- All advantages of direct conversion.
- More difficult image rejection.
- DC spur (offset) outside the signal bandwidth.
- Digital processing includes adjacent channel image rejection.
- All weakness of direct conversion without the DC offset problem.
- In Band image rejection.

0.35μm CMOS Bluetooth Low-IF Receiver IC:

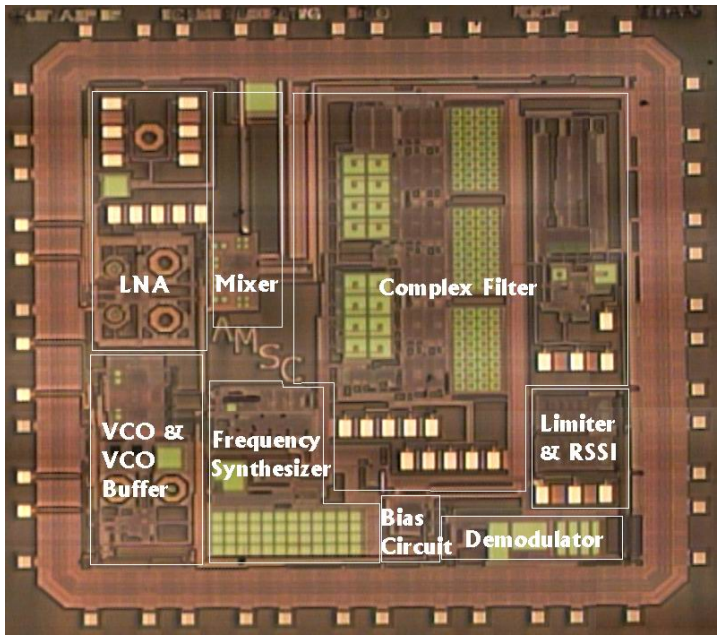
An example of a Low-IF topology

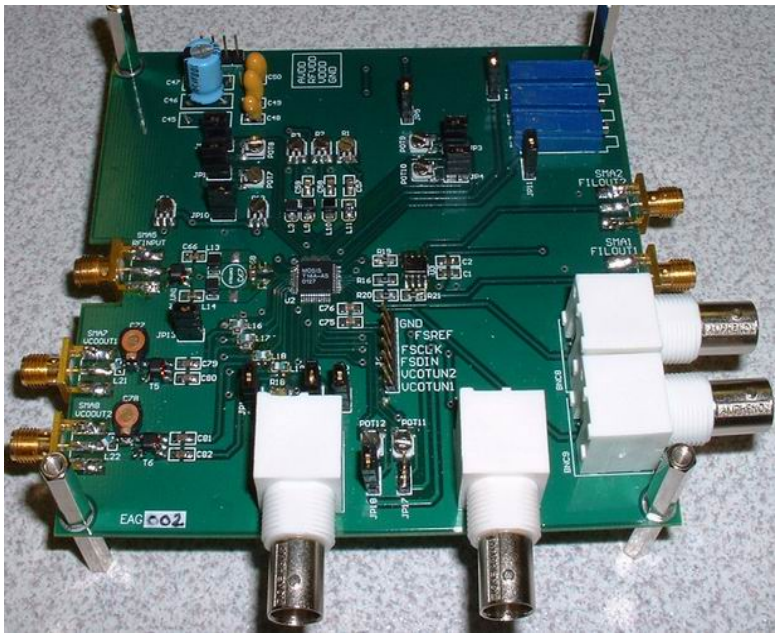


Developed in about 1 ½ years by:

Authors: Wenjun Sheng, Bo Xia, Ahmed Emira, Chunyu Xin, Ari Valero-Lopez, Sung Tae Moon and Edgar Sanchez-Sinencio.

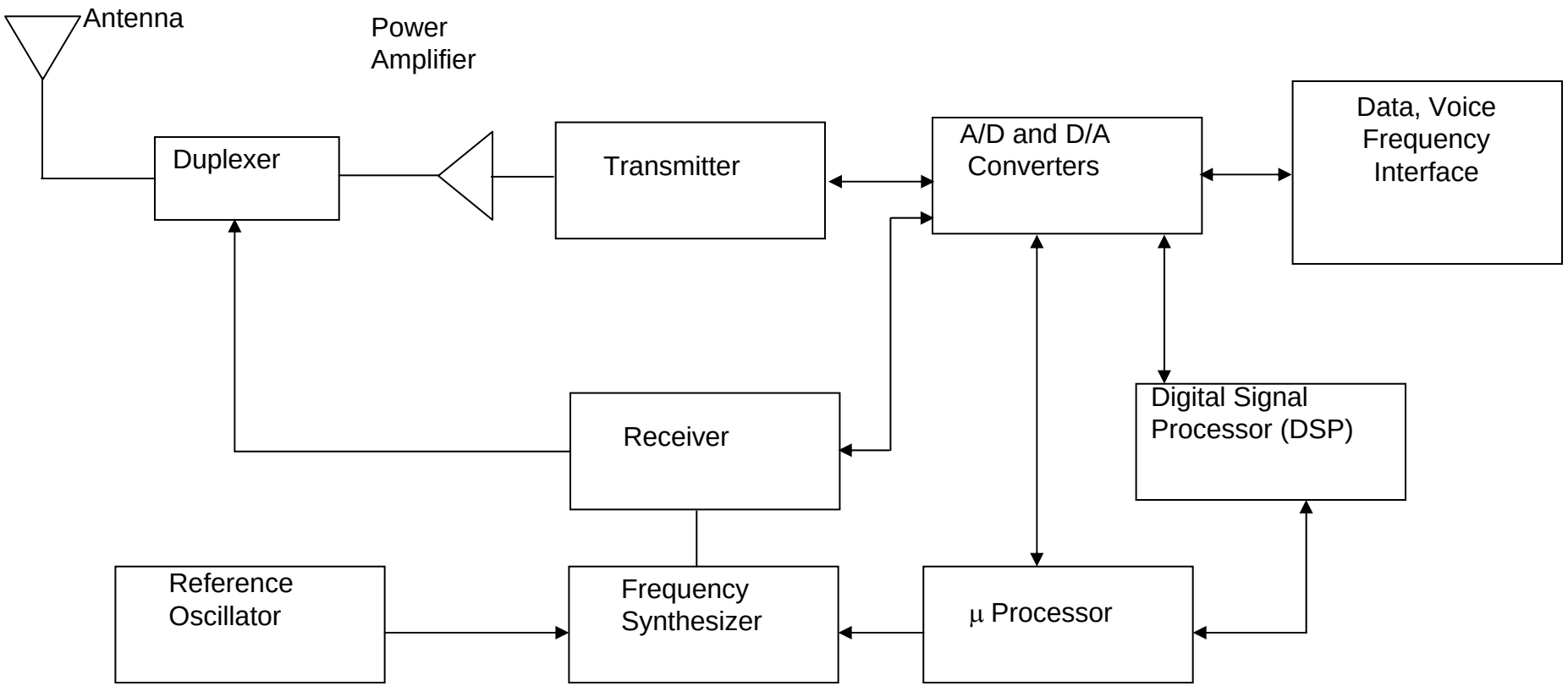
0.35μm CMOS Bluetooth Low-IF Receiver IC



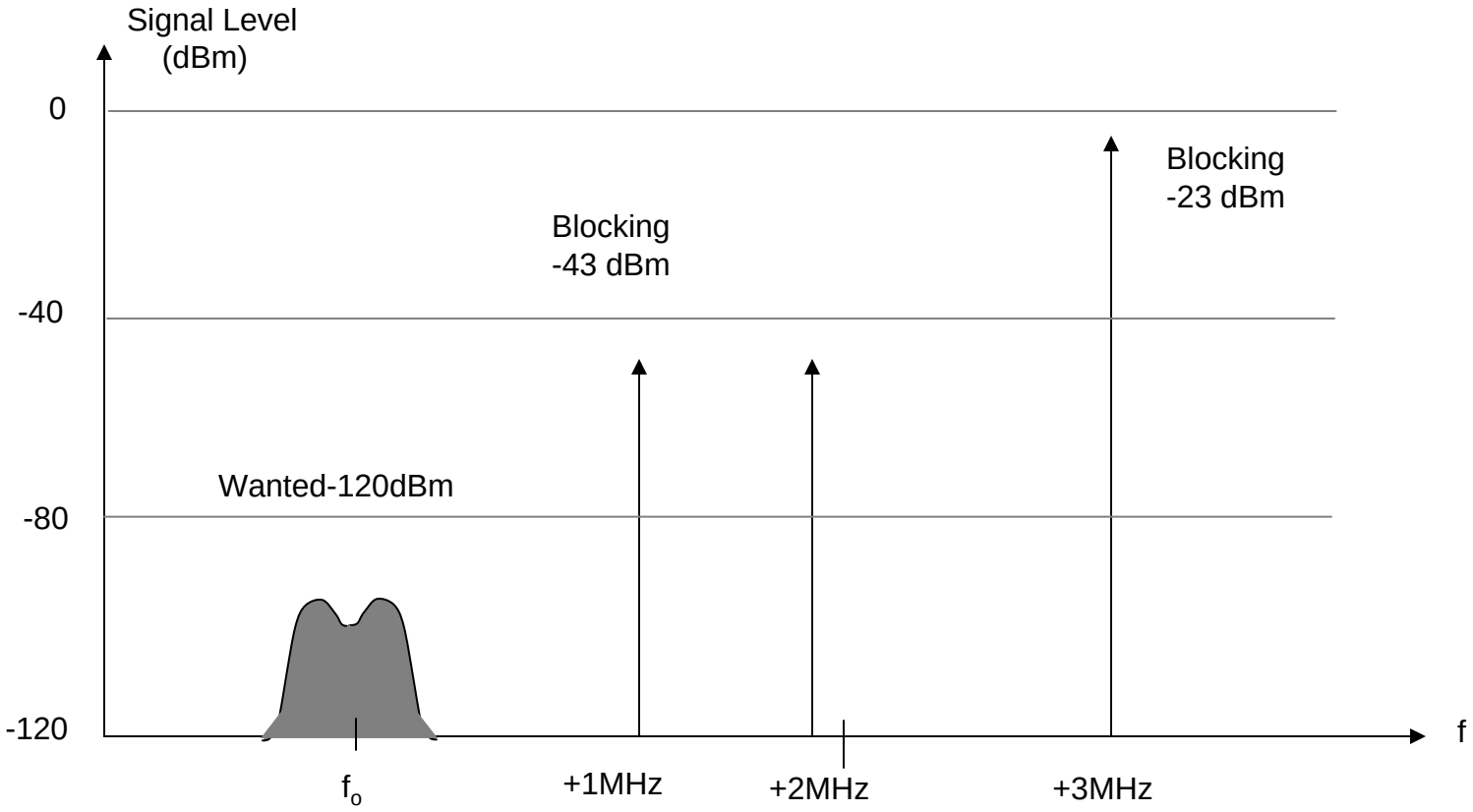


- Publications:
  - 2002 RFIC Conference, Best Student Paper Award (third place).
  - Journal of Solid-State Circuits: January 2003 (Receiver) and August 2003 (Demodulator).
  - Transactions on Circuits and Systems – II: November 2003 (Complex Filter).

TRANSCEIVER CELLULAR RADIO BLOCK DIAGRAM

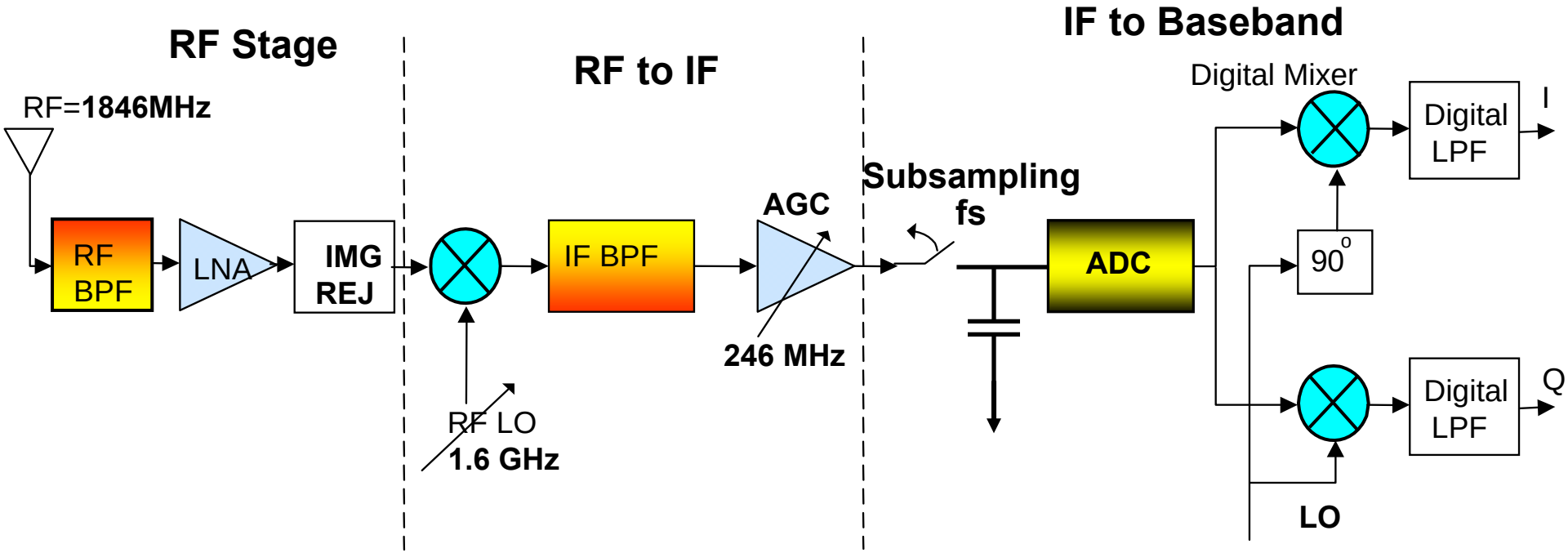


GSM Receiver System Requirements



- Gain of wanted signal > 100 dB
- Noise Figure of LNA input less than 8 dB

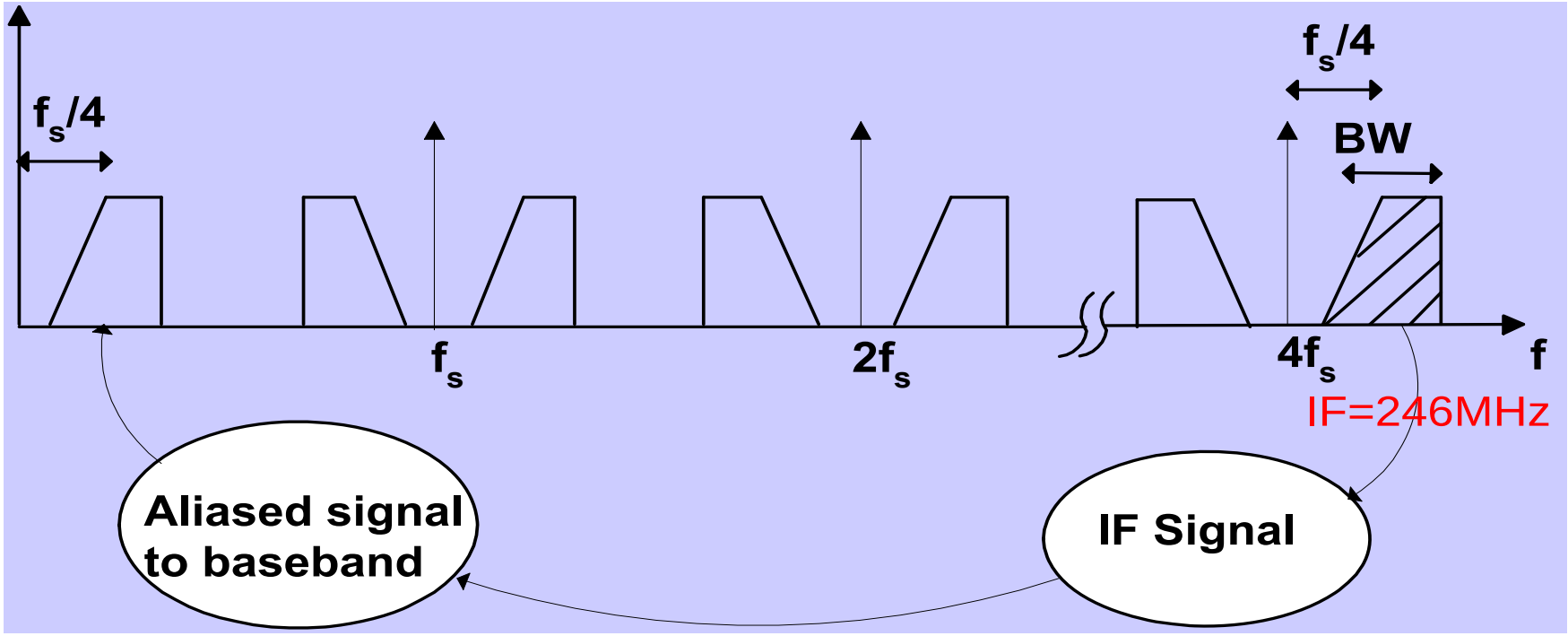
Subsampling Receiver



Example: 1.8 GHz GSM Specifications: **IF carrier frequency = 246 MHz, Channel BW = 200 KHz, Input Dynamic Range = 90 dB.**

- 2 digital low frequency mixers, no noise and distortion.
- Easier I&Q matching.
- No DC offset and 1/f noise. Aliasing
- More digital means easier integration on a CMOS process.
- SNR degradation due to noise folding
- ADC & SH have to run at high clock to minimize noise folding.

Sub-sampling Receiver: Basic Idea



- The sampling rate, f_s, can be much less than the IF carrier.
- But, $f_s > 2 \times BW$ must be satisfied (to avoid destructive aliasing).

Examples of Standards (simplified versions)

	Bluetooth	802.11b (Wi-Fi)	HomeRF
Data rate	1Mb/s	1-11Mb/s	1Mb/s, 5Mb/s
Power	Lower	**Higher**	Variable
Modulation	FH-GFSK	DSSS-CCK	FH-GFSK
Frequency Band	2.401 – 2.48GHz	2.4 – 2.48GHz	2.401-2.480 GHz

IEEE 802.15.4 (“Zigbee”)

Parameter	North America	North America	Europe
Frequency Range	2402-2480 MHz	902-928 MHz	2412-2472 MHZ
Channel spacing	5 MHz	5 MHz	5 MHz
Multiple access method	CSMA/CA	CSMA/CS	TDMA
Duplex method	FDD	FDD	FDD
Users per channel	255	255	255
Modulation	OPQSK, BT=0.5	OPQSK, BT=0.5	GFSK,BT=0.5
Peak bit rate	250 kHz	40 kHz	250 KHz

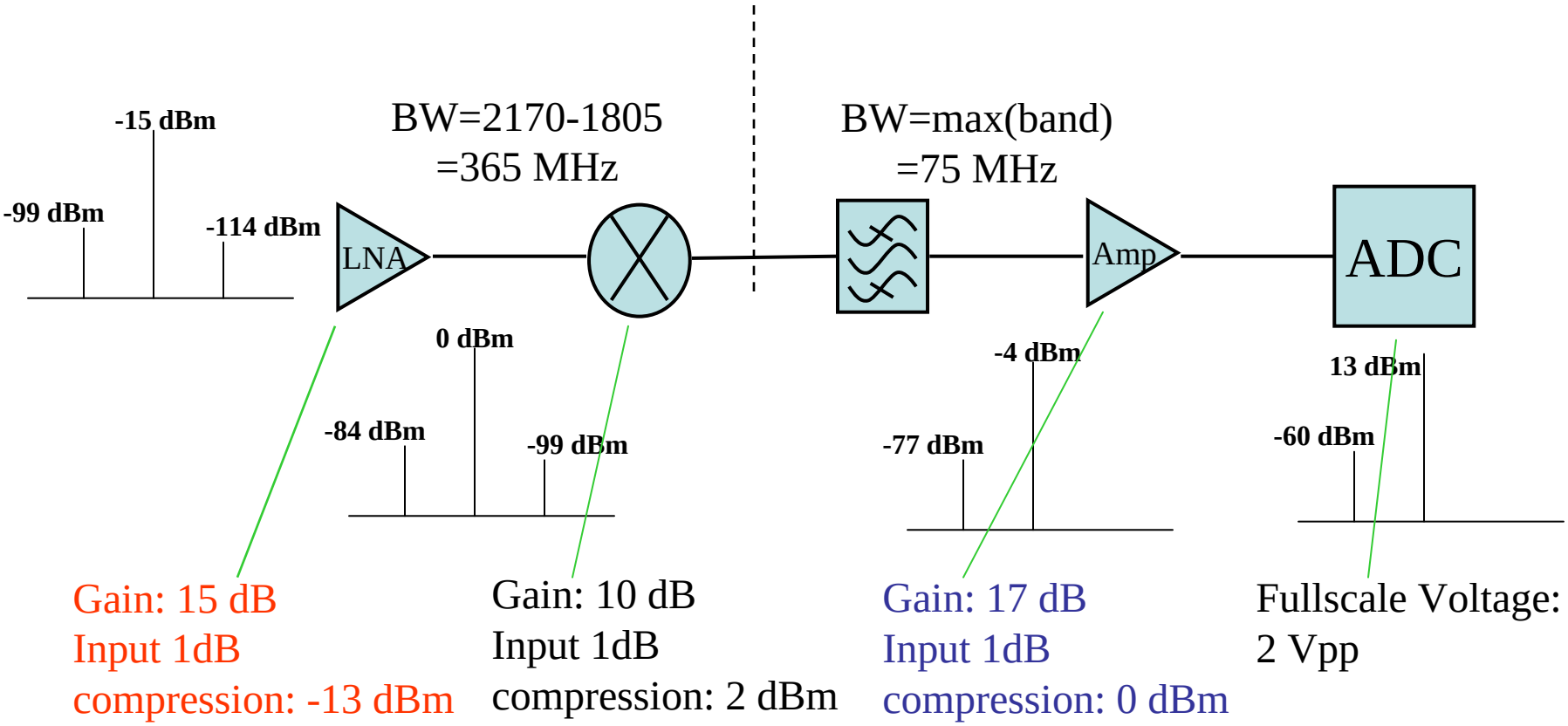
Summary of IS-95 CDMA

Parameter	800 MHz	1900 MHz	Asia
Mobile-to-base frequency	824-849 MHz	1850-1910 MHz	1920-1980 MHz
Base-to-mobile frequency	869-894 MHz	1930-1990 MHz	2110-2170 MHz
Channel spacing	1250 kHz	1250 kHz	1250 kHz
Number of channels	20	48	48
Multiple access method	CDMA/FDM	CDMA/FDM	CDMA/FDM
Duplex method	FDD	FDD	FDD
Users per channel	More than 15	More than 15	More than 15
Modulation	QPKK/OQPSK	QPKK/OQPSK	QPKK/OQPSK
Channel bit rate (chip rate)	1.2288 Mb/s	1.2288 Mb/s	1.2288 Mb/s

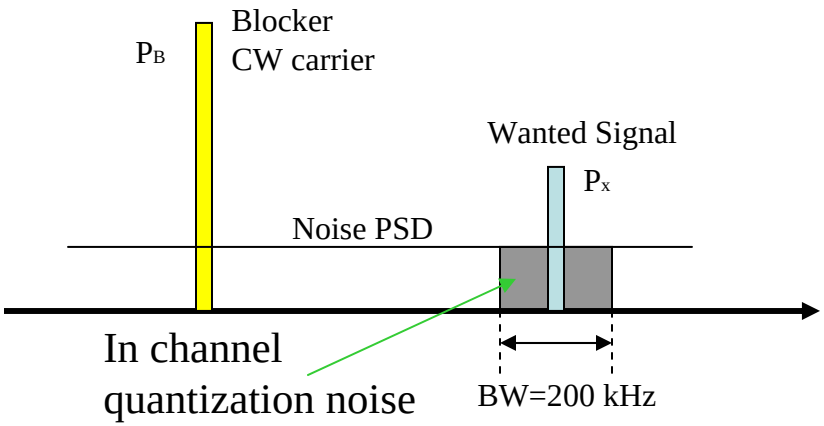
UMTS/DCS1800 Specifications

	DCS1800	UMTS
Frequency Band	1805 - 1880 MHz	2110 - 2170 MHz
Channel BW	200 kHz	5 MHz
System Sensitivity	-102 dBm	-117 dBm(@32ksps)
BER	1e-3	1e-3
Blocking Characteristics	600 - 800 kHz: -43 dBm 800 - 1600 kHz: -43 dBm 1600 - 3000 kHz: -33 dBm > 3000 kHz: -26 dBm	10 - 15 MHz: -56 dBm 15 - 60 MHz: -44 dBm 60 - 85 MHz: -30 dBm > 85 MHz: -15 dBm
Adjacent Channel Interference	Cochannel: -9 dBc 200 kHz: 9 dBc 400 kHz: 41 dBc 600 kHz: 49 dBc	5 MHz: -52 dBm

Multi-Channel, Multi-Mode Dynamic Range (1) DCS1800



Multi-Channel, Multi-Mode Dynamic Range (2) DCS1800



P_B = 13 dBm

P_x = -60 dBm

To ensure that the quantization noise power is negligible compared to that of interferers and other sources of thermal and device noise, choose

SNR_{QF} = 20 dB

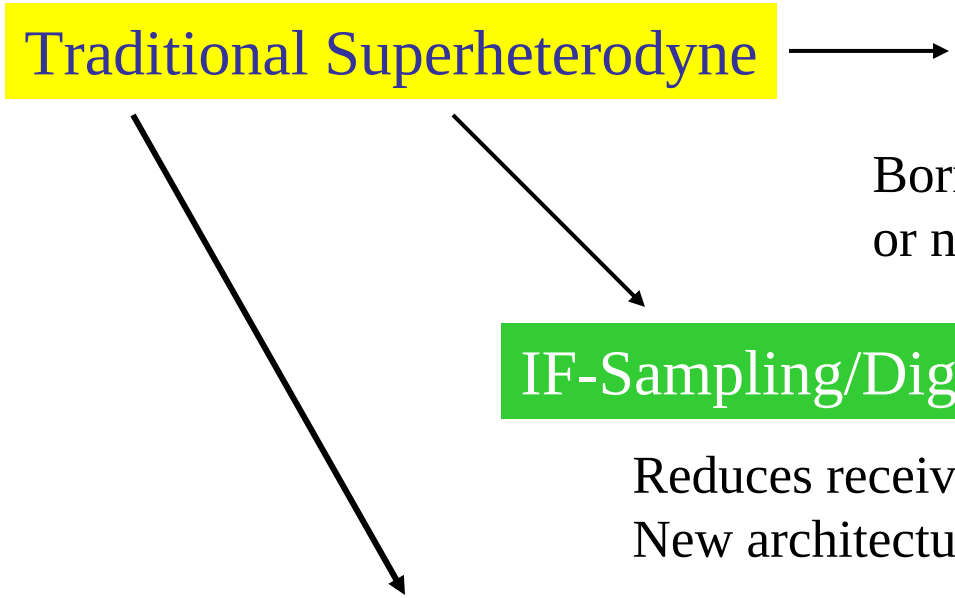
With F_S = 150 MHz, calculated resolution of ADC is 11 bits.
The SFDR (for single blocker) can be calculated by:

$SFDR = P_B - P_x + SNR_{QF}$ = 93 dB

Required ADC Spec.: F_S >= 150 MHz, b = 11, SFDR = 93 dB
Current State of the art ADC:

F_S = 80 MHz, b = 14, SFDR = 100 dB(AD6644)

Receiver Technology Trends

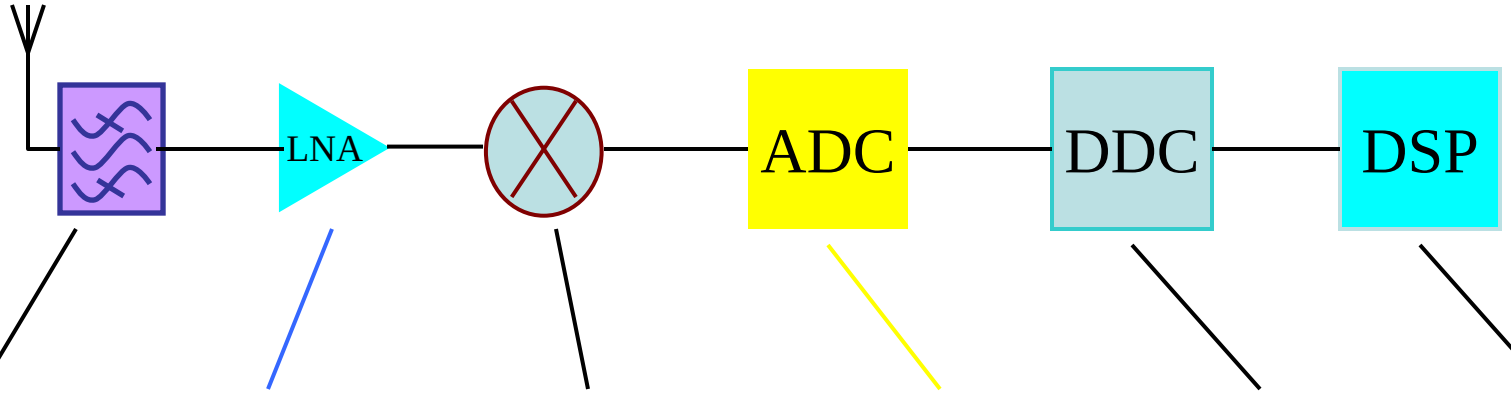


Borrows from handset chip integration,
or new architecture like direct-conversion.

Reduces receiver size by eliminating IF stages
New architectures using more digital processing

Large reduction in receiver size
Major architectures shift to DSP-intensive radio, highly programmable

Software Receiver



Band Select Filter Remove unwanted spectrum

High Intercept Point Amplifiers Amplify signals without the introduction of significant intermodulation products

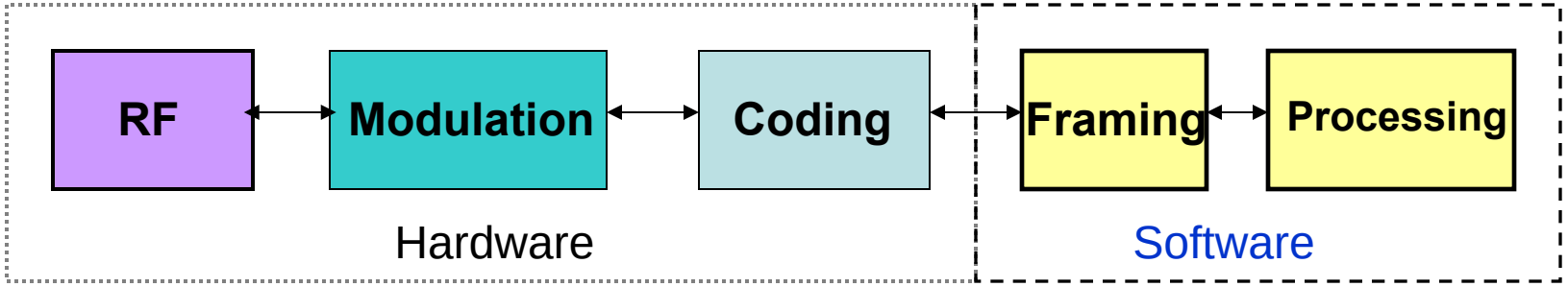
High Intercept Point Mixers translate input spectrum to ADC signal bandwidths

Wide Dynamic Range ADC digitize entire spectrum for digital channel selection

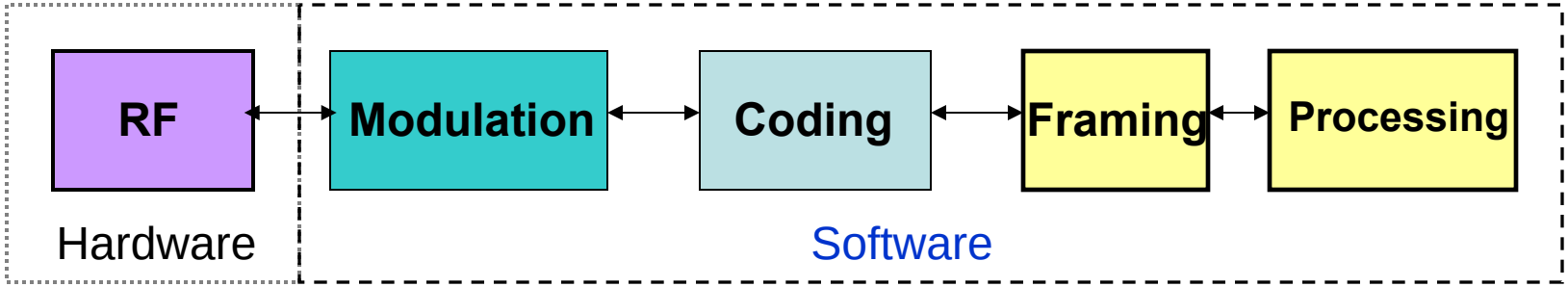
Fixed Function DSP digitally selects and filters the channel of interest

Fast DSP with on-chip Memory demodulates signal

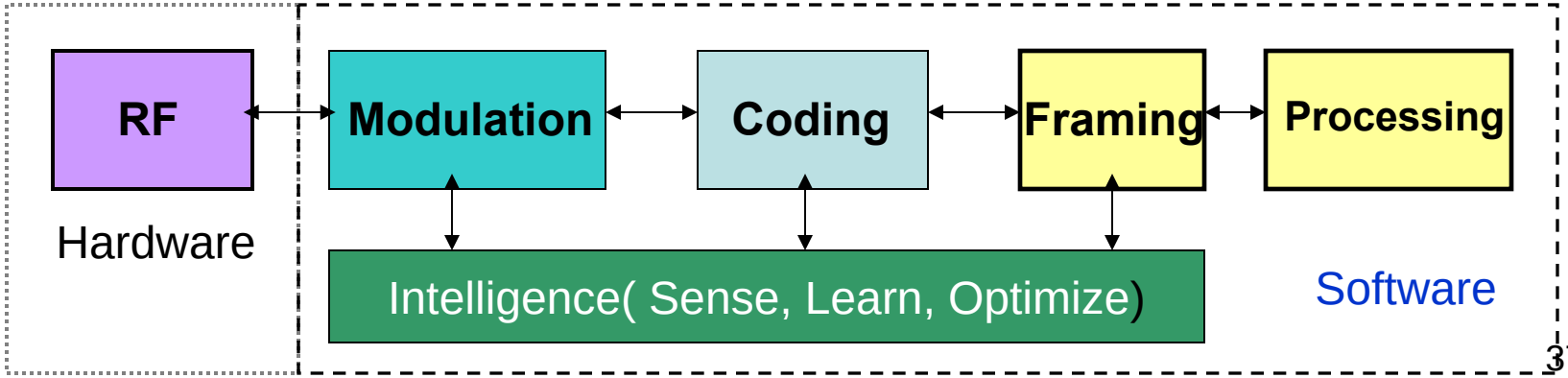
TRADITIONAL RADIO[3]



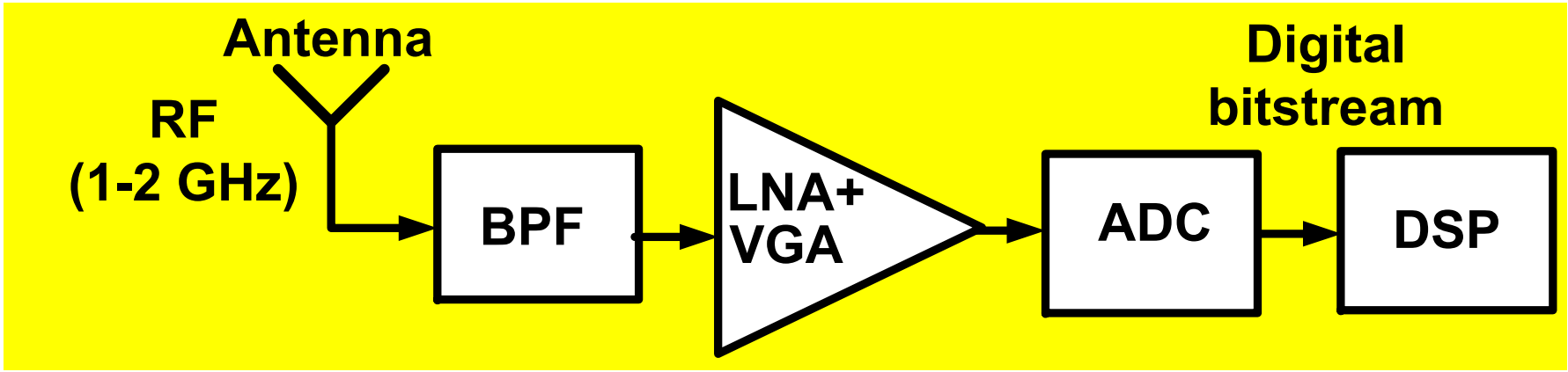
SOFTWARE RADIO



COGNITIVE RADIO

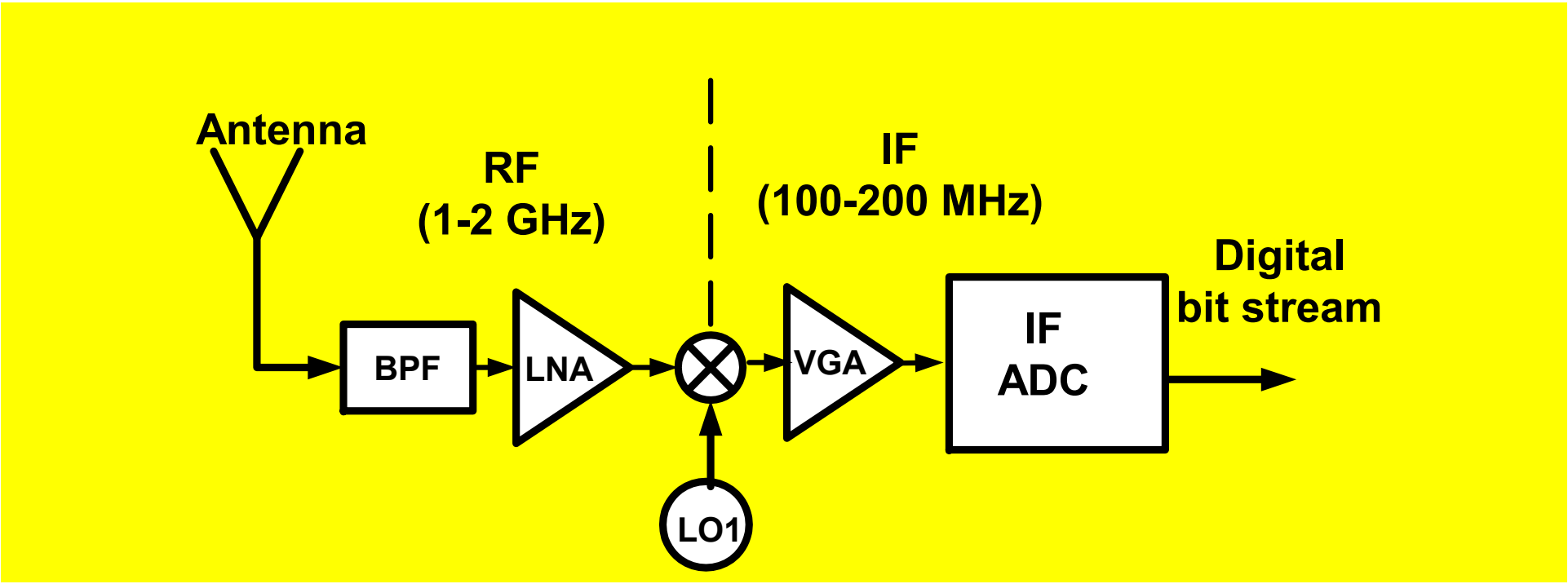


SOFTWARE RADIO



- Idea introduced in 1991 by Joe Mitola
- Direct RF digitization
- Single / multiple channels sets ADC BW
- Reconfiguration by DSP software programs

SOFTWARE DEFINED RADIO



- IF digitization
- No specific standard for IF location
- Reduced DC offset, flicker noise problems

Literature survey

Ref	Type	Fo GHz	Fs GHz	SNR 1 MHz BW	Power (mW)	Tech
Vessal (JSSC 04)	Nyquist (FI)	0 - 0.7	2	48 dB	×3500	SiGe HBT
Kaplan (CICC 03)	CT BP ΣΔ	1.3	4.3	✓62 dB	×6200	InP HBT
Chandrasekaran (CICC 02)	SC LP ΣΔ with mixer	0.9	0.1	25 dB (bad SNDR)	30	0.25µm CMOS
Cherry (TCAS 2000)	CT BP ΣΔ	1	4	51 dB	450	0.5µm SiGe
Gao (VLSI 98)	CT BP ΣΔ	1	4	48 dB	350	0.5µm SiGe
Jayaraman (GaAs 97)	CT BP ΣΔ	0.8	3.2	55 dB	1800	GaAs

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