ECEN 665 (ESS) **Due: November 23, 2009**
Fall 2009

HOMEWORK ASSIGNMENT #6

Problem 1. A VCO using 0.5um CMOS technology and a supply voltage of 3.3V has the following characteristics:

Table HW 6.

VCO Specifications	Performance
Frequency	1.3 GHz
Load Capacitance	200 fF
Phase Noise	≤ -115dBc/Hz at 1MHz
Bias Current	< 1.5 mA
Output Swing (on Single End)	≥ 650 mVpp

(a) Design a single ended and fully differential VCOs with the Passive BP based topology given in the JSSC in 2009 November issue. Provide a table with the simulated specifications. Compare your results with the ones done in HW. 5

(b) Modify your previous FD VCO to obtain a Quadrature Oscillator. Report design procedure and complete simulated results

(c) Propose an arbitrary Phase array using the BP based circuit designed in a).

(d) Compare and discuss results from (a), (b) and (c). Make a table as Table HW 6. to summarize your results. Provide the THD value for all these designs and include it in your comparison table. Discuss your four designs. What are the effects of the linearized negative resistor ? What are the trade-offs ? What are the advantages and disadvantages of the CMOS architecture as opposed to having only NMOS Gm pair ? What is the effect of varying the power supply values?

Problem 2 You are given the task to design a mixer for a broadband system, namely for the ASTC (Advanced Television Systems Committee) standard band of 48 to 860MHz. Just like many other broadband systems the ASTC signal band is crowded with undesirable blockers.

Some of the blockers may be in-band and typically are coming from analog TV (still a problem in some areas), terrestrial digital TV and adjacent ASTC systems, as shown in Fig 1. There are also out of band systems like the GSM 900/1800 and WCDMA standards that present themselves as a problematic issue when considering a multi-standard receiver.

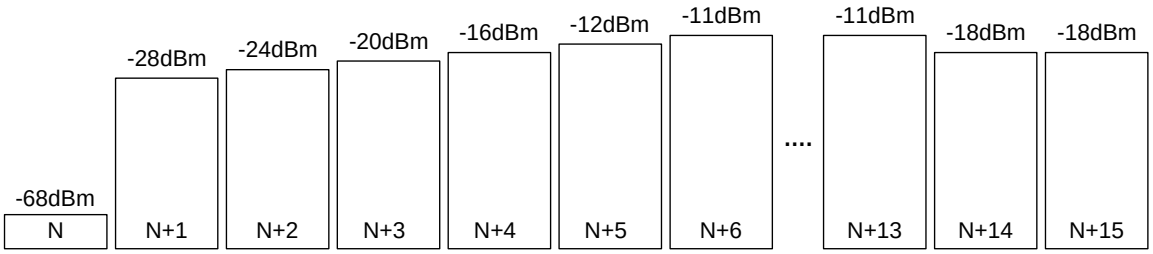

Fig1: ASTC Adjacent channel power levels

All of these unwanted blockers need to be simultaneously processed with the wanted signal. Huge powered blockers put a severe restriction on the linearity of you receiver design. Although the in-band blockers maybe filtered out with a high order (typically larger than 5th order) baseband filters they still remain a problem for the RF front end (LNA and down-conversion Mixer) which needs to process them in a linear fashion.

ASTC
Frequency(MHz): 48-860MHz
Channel Bandwith (MHz): 6/7/8
Modulation: 8VSB
Sensitivity(dBm): -83

Mixer Parameters:
NF (dB): 10
IIP3(dBm): >15
IIP2(dBm): >35
Gain (dB): 15
(All parameters must be met across the whole ASTC band)

Design two different mixers architectures in 0.35um technology. The first design is to be a typical Gilbert Cell architecture with some kind of linearization technique such as source degeneration. The second design is some variation of the Harmonic Rejection Mixer technique [4].

References:

[1] Lerstaveesin, S.; Gupta, M.; Kang, D.; Bang-Sup Song, "A 48–860 MHz CMOS Low-IF Direct-Conversion DTV Tuner," *Solid-State Circuits, IEEE Journal of* , vol.43, no.9, pp.2013-2024, Sept. 2008

[2] A/74 – Receiver Performance Guidelines, with Corrigendum No. 1 and Amendment No. 1 (*http://www.atsc.org/standards/a_74-w-Corr-1-Amend-1.pdf*)

[3] *CMOS RF front-end design for terrestrial and mobile digital television systems*, Xiao, Jianhong, Ph.D., Texas A&M University, 2007,

[4] Ru, Z. and Klumperink, E.A.M. and Wienk, G.J.M. and Nauta, B. (2009) *A Software-Defined Radio Receiver Architecture Robust to Out-of-Band Interference*.: IEEE International Solid-State Circuits Conference, 8-12 February 2009, San Francisco.

The submission of this HW can be done by a team of two if you prefer.