**ECEN 665 (ESS)** **Due: November 11, 2009**
**Fall 2009**

# HOMEWORK ASSIGNMENT #5

Problem 1. A VCO using 0.5um CMOS technology and a supply voltage of 3.3V has the following characteristics:

Table 1.

| VCO Specifications | Performance |
|---|---|
| Frequency | 1.3 GHz |
| Load Capacitance | 200 fF |
| Phase Noise | ≤ -115dBc/Hz at 1MHz |
| Bias Current | < 1.5 mA |
| Output Swing (on Single End) | ≥ 650 mVpp |

(a) Design a VCO with the same topology given in the Laboratory (VCO with NMOS negative Gm pair) to satisfy the above requirements, determine the transconductance Gm associated with the negative resistor (cross coupled NMOS transistors N0 & N1. Provide a table with the simulated specifications.

(b) Modify the VCO to include source degeneration resistors Rs for the transconductance Gm. The new Gm becomes Gm/( 1 + GmRs), increase the power if needed such that the same value of old Gm in (a) is obtained. Assume two cases b.1) GmRs=0.4 and b.2) GmRs=3.4

(c) Design a CMOS VCO (PMOS and NMOS cross-coupled pairs together) with the same specifications given in Table 1.

(d) Compare and discuss results from (a), (b.1), (b.2) and (c). Make a table as Table 1. to summarize your results. Provide the THD value for all these designs and include it in your comparison table. Discuss your four designs. What are the effects of the linearized negative resistor ? What are the trade-offs ? What are the advantages and disadvantages of the CMOS architecture as opposed to having only NMOS Gm pair ? What is the effect of varying the power supply values?

Problem 2 Design a VCO using a ring oscillator topology. Select and justify the Ring Oscillator VCO architecture, your design should meet the same specifications as problem 1 except the ones of phase noise which can be relaxed. Discuss and implement noise reduction techniques for the ring oscillator
Describe your design procedure and provide a table of comparison of results of problems 1 and 2. Discuss in detail those results.