ELEN 665 (ESS)
Fall '09

PROPOSED FINAL PROJECTS

These final projects can be carried out by one student or a team of two students. However it is strongly suggested to have a team of two. Please provide a list of your first three choices by Nov 4 before 4PM. All projects will use 0.35μm unless otherwise specified.

Project 1 Design at the transistor level a UWB LNA for the frequency range 3.1 ~ 4.8GHZ.
Propose a high frequency linearization technique to meet the linearity requirements for the UWB systems. Compare your results with previous reported linearization. The LNA should satisfy the following specifications:

BW: 3.1~4.8GHz
IIP3 > 13dBm
S11<-10dB
S21 > 15dB
NF< 4dB
Minimize Power Consumption.

Use Taylor / Volterra series to do theoretical analysis for the proposed linearization technique.

Project 2. Design a passive RFID to operate in the 13.56 MHZ standard in 0.5um technology. The main objective is to design an enhanced charge pump that can operate with V_T not zero or very small. Propose changes to conventional charge pump circuits to overcome this problem.

Project 3 Design a low phase-noise Ring Oscillator that meet the following specs:
Technology 0.35um, Supply Voltage 2.7V, Oscillating frequency 950 MHz, spot noise -120 [dBc/Hz] @ 100kHz, reference frequency 1ooMHz, reference spur power better than -41dBc, power consumption less than 20mW.
Reference.-
J. Borremans, J. Ryckaert et all, " A Low-Complexity, Low-Phase-Noise, Low Voltage Phase-Aligned Ring Oscillator in 90 nm Digital CMOS", IEEE J. of Solid State Circuits, vol. 44, No.7, pp. 1942-1949, July 2009.

Project 4 Design a Low Power Supply regulation for Ring Oscillator in phase-lock loops. The power supply noise rejection (PSNR) should be better than -25 dB at 3MHz.
Reference.-

A. Araki, S. Gondi, P.K. Hanumolu, " Low-Power Supply Regulation Techniques for Ring Oscillators in Phase-Locked Loops Using a Split-Tuned Architecture"

IEEE J. of Solid State Circuits, vol. 44, No.8, pp. 2169-2181, August 2009.

Project 5
Design a receiver based on the Super Regenerative architecture for a wireless link of 5 mts. The receiver should work on the 27.12 MHz ISM band. The SRR should operate in linear mode.. A fully integrated solution may be possible but you may use external passive devices if necessary. Please describe:

- channel bandwidth
- modulation scheme
- minimum detectable signal level
- frequency selectivity
- intended quench signal waveform

Reference:
[1] Moncunill-Geniz, F.X.; Pala-Schonwalder, P.; Mas-Casals, O., "A generic approach to the theory of superregenerative reception," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.52, no.1, pp. 54-70, Jan. 2005

[2] FCC ISM Band
Regulations http://www.access.gpo.gov/nara/cfr/waisidx_07/47cfr18_07.html

Project 6 Design at the transistor level a 433 MHz RFID tag complying with ISO 18000-7 standard also you will need to study the standard and design the system and building block specifications of the transmitter and receiver

Project 7. Design a RMS power detector satisfying the following specs:

Input Capacitance $\leq$ [10fF, 50fF] [off, on]
Frequency range between 900 MHz and 5 GHz.
Small Area
Moderate Power
Variable dynamic range of at least 40dB

Prob. 8. Design a combined LNA-Mixer in 0.5µm CMOS. The specs to satisfy are:

V_{DD} = 3.3V
Voltage Gain $\leq$ 5 dB
NF $\leq$ 6 dBm
*$|V_{LO}|$ $\geq$ 210mV

The key goal is to minimize power while satisfying specs. Discuss the trade-offs between NF, Power and IIP3. Compare your results with LNA + Mixer and merged LNA and Mixer reported in the literature.

Project 9 Design a 433 Mhz MICS receiver (LNA, Mixer, Channel selection filter, and VCO) for medical applications and wireless sensor applications for the following specs. :

A. Data rate of 20Kbps
B. FSK is used with modulation index of 25m%
C. C. Channel spacing 500KHz
D. D. Adjacent Channel rejection of 50db
E. Sensitivity of -110dBm @0.1% BER.
F. Power consumption less than 1mW

Provide the system level design approach and the specs for each individual building block, while minimizing power consumption. You can select one receiver topology and the other must be a Super-Regenerative structure. Make comparison of both topologist

Final Written Report (December 7, 2009). This final word document must include:

1. Title
2. An abstract
3. Introduction
4. Background and a comparative table of previous results
5. Proposed Solution
    - Conceptual idea of the solution
    - Circuit Design and explanation
    - Design Procedure, how to determine the (W/L)'s, bias.
    - The temperature, noise and process variation effects
6. A Comparative Table between Hand calculation and Simulation
7. Discussion of results with other reported results and suggested improvements.
8. Layout of the Circuit
9. References, a complete list of reference must be included

Oral Presentations in PowerPoint Form, November 30 and December 2, 2009