SIMULATION AND ANALYSIS OF NOISE IN SWITCHED CAPACITOR AMPLIFIER CIRCUITS

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Abstract— Noise is an important factor in switched capacitor amplifiers. There is not a good understanding of device noise in switched capacitor circuits, the basic technique is to use large transistors and capacitance values such that kT/C noise dominates. Besides kT/C noise, however, both device or transistor thermal noise and l/f noise are contributing factors. Techniques to simulate noise in switched capacitor circuits have only recently become available. These techniques have been applied here to a switched capacitor amplifier as is commonly employed in many analog CMOS circuits. A good comparison is obtained between simulations and analytical techniques. It is apparent that device thermal and l/f noise is an important consideration in switched capacitor circuits.

I. INTRODUCTION

Noise is an important factor in switched capacitor amplifiers. There is no good understanding of device noise in switched capacitor circuits, the basic technique is to use large area transistors and capacitance values such that kT/C noise dominates. The level of understanding is best demonstrated by the graduate level textbook which compares device noise to offset voltages but provides no analysis.[1] Besides kT/C, however, noise both device or transistor thermal noise and l/f noise are contributing factors.

Techniques to simulate noise in switched capacitor circuits have only recently become available. There are now good techniques for simulating noise and phase noise in switching circuits provided that the noise sources themselves are truly stationary in nature. The theory behind the various methods of noise simulation in SpectreRF is well understood and documented in SpectreRF technical application notes and material from Cadence. These techniques have been applied here to a switched capacitor amplifier as is commonly employed in many analog CMOS circuits.

II. DEVICE MODELS

SpectreRF allows the user to specify the noise model used in simulating noise behavior of a circuit using the noimod flag. There are four possible values that the *noimod* flag can take (1,2,3 or 4) and based on this value, different noise models are used in simulating the flicker and thermal noise in a circuit [2]. In our simulations the noise model flag, *noimod=1*, for flicker and channel thermal noise was used to simulate and analyze the noise behavior of the switched capacitor amplifier circuit. The model used by SpectreRF to calculate flicker noise is given as [3],

$$Flicker\ Noise = \frac{K_f I_{ds}^{A_f}}{C_{ox} L_{eff}^2 f^{E_f}}\ \mathrm{A^2/Hz} \tag{1}$$

and thermal noise is calculated using the model [3],

$$Thermal\ Noise = \overline{i_D^2} = \frac{8kT}{3}(g_m + g_{ds} + g_{mb})\ \mathrm{A^2/Hz} \tag{2}$$

In Eqn. 1, the parameter K_f is known as the flicker noise coefficient whose value for 0.35µm process is typically 2.4×10^{-28}. When using *noimod=1* in SpectreRF, K_f was specified to calculate output referred 1/f and thermal noise of the switched capacitor amplifier circuit and the effect of channel thermal noise alone was calculated by setting the value of K_f as zero.

Fig. 1 shows the noise response of a single 0.35 micron technology PMOS transistor with width 6µm, channel length 0.5µm, and drain current 3.6µA in a common source configuration with a 200kΩ resistive load at the output. The flicker noise component is modeled by the double sided power spectral density function [2], and the channel thermal noise, or Johnson-Nyquist noise, having a uniform spectral density of $e^2_{J\text{-}N}$. The plot gives the output referred noise spectral density in V^2/Hz and is used to calculate e^2_F and $e^2_{J\text{-}N}$. The output noise due to the 1/f component decreases with frequency and flattens out at the 1/f noise corner, 1.0 MHz in Fig. 1. The output noise in V^2/Hz at frequency of 1Hz gives the value of e^2_F (Eqn. 3) and, the output noise in V^2/Hz where the curve flattens gives the value of $e^2_{J\text{-}N}$. From Fig. 1, we obtain the values $e^2_F = 10^{-8}$ and $e^2_{J\text{-}N} = 2.5\times 10^{-14}$ for the PMOS transistor with a gain of 10 ($gm = 50 \times 10^{-6}$S and R_L = 200kΩ).

$$e_n^2(f) = \frac{e_F^2}{|f|} \tag{3}$$

The mean square transistor drain current noise, i_n^2, can be obtained by dividing the mean square noise voltage in Fig. 1 by the square of the load resistance.

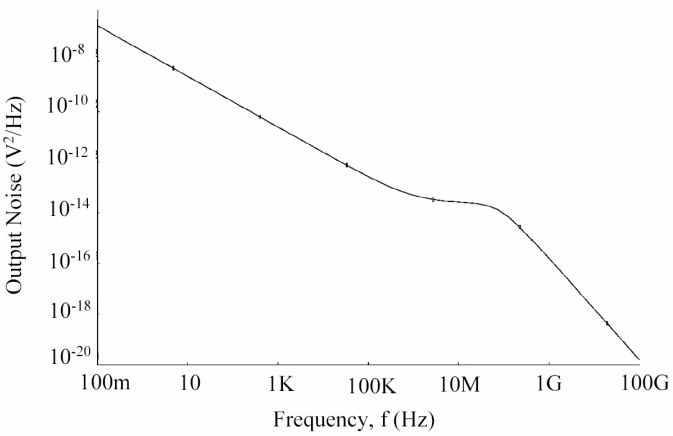

Fig. 1. Noise characteristics of a PMOS transistor

III. Switched Capacitor Circuit

The circuit used in our simulations is given in Fig. 2. It is a conventional two stage CMOS differential amplifier with PMOS input devices designed in the TSMC 0.35 micron process and design rules.

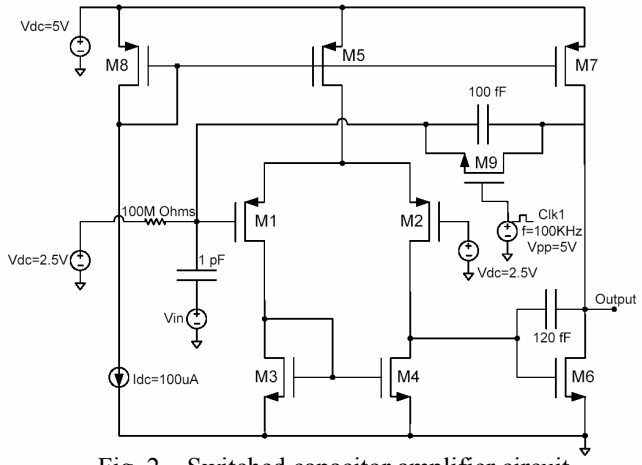

Fig. 2. Switched capacitor amplifier circuit

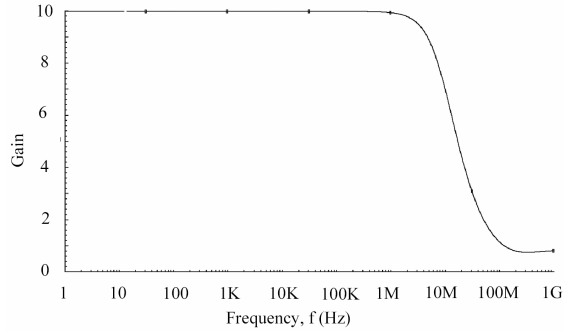

Fig. 3. AC response of switched capacitor amplifier

The transistor channel lengths are larger than minimum dimensions to reduce the device noise, and the widths of the input devices are also made larger than minimum dimensions to reduce noise. Fig. 3 gives the AC response of the circuit without switching with a voltage gain of 10 and a bandwidth of 10MHz. Fig. 4 shows the transient response at 100 kHz and the switching frequency is chosen to be 100kHz.

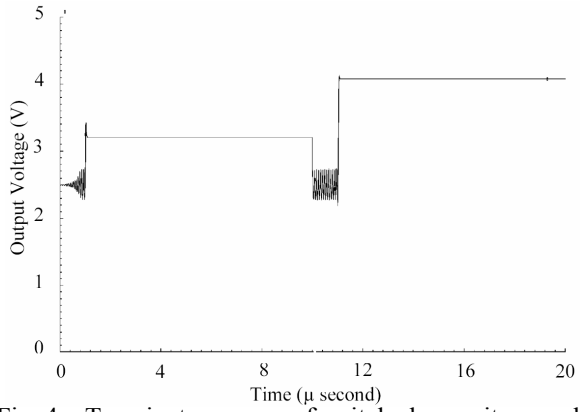

Fig. 4. Transient response of switched capacitor amplifier

IV. Simulation

Traditional circuit simulators such as HSPICE or SWITCAP have limitations in switched bias and when used in noise analysis of switched capacitor circuits. HSPICE, although capable of accounting for second order effects (using transistor-level description) cannot accurately compute transfer and noise characteristics of a switched capacitor amplifier circuit. SWITCAP simulators on the other hand are more dependable in computing noise and transfer characteristics but use high-level behavioral description of circuits and hence do not account for second order effects [4]. SpectreRF circuit simulator provides an excellent solution to directly measure noise and transfer characteristics of circuits using a transistor-level description [5]. SpectreRF uses the Periodic Steady State analysis (PSS) to first compute the periodic operating point of the circuit. The periodic operating point obtained using PSS analysis can then be used to study the frequency response of the circuit by running the Periodic AC analysis (PAC). Finally, the noise behavior of the circuit is analyzed using Periodic Noise analysis (Pnoise) which gives the output referred noise of the circuit.

The noise analysis setup is done using the 'Analog Environment' window from the 'Tools' menu. Using the setup menu the model libraries to be used in circuit simulation is specified. In all our simulations TSMC 0.35μm process technology models were used. The noise analysis options are set from the 'Choose Analysis' menu in analog environment window. The buttons *pss*, *pac* and *pnoise* are selected to specify the simulations parameters to be used in the noise analysis of the circuit. For *pss* analysis, the fundamental tones list box that gives all top-level tones in the circuit is auto filled from the 'Frequency name for 1/period' column entry in the Component Description Format of the clock signal source, clk1. For the clock source, *clk1*, V1 is set to gnd (0V) and V2 set to V_{DD} (+3.3V). The beat period is calculated from the reciprocal of the beat frequency from the fundamental tones list box by checking the *auto calculate* button. Since we are interested only in the output at the clock frequency, the number of harmonics is set to '0'. The *errpreset* option is chosen to be *conservative* to give higher accuracy in the

circuit simulations although it increases simulation time considerably. To improve convergence an additional stabilization time of 1.5 ms for circuit settling was specified using the *tstab* parameter. This results in the transient analysis being performed at least 1.5ms before the PSS analysis attempts to calculate the steady state operation point. To study the frequency response of the circuit a logarithmic type sweep of frequency in the range of 1Hz –set such that *maxacfreq* ≥ $f_{stop} + f_{clk} \times maxsideband$ where f_{clk} is the clock frequency is used.[4] or, by running a pss analysis without specifying *maxacfreq* and then, using the suggested value for maximum ac frequency given by the warning statement in the noise analysis report for subsequent simulations. In our simulations a maximum ac frequency of 15 MHz was used. A higher value for *maxacfreq* gives better accuracy but also makes the simulations considerably slower.

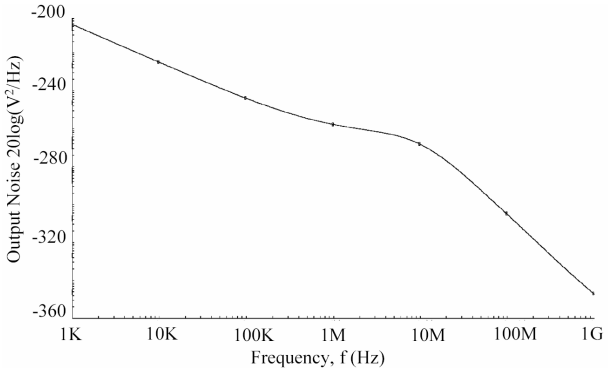

Fig. 5. Output referred noise at output node without switching

As the first step, an AC analysis of the switched capacitor amplifier circuit is performed in the frequency range to be used in the periodic steady state analysis of the circuit. The AC analysis is done to measure the -3dB corner frequency (ω_c) of the amplifier. The input voltage source is specified as Vin =1mV AC at the input. The frequency response of the circuit is then obtained by plotting the AC magnitude of the output signal at the output node. From Fig. 3, the corner frequency is given by the frequency at which the output drops by 3dB and thus f_c = 6 MHz, ω_c is then given by $2\pi f_c$ and is calculated to be 38 Mrad/sec.

Fig. 4 gives the transient response of the circuit at the output node. The output referred 1/f noise and white at the output node is shown in Fig. 5. Note that the plot gives the distribution of 20log(V^2 /Hz) in the frequency range of 1KHz – 100MHz. This plot is obtained by specifying the output node as the positive output node and the negative output node as ground in the *pnoise* analysis output setup.

Fig. 6 gives the simulated noise with switching at the output node for T = 10µs with both white and l/f noise. The value of output referred 1/f noise and white noise is calculated by integrating the area under the curve up to the corner frequency and multiplying by, π/2, and is calculated as 600µV. The effective bandwidth if a uniform spectral density is assumed is, $\pi f_c /2$.

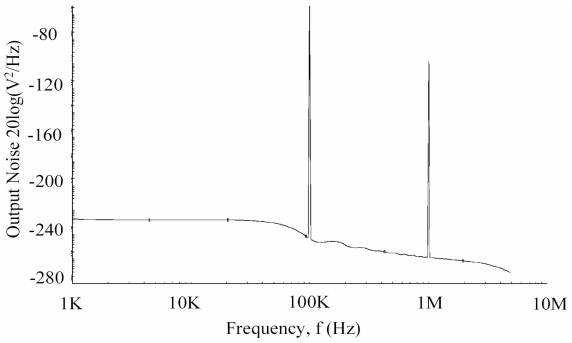

Fig. 6(a). Output referred noise at output node with switching and 1/f and white noise on log scale

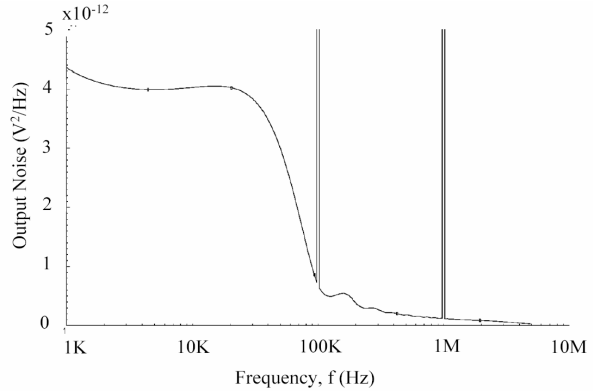

Fig. 6(b). Output referred noise at output node with switching and 1/f and white noise on linear scale

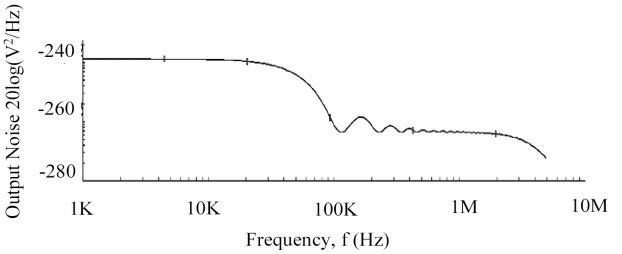

Fig. 7(a). Output referred noise at output node with switching and white noise on log scale

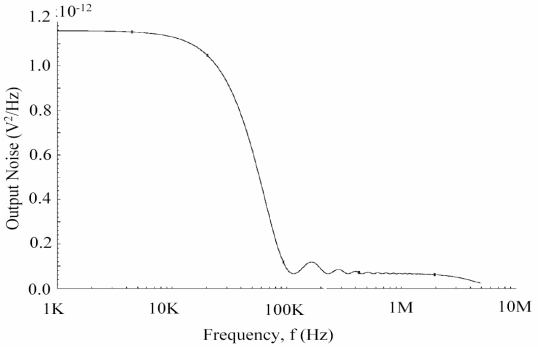

Fig. 7(b). Output referred noise at output node with switching and white noise on linear scale

Fig. 7 gives the simulated noise at the output node with switching for T = 10µs with white noise only. The value of output referred white noise is calculated by integrating the area under the curve up to the corner frequency and multiplying by, π/2, and is calculated as 280µV.

V. Analytical Model

The kT/C reset noise on the input capacitor, Cin, is obtained by integration from the switching frequency up to the bandwidth of the thermal noise produced by the switching transistor as in the conventional derivation of kT/C noise. The effective bandwidth if an uniform spectral density is assumed is, $\pi f_c/2$. Since the bandwidth is much higher than the switching frequency this just produces the classical result, kT/C.[1] When referred to the output this noise is multiplied by the closed loop gain of the amplifier to yield $(kT/Cin)(Cin/Cc)^2$ V^2 or 632 μV at the output.

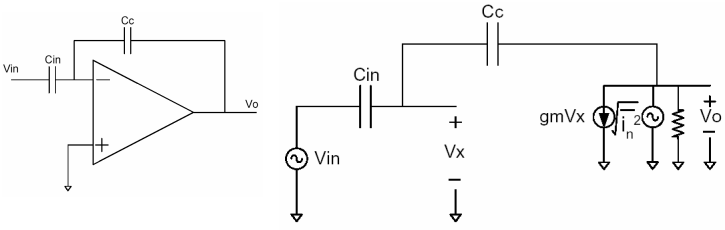

Fig. 8(a). Switched capacitor amplifier used for analytical estimates

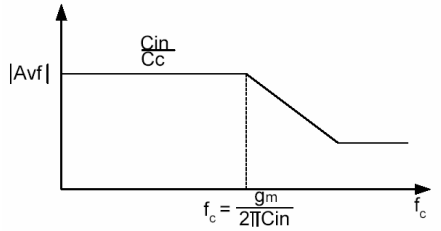

Fig. 8(b). Transfer function of Switched capacitor amplifier used for analytical estimates

The calculations for the device noise sources for T = 10μs or switching frequency of 100kHz are given below as an illustration. A generic CMOS amplifier is used in a negative feedback configuration as shown in Fig. 8(a) with Cin = 1pF and Cc=0.1pF and that has a transfer function as shown in Fig. 8(b). The bandwidth after feedback is $gm/(2\pi Cin)$, in order to have the same corner frequency as the amplifier used for the simulations which also has a gain of ten the transconductance of the generic single stage amplifier has to be about 50μS. This white noise is integrated over the range of frequencies from the switching frequency up to the corner frequency, f_c. However, since the corner frequency is much higher than the switching frequency only the corner frequency, f_c, is important. The effective bandwidth using the "brick wall" approximation [1] is, $(f_c\ \pi)/2$. This results in a thermal noise referred to the input of $(i_n^2/4gm^2)$ and when referred to the output of $(i_n^2/4gm^2)(Cin/Cc)^2$ where $i_n^2 = 8\ kT\ gm/3$ or 5.3×10^{-25} A^2/Hz. Interestingly enough the device thermal noise can also be written as $(2/3)(kT/Cin)(Cin/Cc)^2$ which is just 2/3 the value of the kT/Cin noise and is independent of the detailed characteristics of the amplifier.

The white or Johnson-Nyquist component is then:

$$V^2 = (i_n^2/4gm^2)(Cin/Cc)^2\ (gm/Cin) \quad (4)$$

$$V = 500\ \mu V \quad (5)$$

The l/f noise component can be found by integrating from the switching frequency up to $(\pi f_c)/2$ where f_c is the corner frequency of the amplifier. The magnitude of the l/f noise is taken appropriate to that for a transistor with a tranconductance of 50 μS, or about the same as our single transistor in Fig.1, $e^2_F = 10^{-8}$ V^2/Hz or 2.5×10^{-14} A^2/Hz. The 1/f component is then:

$$V^2 = (i_n^2/gm^2)(Cin/Cc)^2 ln(\pi f_c\ T/2) \quad (6)$$

$$V = 225\ \mu V \quad (7)$$

The analytical estimate for the combination of 1/f component and white noise is then, V = 550 μV.

Values obtained from the simulation using SpectreRF for a switching frequency of 100kHz are:

Johnson-Nyquist component:

$$V = 280\ \mu V \quad (8)$$

1/f component and white noise:

$$V = 600\ \mu V \quad (9)$$

VI. Conclusions

A good comparison is obtained between simulations and analytical techniques It is apparent that device thermal noise and l/f noise is significant in contributing to switched capacitor amplifier noise. 1/f noise can be reduced by using large area devices but the analytical estimate for thermal noise is independent of the detailed characteristics of the amplifier and always comparable to the kT/C noise.

The ability to simulate noise in switched capacitor circuits is an important design tool that will enable large scale integrated switched capacitor designs to be modeled in detail.

References

[1] D. A. Johns and K. Martin, *"Analog integrated circuit design,"* John Wiley & Sons, N.Y., 1997, p. 429.

[2] Design Systems Inc., "*Affirma RF Simulator (Spectre RF) User Guide*", v. 4.4.5, 1999

[3] K. Kundert, "Simulating Switched-Capacitor Filters with SpectreRF," v.4a, 13 Nov. 2003, http://www.designers-guide.com/Analysis/sc-filters.pdf