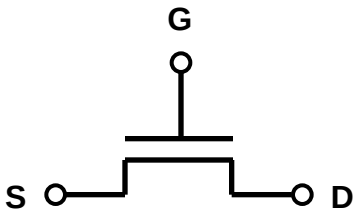
ECEN 622 (ESS)
Fall 2011

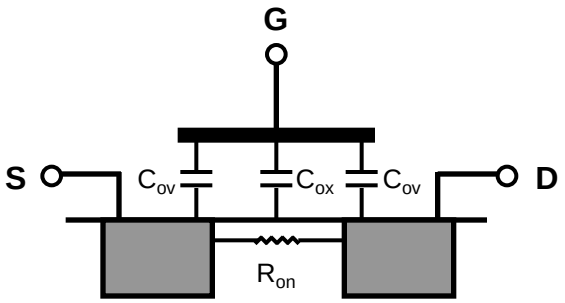
Practical Issues Designing Switched-Capacitor Circuit

Material partially prepared by

Sang Wook Park and Shouli Yan

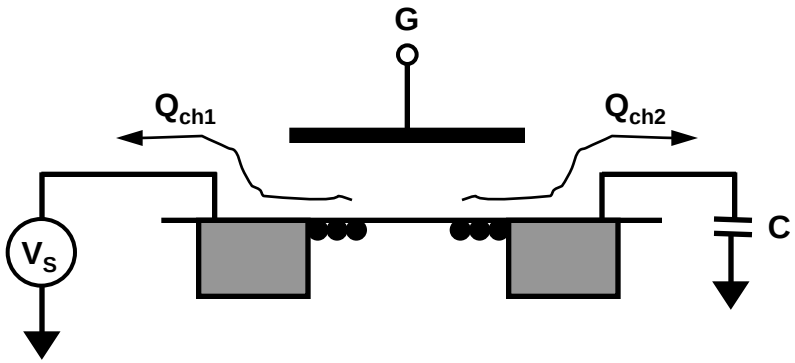
❑ MOS switch





- Excellent R_{off}
- Non-idea Effect
  - ✓ Charge injection, Clock feed-through
  - ✓ Finite and nonlinear R_{on}

❑ Charge Injection



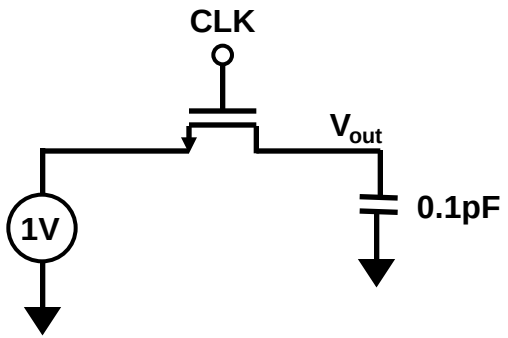
o During TR. is turned on, Q_{ch} is formed at channel surface

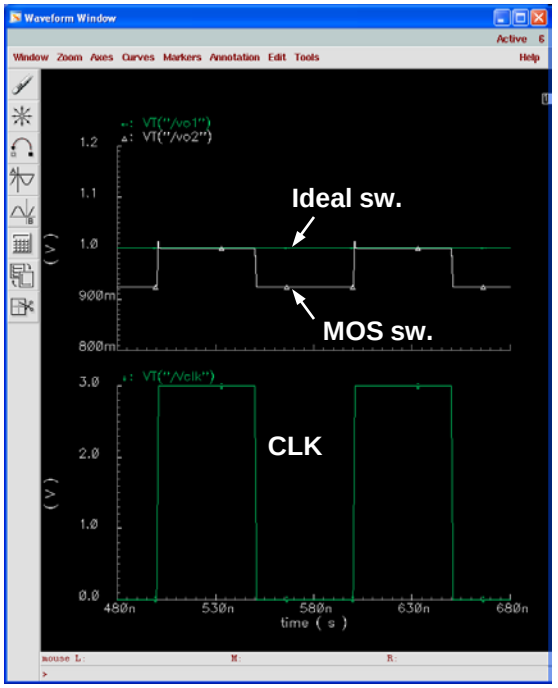
- ✓ $Q_{ch} = WLC_{OX}(V_{GS} - V_{th})$
- ✓ When TR. is off, Q_{ch1} is absorbed by Vs, but Q_{ch2} is injected to C

o Charge injected through overlap capacitor

o Appeared as an offset voltage error on C

❑ Charge Injection Effect

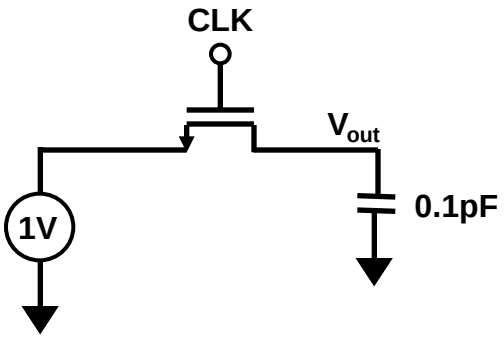


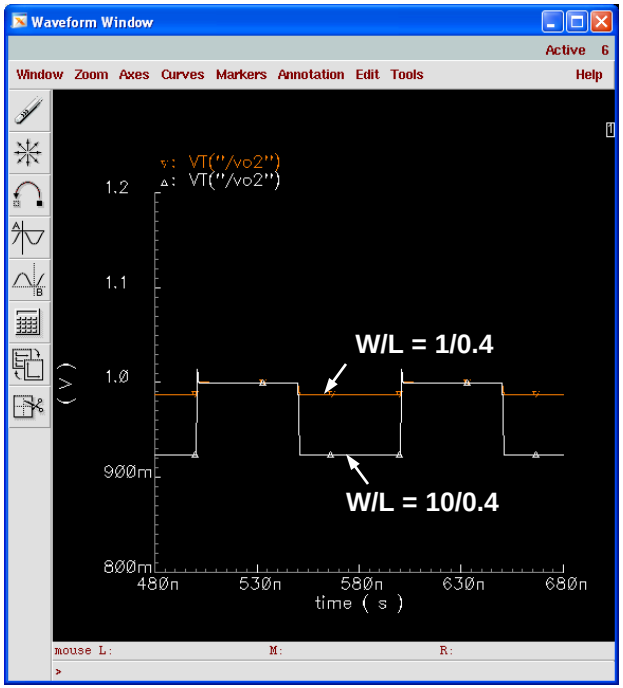


o When clock changes from high to low, Q_{ch2} is injected to C

o Compared to ideal sw., MOS sw. creates voltage error on V_{out}

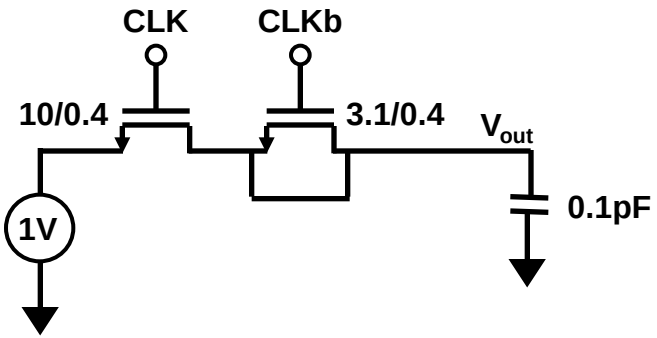
❑ Decrease Charge Injection Effect (1)

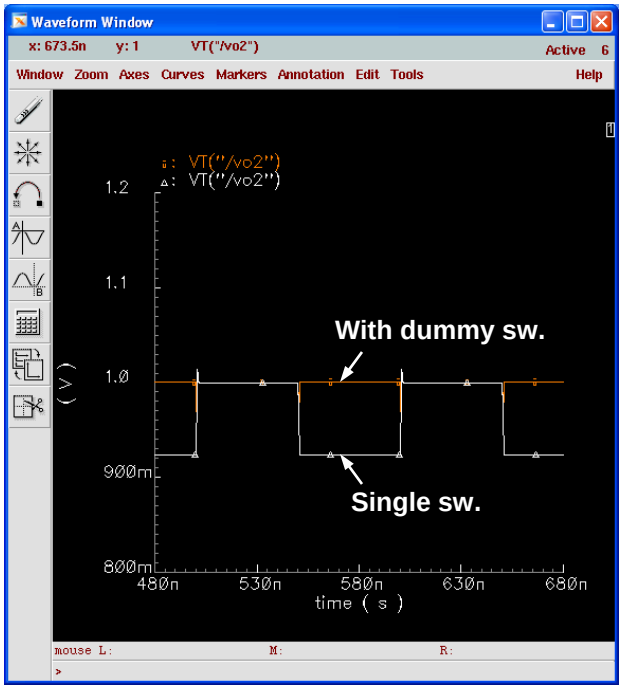




- Decrease the effect of Q_{ch}
- Use either bigger C or small TR. (small ratio of C_{ox}/C)
- Increased R_{on}

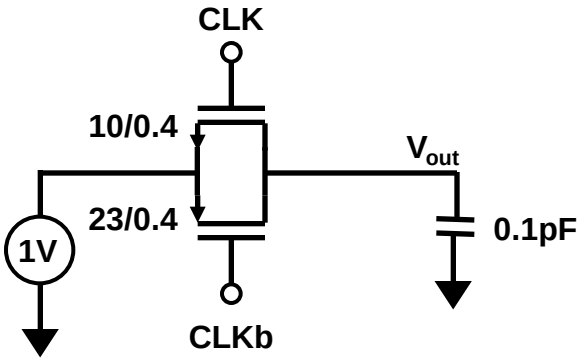
❑ Decrease Charge Injection Effect (2)

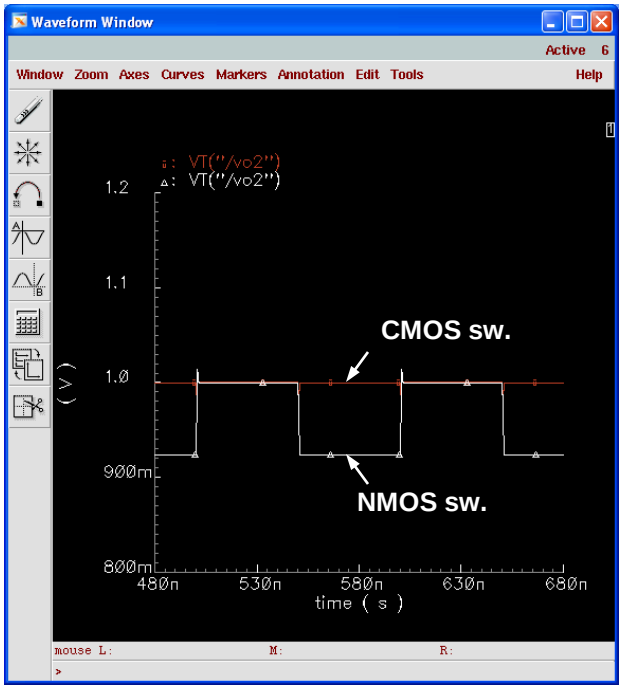




- o Use dummy switch which provides opposite charge
- o Adjust size of dummy sw. for exact canceling
- o Needs opposite clock

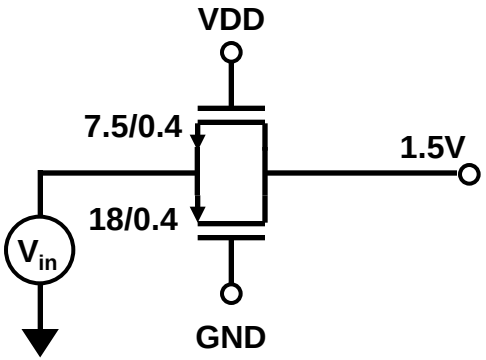
❑ Decrease Charge Injection Effect (3)

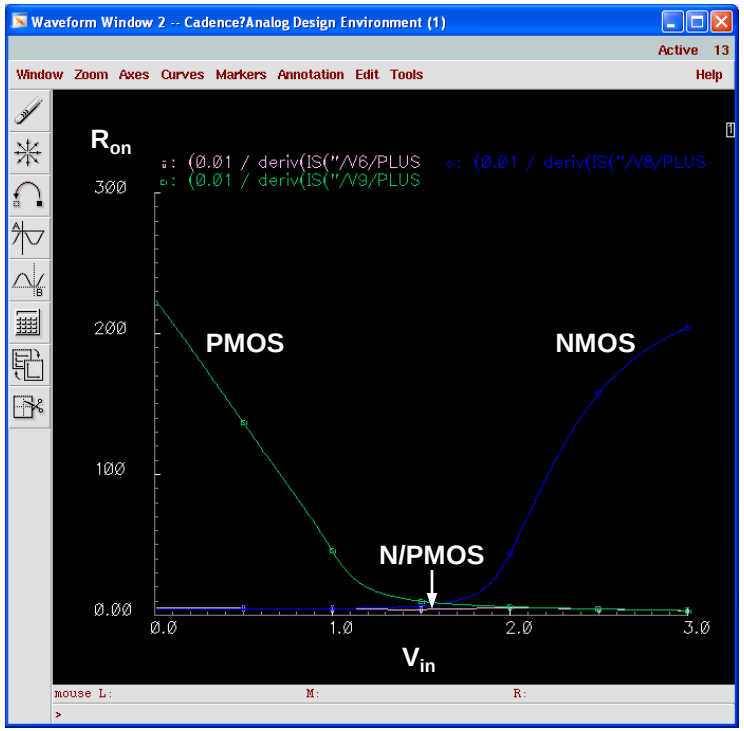




- o Use N/PMOS complementary switch
- o Both Q_{ch} cancel out due to their opposite polarity
- o Needs opposite clock, increased parasitic capacitance

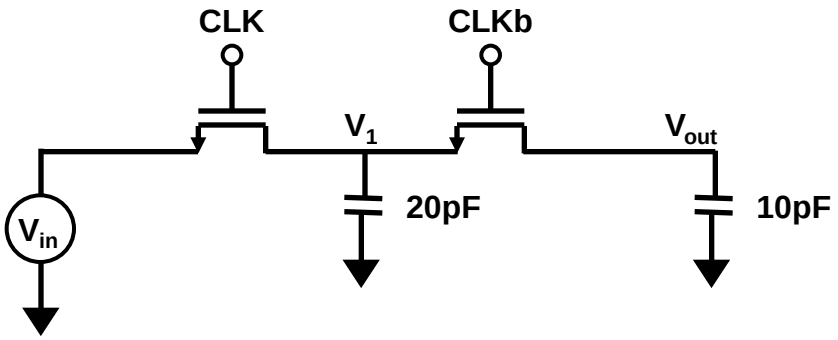
❑ Nonlinear R_{on}





- R_{on} varies with signal amplitude
- CMOS sw. can adopt large signal
- Needs opposite clock, increased parasitic capacitance

❑ Slow Settling due to high R_{on}



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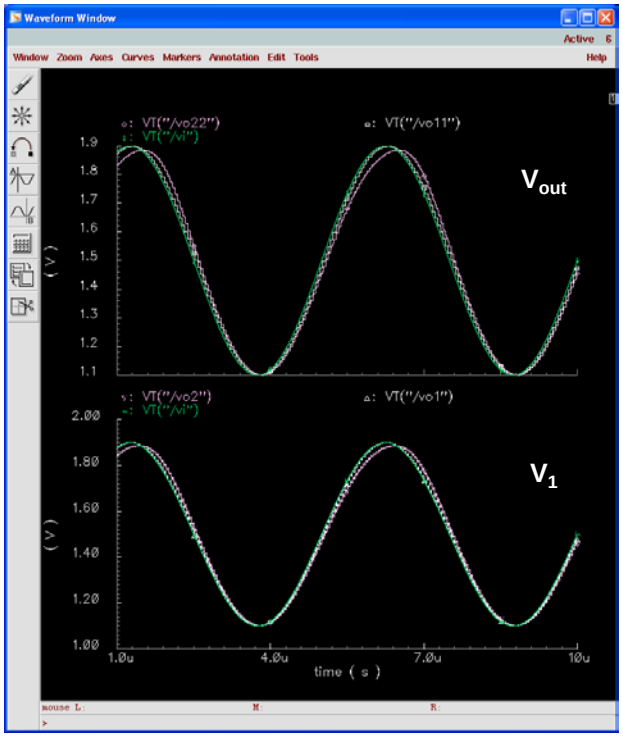
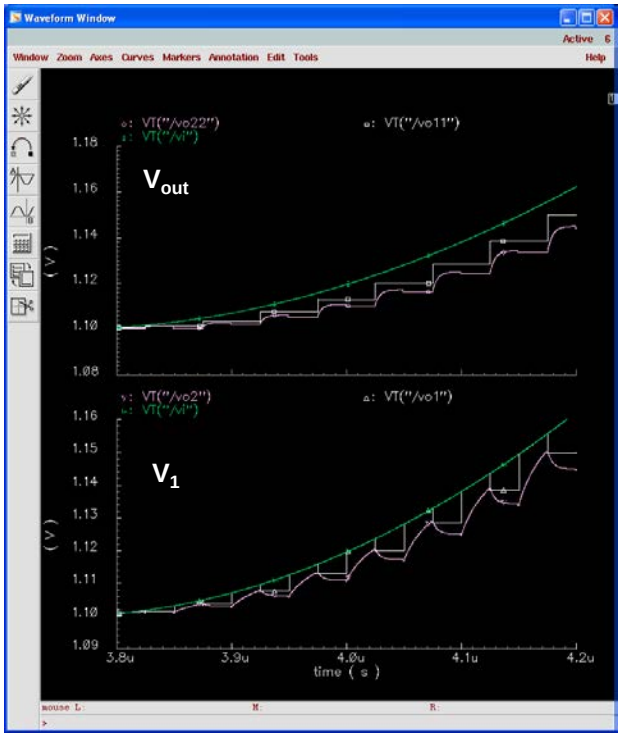
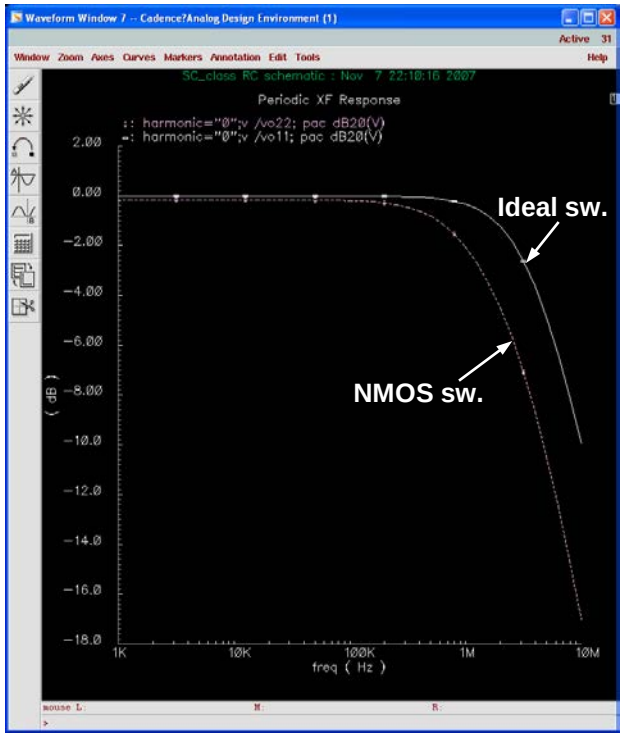
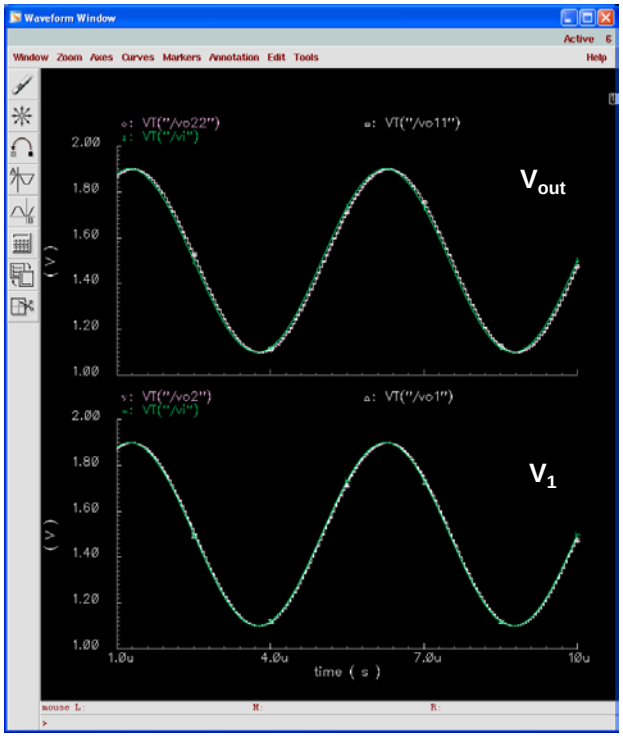


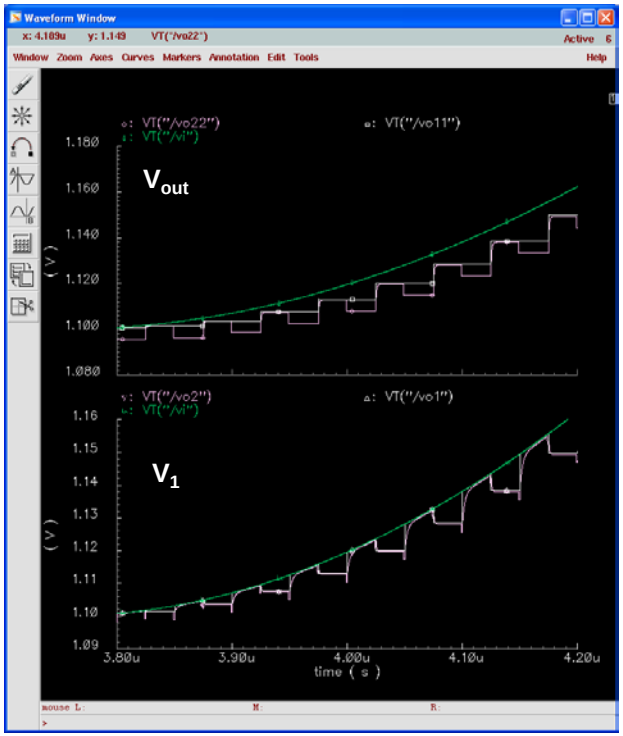


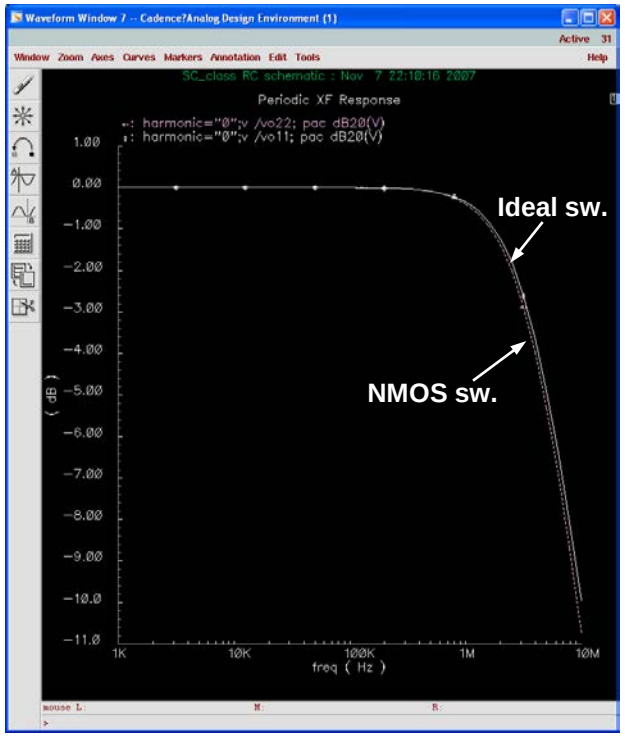


- Small NMOS sw. (5/0.4)
- With high $R_{on,}$ output is not settled
- In case of large signal input, N/PMOS sw. should be used

❑ Slow Settling due to high R_{on}

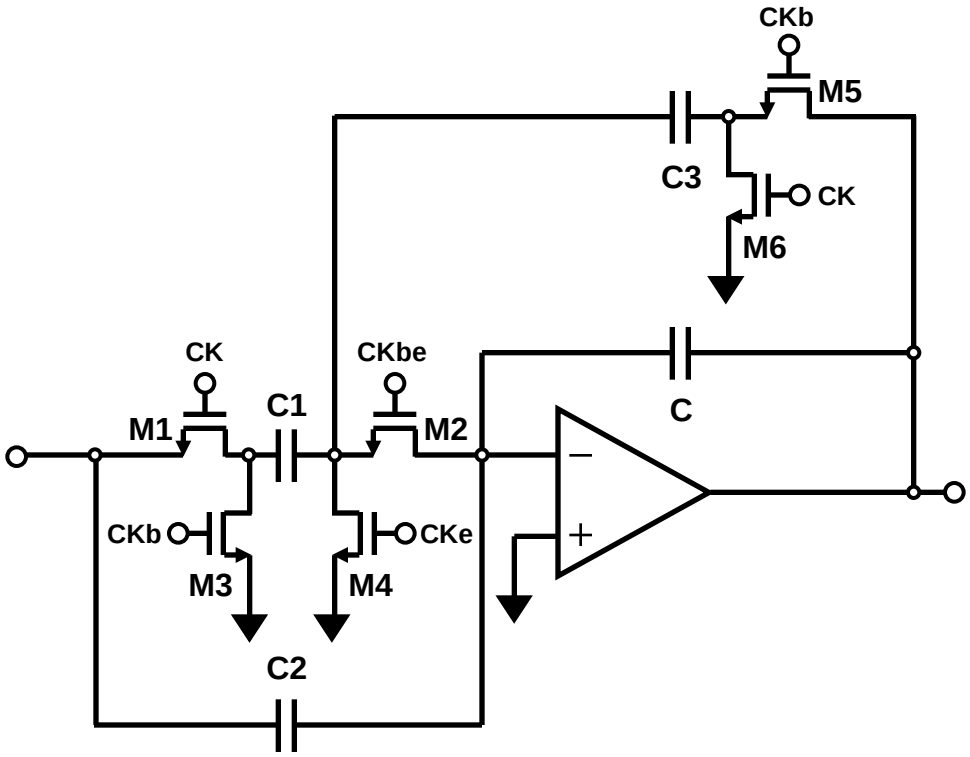


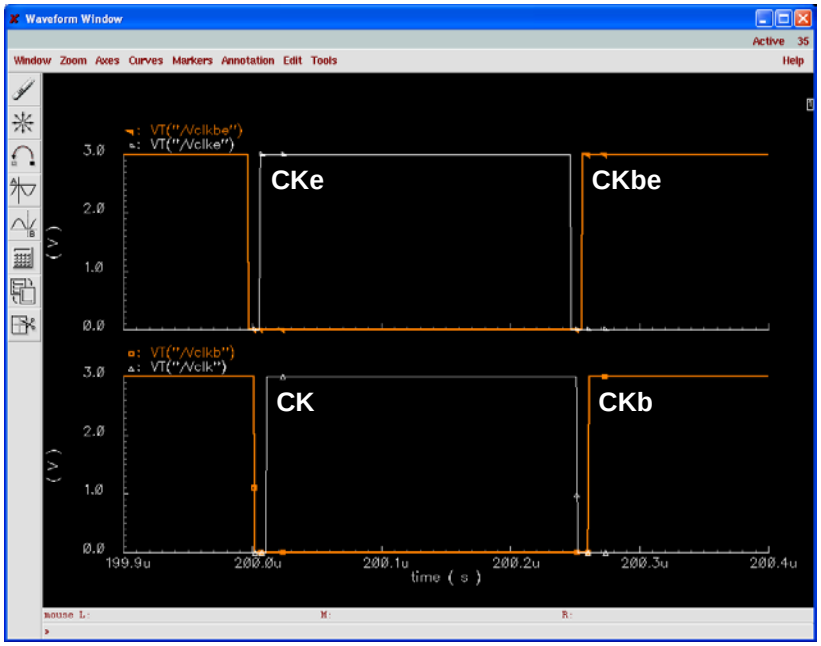




- Large NMOS sw. (20/0.4)
- Low R_{on} makes output settled fast
- Close to ideal sw.

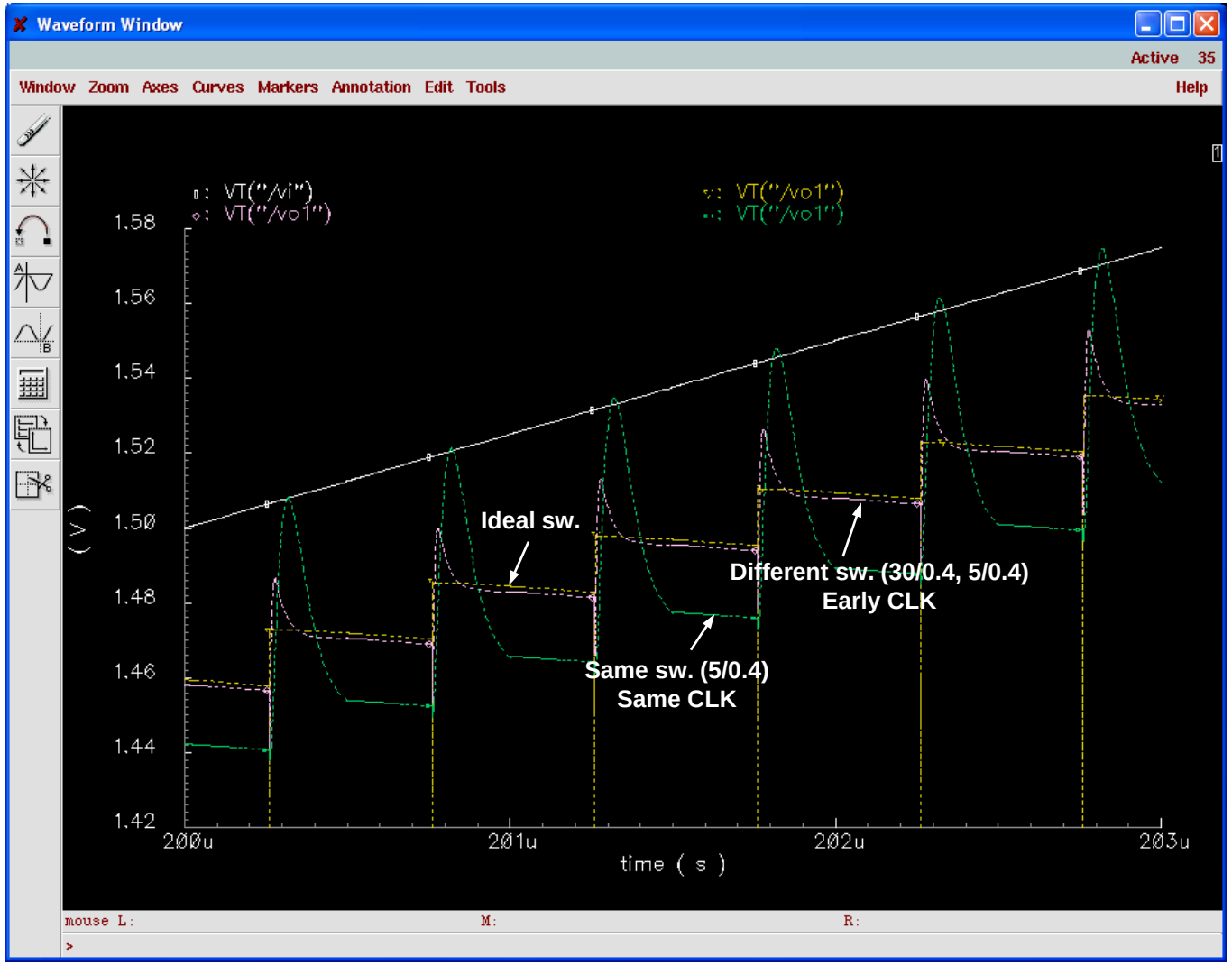
❑ Switch and Clock Arrangement



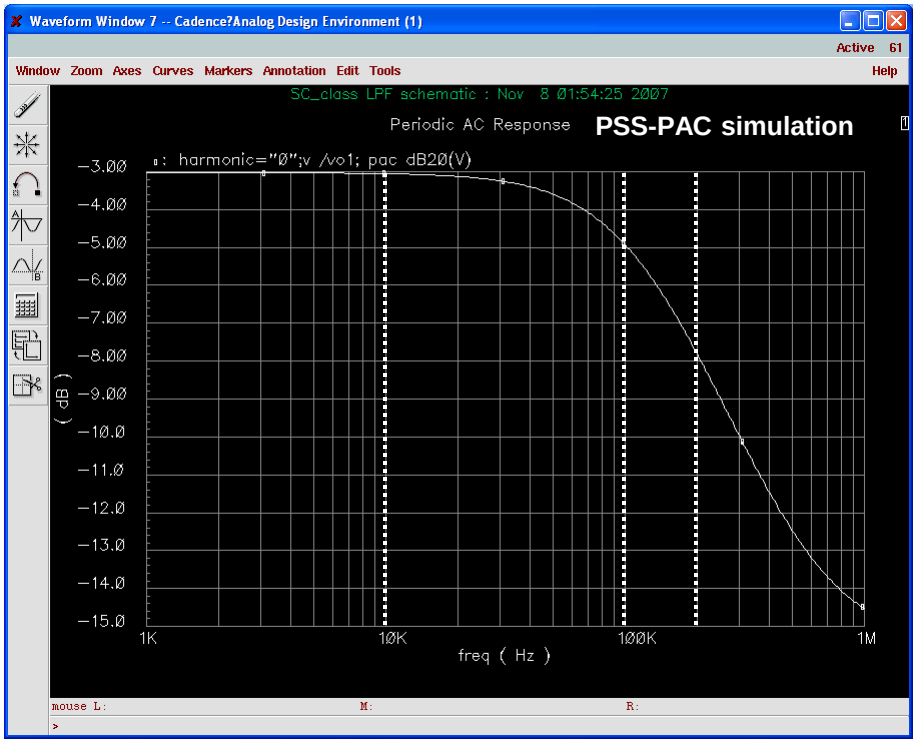


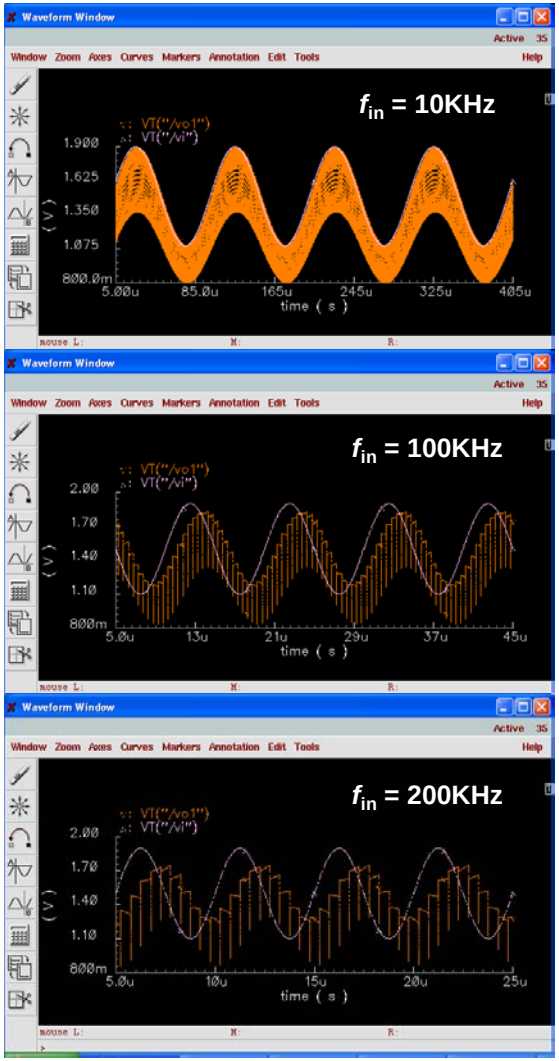
- o M2, M4 : small sw., Others : large sw.
- o M2, M4 turn off earlier : minimize charge injection effect
- o Charge injection
  - ✓ M2, M4 (M3, M6) : Signal independent
  - ✓ Others : Signal dependent

❑ Switch and Clock Arrangement



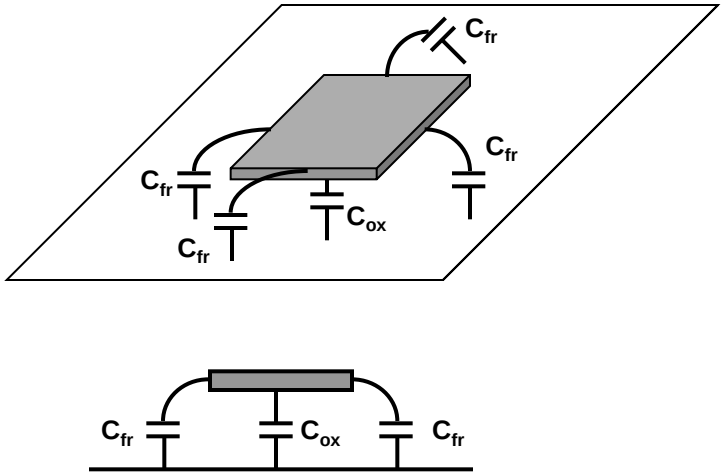
❑ PSS vs. Transient Simulation

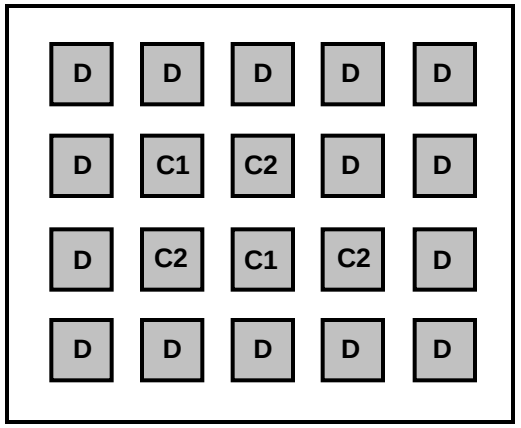




- PSS simulation is used to check the frequency response for Switched-capacitor circuit
- Should be compared with transient simulation

❑ Capacitor Layout

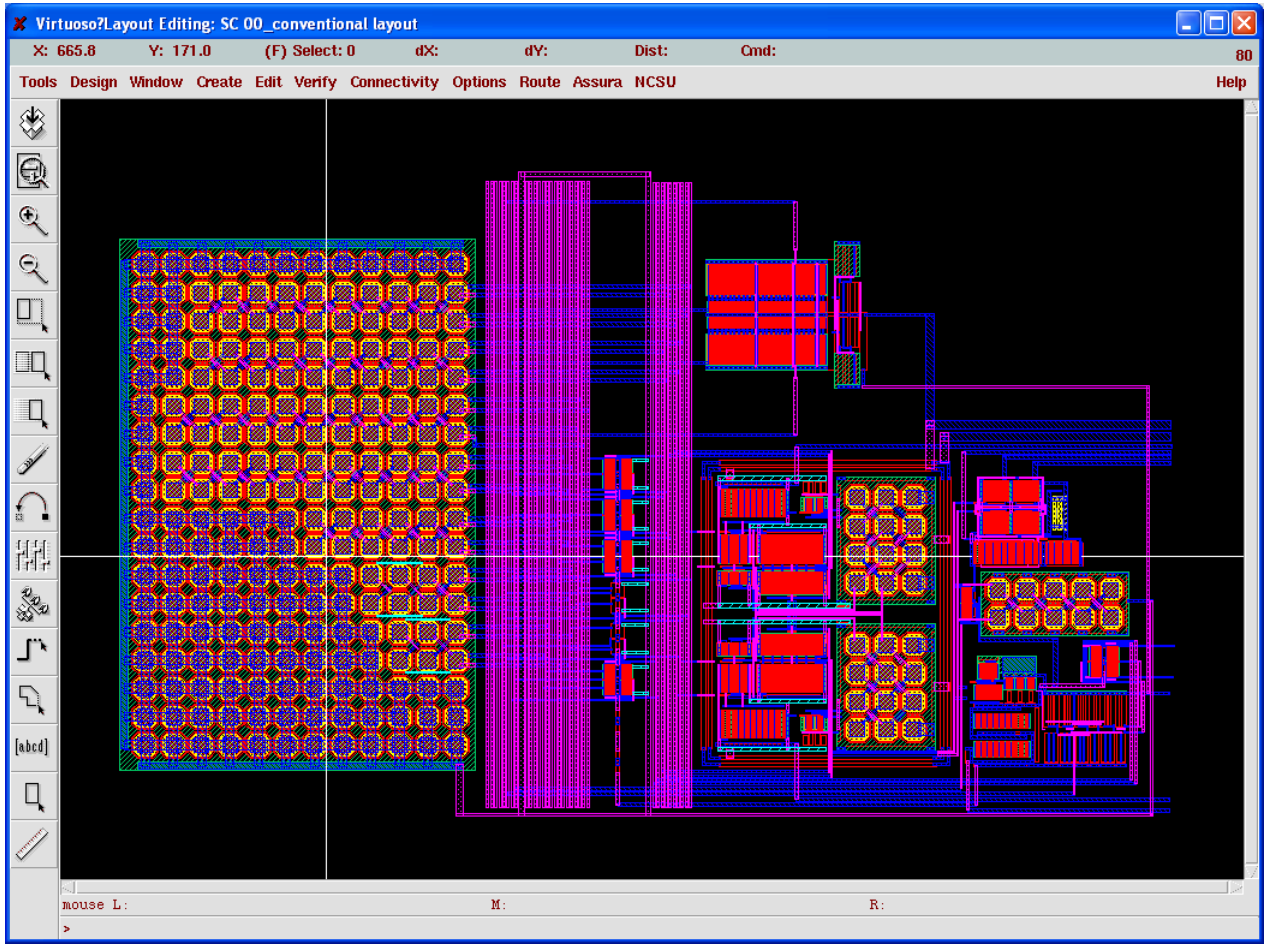




$$\frac{C1}{C2} = \frac{2}{3}$$

- Capacitor is implemented with PIP (poly) or MIM (metal)
- Total capacitance is the sum of C_{ox} and C_{fr}'s
- Ratio is more important than absolute value
- Multiples of unit capacitor can minimize ratio error
- Unit capacitor can be determined by process
- Surrounding capacitor bank with dummies is preferred

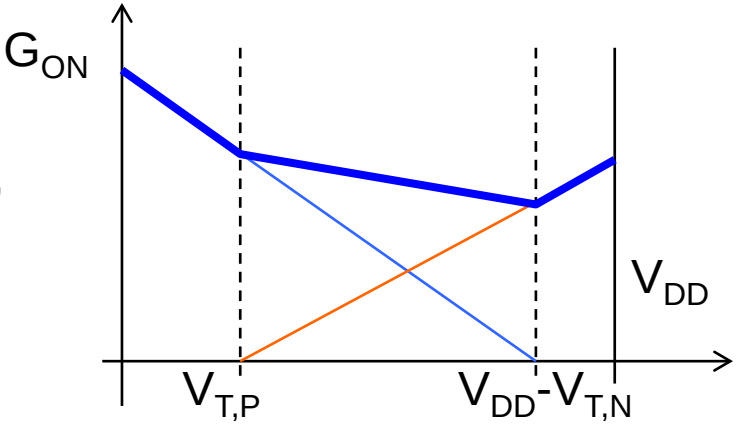
❑ Layout Example



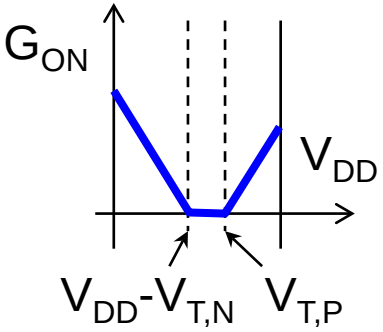
o Example of SC biquad circuit (TSMC 0.35um)

Low Voltage Switched Capacitor Circuits

- Challenges of LV SC circuit design [cas95]
  - SC circuits are widely used in filters, data converters, sample and hold, and other analog signal processing building blocks.
  - LV SC circuit design is very challenging due to the difficulties involved in turning on MOS switches.
- Solutions
  - Low and/or multi Vt process
  - Clock boostering or bootstrap
  - Switched opamp



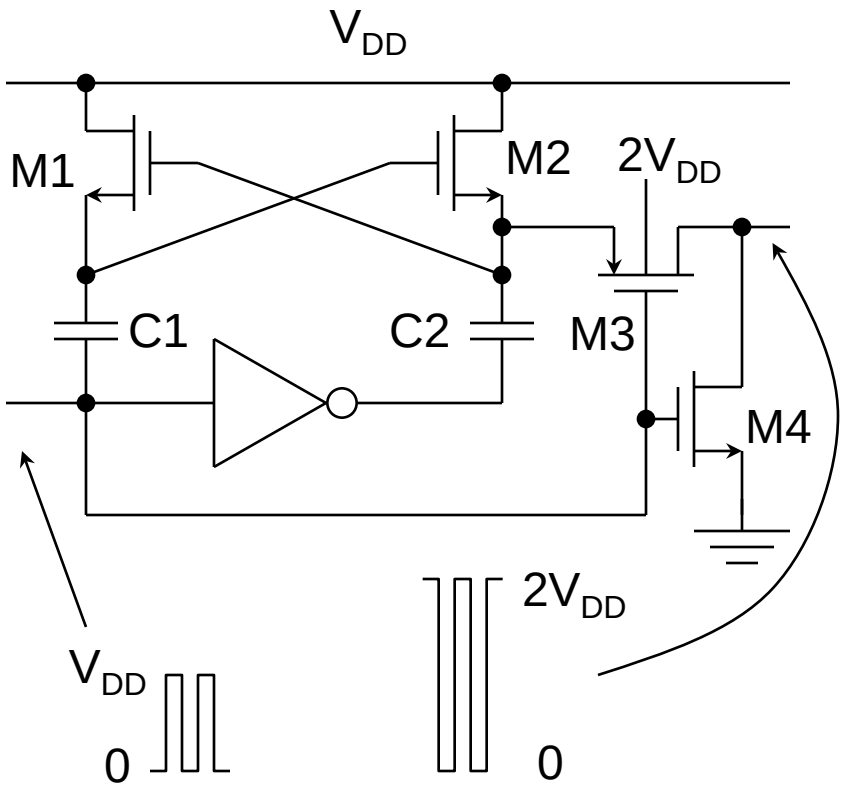
Switch conductance for high V_{DD}(such as 5V)



Switch conductance for low V_{DD}

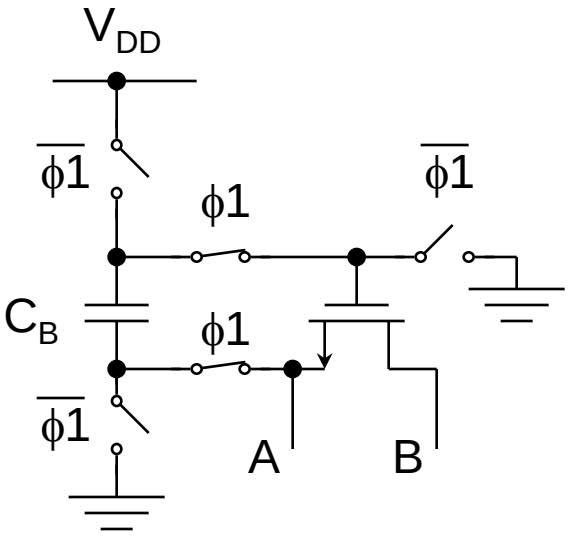
Low Voltage Switched Capacitor Circuits (Cont'd)

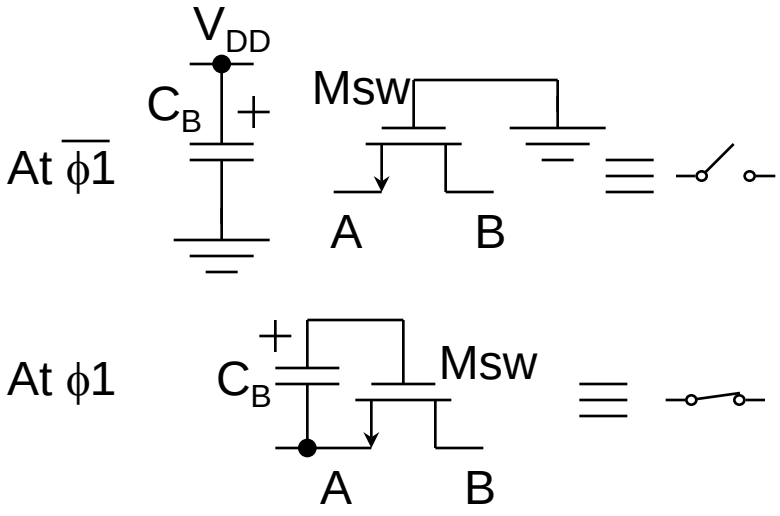
- Low and/or multi Vt process [ada90]
  - Expensive
  - Switch leakage while it is off
  - Vt is not tightly controlled for low Vt transistors
- Clock boostering or bootstrap
  - Earlier work (see right figure) required that transistors could sustain maximum breakdown voltage of 2Vdd [nak91, cho95, rab98]
  - This could not be used in finer technologies due to reduced breakdown voltage



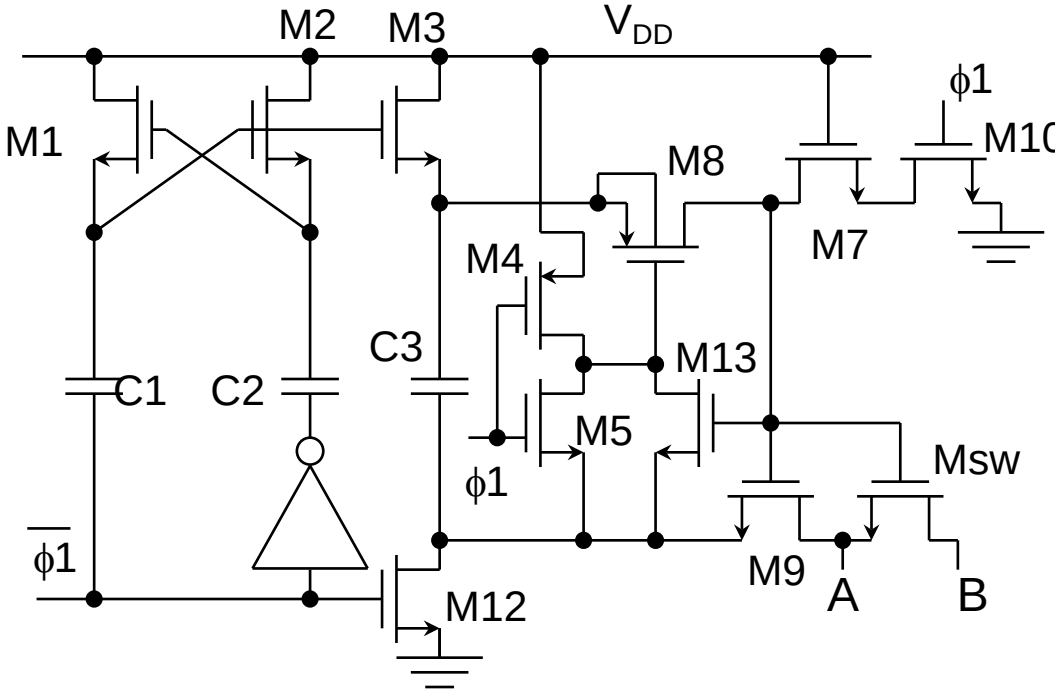
Low Voltage Switched Capacitor Circuits (Cont'd)

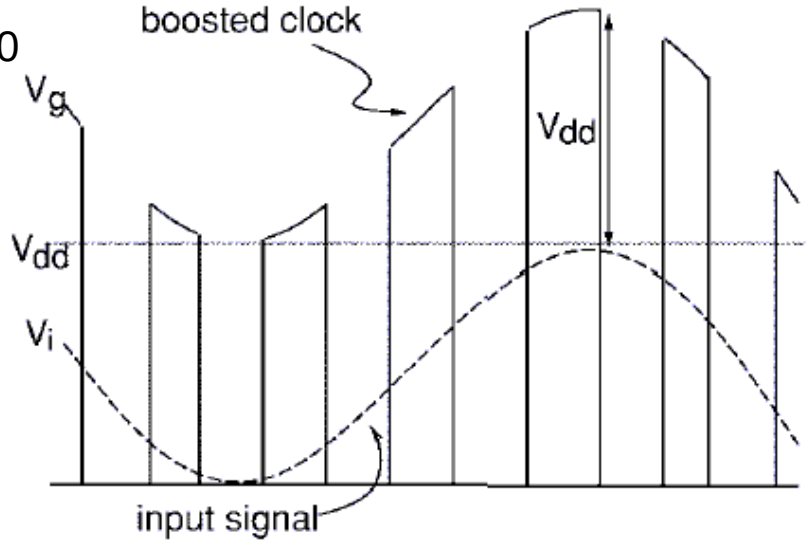
- Constant overdrive bootstrap clock driving solved this problem [abo99]
- Reliability is improved as each transistor just sustains Vdd as maximum voltage
- More power consumption and lower speed due to its complexity
- Potential reliability problem during transient



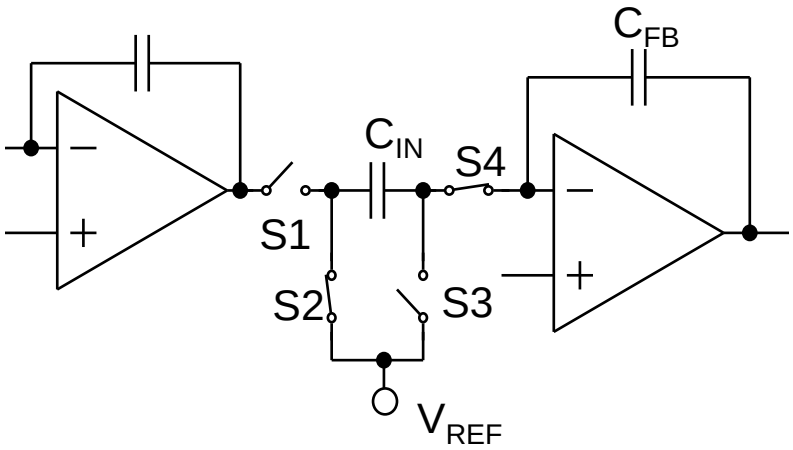


- Detailed schematic and wave form [abo99]
  - M1, M2, C1, C2 and the inverter could be shared by the switches with the same phase, other components need to be repeated for every switch.

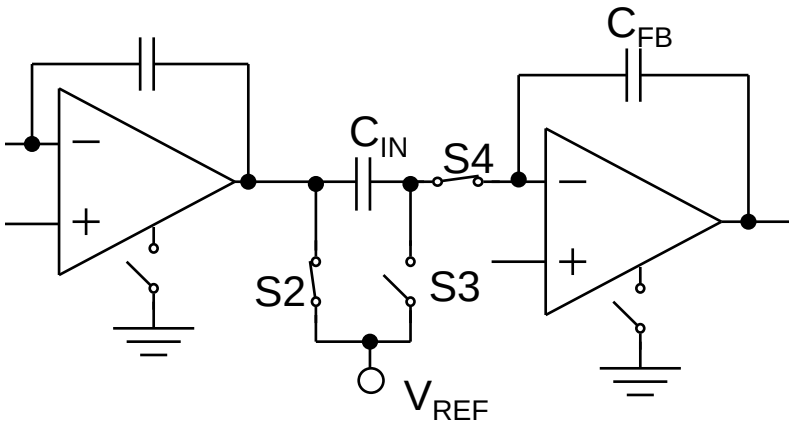




- Switched opamp [cro94,bas97, pel98]
  - In conventional SC circuits, S1 is the critical switch, as it sees wide signal swing
  - Switched opamp eliminated S1 by switching on and off the amplifier
  - True low voltage operation
  - Potential of low power consumption
  - Slower speed (usually clock freq. is around several KHz to 1 or 2 MHz) due to the need to switch on and off the opamp



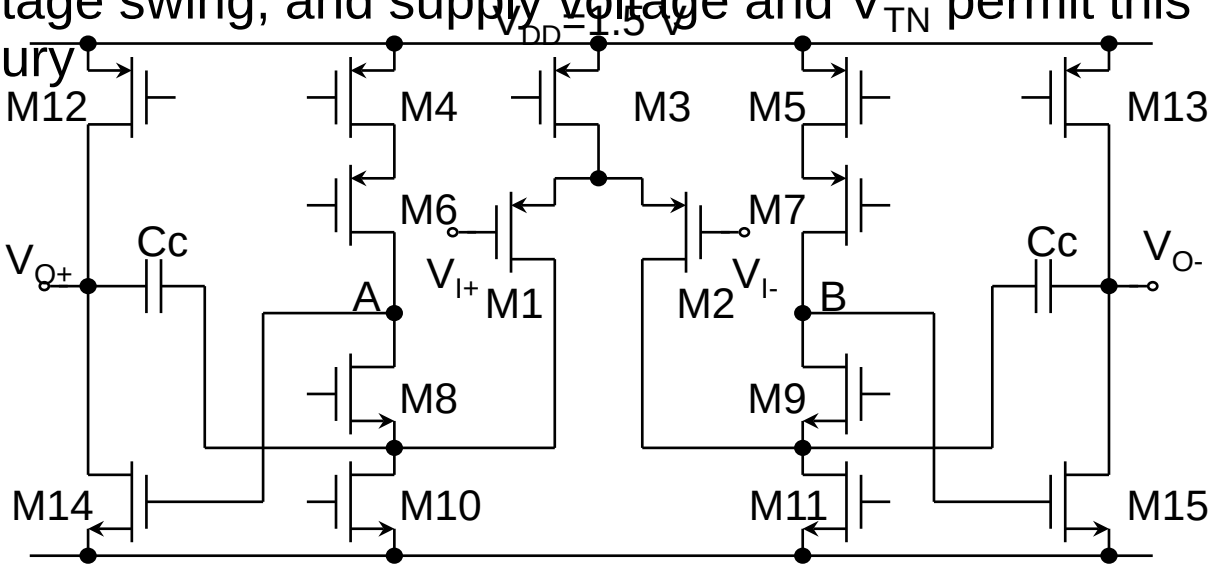
Conventional SC circuits



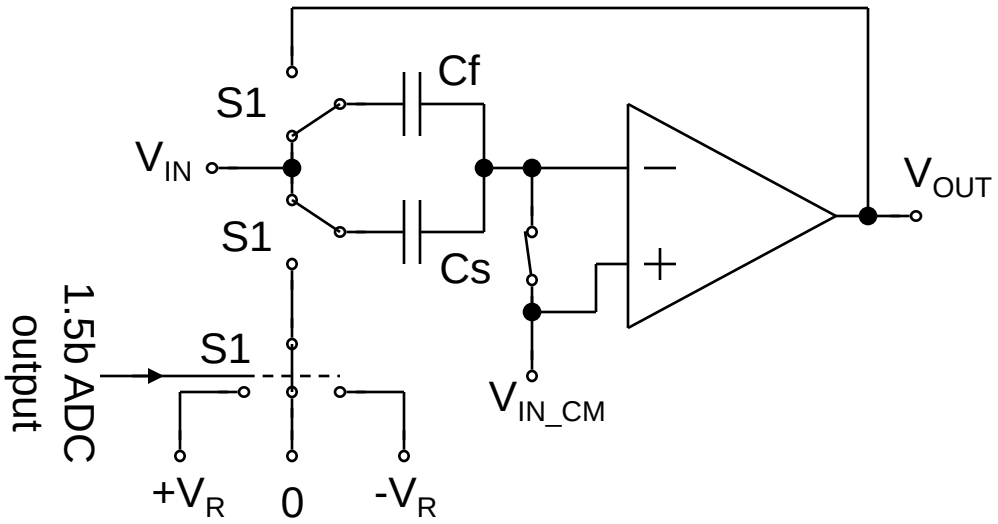
Switched opamp circuits

- Low voltage also poses difficulties for designing the SC Opamps
  - To maximize output voltage swing, cascoding of output transistors should be avoided
  - To achieve required DC gain, two stage architecture may have to be used instead of single stage OTA
  - Frequency compensation is an essential issue to make the amplifier stable and fast settling
  - Input common mode bias voltage need to close one of the supply rails to make input transistors operate correctly (close to Vss -- PMOS input; close to Vdd – NMOS input)
  - Input and output need to be biased at different DC levels, level shift may be necessary for switched opamp circuits

- LV SC opamp design example I [abo99]
  - Two-stage architecture is adopted to achieve high enough gain
  - Simple output stage maximizes output voltage swing
  - First stage is folded-cascode stage with cascode load to obtain a high gain, as nodes A and B have a small signal voltage swing, and supply voltage and V_{TN} permit this luxury

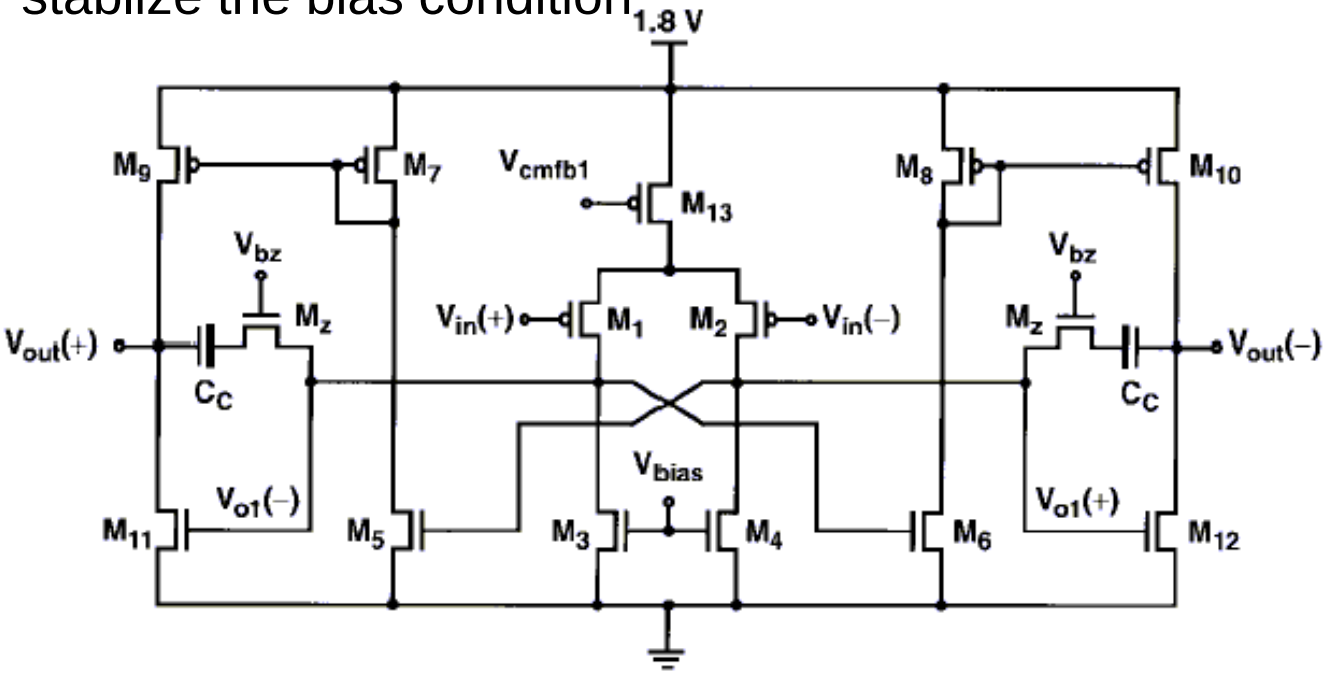


- Cascode frequency compensation [ahu83] is used to have a higher bandwidth over conventinal Miller compensation
- The functionality of the circuit is independent of V_{IN_CM} setting, thus V_{IN_CM} could be set to a DC level which makes the amplifier work properly

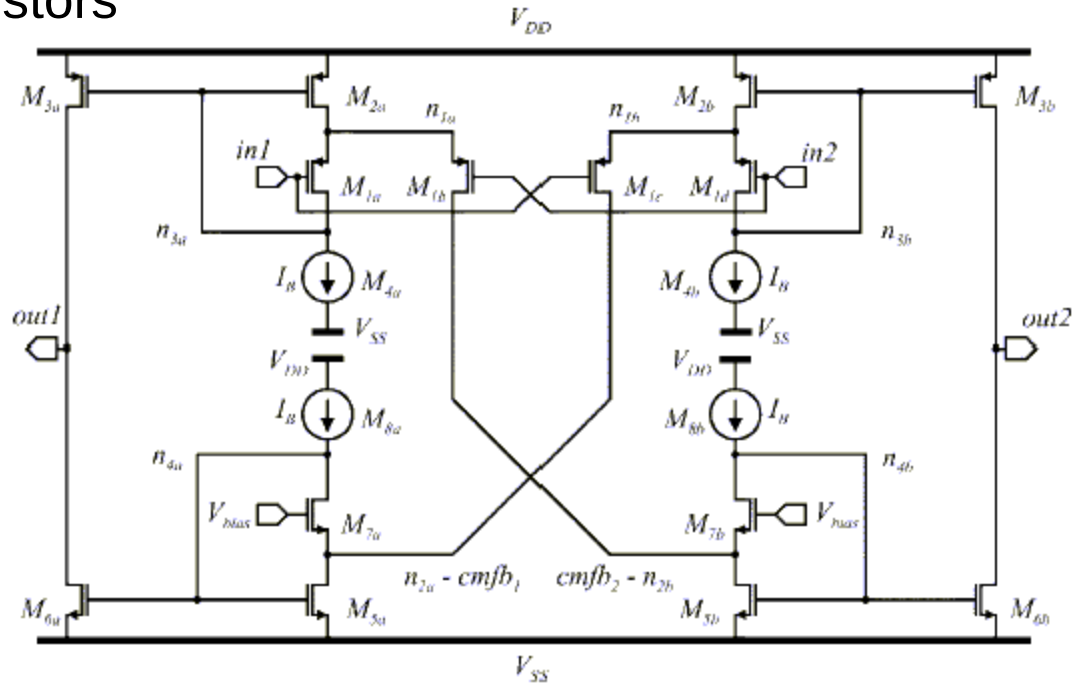


The X2 residue amplifier for 1.5b/stage pipeline A/D converter

- LV SC opamp design example II [rab97]
  - Two-stage architecture with miller compensation
  - Push-pull operation of the second stage maximize driving capacity
  - Two common-mode feedback loops are required to stablize the bias condition



- LV SC opamp design example III [pel98]
  - One-stage architecture is used due to relaxed system requirement for the DC gain
  - Class AB operation lowers power consumption
  - Low voltage current mirror makes more room for the input transistors



References

[abo99] A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999

[ada90] T. Adachi, A. Ishikawa, A. Barlow, and K. Takasuka, “A 1.4 V switched capacitor filter,” *IEEE CICC 1990*, pp. 8.2.1-8.2.4, 1990

[ahu83] B. K. Ahuja, “An improved frequency compensation technique for CMOS operational amplifiers,” *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 629-633, Dec. 1983

[bas97] A. Baschirotto and R. Castello, “A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing ,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1979-1986, Dec. 1997

[cas95] R. Castello, F. Montecchi, F. Rezzi, and A. Baschirotto, “Low-voltage analog filters,” *IEEE Trans. Circuits and Systems – I*, vol. 42, no. 11, pp. 827-840, Nov. 1995

[cho95] T. B. Cho and P. R. Gray, “A 10 b, 20 Msample/s, 35 mW pipeline A/D converter,” *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995

[cro94] J. Crols and M. Steyaert, “Switched-opamp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages,” *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936-942, Aug. 1994

[nak91] Y. Nakagome, et al. “An experimental 1.5-V 64-Mb DRAM,” *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 465-472, April 1991

[pel98] V. Peluso, P. Vancorenland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, “A 900-mV low-power $\Sigma\Delta$ A/D converter with 77-dB dynamic range,” *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887-1897, Dec. 1998

[rab97] S. Rabii and B. A. Wooley, “A 1.8-V digital audio sigma-delta modulator in 0.8 um CMOS,” *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783-796, June 1997