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Low Voltage Analog Circuit Design Techniques: A Tutorial

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SUMMARY

Low voltage (LV) analog circuit design techniques are addressed in this tutorial. In particular, (i) technology considerations; (ii) transistor model capable to provide performance and power tradeoffs; (iii) low voltage implementation techniques capable to reduce the power supply requirements, such as bulk-driven, floating-gate, and self-cascode MOSFETs; (iv) basic LV building blocks; (v) multi-stage frequency compensation topologies; and (vi) fully-differential and fully-balanced systems.

key words: analog circuits, amplifiers, transistor model, bulk-driven, floating-gate, self-cascode, NGCC frequency compensation, fully-differential and fully-balanced systems.

1. Introduction

The market and the need to develop efficient portable electronic equipment have pushed the industry to produce circuit designs with very low voltage (LV) power supply, and also often constrained to low power (LP) consumption. The last case always applies to implantable medical electronic devices. The trend is addressed to both analog and digital circuits. This is a tremendous challenge since many new products are not only required to operate with 3V or less, but need to have superior performance and lower cost to compete in an industry with fast turn around time. This competition has also stimulated the creation of a number of startup companies, where circuit design ideas are vital tools to contend.

In this tutorial, we discuss the key issues in low voltage analog circuit design. The new smaller size process technologies offer opportunities to operate at higher frequencies consuming less power. For analog circuits, this fact partially applies since it is often the case that additional current is needed to keep the same performance when the power supply voltage is decreased. Furthermore, for sub-micron technology it would not be possible to use voltage doublers to enhance the circuit performance due to low breakdown voltage of the transistors.

Another important design aspect is the transistor region of operation. For instance, with transistors operating in strong inversion, it is often the case that more power is used than the required to meet the specifications. Optimal designs involve minimum power consumption and/or silicon area while meeting design specifications. Designers should explore having transistors operating in non-conventional regions of operation. The extreme cases of weak inversion and strong inversion often do not provide a good tradeoff between frequency response, power consumption and silicon area. Thus we should consider a one-equation transistor model for all regions [1, Chapter 2], [2], [3], which allows designers to optimize the circuit performance at minimum cost. Next we will discuss how bulk-driven and floating-gate techniques can help to produce efficient LV circuits with reduced power supply restrictions. Some of the basic building blocks such as current mirrors, differential pairs, and class AB output structures capable to operate in LV are explored and discussed.

In conventional 5V analog circuits, the use of cascode (stacking of devices) circuits yielding high output impedance is attractive and easy to use. However, for less than 2V supply, the cascode circuits are often not feasible due to the reduced voltage headroom available. This implies that growing circuits vertically is not practical for low voltage design, the natural option is to grow horizontally. However, this horizontal design style implies circuits in cascade require a sound design [3]–[5] to maintain stability and high performance. This is because cascade circuits have poles and zeros that potentially might yield an unstable system when they are connected in closed loop. Thus, by judicious manipulating pole and zero positions, a circuit meeting arbitrary specifications can be designed.

In low voltage analog design, fully-differential or balanced structures are ubiquitously used due to the advantages of higher CMRR and PSRR, lower even order distortion, and wider signal swing range. We will address this issue in Section 6.

2. Technology Considerations and an All Region One Equation MOS Transistor Model

2.1 Technology Considerations

Threshold voltage is not proportionally reduced for scaled down technologies. A natural solution is the use of a multi-threshold process technology. Unfortu-

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nately, this kind of technology is more expensive and frequently not easy to reproduce. Some design advantages can be obtained by using BiCMOS technology at the expense of an additional cost, since more fabrication steps are involved. It has been the case that designers using BiCMOS technology produce circuits with better performance than CMOS based designs. However after some time, the CMOS designers come with ingenious design techniques to match BiCMOS circuit performance. The competition between these two technologies will continue, in particular in high frequencies. For microwave frequencies GaAs technology is currently flourishing. However one competitive technology, the SiGe, is a serious contender especially for above 1.5 GHz applications. Also SOI (silicon on insulator) is a hard-radiation tolerant technology with competitive attributes in some applications.

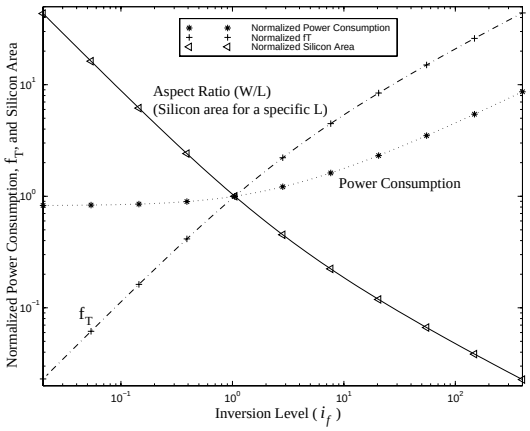

Fig. 1 Normalized power consumption, f_T, and silicon area v.s. i_f.

2.2 All Region One Equation MOS Transistor Model

In the past, low power consumption usually was less critically considered among key design specifications. But today, both increased circuit density of current fine-line CMOS technology and battery-operated portable equipment necessitate low voltage low power system design. For CMOS analog circuits, when the transistors operate in weak inversion region, g_m/I_D reaches the maximum, hence the minimum power consumption can be achieved due to the small quiescent current at the expense of large silicon area and slow speed. When MOS transistors operate in strong inversion, however, although good frequency response and small area are obtained, non-optimum larger power is consumed, and $V_{DS(sat)}$ is high. For most analog circuits, the best tradeoff among area, power and speed can be achieved when the transistors work in moderate inversion region [3]. But conventional MOS transistor models provide different sets of equations for weak and strong inversion regions [6], even in computer simulation tools [7]. Although some complex bridging equations are used in the intermediate region, large errors or discontinuities of the transistor small signal parameters are often unavoidable. Moreover, it is impossible for circuit designers to predict circuit performance in moderate inversion with simple hand calculations. Most designers often assume conservative ways to make the MOS transistors work in strong inversion, with power consumption and speed higher than needed, thus avoiding an optimal design. In recent years, some attempts of MOS modeling have been made to have one-equation model for all the operation regions [1, Chapter 2] [2], [8].

A current based model with one-equation for all regions including weak, moderate, and strong inversion with good accuracy was proposed in [1, Chapter 2], [2], which has been successfully applied in low power analog circuit design [1]–[3]. This physically based model which preserves the structural source-drain symmetry and charge conservation of the MOSFETs has infinite order of continuity for all operation regions. In addition to its computer-implemented version [9], it is also extremely useful for analog circuit design by hand calculations. The details of this model are beyond the scope of this paper. What we are interested in here is how it can be used to optimize the circuit performance in terms of power consumption and speed. A useful set of design equations for a saturated MOSFET using this model is given by:

$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_f}} \tag{1a}$$

$$i_f = \frac{I_D}{I_S} \tag{1b}$$

$$I_S = \mu n C_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \tag{1c}$$

$$f_T \cong \frac{\mu \phi_t}{2\pi L^2} 2(\sqrt{1+i_f}-1) \tag{1d}$$

$$\frac{V_{DS(sat)}}{\phi_t} \cong (\sqrt{1+i_f}-1)+4 \tag{1e}$$

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox}\phi_t} \frac{1}{\sqrt{1+i_f}-1} \tag{1f}$$

where, I_D — the drain current of the MOS transistor, g_m — the transconductance in saturation, n — the slope factor, ϕ_t — thermal voltage, and $i_f = I_D/I_S$ — the inversion level of the MOS transistor.

MOS transistors work in weak inversion for $i_f < 1$, strong inversion for $i_f > 100$, in between is the moderate inversion. Small i_f requires large aspect ratio W/L and area, and large i_f means small area and high speed but large current and power consumption [2], as depicted in Fig. 1 for different tradeoffs between area, f_T and power consumption. A general expression for V_{GS}, if the MOSFET is saturated and $V_{SB} = 0$, can be

written as

$$V_{GS} = V_T + n\phi_t[\sqrt{1+i_f} - 2 + \ln(\sqrt{1+i_f} - 1)] \quad (1g)$$

Eq. (1g) shows that, for strong inversion, V_{GS} reduces to the well-known approximation ($V_T + \sqrt{2nI_D/[\mu C_{ox}(W/L)]}$. For deep weak inversion V_{GS} becomes ($V_T + n\phi_t[\ln(i_f/2) - 1]$). Note that for a MOSFET working in strong inversion, $V_{GS} = V_T$ + a few hundred of mV; for weak inversion, V_{GS} is below V_T, typically by some tens of mV; and in moderate inversion, V_{GS} is slightly above V_T.

In [1, Chapter 2], [2], a simple common-source amplifier was designed using the above current-based model. The model was further utilized in designing low voltage low power 3-stage and 4-stage NGCC [4] amplifiers [3], a 5-fold of power consumption saving was achieved in [3] with the same specifications of voltage gain, bandwidth, and settling time compared with [4].

For illustration purpose, a design procedure for an amplifier utilizing the current-based model may consist of: 1) Obtain the transconductance (g_m) as a function of GBW and load capacitance; 2) Determine f_T from the speed specifications. Usually, f_T should be 3 to 10 times larger than the GBW or the highest frequency at which the circuit operates. 3) Obtain inversion level i_f from f_T (Eq. (1d)), i.e. $i_f = \left(\frac{f_T \pi L^2}{\mu \phi_t} + 1\right)^2 - 1$. 4) Derive other parameters, such as, working currents, geometry ratios, and drain-source saturation voltages from Eqs. (1a), (1f), and (1e) respectively. Interested readers are referred to [1]–[3] for detailed information.

3. Circuit Strategies to Reduce Power Supply Constraints

3.1 Challenges of Low Voltage Analog Circuit Design

Because the threshold voltage and drain-source saturation voltage of fine-line CMOS technologies do not scale down at the same rate as the supply voltage or do not scale at all, with low supply voltage, analog designers face many difficulties and challenges due to the limited voltage headroom. Some circuit structures which can only operate with higher supply voltage with desirable properties and high performance lost their validity in low voltage environment. Instead, alternative circuit structures or even system topologies have to be investigated. Let us take a cascode structure as an example. Cascode and regulated cascode structures are ubiquitously used in analog circuits operating in higher supply voltages, because of the high output impedance and hence high voltage gain without degrading the frequency response [10]. We will compare the low voltage performance of cascode and non-cascode structures [5], which are shown in Fig. 2. Assume that both of M_c and M_s carry the same amount of current I_L, $V_T = 0.75V$, and $V_{DS(sat)} = 0.2V$ (in strong inversion). To make M1

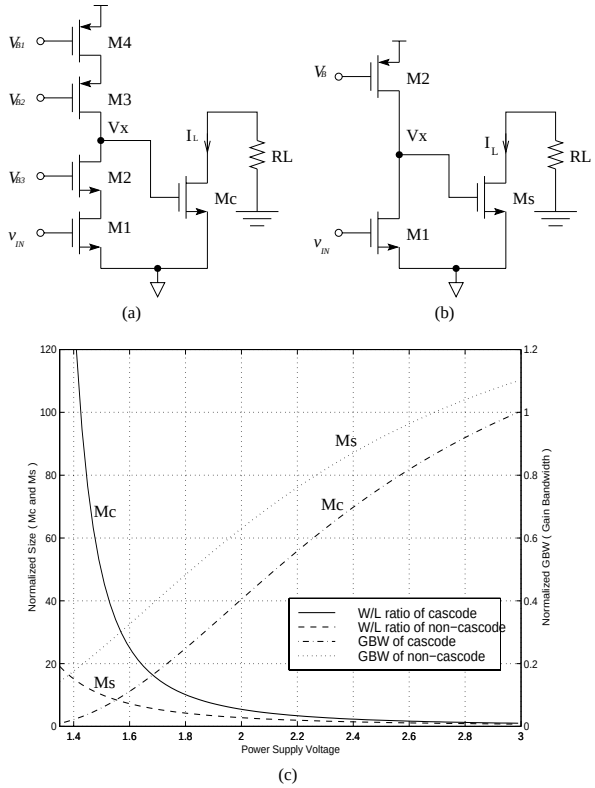

Fig. 2 Cascode and non-cascode structures, (a) A cascode gain stage plus output stage, (b) A simple gain stage plus output stage, (c) normalized transistor size and normalized GBW (at node V_x) v.s. power supply.

in Fig. 2(a) work properly, and to leave some margin for mismatching, a slightly higher V_{DS} than the minimum ($V_{DS(sat)}$) is required. Let's further assume this margin voltage is $V_{DS(margin)} \leqq 0.1V$. Since the voltage swing (at V_x) of cascode structure is less than that of the simple non-cascode structure, the W/L ratio of M_c is expected to be larger than that of M_s, in that way both I_L's in Fig. 2(a) and (b) are equal. Fig. 2(c) shows the curves of the normalized minimum W/L ratios of M_c and M_s and GBW (at node V_x) v.s. supply voltage. We observe that the cascode structure introduces unreasonable M_c size increase and hence undesirable frequency degradation due to the large parasitic capacitance when voltage supply drops below 1.5V. As cascode structure is not suitable for low-voltage operation, we have to use simple non-cascode structures in sub-1.5V applications.

Because simple non-cascode stage has a relatively low voltage gain (g_m/g_o) compared with cascode structure (with a gain of g_m^2/g_o^2), we have to *cascade* simple stages to obtain a comparable gain to that of cascode structures. Amplifiers are designed such that when connected in closed loop they do not present stability problems. This often implies, for the amplifier, to have one dominant pole close to the complex frequency plane origin, and the rest of the poles located as far as possible

from the origin [6], i.e. parasitic non-dominant poles should be placed at high frequencies. Typically pushing poles to higher frequency implies increased power consumption, thus designers should determine the required phase margin and settling time that satisfy requirements without spending more power than the necessary. With multistage amplifiers, because each stage contributes one pole at comparable frequencies, the stability condition becomes difficult, and clever frequency compensation techniques have to be developed [4], [11], We will address this issue in Section 5.

Low supply voltage also poses challenges for switched capacitor (SC) circuits, one of the most important techniques for realizing analog signal processing, because of the difficulties involved in driving some critical switches in the signal path [12], [13]. There are a number of solutions for low voltage SC circuits, including [1, Chapter 10]: 1) using low threshold MOS devices; 2) voltage multiplier or clock boosting techniques [14]; and 3) switched Op Amps [13], [15], [16]. The first is expensive and not compatible with main stream digital CMOS technologies. Moreover, the switches have a large sub-threshold leakage current when being turned off. The second is widely used in industry, however, it may not be able to be applied in future technologies which can not withstand the high boosted clock voltage. The third can only be utilized for low speed systems because of the intrinsic delay involved in switching on and off the Op Amps. Due to the limited space, we will not cover the SC design limitations [1, Chapter 10] further in low voltage environment.

Another issue for LV design is dynamic range degradation. Dynamic range is defined as the ratio of maximum allowable signal voltage swing (or power) under some distortion specifications, over the noise floor. Since the supply voltage, as well as the signal swing, decreases, the noise floor keeps at a relatively constant level, the dynamic range is degraded.

A transistor should conduct some biasing drain current to perform any signal processing task. For a MOSFET, we have to overcome the threshold voltage V_T to make it operate. The threshold voltage V_T does not scale down with the same rate as the maximum allowable power supply voltage when the feature size of modern CMOS processes decreases, mainly because of the sub-threshold current considerations for digital circuit in the mixed-signal environment [17] and the wide spread of V_T value for sub-micron technologies [18]. There are two techniques which can partially overcome the difficulties introduced by the relatively high V_T: 1) Bulk-driven MOSFETs, 2) Floating-gate MOSFETs. Another useful structure for LV applications is self-cascode MOSFET, which could improve the output impedance without much degradation for f_T and voltage swing.

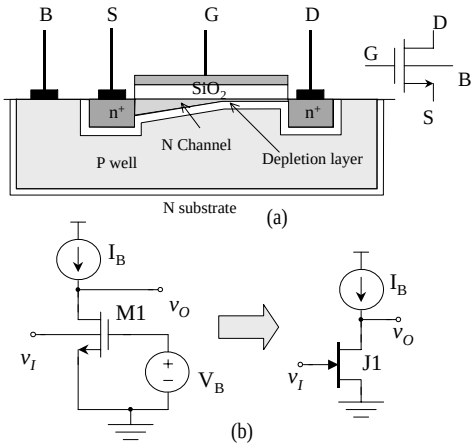

Fig. 3 Bulk-driven MOS transistor, (a) cross section and symbol of an N-channel MOSFET in P-well technology, (b) bulk-driven MOSFET is similar to a JFET transistor.

3.2 Bulk-Driven MOSFETs

A. Guzinski et al proposed bulk-driven MOS transistor concept in 1987 [19], as active components in an OTA differential input stage. It was later used in an OTA-C filter of a CMOS telephone circuit [20]. The original purpose of the bulk-driven differential amplifier was to yield a small g_m and to improve linearity. In [21] a 1-V Op Amp was designed utilizing the depletion characteristic of the bulk-driven MOS transistors to have a rail-to-rail common-mode input range and to meet the low supply voltage requirement.

The cross section of an N-channel MOSFET structure is illustrated in Fig. 3(a). For a conventional MOSFET, conductivity of the channel, hence the drain current I_D, is controlled by the gate-source voltage V_{GS}. Bulk-source voltage V_{BS} could also affect I_D, which is normally a parasitic effect, and may introduce unwanted g_{mb} and degrade the signal path. But if we keep V_{GS} constant as a bias voltage, and apply signal at the bulk gate (the P-well), we could obtain a JFET like transistor (Fig. 3(b)). Note that we use g_{mb} instead of g_m in the signal path, the former is considerably less than the latter by a factor of 0.2 to 0.4, and the input capacitance is $(C_{b,sub} + C_{bs})$ instead of $(C_{gs} + C_{gb})$.

Desirable characteristics of bulk-driven transistors are: i) Depletion characteristics avoid V_T requirement in the signal path, voltage swing for low voltage supply is increased, and minimum operational supply voltage is pushed to its limit. ii) We can use the conventional front gate to modulate the bulk-driven MOS transistor.

Unfortunately, there are also some disadvantages: i) The transconductance of a bulk-driven MOSFET is substantially smaller than that of a conventional gate-driven MOS transistor, which may result in lower GBW and worse frequency response. ii) The polarity of the bulk-driven MOSFETs is technology related. For a P

(N) well CMOS process, only N (P) channel bulk-driven MOSFETs are available. This may limit its applications. iii) The equivalent input referred noise of a bulk-driven MOS amplifier is larger than a conventional gate-driven MOS amplifier because of its smaller transconductance. iv) Prone to turn on the parasitic bipolar transistors, which may result in a latch-up problem.

3.3 Floating-Gate MOSFETs

Another technique to reduce the supply requirement of low voltage analog circuit is the floating-gate technique. Floating-gate MOS transistors have been used in digital EPROM or EEPROM for decades, but they are not so widely used in analog circuits. A number of papers have been published for applications of floating-gate technique in analog circuits, such as floating-gate CMOS analog trimming circuit [22], neural network components, multipliers [23], D/A converters[24] and amplifiers [25]–[27].

The layout and circuit symbol of a multi-input floating-gate MOSFET is depicted in Fig. 4. The floating-gate MOSFET is similar to a conventional MOSFET in the sense that the floating-gate is equivalent to the gate of a conventional transistor, except that the voltage of floating-gate V_{FG} is not controlled directly but by the control gates through capacitance coupling. The floating-gate voltage can be expressed as

$$V_{FG} = (Q_{FG} + C_{FG,D}V_D + C_{FG,S}V_S + C_{FG,B}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi})/C_\Sigma \quad (2)$$

where Q_{FG} is the static charge on the floating-gate, and $C_\Sigma = C_{FG,D} + C_{FG,S} + C_{FG,B} + \sum_{i=1}^{n} C_{Gi}$ is the total capacitance seen at the floating-gate.

The drain current I_D v.s. V_{GS} characteristic is similar to that of conventional MOSFET if we treat $V_{FG,S}$ of the floating-gate MOSFET as V_{GS} of a conventional MOSFET. Note that because V_{FG} is dependent on V_D due to the parasitic $C_{FG,D}$, the output impedance is considerably degraded and is lower than that of the conventional MOSFET [1].

An exciting property of floating-gate MOSFET is that the electric isolation from the floating-gate to other nodes is so ideal that the electric charge can stay there for several years with the variation of less than 2% in room temperature [1, Chapter 5]. We can change the equivalent threshold voltage seen from the control gates by varying the amount of static charge on the floating-gate. The static charge Q_{FG} can be changed in three ways[1, Chapter 5]: 1) ultra-violet light shining, 2) hot-electron injection, and 3) Fowler-Nordheim (FN) tunneling. In ultra-violet light, the S_iO_2 layer becomes temporarily conductive, and the static charge can leak away. Programming using hot-electron injection can be easily controlled, but need a large current. FN tunneling requires small current, however, a high voltage from 14 to 30V, depending primarily on the oxide thickness of the process, is required. By these programming techniques, we can change the equivalent V_T seen from the control gates to have a low V_T MOSFET, but the relatively complex programming circuits and/or higher programming voltage limit its low voltage applications.

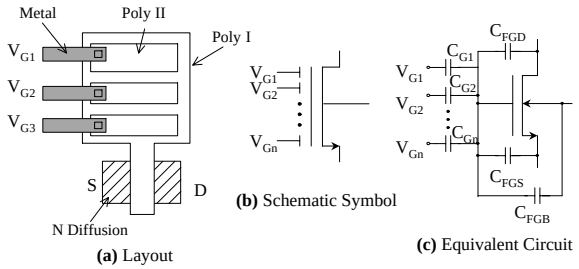

Fig. 4 Multi-input floating-gate MOSFET, (a) layout, (b) schematic symbol, (c) equivalent circuit

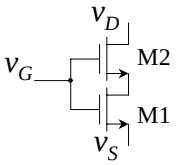

Fig. 5 Self-cascode MOSFET

Note that for MOSFETs with the same aspect ratio and bias drain current, bulk-driven and multi-input floating-gate transistors have the same drain current noise [28] as the conventional MOSFETs, however, smaller equivalent transconductance of the former two results in a higher input referred noise voltage.

3.4 Self-Cascode MOSFETs

Self-cascode configuration [29] shown in Fig. 5 provides a high output impedance with larger voltage headroom than the conventional cascode structures. The lower (upper) transistor M1 (M2) operates in non-saturation (saturation) region. For $(W/L)_2 >> (W/L)_1$, the circuit behaves like a single M1 operating in saturation region but without severe channel-length modulation effects. The output resistance is roughly proportional to $(W/L)_2/(W/L)_1$ and $V_{DS(sat)} = V_{GS} - V_T$ the same as in a single MOSFET. Note that it is not necessary to have different V_{T1} and V_{T2} for the circuit to operate properly. However, it could help to improve the output impedance [30], [31] to have $V_{T1} > V_{T2}$.

A number of excellent discussions from various aspects on low voltage low power analog and mixed-signal circuit and system design could be found in [1], [32].

4. Low Voltage Analog Building Blocks

In this section, we will discuss basic analog building blocks for low voltage design, including current mirrors, differential input stages, and output stages.

4.1 Low Voltage Current Mirrors

For modern CMOS technologies with shorter channel lengths, smaller voltage gain (due to short channel effect) and lower supply voltage impose many constraints on the performance and circuit structures of the current mirrors.

Desirable characteristics of LV current mirrors are: i) low AC equivalent input resistance r_{in}, and small DC voltage drop at the input node; ii) high output impedance, thus the output current is independent on the output voltage, whether in DC or AC; iii) low output compliance voltage†, such that maximum voltage swing at the output node is allowed; iv) good frequency response for high frequency applications; v) a linear current transfer ratio B. In most cases B should be constant and ideally is set by the transistor geometry ratios. In current-mode data converters, a precise transfer ratio over a wide current range is required.

The simplest current mirror is shown in Fig. 6(a). Other current mirror structures are mainly focused on the following design objectives: i) increase the output impedance but keep output compliance voltage as small as possible; ii) lower input resistance; iii) decrease input DC voltage drop; iv) to have an accurate current transfer ratio.

Cascode or regulated cascode structures (Fig. 6(b,c)) can be used [6], [28] to increase the output impedance. Fig. 6(b) is the basic cascode structure and it can be enhanced vertically to more levels [34] with the cost of increased compliance voltage. Regulated cascode is a good technique to increase output impedance without degradation of output voltage swing at the expense of an extra amplifier (Fig. 6(c)), which can be an Op Amp [10] or a simple common-source voltage gain stage [35]. There are a number of transistor level implementations of cascode and regulated cascode structures (Fig. 6(e,f)), following the basic structures of Fig. 6(b),(c) and (d) [6], [28], [35], [36]. The symmetrical structure of Fig. 6(d,e,f) renders a more accurate current transfer ratio depending on the matching property of the left half and right half of the circuit. Active input (Fig. 6(g,h))[33] could considerably lower the input impedance, and has a well controlled input bias voltage, it can be used in some high precision applications. Care must be taken to ensure the stability of the feedback loop [33], [37] in the active-input and/or regulated cascode structures. Table 1 summarizes the key characteristics of simple, cascode (only output part), and active-input (only input part) current mirrors.

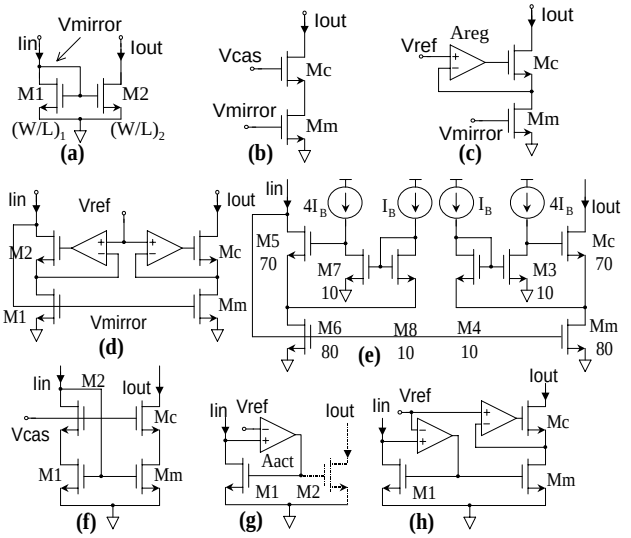

Fig. 6 Current mirrors, (a) simple, (b) cascode output, (c) regulated cascode output, (d) symmetrical regulated cascode structure, (e) one implementation of (d), (f) high swing current mirror, (g) active-input current mirror [33], (h) active-input regulated-cascode current mirror [33].

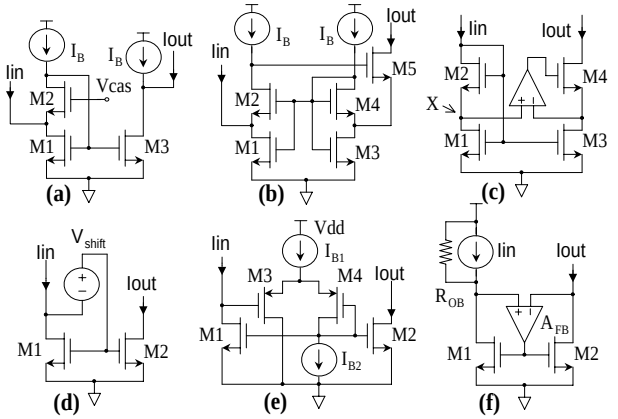

Fig. 7 Low voltage current mirrors, (a) high swing current mirror with input current injected to the source of M_3, (b) Prodanov's structure [38], (c) Itakura's structure [39], (d,e) Ramírez-Angulo's current mirror with input level shift [40], (f) F. You's structure [41].

In addition to the structures in Fig. 6 which are suitable for 3-V operation, there are a number of other LV current mirrors. For some LV circuits, a low voltage drop less than one V_{GS} over the input node of the current mirror is required. Besides the active-input structure (Fig. 6(g,h)) which can satisfy this requirement with a properly selected V_{ref}, some other structures are illustrated in Fig. 7(a,b,d,e). Fig. 7(a) is similar to Fig. 6(f), whereas the input current is injected to

†Compliance voltage is defined as the minimum DC output voltage drop at which the output branch of the current mirror remains in saturation and still has a high output impedance [6, pp. 380-381].

Table 1 Circuit characteristics of simple, cascode(only output), and active-input(only input) current mirrors

	Simple	Cascode	Reg. Cascode [28]	Active Input [33]
Input conductance	$g_{m1}+g_{ds1}\cong g_{m1}$	/	/	$g_{m1}A_{act}$
Output conductance	g_{ds2}	$\frac{g_{ds,m}g_{ds,c}}{g_{m,c}}$	$\frac{g_{ds,m}g_{ds,c}}{A_{reg}g_{m,c}}$	/
DC input voltage	V_{GS}	/	/	V_{ref}
Min. output comp. voltage	$V_{DS(sat)}$	$2V_{DS(sat)}$	$2V_{DS(sat)}$	/

the source instead of the drain of M2, with the advantage of a lower input voltage drop. For Fig. 7(b) and (c), the bottom transistors (M1 and M3) of the "cascode" structure operates in the ohmic region, thus a lower output compliance voltage by about 0.2 to 0.4 V is achieved compared with conventional high swing cascode structure (Fig. 6(f)). An attractive feature of Fig. 7(b) is its extremely low input voltage drop due to ohmic region operation of M1, which may be less than 0.1V. However, it is more sensitive to mismatch than conventional topologies. An Op Amp is used in Fig. 7(c) to force M1 and M3 to have the same V_{DS} hence the drain currents with the same value assuming they have the same aspect ratio. A possible modification to the circuit in Fig. 7(c) is to inject the input current at the source of M2 (node X) to obtain a very low input voltage drop, with some minor changes to the biasing circuitry. The cost we have to pay for the low voltage operation of Fig. 7(a)-(c) is a slightly degraded frequency response. One attractive LV technique to reduce headroom voltage limitations is the use of floating voltage sources (level shifting) [1], [40], [42]. A level shifter is utilized in Fig. 7(d) to have a low input voltage ($V_{GS}-V_{shift}$), one possible implementation is depicted in Fig. 7(e) [40]. Another novel low voltage current mirror mainly used to implement LV tail current of differential amplifiers was proposed [41] with a negative output resistance which is approximately given by $r_o=-R_{OB}\dfrac{(W/L)_{M1}}{(W/L)_{M2}}$.

Observe that the simple current mirror (Fig. 6(a)) has mainly one pole in the transfer function and behaves as a first-order low-pass filter, other more elaborated current mirrors have multiple poles. For instance, the input stage of Fig. 6(f) and Fig. 7(a) behaves as a second-order filter, and the designer should size transistors and/or bias currents for optimal settling time and frequency response, i.e., $Q<1/\sqrt{2}$ or equivalent $(g_{m2}C_{p2})/(g_{m1}C_{p1})<1/2$, where C_{p1} and C_{p2} are the parasitic capacitance at the drains of M1 and M2 respectively, and g_{m1} and g_{m2} are the transconductance of these two transistors.

4.2 Differential Input Stages

Differential input stage plays an important role in the Op Amps or OTAs. Its design directly affects the performance of the whole amplifier such as input CMR

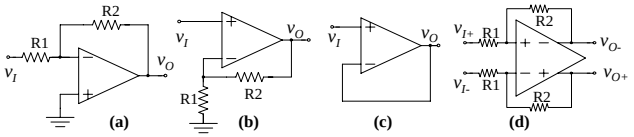

Fig. 8 Op Amp configurations, (a) inverting configuration, (b) non-inverting configuration, (c) voltage follower (or voltage buffer, a special case of (b)), (d) fully-differential configuration.

Table 2 Input common-mode swing of Op Amp configurations

Configuration	Input common-mode voltage swing
Inverting	$\cong 0$
Non-inverting	$V_{SUP}R_1/(R_1+R_2)$ †
Voltage follower	rail-to-rail
Fully-differential	$v_{I,CM}R_2/(R_1+R_2)$

† V_{SUP} is the total power supply voltage.

(Common-Mode Range) and CMRR (Common-Mode Rejection Ratio). Fig. 8 illustrates Op Amp working configurations, with input common-mode (CM) swing requirements summarized in Table 2. Note that Op Amp non-inverting single-ended configuration, especially the voltage follower, needs a large input CM swing. For inverting single-ended configuration, the input CM swing is nearly zero. Fully differential systems usually have common-mode feedback (CMFB) circuitry to control their output CM voltages. Thus most of the amplifiers in a fully-differential system have a near zero CM input swing, except the amplifiers which direct couple the signals coming from the outside world at the very front of the signal processing chain. OTAs are often used in open loop, either single-ended or fully-differential configurations. For OTA single-ended configurations, one of the differential inputs usually directly wires to AC ground, rendering an input CM swing as one half of the differential-mode (DM) swing. In fully-differential configurations, the CM input voltage of an OTA or Op Amp is fixed by the CMFB circuitry of the previous stage. In most cases, the input CM swing for OTAs is not a critical issue. The AC ground of the system should be carefully selected to yield a maximum input and output voltage swing.

For systems designed with 3V or higher supply voltage (more precisely, with $V_{SUP}>V_{TP}+V_{TN}+4V_{DS(sat)}$), N-P complementary rail-to-rail input stage can be adopted, as shown in Fig. 9(a). The problem of this simple structure is that in the central part of

Table 3 Summary of some constant g_m techniques for N-P complementary input stage

	Principle	Δg_m †	Slew Rate	Comments
1	keep $I_N + I_P$ constant [43], [44]	6% for weak inversion, 40% for strong inversion	Constant	Work well in weak inversion, not suitable for high speed application
2	keep $\sqrt{I_P} + \sqrt{I_N}$ [45], [46] or $\sqrt{K_{P,N}(\frac{W}{L})_N I_N} + \sqrt{K_{P,P}(\frac{W}{L})_P I_P}$ [47] constant	About 10% measured[47].	$\sqrt{2}$ times variation	Depends on quadratic characteristic of MOSFETs, which is not accurately followed by short channel transistors, and also has some error introduced by weak inversion operation in takeover.
3	4 times I_N or I_P when only one pair operates [45]	+15% systematic variation at the 2 takeover regions	2 times variation	1) Same with case 2, but we can change 4 to other numbers for short channel transistors. 2) +15% systematic g_m variation.
4	Back up pair with current switches [48] or 6-pair structure [49]	+20% systematic variation at the 2 takeover regions	Constant	Constant slew rate but +20% systematic g_m variation.
5	Maximum/minimum current selection [50]	5% (strong inversion) and 20% (weak inversion)	Constant	Small g_m variation (for strong inversion) and constant slew rate.
6	Electronic zener [51]	8%	Constant	Same with case 2.
7	Level shift [52]	±4% after tuning, 13% before tuning	Constant	g_m variation is sensitive to V_T and supply voltage changes.

† Δg_m represents the g_m deviations from its nominal value.

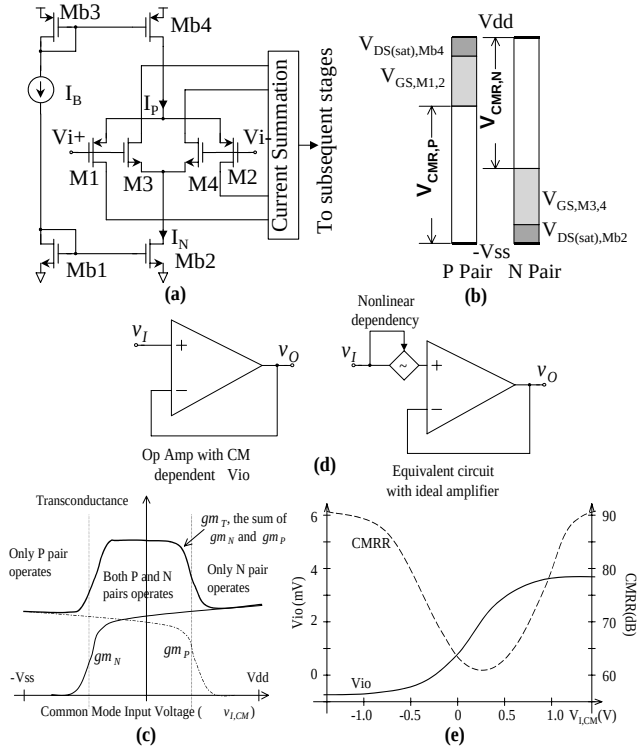

Fig. 9 N-P complementary CMOS rail-to-rail input stage, (a) basic configuration, (b) CM swings of N and P pairs (CMR_P and CMR_N), (c) g_{mT} variations with input CM voltage, (d) the effect of CM dependent input offset voltage, (e) $V_{i,cm}$ and CMRR v.s. $V_{I,CM}$ of (d).

the CM swing, both of N and P pairs operate, rendering a total transconductance (g_{mT}) which is about twice of that when the CM voltage is close to either of the supply rails and only the P or N pair is operating. Constant transconductance (g_m) rail-to-rail input stage is necessary to have an optimized frequency compensation and better linearity. There are a number of constant g_m techniques reported in literature, some of them are summarized in Table 3.

Because of the input offset voltage difference between the N and P pairs, the input referred offset voltage (V_{io}) of the input stage, hence, that of the whole amplifier will change with the common-mode (CM) input voltage swing. The input offset voltages of the N (V_{ioN}) and P (V_{ioP}) pairs, consist of systematic offset voltage, introduced by signal path asymmetry, and random offset voltage, due to the mismatches of some critical components. The dependence of input offset voltage V_{io} on the CM voltage gives rise to total harmonic distortion, or THD, at the output of the amplifier, which can not be suppressed by the external feedback loop, as shown in Fig. 9(d). This effect greatly degrades the THD performance of the whole buffer amplifier. Normally V_{io} variation could be several mV even when very careful circuit design and layout have been performed. Assuming the input offset voltage variation is as low as 2mV, and signal amplitude is 2.8Vp-p, the THD caused by the V_{io} variation could be as high as about -54dB, which is not sufficient for some high precision applications. The direct consequence caused by CM dependent V_{io} is the degraded CMRR, especially at the takeover region between N and P input pairs (Fig. 9(e)). A technique to minimize the CMRR degradation is by reducing the variation slope of the input offset voltage with the input CM level [53]. This can be achieved by making the takeover region as large as possible. However, this is limited by the available headroom voltage which becomes a serious problem for LV applications.

For very low voltage supply (say 1.5V), to main-

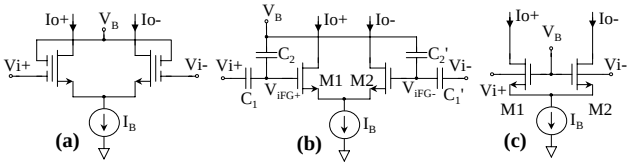

Fig. 10 Floating-gate and bulk-driven MOS input stages, (a) floating-gate MOS input stage, (b) equivalent circuit of (a), (c) bulk-driven MOS input stage.

tain a rail-to-rail CM input voltage swing is extremely difficult, because of the V_{GS} requirement of MOSFET, which usually consumes a large portion of the supply voltage. For inverting configuration (single-ended), input CM swing is nearly zero. Although the input CM voltage need to be close to V_{DD} (for N input pair) or V_{SS} (for P input pair) to make the input stage operate in very low voltage environment, it is not a severe problem as judicious voltage shifter [42] in the input stage can be devised, especially for sampled data circuits [15], [16]. For non-inverting configuration, especially for voltage buffer, wide CM input swing is necessary.

Floating-gate MOSFET differential pair can be used to obtain a rail-to-rail input CM range [27], as illustrated in Fig. 10(a) with the equivalent circuit in Fig. 10(b). V_B can be directly wired to V_{DD} for simplicity and the widest CM range. The rail-to-rail input CM range is intrinsically obtained by attenuating the input voltage. Define k_{in} as $k_{in} = C_1/C_\Sigma$ (Fig. 10(b)), the input voltage attenuation factor. Where C_1 is the capacitance of the input control gate, and C_Σ is the total capacitance seen from the floating-gate. Note that the input referred noise is increased by the factor of $1/\sqrt{k_{in}}$, compared with that of non-attenuated conventional differential pair, assuming the same g_m is achieved. With floating-gate static electric charge Q_{FG} and $V_B = V_{DD}$, to obtain an rail-to-rail swing, we need to satisfy

$$\begin{aligned} V_{SUP} &\geqq \frac{V_{FGS,M1} - Q_{FG}/C_\Sigma + V_{DS(sat),IB}}{1-k_{in}} \\ &= \frac{V_T - V_Q + V_{DS(sat),M1} + V_{DS(sat),IB}}{1-k_{in}} \quad (3) \\ \text{for} \quad & V_Q < V_T - V_{SUP,D} \end{aligned}$$

where $V_Q = Q_{FG}/C_\Sigma$, which is the equivalent voltage shift introduced by Q_{FG}, and $V_{SUP,D}$ is the voltage drop between V_{DD} to the drains of the M1 and M2. The lower supply voltage rail-to-rail operation requires a smaller attenuation factor k_{in}. By altering V_Q, the circuit may yield a better low voltage performance. If $V_Q = V_T - V_{SUP,D}$, we can obtain

$$V_{SUP} \geqq \frac{V_{SUP,D} + V_{DS(sat),M1} + V_{DS(sat),IB}}{1-k_{in}}$$

Usually, $V_{SUP,D}$ is around 0.2 to 0.4V if folded-cascode structure is used. Assuming all $V_{DS(sat)}$'s are 0.2V (for strong inversion), the minimum voltage supply is given

$$V_{SUP,min} = \frac{0.7}{1-k_{in}}(V)$$

Unfortunately, altering V_Q often requires complicated circuits and/or high programming voltages [1, Chapter 5].

Low voltage rail-to-rail CM input swing can also be achieved using bulk-driven differential pair (Fig. 10(c)) [21]. This type of input stage requires very low voltage supply, about $(V_{GS} + V_{DS(sat)})$. Its shortcoming is that the transconductance changes dramatically (about 2 times) with the CM input voltage.

Another technique to realize near rail-to-rail CM input swing is using resistive dynamic level shift [54], [55], as depicted in Fig. 11. When supply voltage drops to below $(2V_T + 4V_{DS(sat)})$, the N-P complementary input stage (Fig. 9(a)) does not provide a rail-to-rail CM input range, as illustrated in Fig. 11(a). The problem can be solved if four level shifters are inserted between the direct inputs and the gates of the input stage transistors Fig. 11(b). Because active components cease to operate under small voltage headroom, we have to resort to passive components, i.e. resistors, to realize the level shifters. The bipolar version of this concept was proposed in [54], and a 1-V near rail-to-rail input and output bipolar Op Amp was successfully implemented. Without level shift, the minimum supply voltage for a bipolar N-P complementary input stage to render a rail-to-rail input CM range is about 1.5V. Thanks to the dynamic level shift, the amplifier [54] could still operate with near rail-to-rail CM input range when the supply voltage reaches 1V. As illustrated in Fig. 11(c), the input voltage is applied to the P and N differential pairs through voltage level shift resistors $R_{L1} \sim R_{L4}$. The level shift currents, as well as the level shift voltages (V_{SHIFT}), which are shaped through a feedback network (not in the figure), change with the CM input voltage, as shown in Fig. 11(d). Fig. 11(d) also illustrates the curves of the base voltages of the input transistors v.s. CM input voltage v_{ICM}. The input stage has a constant g_m over the whole CM range by controlling the tail currents of the NPN and PNP input pairs to have a constant total current. When v_{ICM} is close to the positive (negative) supply, N (P) pair operates with $V_{SHIFT} = 0$, when v_{ICM} shifts towards the central part of the supply voltage, the level shift currents as well as V_{SHIFT} start to increase, rendering a relatively constant CM voltage at the N (P) pair bases which keeps the N (P) pair operative. V_{SHIFT} comes to its maximum, when v_{ICM} reaches the central point of the supply voltage.

A 1-V rail-to-rail input Op Amp of CMOS version (Fig. 11(e)) was implemented by Duque-Carrillo et al [55] following the idea of [54]. The working principle of the level shift current generator is illustrated in Fig. 11(f). The level shift current v.s. v_{ICM} characteristic is

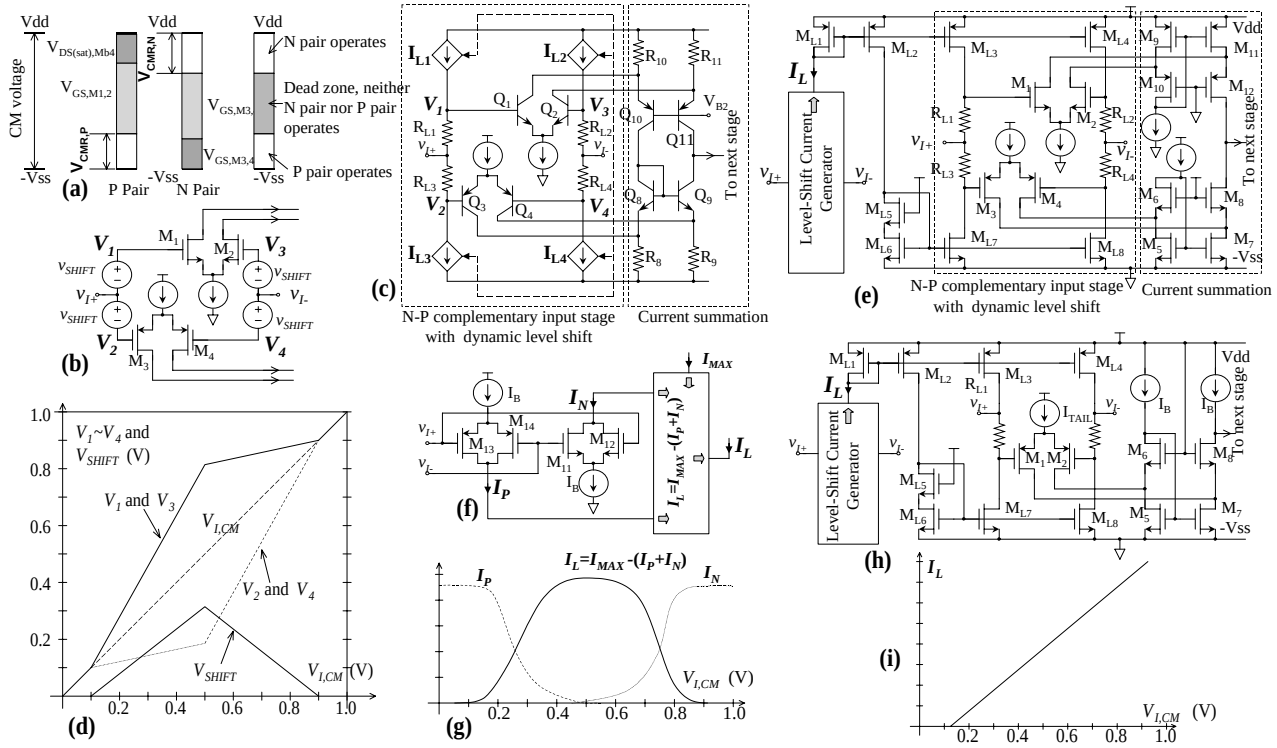

Fig. 11 Rail-to-rail input stage with dynamic level shift, (a) the N-P complementary input stage (Fig. 9(a)) has a dead zone in the central part of the CM swing when $V_{SUP} < 2V_T + 4V_{DS(sat)}$, (b) the problem can be solved by four level shifters, (c) 1-V bipolar rail-to-rail input stage [54], (d) $V_1 \sim V_4$ and V_{SHIFT} v.s. CM input voltage, (e) 1-V CMOS rail-to-rail N-P complementary input stage [55], (f) the working principle of level-shift current generator in (e), (g) I_P, I_N, and I_L v.s. v_{ICM}, (h) rail-to-rail P-channel input stage [55], (i) level-shift current v.s. v_{ICM} in (h).

shown in Fig. 11(g). The transconductance of this amplifier is not constant due to its simple design. Another Op Amp with a rail-to-rail CMR for a 1-V operation was implemented in the same paper [55] only with a P differential pair. Figs. 11(h) and (i) show the circuit schematic and level-shift current characteristics, respectively. The distortion performance is much better than in the previous case of Fig. 11(e), as a consequence of only using one differential pair, and therefore, no problem with the offset voltage variation exists. However, the price paid is a more difficult design, high input offset current, and low input impedance. The problem of the resistor area is more critical in the approach represented in Fig. 11(e) compared with Fig. 11(h), 4 resistors are used instead of 2. Note that the input CM range is reduced within the supply rails by the compliance voltages of the level current sources, usually, one $V_{DS(sat)}$ if simple non-cascode structures are used.

4.3 Low Voltage Output Stages

According to the types of loads, the driving capability of the output stages differs. For switched capacitor circuits which have high impedance capacitive loads, class A output stage is a good choice. Simple non-cascode common-source amplifier can be used, as well as the cascode and regulated cascode structures (Fig. 6(b)-(d)) to obtain a large voltage gain at the expense of reduced output swing [10]. For other applications, especially when the amplifier needs to drive off chip low resistive or high capacitive load, like earphone, class B or class AB output stage has to be utilized to have a large driving capability, and at the same time, a small quiescent current to save power especially in battery operated equipment. The output stage usually consumes most of the power of the amplifier in such cases. For low voltage designs, a rail-to-rail output swing is desirable to efficiently utilize the power supply voltage.

Common-drain voltage follower output stage (Fig. 12(a)) is rarely used in low voltage design due to its small output voltage swing as a result of stacking of $V_{GS,P}$ and $V_{GS,N}$. Instead, we have to use common-source class AB configurations (Fig. 12(b)). Compared with the common-drain voltage follower, this kind of output stage has a higher output impedance, and usually a higher voltage gain. For Fig. 12(b), some required or preferred characteristics are: i) a large enough transconductance to satisfy the stability condition [4];

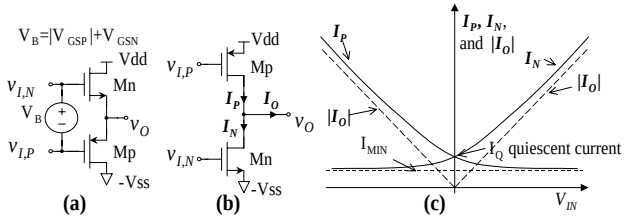

Fig. 12 Class AB output stage, (a) common-drain voltage follower (can not be used in low voltage amplifiers), (b) common-source structure which features a rail-to-rail swing, (c) ideal input-output transfer characteristic for class AB output stage.

ii) small quiescent current I_Q and large output current when driving heavy load (i.e. small resistance or large capacitance) to fully utilize the power from the voltage supply; iii) rail-to-rail output swing as discussed before; iv) the output stage should have a fast switching speed or a small switching delay between the N and P transistors, in order to minimize crossover distortion at high frequencies. The switching delay is introduced by charging and discharging the parasitic gate capacitors of the output transistors. When one transistor is turned on and driving the load, the other transistor can not switch off completely, instead, it should conduct a small amount of current for fast turn-on at next half of the signal period. The ideal input output transfer characteristic is shown in Fig. 12(c).

There are basically two categories of the CMOS class AB output stage depending on how the quiescent current is controlled: i) without feedback loop [56], [57], and ii) with feedback loop [5], [43], [45]–[47], [58], [59]. Usually, the latter has a better accurate control over the quiescent current and can operate at lower supply voltage, but with a reduced speed and may have stability problem because of the feedback loop.

Monticelli's class AB output structure [56] as shown in Fig. 13(a) is widely used in low voltage designs. The input currents i_{I1} and i_{I2} can be obtained from simple or cascode transconductor illustrated in Fig. 13(b and c), which can be further improved by regulated cascode structure similar to Fig. 6(c) to have a higher gain. One desirable property of this structure is that, with a sound design, the output transistors will never cut off, and it can have a larger voltage gain depending on the impedance of the current sources I_B's and the output impedance of the driving circuitry. The minimum supply voltage requirement of this structure is $(2V_T + 3V_{DS(sat)})$, which is about $2.2V$ for $V_T = 0.75V$. But with the minimum voltage supply, the driving capacity is near zero, because the over-drive voltage for the output transistors is only $(V_{SUP} - 2V_T - 2V_{DS(sat)})$. One nice analysis of this structure by R. F. Wassenaar et al can be found in [1, pp. 264-266]. The bias currents I_B's can be merged with previous driving stage, possibly a rail-to-rail constant g_m input stage, with the advantage of

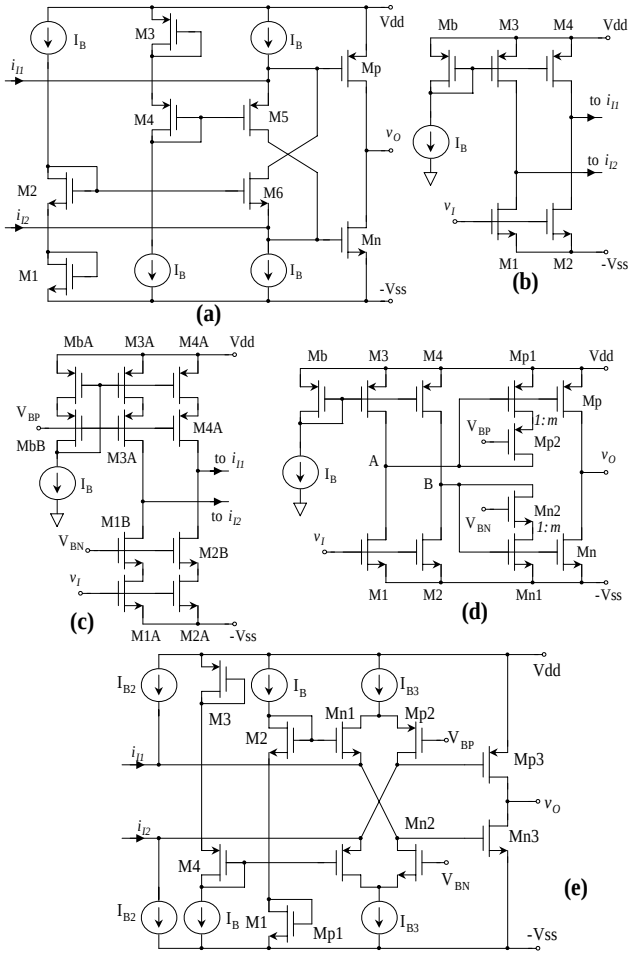

Fig. 13 Class AB output stage without negative feedback loop, (a) Monticelli's class AB output stage[56], (b) simple and (c) cascode input transconductors for (a), (d) You et al's class AB output stage[57], (e) a new class AB output stage.

compact circuit structure and lower current consumption [44], [60].

You et al's structure [57] illustrated in Fig. 13(d) has a minimum supply voltage of $(V_T + 2V_{DS(sat)})$ (about 1.2V for $V_T = 0.75V$) and has a very good class AB behavior. In this circuit, Mn2 (Mp2) has a smaller aspect ratio (W/L) than Mn1 (Mp1). In quiescent condition, Mn1 and Mn2 (Mp1 and Mp2) work in saturation region, Mn1 and Mn (Mp1 and Mp) form a current mirror with the current transfer ratio of m. When V_A and V_B increase (decrease) due to the input voltage change, the incremental resistance at node B (A) tends to increase as Mn1 (Mp1) will be driven out of saturation to linear region due to the increase of $V_{GS,Mn2}$ ($V_{SG,Mp2}$), a larger voltage gain will result at node B (A). The price paid is its relatively low gain, because of the low impedance at node A and B in Fig. 13(d).

A new class AB structure is proposed and depicted in Fig. 13(e). This circuit has some similar-

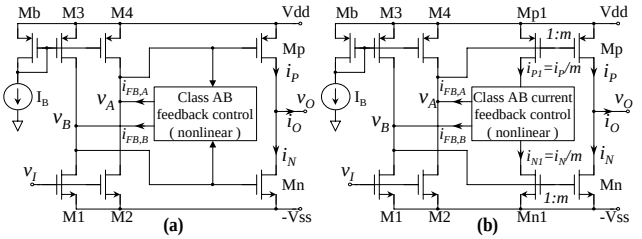

Fig. 14 Class AB output stage with negative feedback loop, the class AB control block may sense the v_{GS} (a) or drain currents (b) of the output transistors.

ity with Monticelli's structure with improved overdrive voltage for the output transistors by V_T, which is $V_{SUP} - V_T - 2V_{DS(sat)}$ for our proposed structure, whereas, $V_{SUP} - 2V_T - 2V_{DS(sat)}$ for Monticelli's structure, with the cost of a slightly increased bias current. This improvement is very desirable in low voltage applications due to the increased driving capability.

The characteristics of these three class AB structures are summarized in Table 4.

The working principle of the class AB control with a feedback loop is depicted in Fig. 14. The class AB control block may sense the v_{GS} (Fig. 14(a)) or the drain currents (by Mn1 and Mp1, Fig. 14(b)) of the output transistors, and generates currents $i_{FB,A}$ and $i_{FB,B}$ (usually $i_{FB,A} = -i_{FB,B}$) and feeds them back to some high impedance nodes in the signal path, most often, the gates of the output transistors. Note that the common-mode voltage of V_A and V_B controls the difference of i_P and i_N, which actually is the output current i_L; whereas the difference of V_A and V_B controls the common-mode current of i_P and i_N, which is the quiescent current of the output transistors. The class AB feedback control intrinsically has a nonlinear behavior, which can be implemented by nonlinear circuitry. There are several implementations of the class AB control block in Fig. 14(a)(b), mainly including, i) minimum selectors [45], [59], [61], which are derived from [58], and ii) MTL (MOS Translinear Loop) [62] based [1, pp. 259-263], [46], [47].

5. Multi-Stage Frequency Compensation [4]

In Section 3.1, we have discussed the difficulties involved in the design of high gain very low voltage amplifiers because of the stability considerations of multi-stage structures. NGCC (Nested G_m-C Compensation) [4] is an excellent multi-stage frequency compensation technique which could lead to a simple design procedure and better predictable performance compared with NMC (Nested Miller Compensation) [11] and other multi-stage frequency compensation techniques. We will reformulate the equations in this section by considering the parasitic capacitors in the internal nodes, since in LV LP design, transistors usually work in moderate inversion region, internal parasitic capacitance frequently can not be ignored. The new equations presented in this section could render optimized smaller values of frequency compensation capacitors as well as the transistor transconductances. Hence a low power design, meeting the constraints of noise and matching considerations, is feasible.

Fig. 15(a) is a simple 2-stage amplifier without frequency compensation. Although the DC voltage gain achieved is $\frac{g_{m1}g_{m2}}{g_{o1}g_L}$, which is higher than that of one stage non-cascode amplifier, there are two poles present which are located at: $\omega_{p1} = g_{o1}/C_{p1}$ and $\omega_{p2} = g_L/C_{p2}$. Miller frequency compensation capacitor C_m can be added to yield a one dominant pole frequency response, as shown in Fig. 15(b). The gain can be expressed as

$$A_v(s) = A_0 \frac{1 - s/z}{s^2/(p_1 f_2) + s/p_1 + 1} \tag{4}$$

where $A_0 = \frac{g_{m1}g_{m2}}{g_{o1}g_L}$, $z = \frac{g_{m2}}{C_m}$, $p_1 = \frac{g_{m1}}{C_m A_0} = \frac{f_1}{A_0}$, $f_1 = \frac{g_{m1}}{C_m}$, $f_2 = \frac{g_{m2}}{C_L(1 + C_{p1}/C_L + C_{p1}/C_m)}$.

One RHP (Right Half Plane) zero $z = \frac{g_{m2}}{C_m}$ is introduced due to the direct high frequency signal path through C_m, which degrades the stability of the amplifier in close loop. A g_{mf1} feedforward path could be used to eliminate the RHP zero. This technique is depicted in Fig. 15(c). The transfer function of the amplifier is still like Eq. (4), but the zero changes to

$$z = \frac{1}{\frac{C_m}{g_{m2}} - \frac{g_{mf1}(C_m + C_{p1})}{g_{m1}g_{m2}}}$$

When $g_{mf1} = g_{m1}\frac{C_m}{C_m + C_{p1}}$, z goes to ∞, thus Eq. (4) yields

$$A_v(s) = A_0 \frac{1}{s^2/(p_1 f_2) + s/p_1 + 1} \tag{5}$$

We can increase the voltage gain A_0 by adding more stages. Extending two-stage amplifier to three-stage we can obtain the structure as illustrated in Fig. 15(d). The topology can be further extended in a nested fashion to n stages as depicted in Fig. 15(e). Generally, for an n-stage NGCC amplifier, define $k_i = \frac{C_{pi}}{C_{mi}}$ and $m_i = \frac{C_{mi}}{C_L}$ (i from 1 to $n-1$), when $g_{mfi} = g_{mi}\frac{C_{mi}}{C_{mi} + C_{pi}}$ (i from 1 to $n-1$), the transfer function of the amplifier is

$$A_v(s) = \frac{A_0}{\frac{s^n}{p_1 \prod_{i=2}^{n} f_i} + \frac{s^{n-1}}{p_1 \prod_{i=2}^{n-1} f_i} + \cdots + \frac{s^2}{p_1 f_2} + \frac{s}{p_1} + 1} \tag{6}$$

Table 4 Characteristics of the class AB output stages illustrated in Fig. 13.

	Monticelli's [56]	You's [57]	Proposed
Min. supply voltage	$2V_T + 3V_{DS(sat)}$	$V_T + 2V_{DS(sat)}$	$2V_T + 3V_{DS(sat)}$
Max. V_{ov} of output transistors	$V_{SUP} - 2V_T - 2V_{DS(sat)}$	$V_{SUP} - V_T - V_{DS(sat)}$	$V_{SUP} - V_T - 2V_{DS(sat)}$
Voltage gain (Av)	High	Low	High
Can Av be improved by cascode?	Yes	No	Yes

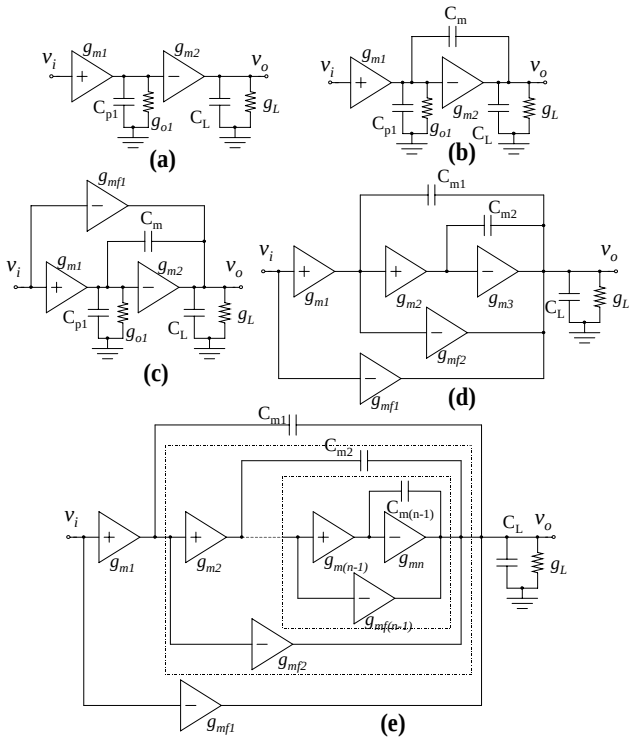

Fig. 15 Two-stage cascade, Miller compensated, and NGCC (Nested $Gm-C$ Compensation) amplifier topologies, (a) 2-stage cascaded amplifier, (b) Miller compensated 2-stage amplifier, (c) $Gm-C$ feedforward principle, (d) 3-stage NGCC amplifier, (e) n-stage nested $Gm-C$ compensation topology.

where $A_0 = \left(\prod_{i=1}^{n-1} \frac{g_{mi}}{g_{oi}}\right) \frac{g_{mn}}{g_L}$, $p_1 = \frac{g_{m1}}{C_{m1}A_0} = \frac{f_1}{A_0}$, $f_1 = \frac{g_{m1}}{C_{m1}}$, $f_i = \frac{g_{mi}}{C_{mi}} \frac{1}{1+k_i}$ (i from 2 to $n-1$), and $f_n = \frac{g_{mn}}{C_L} \frac{1}{\left(1+\sum_{i=1}^{n-1} \frac{m_i k_i}{1+k_i}\right)(1+k_{n-1})}$.

Detailed NGCC amplifier design methodology, stability, bandwidth and settling considerations, as well as CMOS implementations and experimental results, are found in [3], [4].

6. Fully Differential and Fully Balanced Systems

In mixed-signal analog/digital systems, the switching operation of the digital circuits is extremely harmful to the analog subsystem, since it pollutes the power supply voltage as well as substrate potential of the chip, and couples to the analog circuits through electro-magnetic effects. Most digital noises are present in common-mode fashion, thus fully-differential configurations are highly desirable for low voltage systems since it is intrinsically immune to common-mode noises. Other advantages of fully-differential configuration are higher signal voltage swing and lower even order distortion.

The input and output signals of a fully-differential system can be either voltage or current. In our context, we only discuss voltage-mode circuits. For a fully-differential system as shown in Fig 16(a), the differential-mode (DM) and common-mode (CM) input and output voltages are defined as, $v_{I,DM} = v_{I+} - v_{I-}$, $v_{O,DM} = v_{O+} - v_{O-}$, $v_{I,CM} = (v_{I+} + v_{I-})/2$ and $v_{O,CM} = (v_{O+} + v_{O-})/2$. Where $v_{I,DM}$, $v_{O,DM}$ are the DM input and output voltages, respectively. $v_{I,CM}$ and $v_{O,CM}$ are the CM input and output voltages.

For an amplifier with simple resistive feedback (Fig. 16(b)), the DM voltage gain is given by,

$$A_{v,DM,cl} = \frac{v_{o+} - v_{o-}}{v_{i+} - v_{i-}} = \frac{A_{v,DM,ol}\frac{R_2}{R_1+R_2}}{A_{v,DM,ol}\frac{R_1}{R_1+R_2} + 1} \cong \frac{R_2}{R1} \tag{7}$$

where $A_{v,DM,ol}$ is the DM open loop voltage gain, whereas $A_{v,DM,cl}$ is the DM close loop voltage gain. Observe that, the output common-mode (CM) voltage, $(v_{O+} + v_{O-})/2$, can be any value and the circuit still remains in equilibrium condition. The feedback network in Fig. 16(b) only affects the differential-mode (DM) signal, the CM output voltage remains in open loop and is not well defined. In practice, the CM output voltage has to be fixed to a certain value, such that the output stage is not saturated or cut off, thus the DM signal can reach its maximum voltage swing. Therefore a feedback loop which controls the CM component of the output voltage, called common-mode feedback (CMFB), has to be inserted into the fully-differential system. The conceptual model, using single-ended amplifiers, of a fully-differential Op Amp with CMFB loop is shown in Fig. 16(c). The CMFB loop is redrawn in Fig. 16(d) with the CM voltages before CMFB ($v'_{O,CM} = (v'_{O+} + v'_{O-})/2$) and after CMFB ($v_{O,CM} = (v_{O+} + v_{O-})/2$).

The DC CM output voltage is set to V_{REF} due to the CMFB amplifier in the negative feedback loop, thus the CM output voltage signal can be expressed as

$$v_{O,CM} = \frac{v'_{O,CM}}{A_{CMFB} + 1} \tag{8}$$

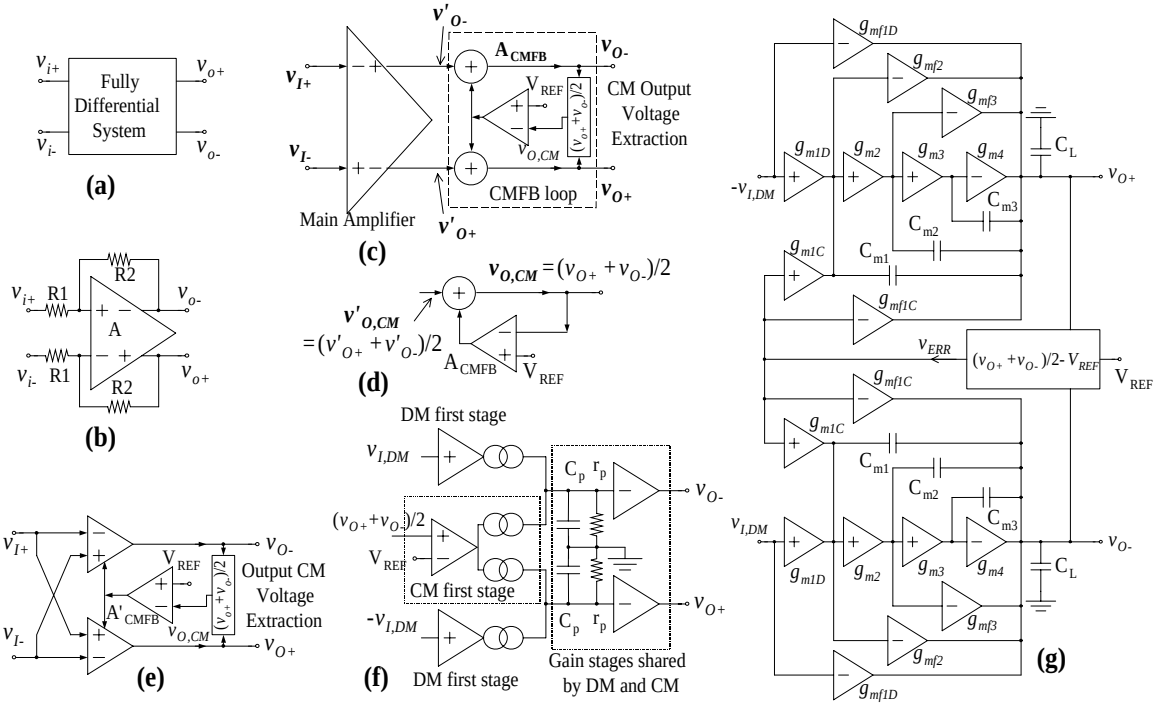

Fig. 16 Fully differential and fully-balanced systems, (a) fully-differential system, (b) a conceptual fully-differential amplifier, (c) conceptual common-mode feedback (CMFB) working principle, (d) simplified diagram of CMFB circuit, (e) CMFB implementation principle, (f) transform single-ended amplifiers to fully-differential one by simple modification, (g) an example: a fully-balanced NGCC amplifier.

The output CM voltage is attenuated by $(A_{CMFB}+1)$, where A_{CMFB} is the gain of the CMFB amplifier. Note that Fig. 16(c) can never be used in a practical design, except for one-stage amplifiers. For multi-stage amplifiers, because of the CM voltage deviations at the internal (high impedance) nodes, the voltage gain stages may be saturated or cut off by the CM voltage offset. We have to apply a CM correction signal (current) to suitable internal nodes of the amplifier, as shown in Fig. 16(e∼f). In this way, all the stages of the amplifier will be working properly, even if there is a large CM offset from the first stage of the DM amplifier.

Fig. 16(d) indicates that the CM amplifier works in unity-gain feedback configuration, the stability of the CM loop must be ensured. The stability condition is similar to that of the main DM amplifier, as long as the main DM amplifier is unity gain stable. In practice, it is very desirable to achieve similar performance in DM and CM loops. For that reason, both loops should share most of the circuitry (Fig. 16(e-f)). However, care should be taken since the CM loop always has some extra poles or zeros introduced by the CM extractor circuitry, especially for high frequency applications. Fig. 16(f) shows that except for the first stage, all other stages are shared by the CM and DM channels. Thus, we just need to copy the input stage from the fully-differential main amplifier to the single-ended (but with two parallel channels) CMFB amplifier.

Motivated by the above analysis, the NGCC amplifier was extended from single-ended version to fully-differential version [63], by copying the input stage of the single-ended NGCC amplifier to the CMFB channel, i.e., we add input transconductor g_{m1C} and g_{mf1C} for the CMFB amplifier. Good symmetry between DM and CM channels results, as they have the same NGCC topology. A general design methodology was independently proposed by Czarnul et al [64] to extend single-ended amplifier to fully-balanced version.

To make the CMFB amplifier and the main differential amplifier to yield the same frequency response (i.e., the same GBW), it is imposed that

$$g_{m1D} = \frac{g_{m1}}{2} \tag{9a}$$

$$g_{mf1D} = \frac{g_{mf1}}{2} \tag{9b}$$

and

$$g_{m1C} = g_{m1} \tag{9c}$$

$$g_{mf1C} = g_{mf1} \tag{9d}$$

where g_{m1} and g_{mf1} are the first stage transconductances of the main and feedforward branches of single-ended NGCC amplifier, as depicted in Fig. 15.

The output CM voltage extractor can be implemented via an RC voltage divider for Op Amps, as

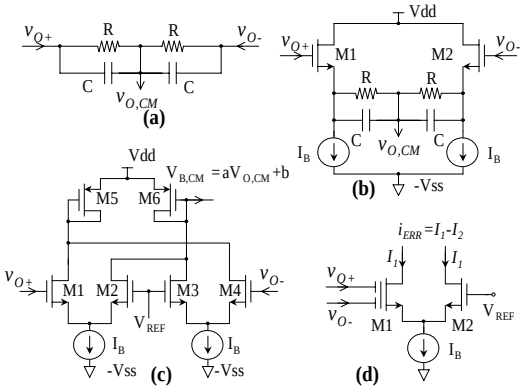

Fig. 17 Common-mode voltage detector schemes, (a) RC voltage divider, (b) common-drain voltage follower and RC voltage divider, (c) balanced double-differential-pair structure, (d) floating-gate common-mode voltage detector.

shown in Fig. 17(a). But it is not suitable for OTAs because the high output impedance is degraded by the loading effect of the RC components. Several high input impedance CM extractor have been proposed [65] (Fig. 17(b-c)) at the expense of limited DM and/or CM swing and nonlinearity. In fact, for very low voltage applications, the conventional high-output impedance CM extractors are not able to operate properly since the amplifier output signals are not large enough to turn-on any MOSFETs. In such cases, one viable solution [42] consists in shifting and attenuating these signal via passive resistor voltage dividers at the expense of reducing the input resistance of the CM detector. Note that the output signal for the balanced double-differential-pair structure (Fig. 17(c)) is a bias voltage ($V_{B,CM}$) capable to generate the bias currents to be injected to appropriate nodes. The small signal correction voltage of $V_{B,CM}$ is $v_{b,cm} = (v_{o+} + v_{o-})g_{m1}/g_{m6}$. The high input impedance is obtained at the cost of limited DM swing, which is determined by the $(V_{GS} - V_T)$ of M1∼M4 under quiescent conditions, and nonlinearity due to the second-order effects. A proposed simple CM extraction scheme using floating-gate techniques is illustrated in Fig. 17(d). v_{O+} and v_{O-} have the same coupling capacitance to the floating-gate of M1, thus we can obtain the average of v_{O+} and v_{O-} at the the floating-gate, and compare with V_{REF}. $i_{ERR} = g_m(v_{CM} - V_{REF})$ is the error current which is proportional to $(v_{CM} - V_{REF})$. i_{ERR} could be applied to some nodes or mirrored as a correction current. This CM scheme has a wide linear range which is not limited by DM swing between v_{O+} and v_{O-}. A related structure independently developed has been reported in [66].

One alternative technique to implement a fully-differential system using single-ended Op Amps is via common-mode feedforward (CMFF) [64]. Similar CMFF technique was used for pseudo-differential OTA design in [12].

7. Conclusions

A number of topics concerning low voltage analog circuit design were reviewed. The one-equation MOSFET model for all operation regions is an excellent tool to optimize circuit performance between different tradeoffs, such as power consumption, silicon area and speed, for LV LP analog design. Although there are some performance degradations for the bulk-driven and floating-gate MOSFET transistors, they are very useful components in specific LV applications. Self-cascode structure is a viable way to increase the output impedance of short channel transistors. We also reviewed a number of key building blocks for LV analog circuits. Then, we reformulated the NGCC equations for designing LV LP multi-stage amplifiers. Fully differential and balanced systems are revisited in the last part of this paper.

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References

[1] E. Sánchez-Sinencio and A. G. Andreou, Ed., *Low-Voltage/Low-Power Integrated Circuits and Systems*, IEEE Press, 1999.

[2] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[3] X. Xie, M. C. Schneider, E. Sánchez-Sinencio, and S. H. K. Embabi, "Sound design of low power nested transconductnce-capacitance compensation amplifiers," *Electronics Letters*, vol. 35, pp. 956–958, June 1999.

[4] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Multistage amplifier topologies with nested gm-C compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997.

[5] F. You, *Low Voltage Analog Circuit Design*, Ph.D. thesis, Texas A&M University, College Station, TX 77843, U. S. A., Dec. 1996.

[6] K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circiuts and Systems*, McGraw-Hill, Inc., New York, 1994.

[7] Y. P. Tsividis and K. Suyama, "MOSFET modeling for analog circuit CAD: problems and prospects," *IEEE J. Solid-State Circuits*, vol. 29, no. 3, pp. 210–216, March 1994.

[8] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83–114, 1995.

[9] O. C. F. Gouveia, A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "The ACM model for circuit simulation and equations for SMASH," see `http://www.dolphin.fr`.

[10] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, Dec. 1990.
[11] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*, Kluwer, Boston, MA, 1995.
[12] R. Castello, F. Montecchi, F. Rezzi, and A. Baschirotto, "Low-voltage analog filters," *IEEE Trans. Circuits and Systems - I*, vol. 42, no. 11, pp. 827–840, Nov. 1995.
[13] J. Crols and M. Steyaert, "Switched-opamp: an approach to realize full CMOS switched capacitor circuits at very low power supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936–942, Aug. 1994.
[14] T. B. Cho and P. R. Gray, "A 10 b 20 Msamples/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, March 1995.
[15] A. Baschirotto and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1979–1986, Dec. 1997.
[16] V. Peluso, P. Vancorenland, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 900-mV low-power $\Delta\Sigma$ A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, Dec. 1998.
[17] H. Iwai, "CMOS Technology — Year 2010 and beyond," *IEEE J. Solid-State Circuits*, vol. 34, no. 3, pp. 357–366, March 1999.
[18] E. H. Li and H. C. Ng, "Parameter sensitivity of narrow-channel MOSFET's," *IEEE Electron Device Letter*, vol. 12, no. 11, pp. 608–610, Nov. 1991.
[19] A. Guzinski, M. Bialko, and J. C. Matheau, "Body-driven differential amplifier for application in continuous-time active-C filer," *Proc. European Conf. Circuit Theory and Design (ECCTD '87)*, pp. 315–320, 1987.
[20] F. Dielacher, J. Hauptmann, J. Reisinger, R. Steiner, and H. Zojer, "A software programmable CMOS telephone circuit," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 1015–1026, July 1991.
[21] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Design 1-V op amps using standard digital CMOS technology," *IEEE Trans. Circuits and Systems II : Analog and Digital Signal Processing*, vol. 45, no. 7, pp. 769–780, July 1998.
[22] E. Säckinger and W. Guggenbuhl, "An analog trimming circuit based on a floating-gate device," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1437–1440, Dec. 1988.
[23] H. R. Mehrvarz and C. Y. Kwok, "A novel multi-input floating-gate MOS four-quadrant analog multiplier," *IEEE J. Solid-State Circuits*, vol. 31, no. 8, pp. 1123–1131, Aug. 1996.
[24] L. Yin, S. H. K. Embabi, and E. Sánchez-Sinencio, "A floating gate MOSFET D/A converter," *IEEE Proc. ISCAS '97*, vol. 1, pp. 409–412, 1997.
[25] A. Thomsen and M. A. Brooke, "A programmable piecewise linear large-signal CMOS amplifier," *IEEE J. Solid-State Circuits*, vol. 28, no. 1, pp. 84–89, Jan. 1993.
[26] C.-G. Yu and R. L. Geiger, "Very low voltage operational amplifier using floating gate MOSFETs," *IEEE Proc. ISCAS '93*, vol. 2, pp. 1152–1155, 1993.
[27] J. Ramirez-Angulo, S. C. Choi, and G. Gonzalez-Altamirano, "Low-voltage circuits building blocks using multiple-input floating-gate transistors," *IEEE Trans. Circuits and Systems I : Fundamental Theory and Applications*, vol. 42, no. 11, pp. 971–974, Nov. 1995.
[28] D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc., New York, 1997.
[29] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," *IEEE J. of Solid-State Circuits*, vol. 29, pp. 1094–1101, Sep. 1994.
[30] R. Castello, A. G. Grassi, and S. Donati, "A 500-nA sixth-order bandpass SC filter," *IEEE J. of Solid-State Circuits*, vol. 25, pp. 669–676, June 1990.
[31] I. Fujimori and T. Sugimoto, "A 1.5V, 4.1mW dual-channel audio delta-sigma D/A converter," *IEEE J. of Solid-State Circuits*, vol. 33, pp. 1863–1870, Dec. 1998.
[32] A. Rodríguez-Vázquez and E. Sánchez-Sinencio, Eds., *Special Issue on Low-Voltage and Low Power Analog and Mixed-Signal Circuits and Systems, IEEE Trans. Circuits and Systems, Vol. 42, No. 11*, IEEE, Nov. 1995.
[33] T. Serrano and B. Linares-Barranco, "The active-input regulated-cascode current mirror," *IEEE Trans. Circuits and Systems II : Analog and Digital Signal Processing*, vol. 41, pp. 464–467, June 1994.
[34] P. J. Crawley and G. W. Roberts, "High-swing MOS current mirror with arbitrary high output resistance," *Electronic Letters*, vol. 28, no. 4, pp. 361–363, 1992.
[35] E. Säckinger and W. Guggenbuhl, "A high-swing, high-impedence MOS cascode circuit," *IEEE J. Solid-State Circuits*, vol. SC-25, no. 1, pp. 289–298, Feb. 1990.
[36] U. Gatti, F. Maloberti, and G. Torelli, "A novel CMOS linear transconductance cell for continuous-time filters," *IEEE Proc. ISCAS '90*, vol. 2, pp. 1173–1176, 1990.
[37] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "A design scheme to stabilize the active gain enhancement amplifier," *IEEE Proc. ISCAS '95*, vol. 3, pp. 1976–1979, 1995.
[38] V. I. Prodanov and M. M. Green, "CMOS current mirrors with reduced input and output voltage requirements," *Electronics Letters*, vol. 32, no. 2, pp. 104–105, Jan. 1996.
[39] T. Itakura and Z. Czarnul, "High output-resistance CMOS current mirrors for low-voltage applications," *IEICE Trans. Fundamentals*, vol. E80-A, no. 1, pp. 230–232, Jan. 1997.
[40] J. Ramírez-Angulo, "Current mirrors with low input voltage requirements for built in current sensors," *IEEE Proc. ISCAS '94*, pp. 529–532, 1994.
[41] F. You, S. H. K. Embabi, J. F. Duque-Carrillo, and E. Sánchez-Sinencio, "An improved tail current source for low voltage applications," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1173–1180, Aug. 1997.
[42] J. Ramírez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba, "Simple technique for op amp continuous time 1V supply operation," *Electronics Letters*, vol. 35, no. 4, pp. 263–264, Feb. 1999.
[43] J. H. Huijsing and D. Linebarger, "Low voltage operational amplifier with rail-to-rail input and output stages," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1144–1150, Dec. 1985.
[44] W.-C. S. Wu, W. J. Helms, J. A. Kuhn, and B. E. Byrkett, "Digital-compatible high-performance operational amplifier with rail-to-rail input and output ranges," *IEEE J. Solid-State Circuits*, vol. 29, no. 1, pp. 63–66, Jan. 1994.
[45] R. Hogervorst, R. J. Wiegerink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage," *IEEE Proc. ISCAS '92*, pp. 2876–2879, 1992.
[46] J. H. Botma, R. F. Wassenaar, and R. J. Wiegerink, "A low voltage CMOS op amp with a rail-to-rail constant-gm input stage and a class AB rail-to-rail output stage," *IEEE Proc. ISCAS '93*, vol. 2, pp. 1314–1317, May 1993.
[47] S. Sakurai and M. Ismail, "Robust design of rail-to-rail CMOS operational amplifiers for a low power supply voltage," *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp. 146–156, Feb. 1996.

[48] R. Hogervorst, S. M. Safai, and J. H. Huijsing, "A programmable 3-V CMOS rail-to-rail opamp with gain boosting for driving heavy loads," *IEEE Proc. ISCAS '95*, pp. 1544–1547, 1995.

[49] W. Redman-White, "A high bandwidth constant gm and slew-rate rail-to-rail CMOS input circuit and its application to analog cells for low voltage VLSI systems," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 701–712, May 1997.

[50] C. Hwang, A. Motamed, and M. Ismail, "LV opamp with programmable rail-to-rail constant-gm," *IEEE Proc. ISCAS '97*, vol. 3, pp. 1988–1991, 1997.

[51] R. Hogervost, J. P. Tero, and J. H. Huijsing, "Compact CMOS constant-gm rail-to-rail input stage with gm-control by an electronic zener diode," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 1035–1040, July 1996.

[52] M. Wang, T. L. Mayhugh, Jr., S. H. K. Embabi, and E. Sánchez-Sinencio, "Constant-gm rail-to-rail CMOS opamp input stage with overlapped transition region," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 148–156, Feb. 1999.

[53] J. F. Duque-Carrillo, J. M. Valverde, and R. Perez-Aloe, "Constant-gm rail-to-rail common-mode range input stage with minimum CMRR degradation," *IEEE J. Solid-State Circuits*, vol. 28, no. 6, pp. 661–666, June 1993.

[54] J. Fonderie, M. M. Maris, and E. J. Schnitger, "1-V operational amplifier with rail-to-rail input and output ranges," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1551–1559, Dec. 1989.

[55] J. F. Duque-Carrillo, J. L. Ausin, G. Torelli, J. M. Valverde, and M. A. Dominguez, "1-V rail-to-rail operational amplifiers in standard CMOS technology," *IEEE J. Solid-State Circuits*, Jan. 2000, to appear.

[56] D. M. Monticelli, "A quad CMOS single-supply Op Amp with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1026–1034, Dec. 1986.

[57] F. You, S. H. K. Embabi, and E. Sánchez-Sinencio, "Low-voltage class AB buffers with quiescent current control," *IEEE J. Solid-State Circuits*, vol. 33, no. 6, pp. 915–920, June 1998.

[58] E. Seevinck, W. de Jager, and P. Buitendijk, "A low-distortion output stage with improved stability for monolithic power amplifiers," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 794–801, June 1988.

[59] F. N. L. Op't Eynde, P. F. M. Ampe, L. Verdeyen, and W. M. C. Sansen, "A CMOS large-swing low-distortion three-stage class AB power amplifier," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 265–273, Feb. 1990.

[60] R. Hogervost, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3-V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, Dec. 1994.

[61] K.-J. de Langen and J. H. Huijsing, "Compact low-voltage power-efficient CMOS operational amplifier cells for VLSI," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, Oct. 1998.

[62] E. Seevinck and R. J. Wiegerrink, "Generalized translinear circuit principle," *IEEE J. Solid-State Circuits*, vol. 26, no. 8, pp. 1098–1102, Aug. 1991.

[63] G. Xu, S. H. K. Embabi, P. Hao, and E. Sánchez-Sinencio, "A low-voltage fully differential nested gm capacitance compensation amplifier: analysis and design," *IEEE Proc. ISCAS '99*, vol. 2, pp. 606–609, 1999.

[64] Z. Czarnul, T. Itakura, N. Dobashi, T. Ueno, T. Iida, and H. Tanimoto, "Design of fully balanced analog systems based on ordinary and/or modified single-ended opamps," *IEICE Trans. Fundamentals*, vol. E82-A, no. 2, pp. 256–270, Feb. 1999.

[65] J. F. Duque-Carrilo, "Control of the common-mode component in CMOS continuous-time fully differential signal processing," *Analog Integrated Circuits and Signal Processing*, pp. 131–140, Sep. 1993.

[66] G. González-Altamirano and J. Ramírez-Angulo, "Analog building blocks for a sampled data fast wavelet transform CMOS VLSI implementation," *IEEE Proc. ISCAS '98*, vol. 2, pp. 382–385, 1998.

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