Low Voltage Circuit Design Techniques

ELEN 607 (ESS)

Analog and Mixed-Signal Center (AMSC)
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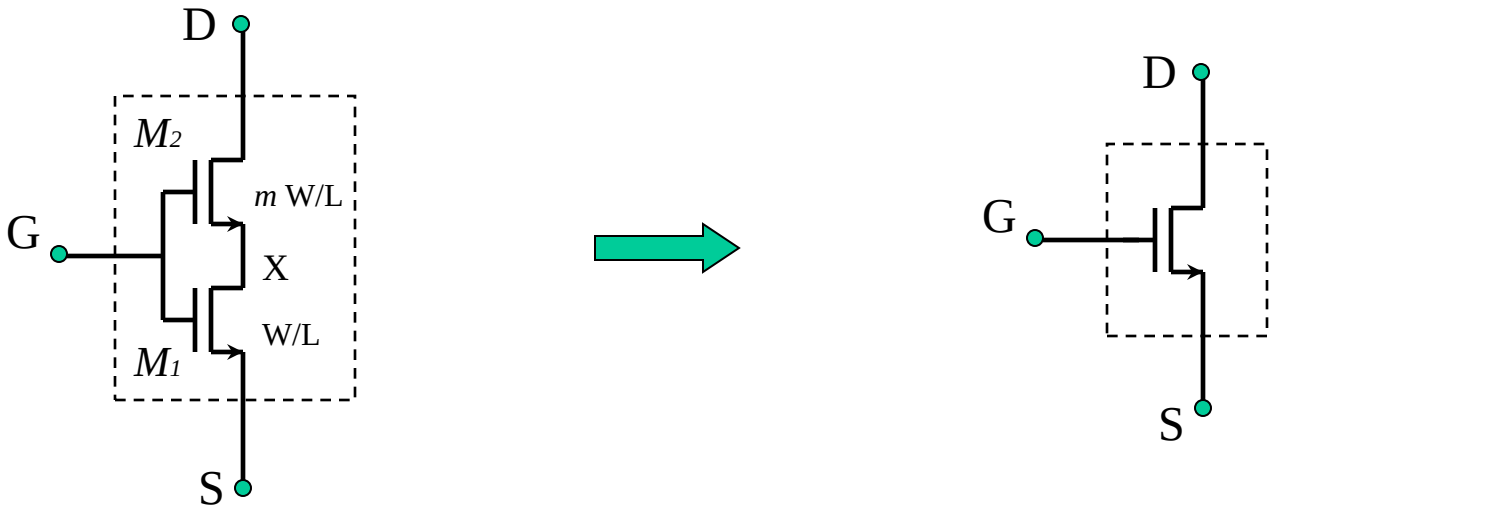
What is a Self-Cascode Composite Transistor?



(a) Self-Cascode Composite NMOS Transistor (b) Equivalent Simple Transistor

In practical cases, for optimal operation the W/L ratio of M_2 should be larger than that of M_1, *i.e.* $m>1$.

The 2-transistor structure can be treated as a composite transistor, which has a much larger effective channel length (thus lower output conductance).

Working Conditions [5]

For the composite transistor to function properly, both M_2 and M_1 should conduct, thus, the following conditions should be satisfied:

$$V_G - V_X - V_T > 0 \qquad (1)$$

$$V_G - V_S - V_T > 0 \qquad (2)$$

We can rewrite (1) as:

$$V_X - V_S < V_G - V_S - V_T = V_{DSAT} \qquad (3)$$

From (3) we know that transistor M_1 must be in linear region. Depending on the drain voltage, transistor M_2 can work in saturation region or linear region.

Equivalent Transistor Parameter (I)

For the composite transistor work in saturation region, we know M_2 should in saturation and M_1 is in linear region. Thus, we can write equations for these two transistors as:

$$i_1 = \frac{\beta_2}{2}(V_{GS} - V_X - V_T)^2 \qquad i_1 = \beta_1\left(V_{GS} - V_T - \frac{1}{2}V_X\right)V_X$$

Solving i_1 we can obtain:

$$i_2 = \frac{1}{2}\frac{\beta_2\beta_1}{\beta_2 + \beta_1}(V_{GS} - V_T)^2$$

From (3), we have $\beta_{eq} = \dfrac{\beta_2\beta_1}{\beta_2 + \beta_1}$

If $\beta_2 = m \cdot \beta_1$ $\qquad \beta_{eq} = \dfrac{m}{m+1}\beta_1 = \dfrac{1}{m+1}\beta_2$

$$\Rightarrow \quad \beta_{eq}\Big|_{m->\infty} = \beta_1$$

Comments on V_{DSAT}

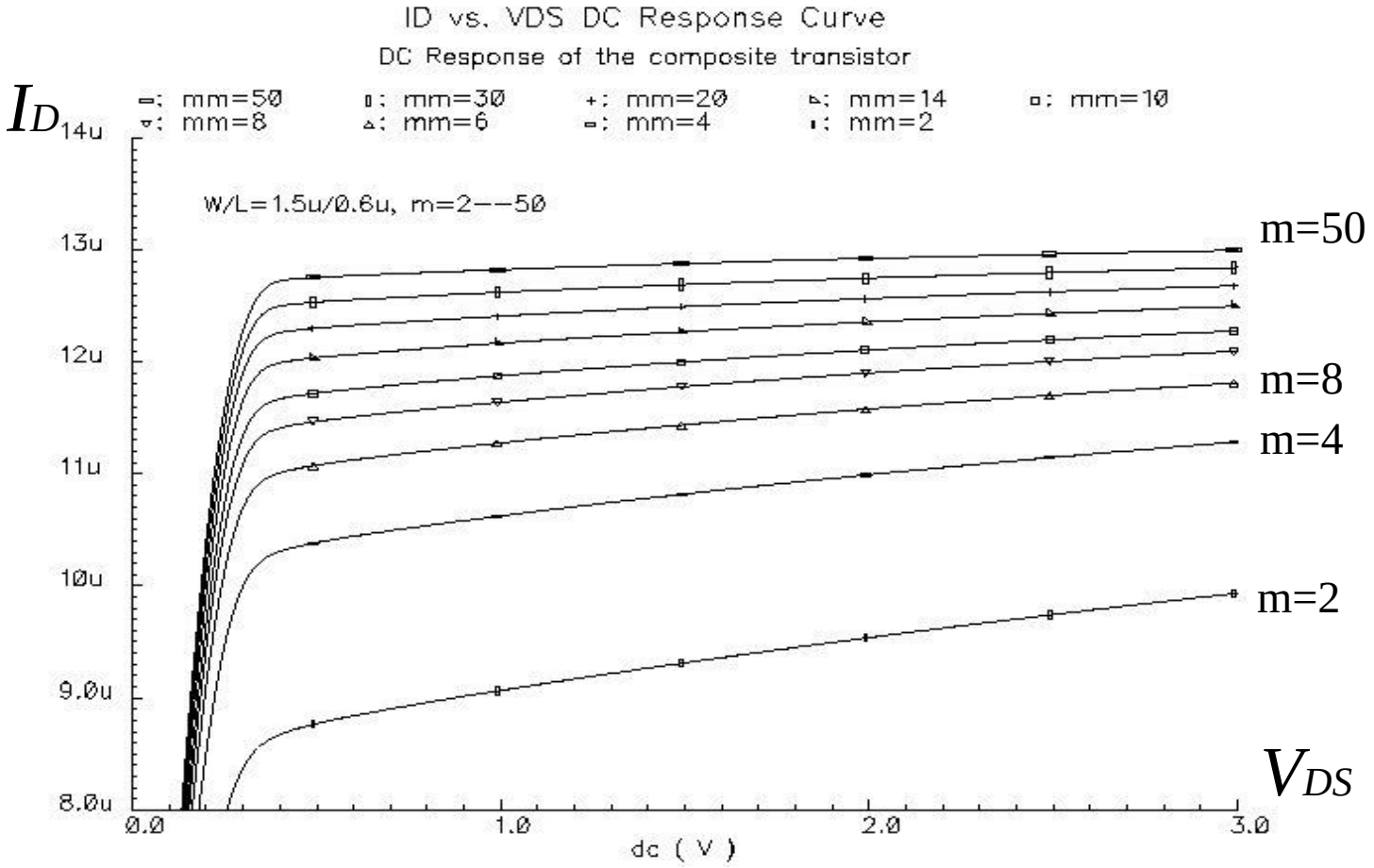
Because transistor M_1 always operates in linear region while the top transistor operates in saturation or linear region. Voltage between the source and drain terminal of M_1 is so small that there is no discernable V_{DSAT} difference in both the composite and simple transistors. Thus,self-cascode structure can be used in ***low voltage applications***.

$$V_{DSAT-eq} = V_{DSAT-M2} + V_{DS-M1} = V_{DSAT-M2} + I_{D2}R_{M1}$$

where $$R_{M1} = \frac{1}{\mu C_{OX}\left(V_{GS} - V_T\right)\frac{W}{L}}$$

The operating voltage of a regular cascode circuit is much higher than that of a single transistor. This characteristic makes regular cascode circuit not suitable for low voltage applications.

DC Simulation Results (I)



Effect of *"m"* on the output characteristics

DC Simulation Results (II)

From simulations (TMSC 0.35um process), we observe that:

m	W/L	Equivalent W/L
2	1.5/0.6	1.7/0.9
4	1.5/0.6	2.5/1.5
6	1.5/0.6	3.0/2.1
8	1.5/0.6	3.3/2.4
10	1.5/0.6	3.8/3.0
20	1.5/0.6	20/24

When *m* is larger, the effective length *L* is also larger

Equivalent (W/L)Transistor Parameter

Because β is proportional to W/L, we can have the equivalent W/L derived from previous results:

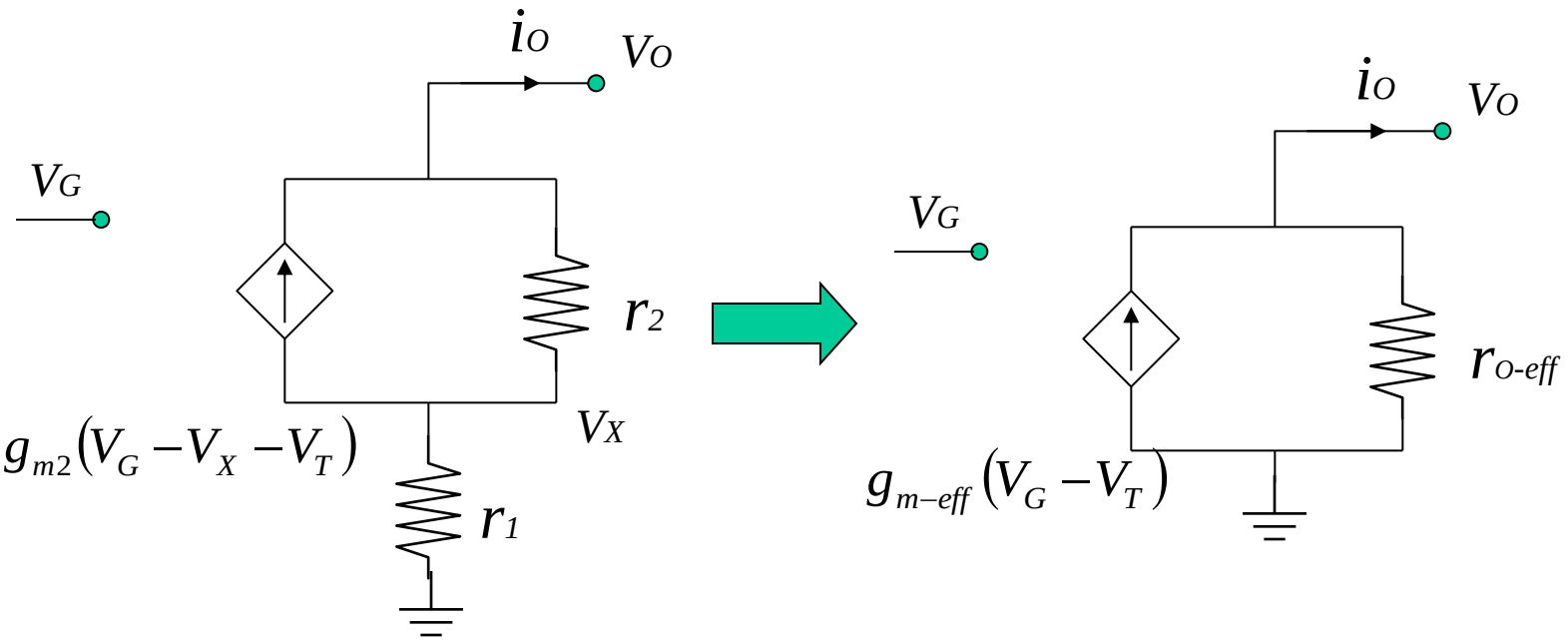
$$\left(\frac{W}{L}\right)_{eq} = \frac{\left(\frac{W}{L}\right)_2 \cdot \left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2 + \left(\frac{W}{L}\right)_1}$$

If lengths of M_2 and M_1 are equal, and M_2 is m times wider than M_1, the equivalent W/L ratio is:

$$\left(\frac{W}{L}\right)_{eq} = \frac{m}{m+1}\left(\frac{W}{L}\right)_1 = \frac{1}{m+1}\left(\frac{W}{L}\right)_2$$

Equivalent Output Impedance

(Low frequency small signal)

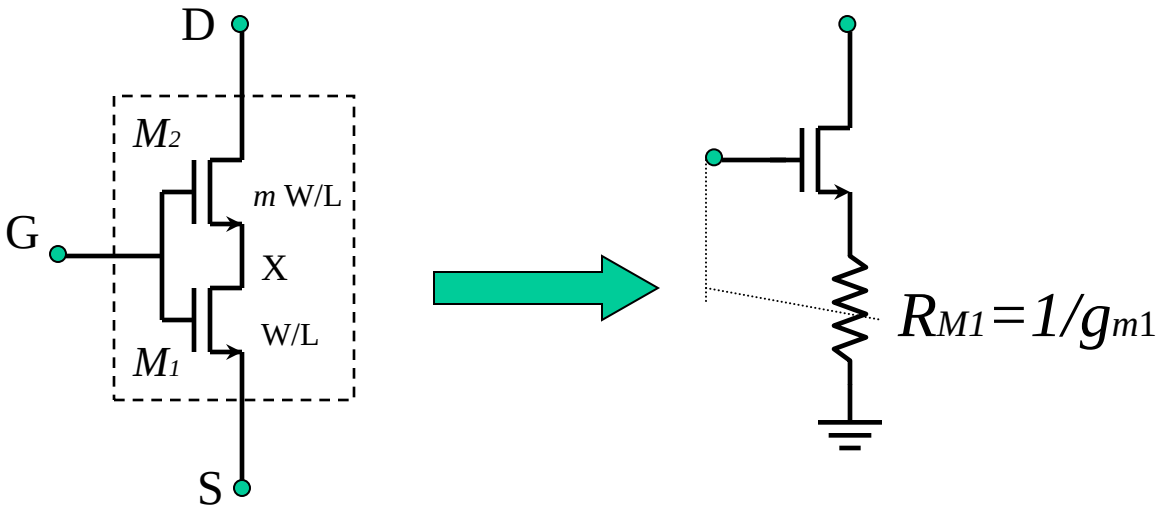


The equivalent output impedance of the composite transistor is:

$$r_o = g_{m2} r_2 r_1 - r_2 - r_1 \approx (g_{m2} r_1 - 1) r_2 = (m \cdot g_{m1} r_1 - 1) r_2 = (m-1) \cdot r_2$$

$$(m >> 1)$$

Effective Transconductance

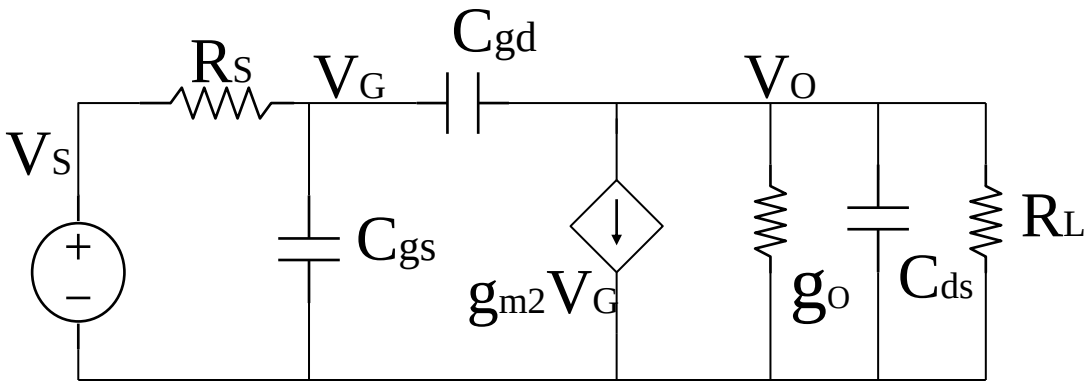


The lower transistor M_1 is equivalent to a resistor But this resistor is input dependent..

The effective transconductance of the composite transistor is approximately equal to the transconctance of M_1:

$$g_{m\text{-}eff}=g_{m2}/m=g_{m1}$$

Small-Signal Equivalent Circuit (Single Transistor)



$$A_V(s) = \frac{A_2 s^2 + A_1 s + A_0}{B_2 s^2 + B_1 s + B_0}$$

Equations:

$$\frac{V_G - V_S}{R_S} + V_G \cdot sC_{gs} + (V_G - V_O) \cdot s \cdot C_{gd} = 0$$

$$\frac{V_O}{R_L} + V_O \cdot g_O + V_O \cdot s \cdot C_{ds} + g_{m2} \cdot V_G + (V_O - V_G) \cdot s \cdot C_{gd} = 0$$

Solve this equation set we can obtain the voltage gain as a function of the frequency:

$$A_2 = (C_{gs}C_{gd} + C_{gs}C_{ds} + C_{ds}C_{gd}) \cdot R_L$$

$$A_1 = (g_{m1}C_{gd} + g_0C_{gd} + g_0C_{gs} + g_{m2}C_{gd}) \cdot R_L$$

$$A_0 = -g_{m1}g_{m2} \cdot R_L$$

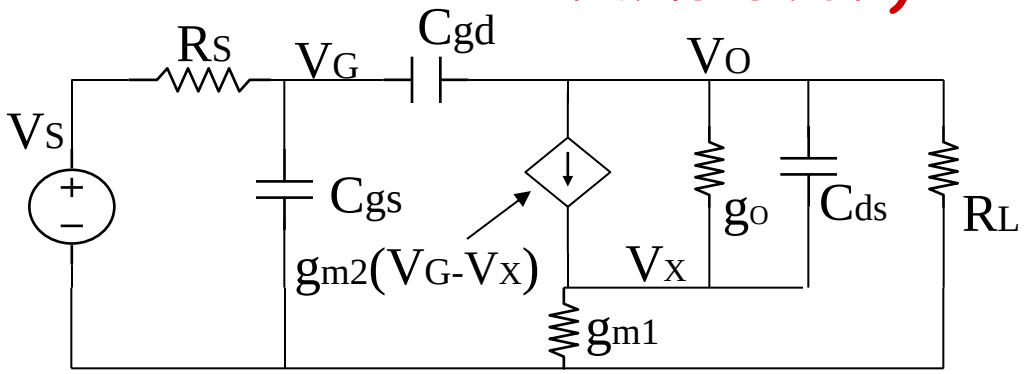
$$B_2 = (g_{m1}R_LR_S + R_L + R_S)(C_{gs}C_{ds} + C_{gs}C_{gd} + C_{ds}C_{gd})$$

$$B_1 = (C_{gs} + C_{ds}) + (C_{gd} + C_{ds}) \cdot g_{m1}R_L + (C_{gs} + C_{gd})(g_{m1}R_S + g_0R_Lg_{m1}R_S + g_0R_S + g_0R_L) + C_{gd}g_{m2}(R_L + R_S + g_{m1}R_LR_S)$$

$$B_0 = g_{m2} + g_0 + g_{m1} + g_{m1}R_Lg_0$$

This function has 2 poles and 2 zeros, but it is too complex!

Small-Signal Equivalent Circuit (Composite Transistor)



$$A_V(s) = \frac{A_2 s^2 + A_1 s + A_0}{B_2 s^2 + B_1 s + B_0}$$

Circuit Equations

$$(V_G - V_S)/R_S + V_G \cdot sC_{gs} + (V_G - V_O)\cdot s \cdot C_{gd} = 0$$

$$\frac{V_O}{R_L} + (V_O - V_X)\cdot(g_O + s\cdot C_{ds}) + g_{m2}\cdot(V_G - V_X) + (V_O - V_G)\cdot s \cdot C_{gd} = 0$$

$$V_X \cdot g_{m1} - g_{m2}\cdot(V_G - V_X) + (V_X - V_O)\cdot(g_O + s\cdot C_{ds}) = 0$$

Solving this equation set we can obtain the voltage gain as a function of the frequency:

$$A_2 = (C_{gs}C_{gd} + C_{gs}C_{ds} + C_{ds}C_{gd})\cdot R_L$$

$$A_1 = (g_{m1}C_{gd} + g_0 C_{gd} + g_0 C_{gs} + g_{m2}C_{gd})\cdot R_L$$

$$A_0 = -g_{m1}g_{m2}\cdot R_L$$

$$B_2 = (g_{m1}R_L R_S + R_L + R_S)(C_{gs}C_{ds} + C_{gs}C_{gd} + C_{ds}C_{gd})$$

$$B_0 = g_{m2} + g_0 + g_{m1} + g_{m1}R_L g_0$$

$$B_1 = (C_{gs} + C_{ds}) + (C_{gd} + C_{ds})\cdot g_{m1}R_L + (C_{gs} + C_{gd})(g_{m1}R_S + g_0 R_L g_{m1}R_S + g_0 R_S + g_0 R_L) + C_{gd}g_{m2}(R_L + R_S + g_{m1}R_L R_S)$$

Effect of the Capacitor C_{gd} (Simple)

Let's assume $C_{gs}=0$ $C_{ds}=0$ $R_L g_0 << 1$, thus

$$A_1 = C_{gd} R_L$$
$$A_0 = -g_{m2} R_L$$
$$A_2 = 0$$

$$B_2 = 0$$
$$B_1 = C_{gd} R_L R_S g_0 + C_{gd} \cdot R_L + (g_{m2} R_L + 1) R_S C_{gd}$$
$$\cong C_{gd} R_S g_{m2} R_L$$
$$B_0 = R_L g_0 + 1 \cong 1$$

The simplified transfer function is:

$$A_V(s) = \frac{A_1 s + A_0}{B_1 s + B_0}$$

This means that if we consider the effect of only C_{gd}, the function is simplified to one pole and one zero

One zero:

$$\omega_Z = \frac{g_{m2}}{C_{gd}}$$

One pole:

$$\omega_P = \frac{1}{g_{m2} R_L R_S C_{gd}}$$

Effect of the Capacitor C_{gd} (Composite)

Let's assume $C_{gs}=0$ $C_{ds}=0$ $R_L g_0 << 1$, thus

$$A_2 = 0$$

$$A_1 = \left(g_{m1}C_{gd} + g_0 C_{gd} + g_{m2}C_{gd}\right)\cdot R_L \cong \left(g_{m1}+g_{m2}\right)\cdot C_{gd}R_L$$

$$A_0 = -g_{m1}g_{m2}\cdot R_L$$

$$B_2 = 0$$

$$B_1 = C_{gd}\cdot\left(g_{m1}R_L + g_{m1}R_S + g_0 R_L g_{m1}R_S + g_0 R_S + g_0 R_L + g_{m2}R_L + g_{m2}R_S + g_{m1}g_{r}\right.$$

$$\cong C_{gd}g_{m2}R_L\cdot\left(1+g_{m1}R_S\right)$$

$$B_0 = g_{m2} + g_0 + g_{m1} + g_{m1}R_L g_0 \cong g_{m2}$$

The simplified transfer function is:

$$A_V(s) = \frac{A_1 s + A_0}{B_1 s + B_0}$$

One zero:

$$\omega_Z = \frac{g_{m1}g_{m2}}{\left(g_{m1}+g_{m2}\right)C_{gd}} \cong \frac{g_{m1}}{C_{gd}}$$

One pole:

$$\omega_P = \frac{1}{\left(1+g_{m1}R_S\right)R_L C_{gd}} \cong \frac{1}{g_{m1}R_S R_L C_{gd}}$$

Comments on the Poles and Zeros

Consider the effect of C_{gd} only, we can get the following conclusion:

The pole of the simple transistor is higher than that of the composite transistor.

$$\frac{\omega_{Z-Composite}}{\omega_{Z-Simple}} = \frac{g_{m1}}{g_{m2}} = \frac{1}{m}$$

The same conclusion can be applied to zeros:

$$\frac{\omega_{P-Composite}}{\omega_{P-Simple}} = \frac{g_{m1}}{g_{m2}} = \frac{1}{m}$$

Frequency Parameters

The transition time τ increases as the value of *m*.
According to reference[1], The relationship is:

$$\tau \cong \tau_u \left(1+\sqrt{1+m}\right)$$

Where τ_u is the transition time of an unit transistor used in the self-cascode structure.

For the saturated MOS transistor in strong inversion parameters ω_T (Cutoff frequency) and τ are related by:

$$\tau\omega_T = 2$$

Advantage of the Self-Cascode Structure

The main advantage of this structure is smaller transistor area. The sum of areas of M_D and M_S is smaller than the area of the equivalent simple transistor.

The table below shows the simulation results with MOSIS TSMC 0.35u CMOS process:

MS W/L	m	MD W/L	Equivalent FET W/L	Area Ratio*	Gain (RL=inf.)
3.0/0.6u	3	9.0u/0.6u	5.6u/1.2u	7.2/6.72	42dB
3.0u/0.6u	8	24.0u/0.6u	38.5u/12.0u	16.2/462.0	47dB
1.5u/0.6u	11	16.5u/0.6u	9.9u/12.0u	10.8/118.8	44dB

* COMPOSITE/SINGLE

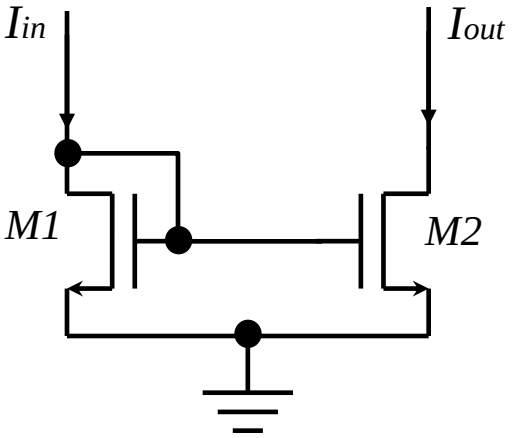
For equal chip area:

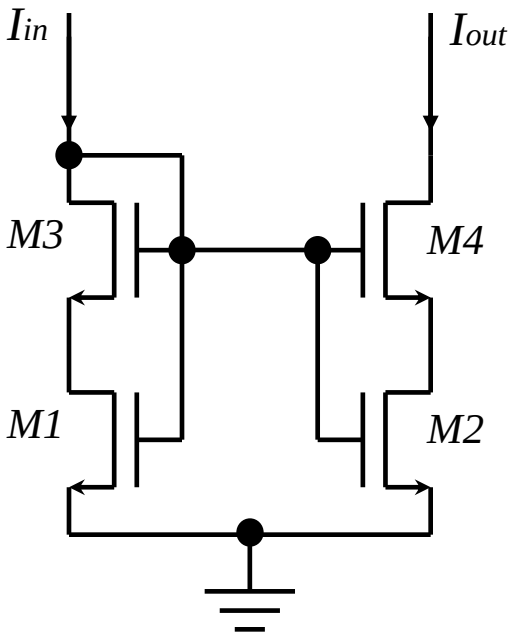
$$A_{V-CASCODE} > A_{V-SELF-CASCODE} > A_{V-SIMPLE-TRANSISTOR}$$

To achieve the same voltage gain:

$$AREA_{CASCODE} < AREA_{SELF-CASCODE} < AREA_{SIMPLE-TRANSISTOR}$$

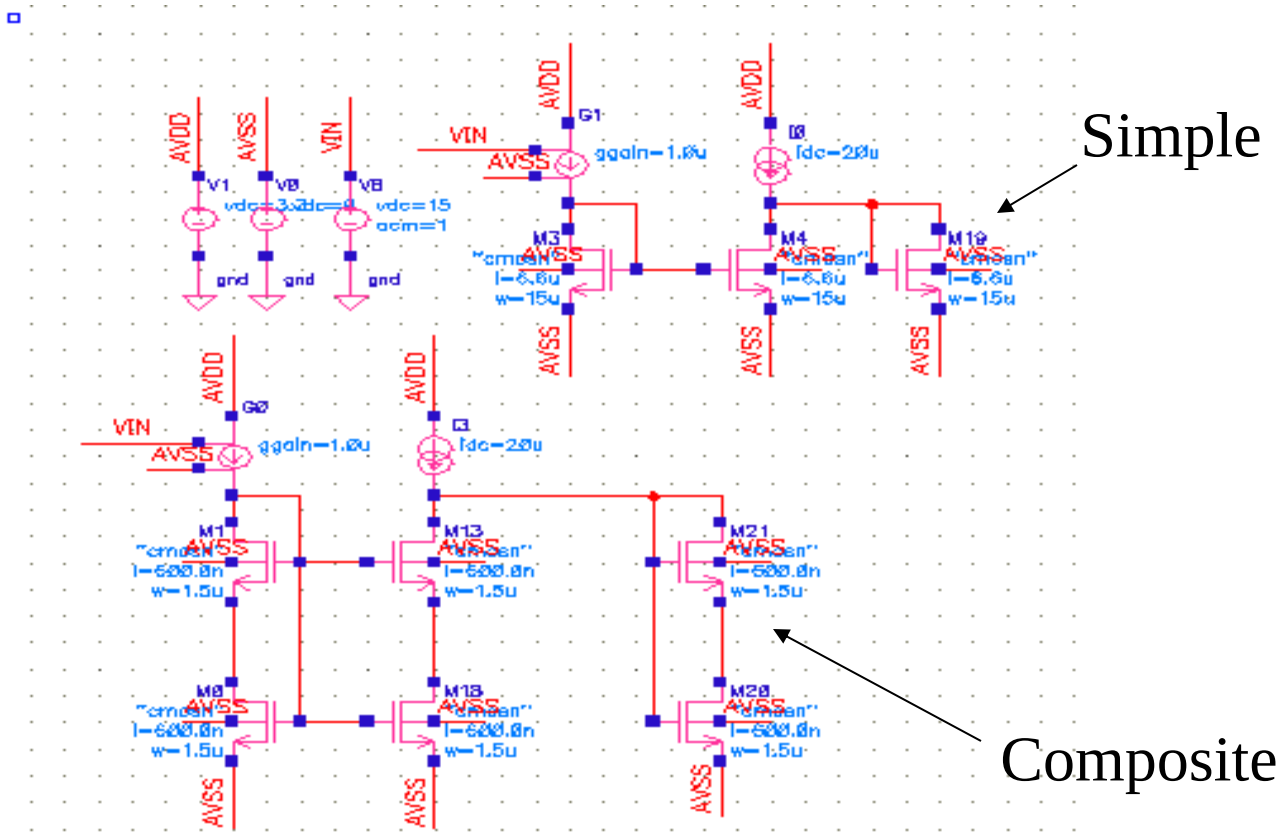
Applications (I)--Current Mirror





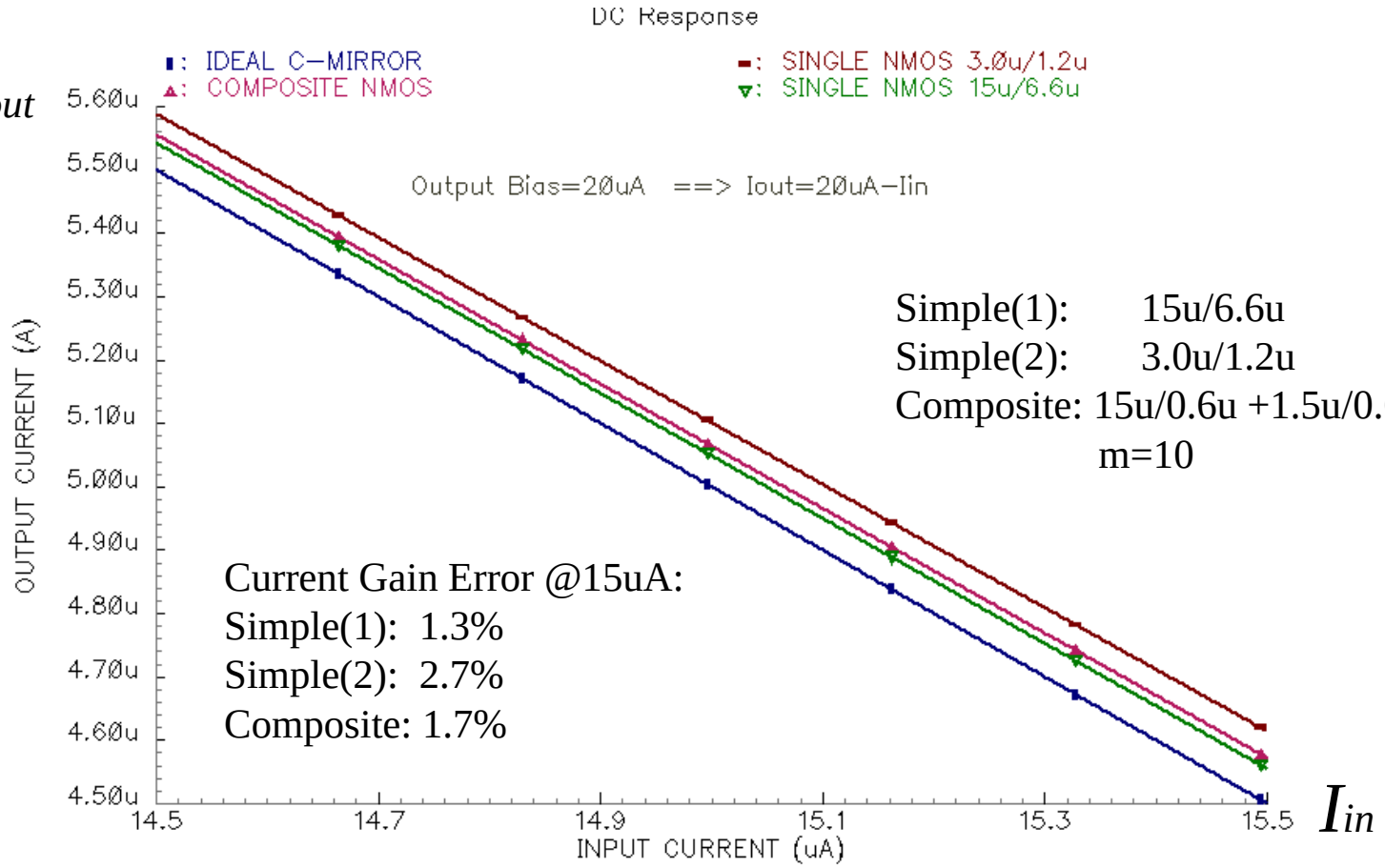
Simple transistors can be substituted with self-cascode structure to achieve better performance. (i.e. higher output impedance)

Schematic of the Circuit for Simulation



Model: TMSC 0.35um CMOS Process

Current Mirror Simulation Results (DC)



$20\text{-}I_{out}$

I_{in}

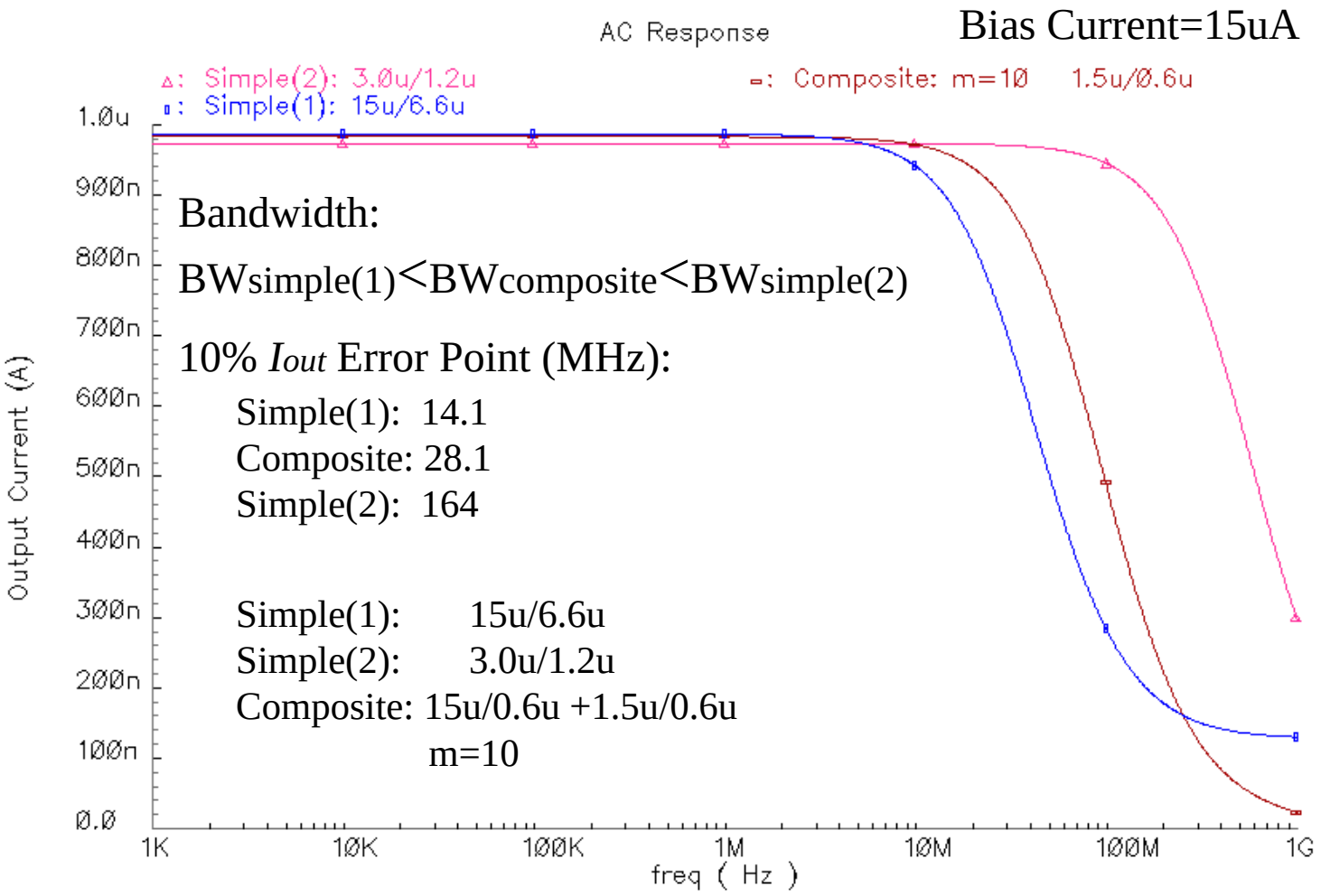
Simple(1): 15u/6.6u
Simple(2): 3.0u/1.2u
Composite: 15u/0.6u +1.5u/0.6u
m=10

Current Gain Error @15uA:
Simple(1): 1.3%
Simple(2): 2.7%
Composite: 1.7%

g_0/g_m:
Simple(1): 3.5e-3
Simple(2): 7.3e-3 (smaller = better)
Composite: 4.2e-3

Current Mirror Simulation Results (AC)

Bias Current=15uA



Bandwidth:

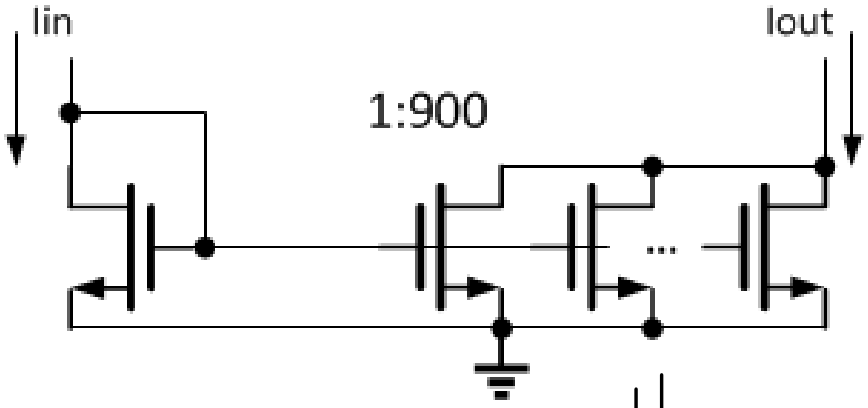
BWsimple(1)<BWcomposite<BWsimple(2)

10% *Iout* Error Point (MHz):

Simple(1): 14.1
Composite: 28.1
Simple(2): 164

Simple(1): 15u/6.6u
Simple(2): 3.0u/1.2u
Composite: 15u/0.6u +1.5u/0.6u
m=10

Application (I) – Current Mirrors



Traditional Current Mirror

Huge Area (**901T**)

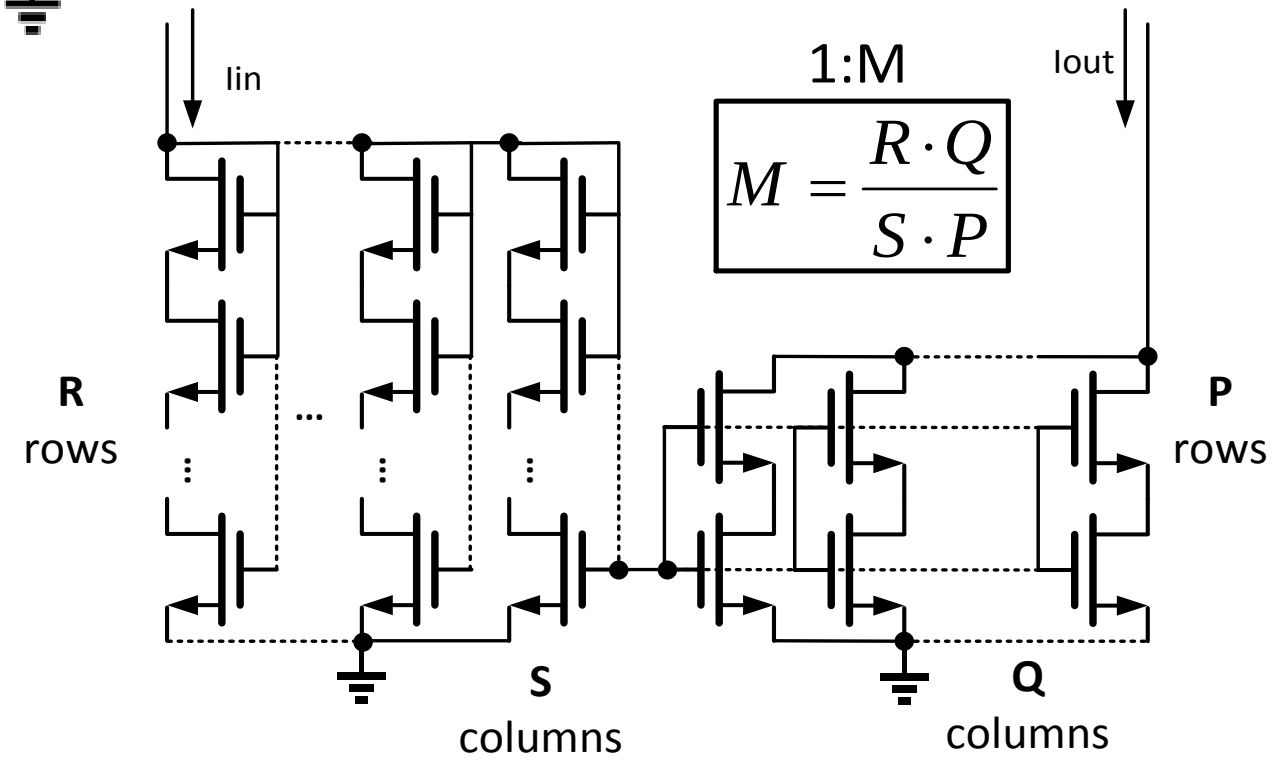
Series-Parallel Current Mirror

Ex. R = 30, S = 1

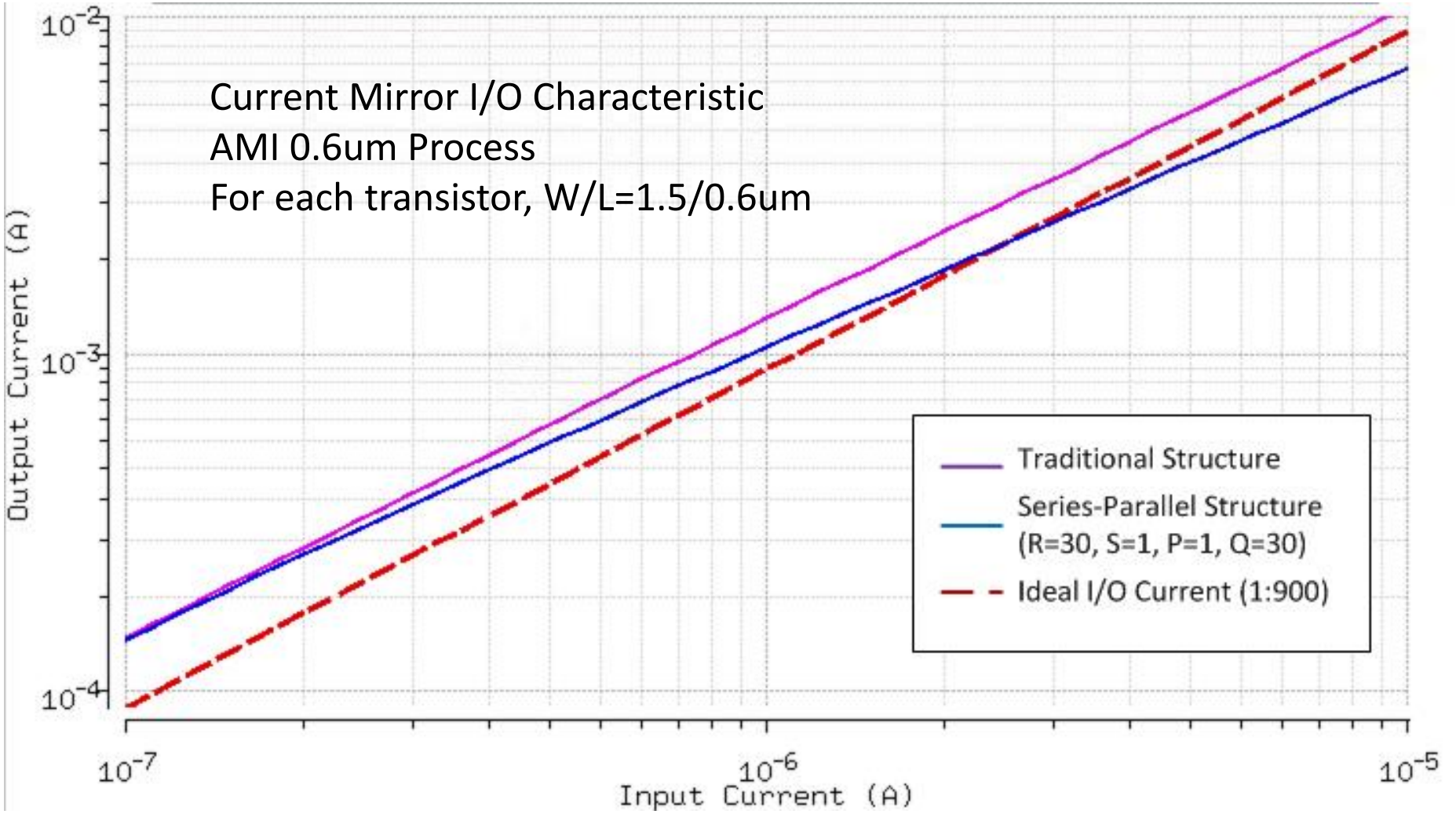
Q = 30, P = 1

Ratio: 1:900

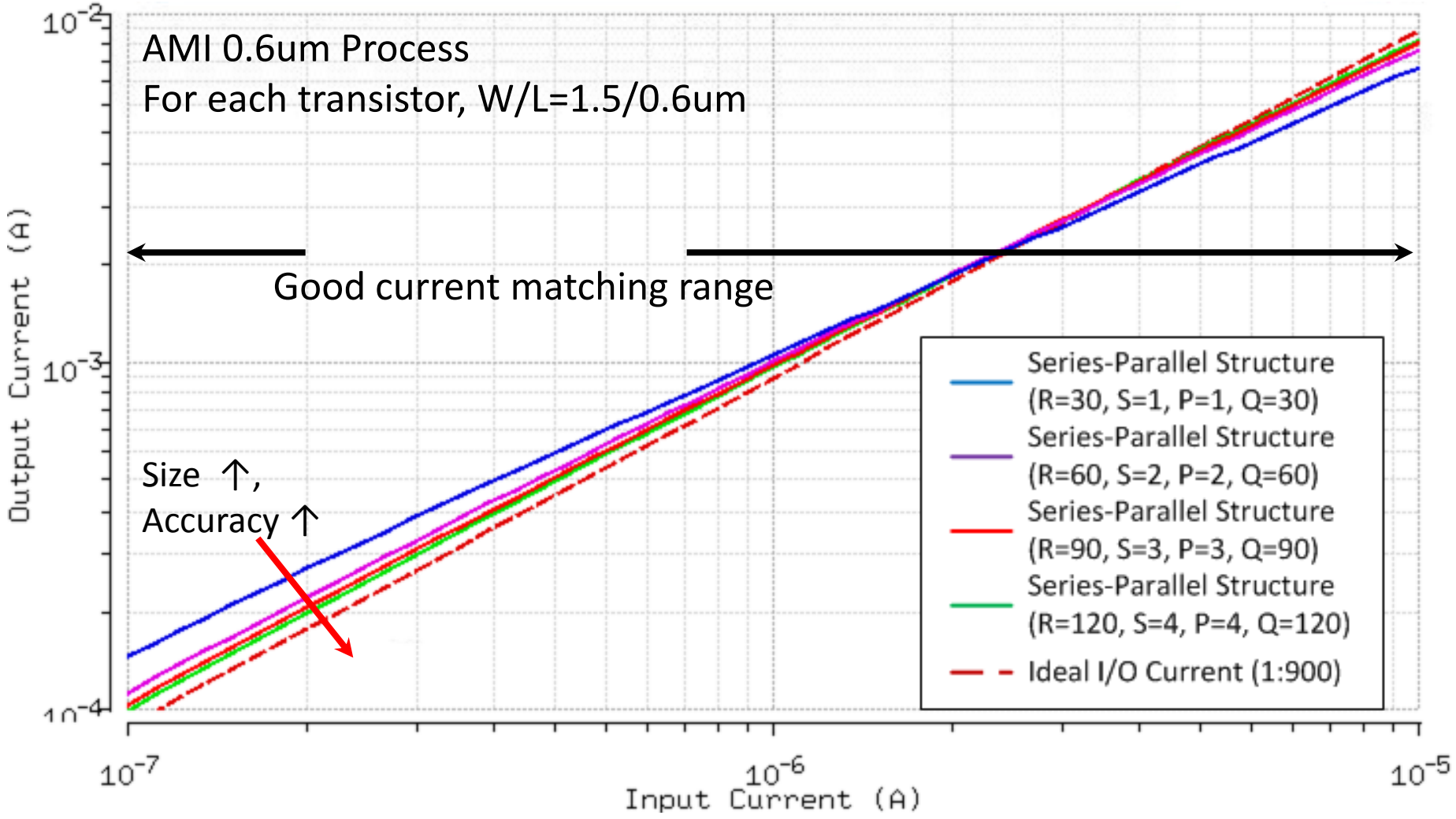
Area: **60T**



Traditional vs. Series-Parallel



Series-Parallel Current Mirror



Compare Current Mirrors

Series-Parallel current mirror improves the output impedance

	R	S	P	Q	M	Area	Input Imp.	Output Imp.
Trad.	1	1	1	900	900	901T	**71.5K**	4.0K
Series-Parallel	30	1	1	30	900	**60T**	356.8K	12.4K
	60	2	2	60	900	240T	357.3K	20.7K
	90	3	3	90	900	540T	357.5K	28.8K
	120	4	4	120	900	960T	357.6K	**36.8K**

Output Impedance Comparison

Input Current = **1uA**, Ratio = 1:900

Compare Current Mirrors

	R	S	P	Q	M	Area	Input Imp.	Output Imp.
Trad.	1	1	1	900	900	901T	**19.1K**	800
Series-Parallel	30	1	1	30	900	**60T**	155.4K	4.3K
	60	2	2	60	900	240T	154.4K	4.8K
	90	3	3	90	900	540T	154.1K	5.5K
	120	4	4	120	900	960T	154.1K	**6.2K**

Output Impedance Comparison

Input Current = **10uA**, Ratio = 1:900

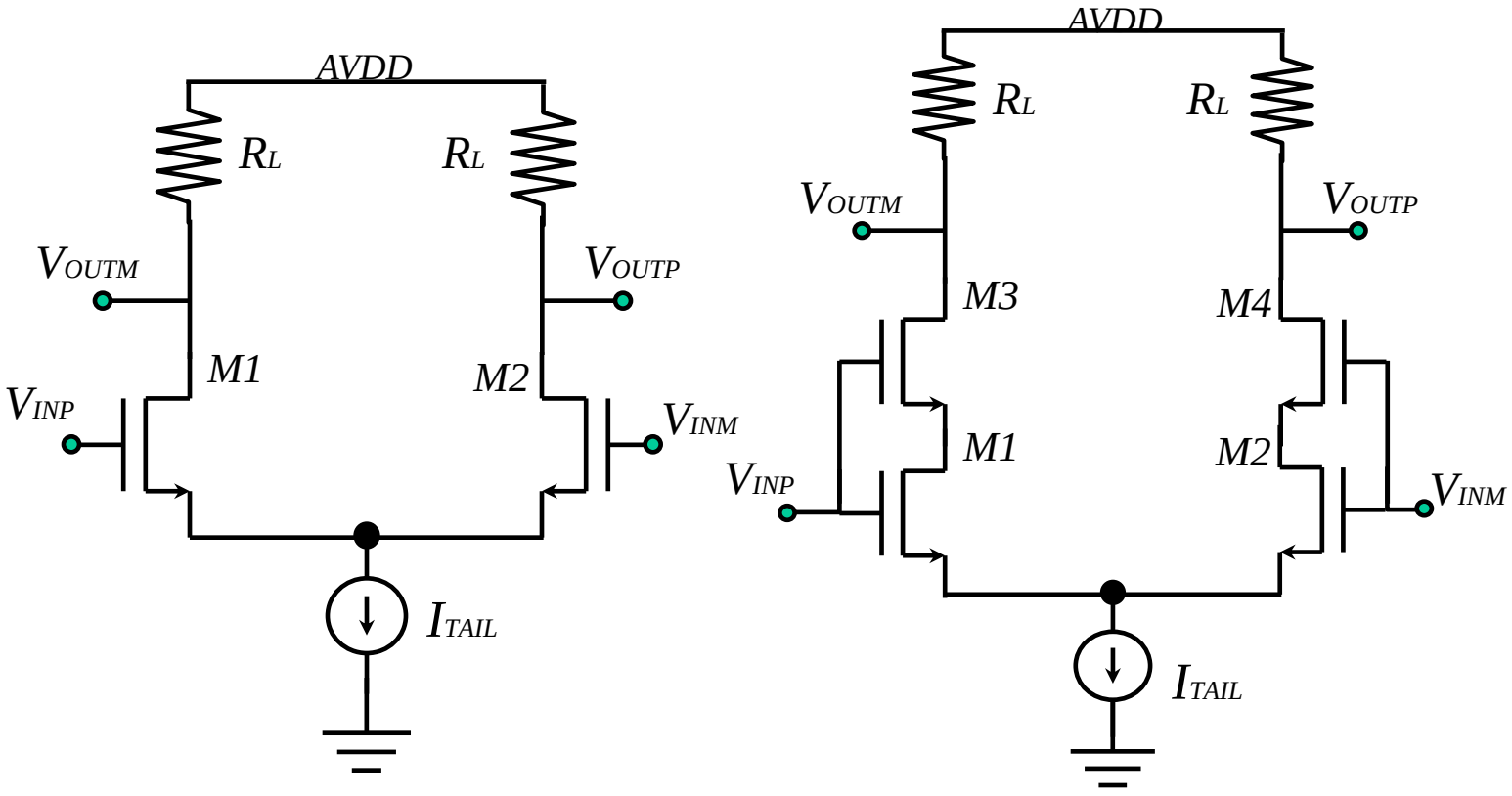
Voltage Swing

Stacked transistors limit the output swing of S-P current mirror

	R	S	P	Q	Output Vdsat (Iin=1uA)	Output Vdsat (Iin=10uA)
Trad.	1	1	1	900	**89mV**	**245mV**
Series-Parallel	30	1	1	30	441mV	1.4V
	60	2	2	60	303mV	1.0V
	90	3	3	90	244mV	830mV
	120	4	4	120	210mV	720mV

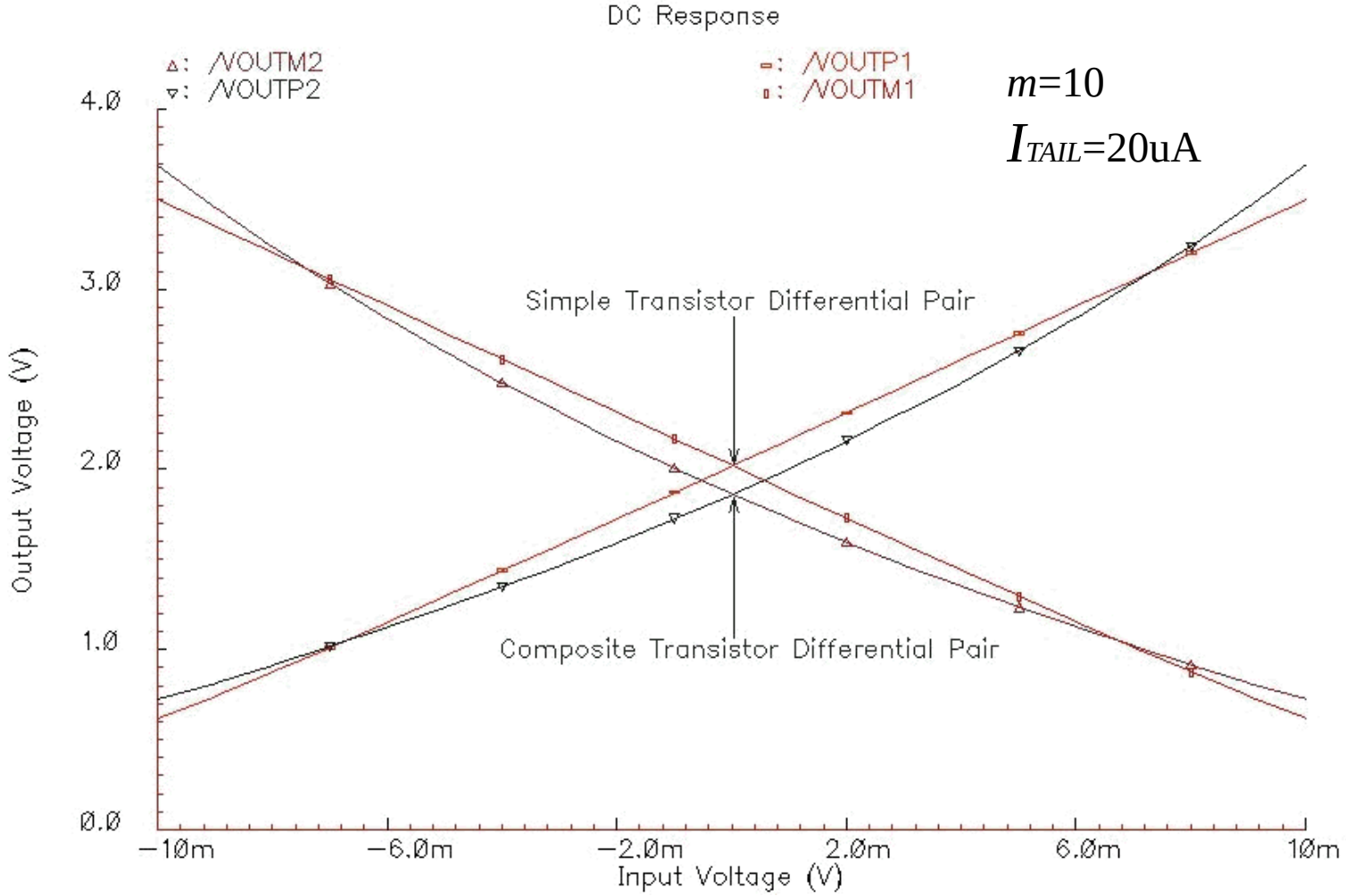
Vdsat (equivalent) of the output transistor reveals the max swing of the output voltage

Applications (II)--Differential Pair



Composite transistors can replace single transistors in a differential pair. Through self-cascode structure, higher voltage gain can be achieved.

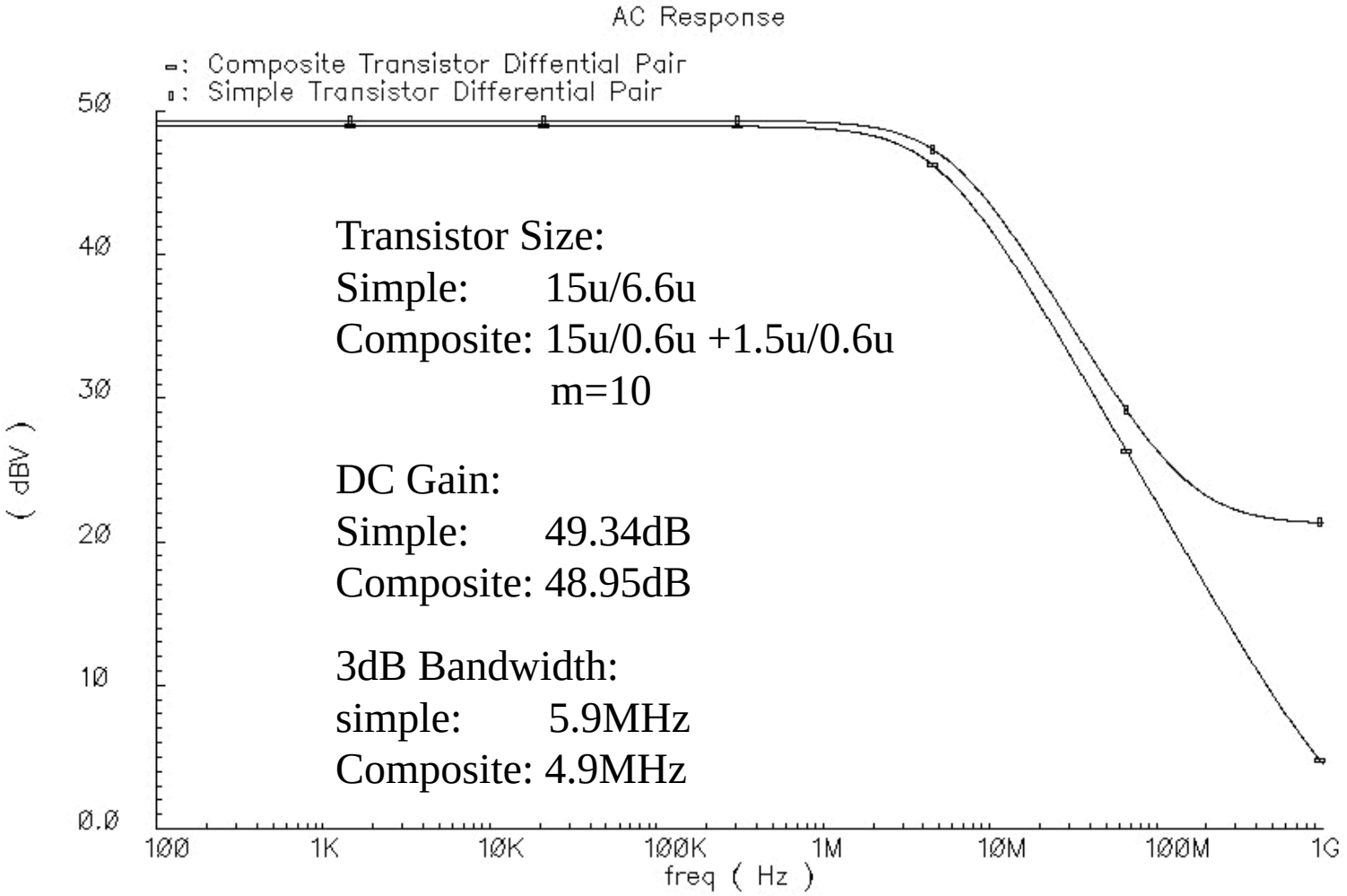
Differential Pair Simulation Results (DC)



m=10

I_{TAIL}=20uA

Differential Pair Simulation Results (AC)



Transistor Size:
Simple: 15u/6.6u
Composite: 15u/0.6u +1.5u/0.6u
m=10

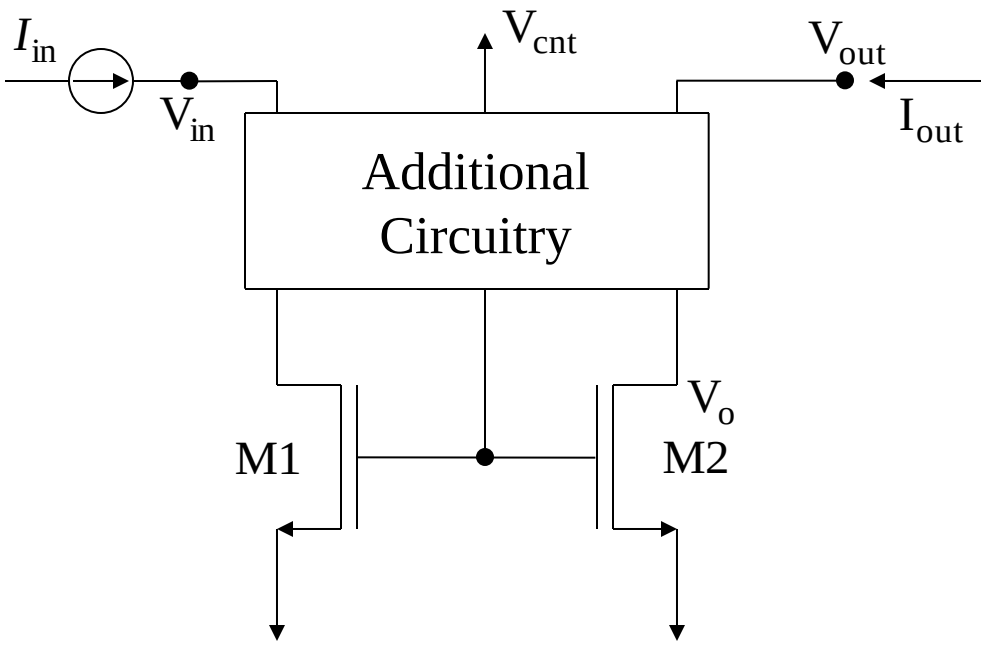
DC Gain:
Simple: 49.34dB
Composite: 48.95dB

3dB Bandwidth:
simple: 5.9MHz
Composite: 4.9MHz

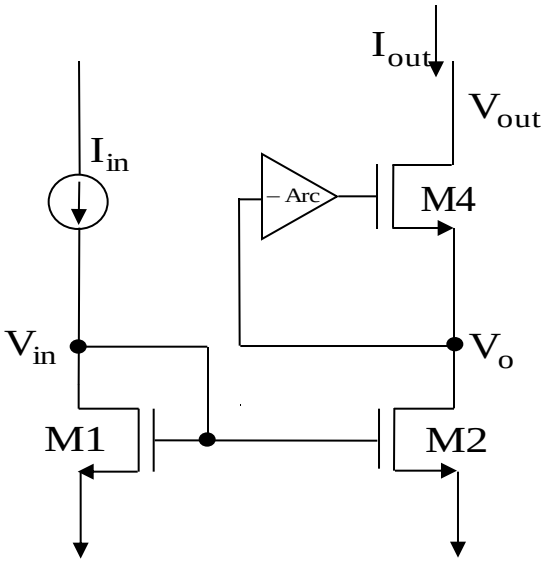
References

1. C. Galup-Montoro, etc., “Series-Parallel Association of FET’s for High Gain and High Frequency Applications”, *IEEE JSSC*, Sept. 1994
2. D. Ceuster, etc., “Improvement of SOI MOS current-mirror performances using serial-parallel association of transistors”, *Electronics Letters*, Feb. 1996
3. P. Furth, H. Om’mani, “A 500-nW Floating-Gate Amplifier with Programmable Gain”, IEEE 1999
4. I. Fujimori, T. Sugimoto, “A 1.5V, 4.1mW Dual-Channel Audio Delta-Sigma D/A Converter”, *IEEE JSSC*, Dec. 1998
5. Personal note from Dr. Ugur Cilingiroglu
6. Yunchu Li, examples and SPICE tables

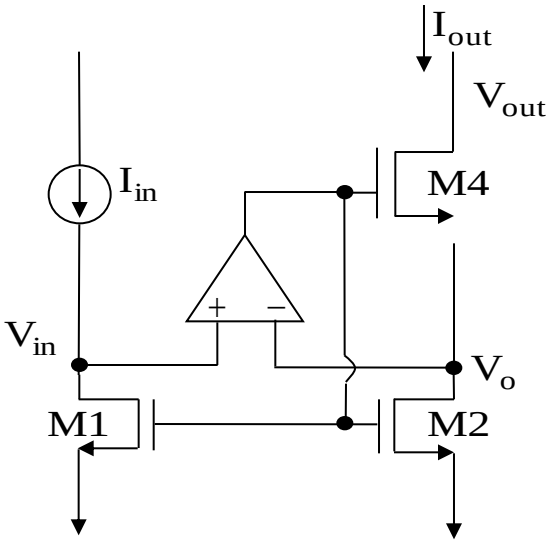
LOW VOLTAGE CURRENT-MIRRORS



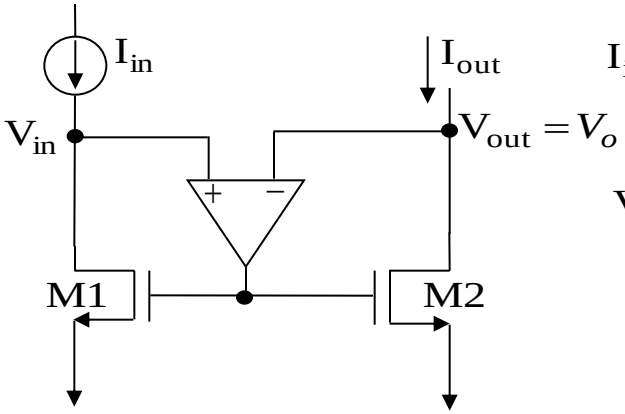
General scheme for high-performance current mirror structure.



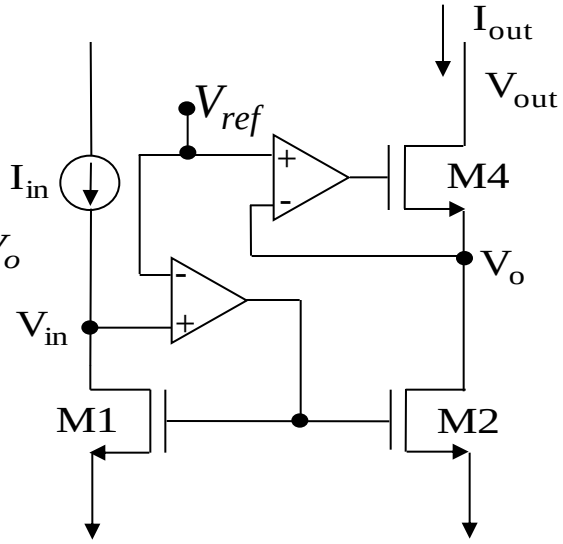
(a)



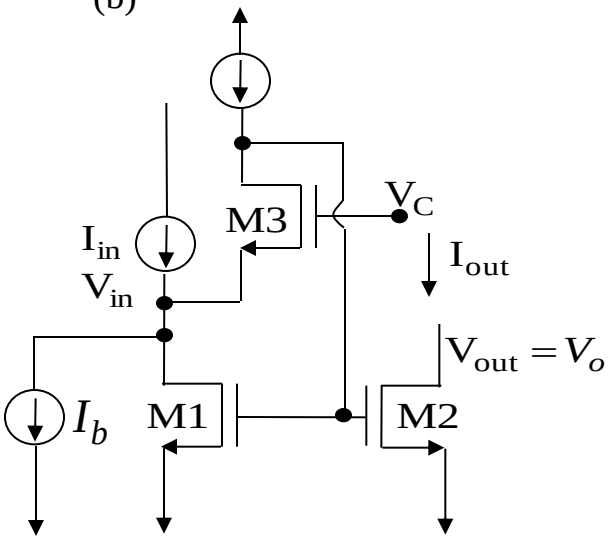
(b)



(c)



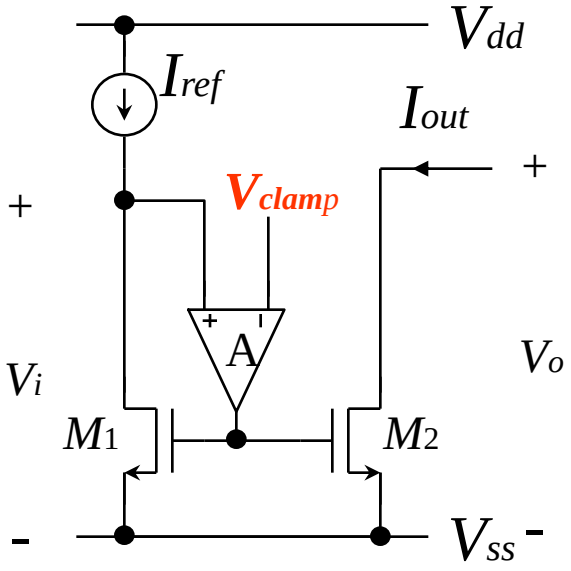
(d)



(e)

High-performance current mirrors:

Conventional active-input current mirror



$$V_{i\min} = \max\left(\frac{V_{DSAT1} + V_T}{A} + V_{Clamp}, V_{DSAT1}\right)$$

$$V_{0\min} = V_{DSAT2}$$

$$R_{in} \approx \frac{1}{A \cdot g_{m1}}$$

$$R_{out} \approx \frac{1}{g_{o2}}$$

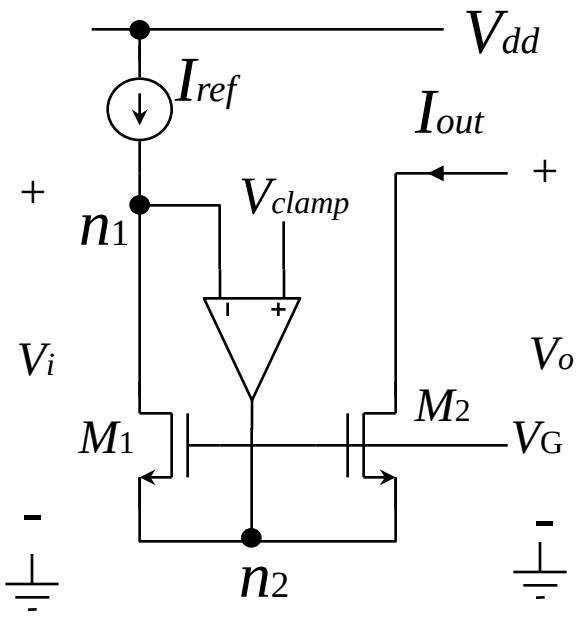
Advantage:

- Lower input impedance

Disadvantage:

- To achieve stability, g_{m1} can not be arbitrarily small. Thus, can not work over a wide current range.
- Compensation of the amplifier depends on the value of *Iref*.

Improved active input current mirrors (I)



Advantage:

This current mirror can operate over a very wide range of currents: from values equal to junction leakage currents up to the maximum current the OTA might be able to sink.

Disadvantage:

- Additional compensation capacitor between $n1$ and $n2$ may required to achieve stability
- The OTA must be able to sink twice the maximum expected value for I_{ref}, which imposes an important design constraint for the OTA.

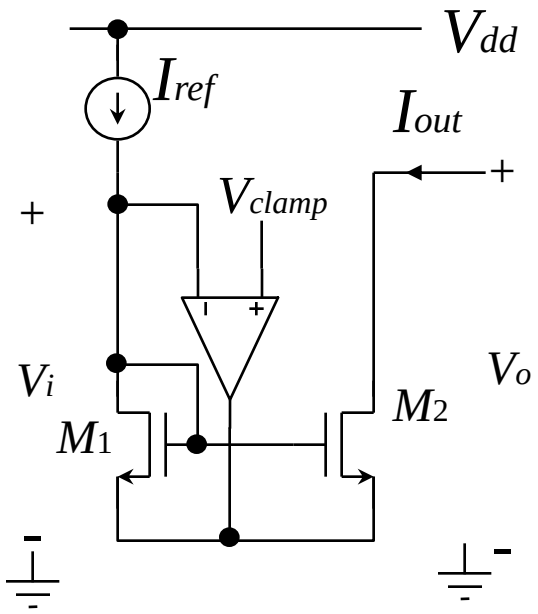
$$V_{i\min} = \max\left(\frac{V_T + V_{DSAT} - V_G}{A} + V_{clamp}, \frac{V_{DSAT} + A \cdot V_{clamp}}{A+1}\right)$$

$$V_{0\min} = V_{DSAT2}$$

$$R_{in} \approx \frac{1}{A \cdot g_{m1} + (1+A) \cdot g_{o1}} \approx \frac{1}{A \cdot g_{m1}}$$

$$R_{out} \cong \frac{1}{g_{o2}}$$

Improved active input current mirrors (II)



Advantage:

- This current mirror can operate over a very wide range of currents: from values equal to junction leakage currents up to the maximum current the OTA might be able to sink.
- If the differential voltage amplifier is already compensated for unity gain feedback, the circuit is always stable.

Disadvantage:

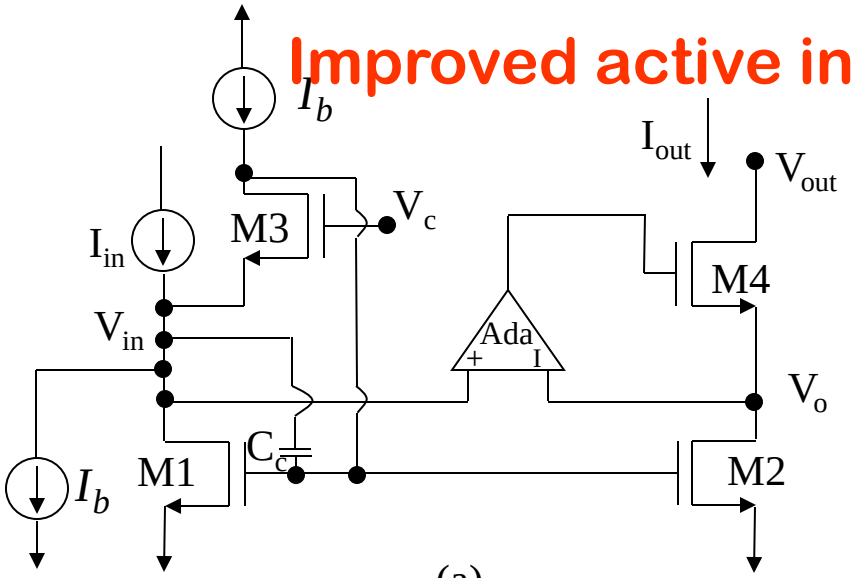
- Higher power supply may be required for amplifier
- More chip area and power consumption

$$V_{i\min} = \frac{V_{DSAT1} + V_T + A \cdot V_{clamp}}{A+1}$$

$$R_{in} \approx \frac{1}{(1+A)\cdot(g_{m1}+g_{o1})} \approx \frac{1}{(1+A)\cdot g_{m1}}$$

$$R_{out} \approx \frac{1}{g_{o2}}$$

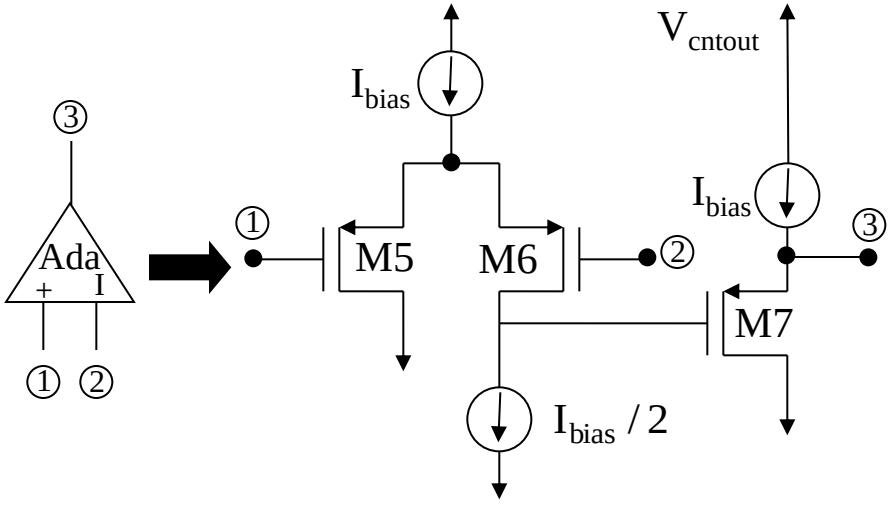
Improved active input current mirrors (III)



(a)

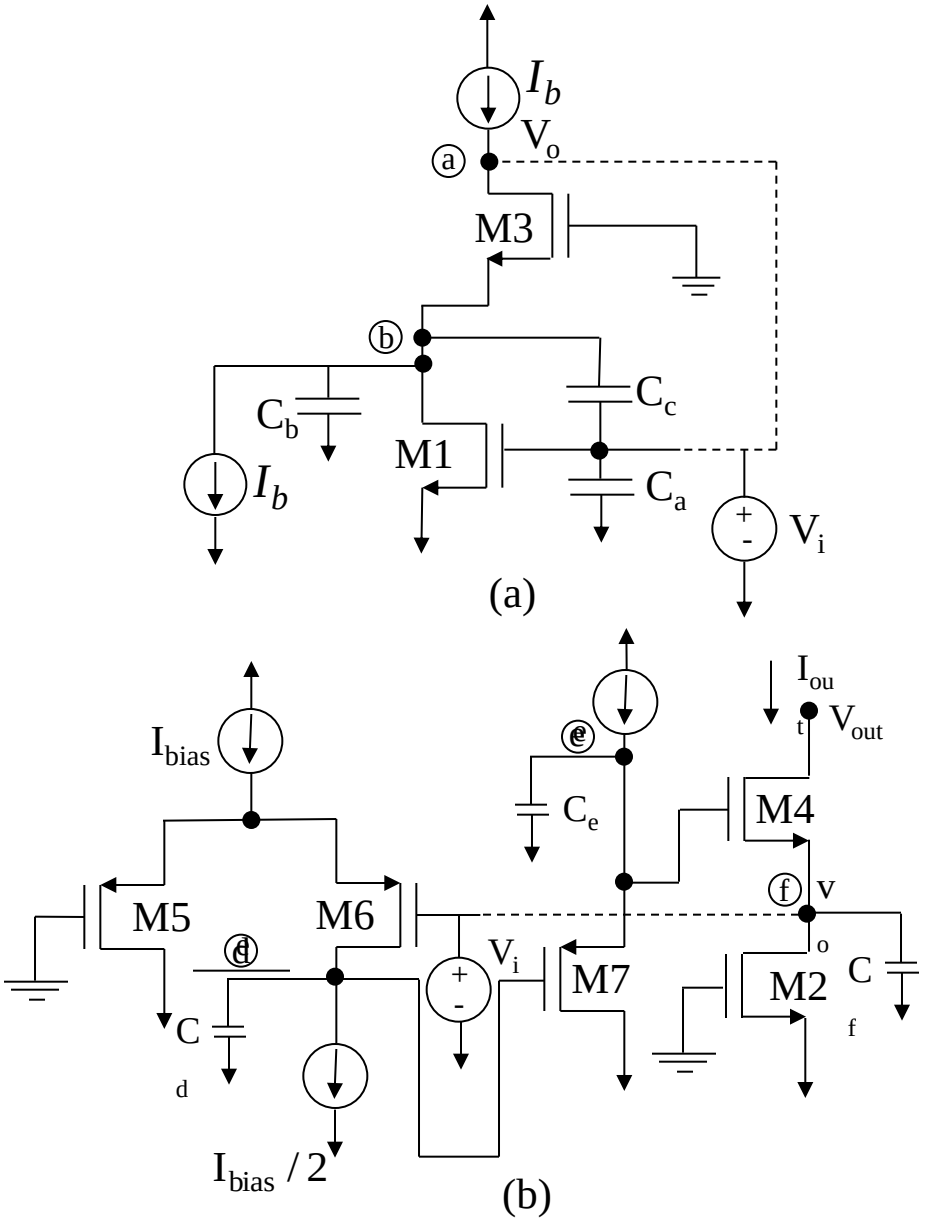
$$V_{OUT} > 2V_{DSAT}^{Q} + V_{oV}^{MAX}$$

$$V_{CNOUT}^{MIN} \cong \left|V_{tp}\right| + 3V_{DSAT}^{Q} + V_{oV}^{MAX}$$



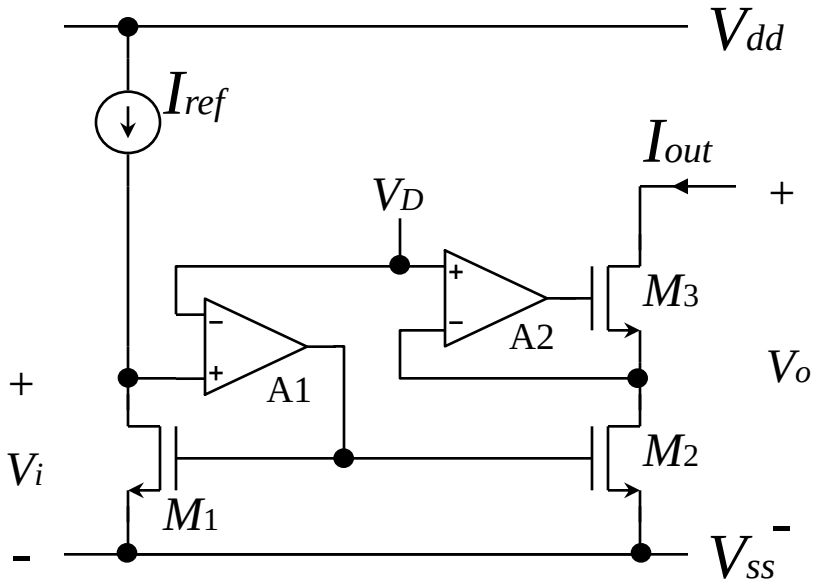
(b)

(a) Proposed low-voltage high-performance current mirror.
(b) Implementation of the differential amplifier A_{da}.



Open-loop response analysis: (a) input side and (b) output side.

Active regulated cascode current mirror



$$V_{i\min} = \max\left(\frac{V_T + V_{DSAT}}{A1} + V_D, V_{DSAT}\right)$$

$$V_{o\min} = 2V_{DSAT}$$

$$R_{in} \approx \frac{1}{A1 \cdot g_{m1}}$$

$$R_{out} = \frac{g_{m3}(1 + A2)}{g_{o3}g_{o2}}$$

Advantages:

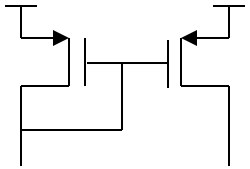
- High output impedance
- Low input impedance

Disadvantages:

- Poles and zeros may cause unstability
- more power and area

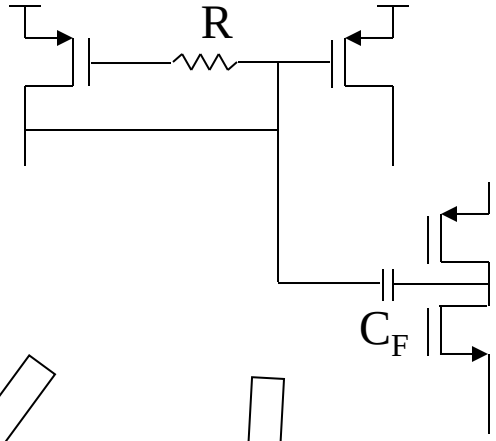
Techniques for Wideband Amplifiers

Conventional



CM

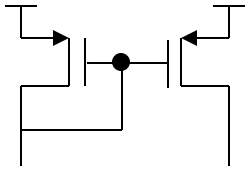
Wideband Alternative



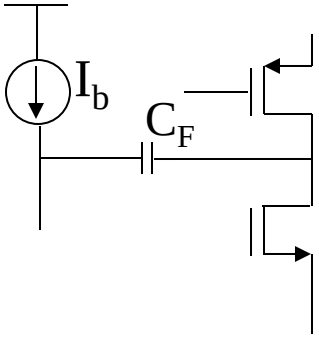
Frequency Dependent Current Mirror (FDCM)

$C_F >> Cgs$

$0.1K < R < 1K$



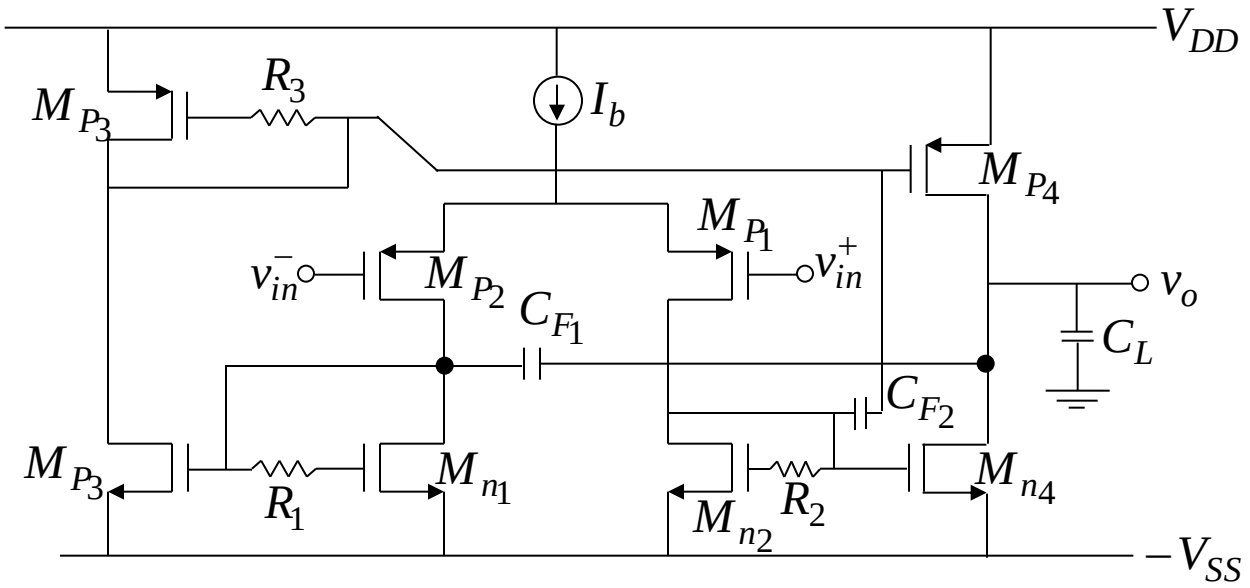
Low Frequency Behavior



High Frequency Behavior

T. Itakura and T. Iida, "A Feedforward Technique with Frequency-Dependent Current Mirrors for a Low-Voltage Wideband Amplifier," *IEEE J. Solid-State Circuits*, Vol. 31, No.6, pp. 847-849, June 1996.

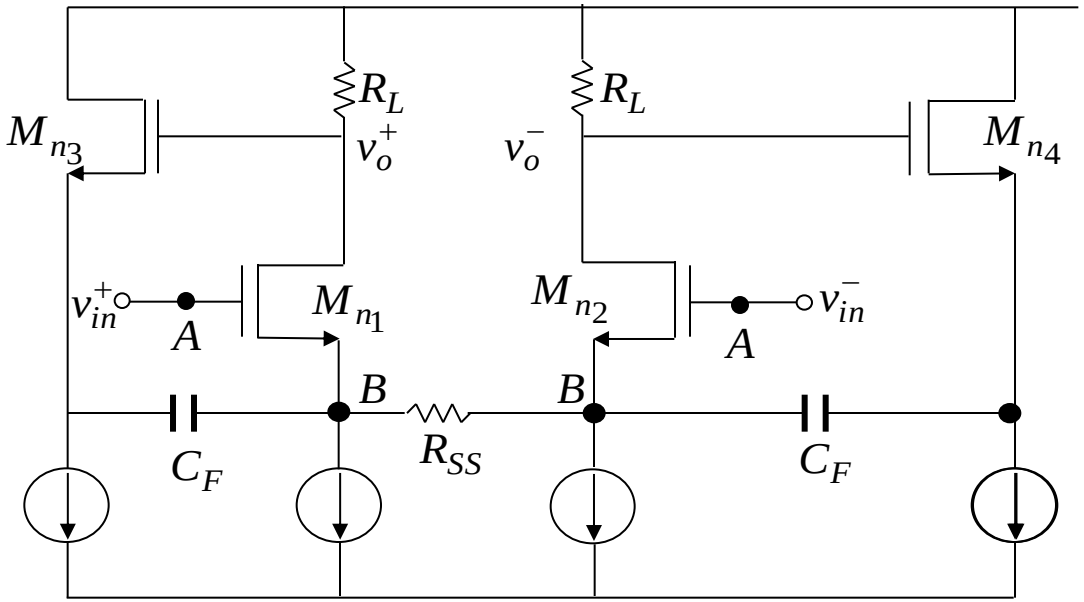
An example of its use:



Wideband Amplifier with Feedforward Technique

- C_{F1} by passes two current mirrors.
- C_{F2} is fed forward to the input of another FDCM and signal is amplified.

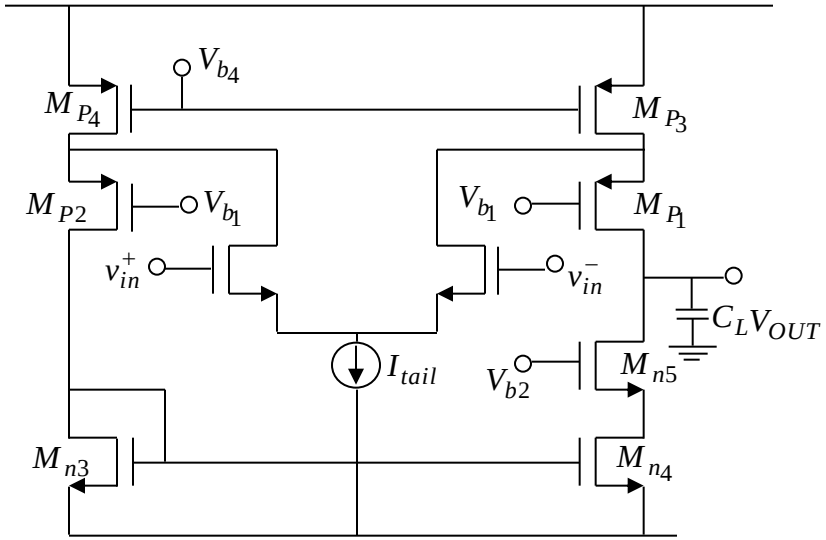
Next, we discuss different families of wideband reported in the literature.



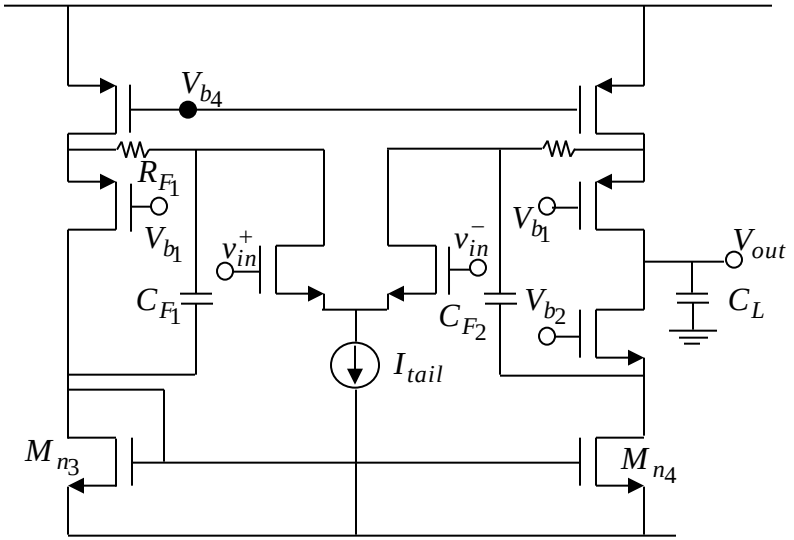
- An alternative is to connect C_F instead to nodes B to nodes A

F. Centurelli et al, "A Bootstrap Technique for Wideband Amplifiers," *IEEE Trans. on Circuits And Systesm – I*, Vol. 49, No. 10, pp. 1474-1480, October 2002

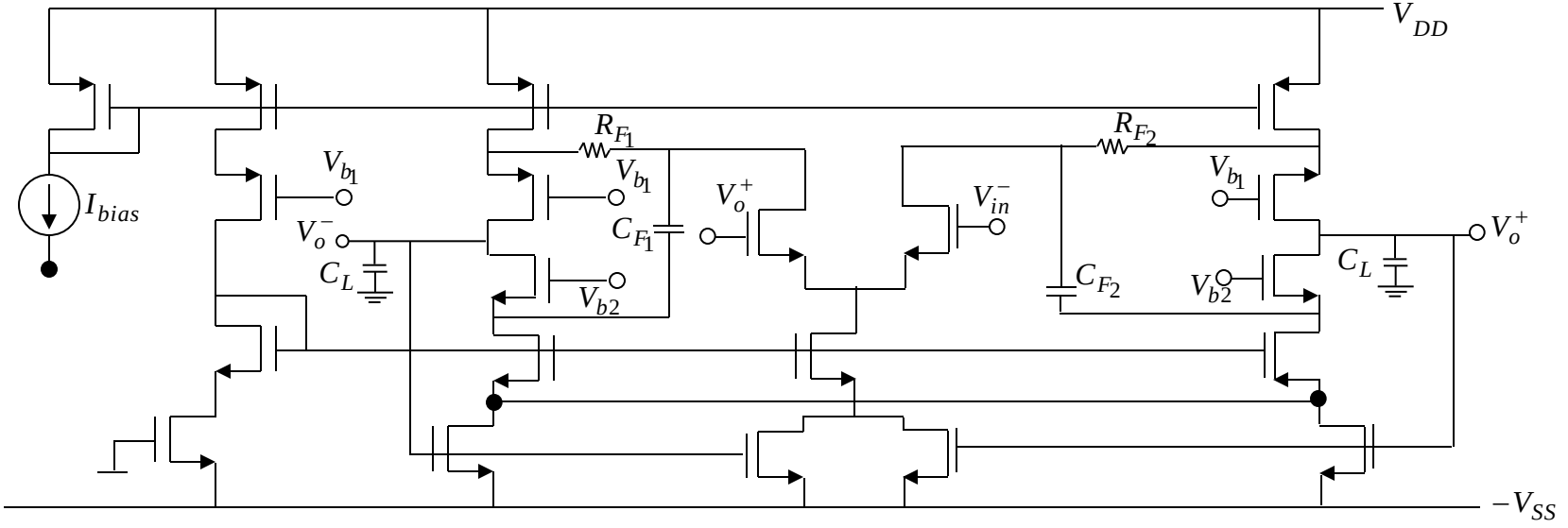
FOLDED-CASCODE WIDEBAND AMPLIFIER



Conventional Folded-Cascode (FC)



FC with Capacitive Feedforward



Differential Wideband Amplifier

F. Opt Eynde, W. Sansen, "A CMOS Wideband Amplifier with 800MHz Bandwidth," *IEEE Custom Integrated Circuits Conf.*, pp. 9.1.1-9.1.4, 1991

References

[1] E. Sánchez-Sinencio and A. Andreou, Editors, " *Low Power/Low Voltage Integrated Circuits and Systems*, Piscataway, IEEE Press, 1999.

[2] K. Laker, W. Sansen, "*Design of Analog Integrated Circuits and Systems*", McGraw-Hill, New York, 1994

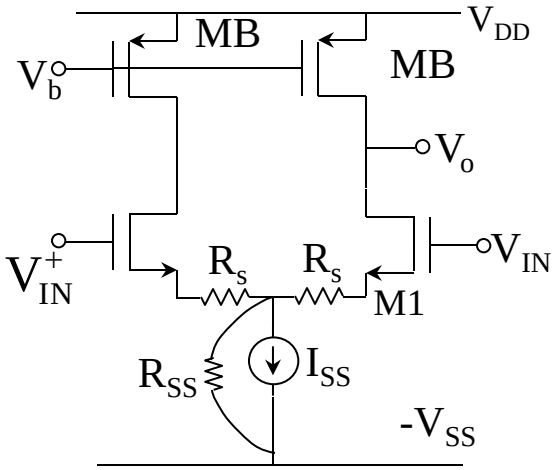
[3] Edgar Sánchez-Sinencio, ELEN626 Notes, 1998

[4] Teresa Serrano-Gotarredona, etc., "Very wide range tunable CMOS/Bipolar Current Mirrors with Voltage Clamped Input", *IEEE Trans. On Circuits and Systems*, Oct. 1998.

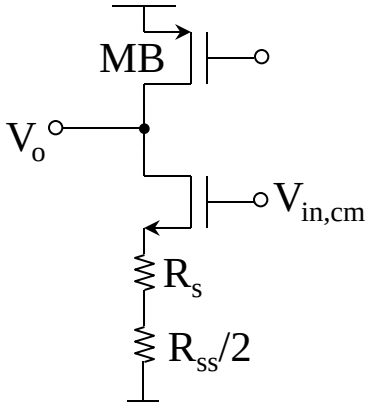
[5] D.A. Johns and K. Martin, "*Analog Integrated Circuit Design*", New York, John Wiley 1997

[6] R. Jacob Baker, H. Li, etc., "*CMOS Circuit Design, Layout, and Simulation*", IEEE Press, 1997.

Different OTAs

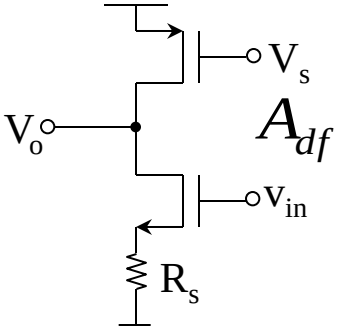


Source Degenerated OTA-1



Common-Mode Equivalent Circuit

$$A_{cm} = \frac{g_{m,n}\left(r_{ds,p} \,||\, \left[\left(g_{m,n}+g_{mb,n}\right)r_{ds,n}\left(R_s+2R_{ss}\right)+r_{ds,n}+R_s+2R_{ss}\right]\right)}{1+\left(g_{m,n}+g_{mb,n}\right)\left(R_s+2R_{ss}\right)} \quad (1)$$



$$A_{df} = \frac{1}{2}\frac{g_{m,n}\left(r_{ds,p} \,||\, \left[\left(g_{m,n}+g_{mb,n}\right)r_{ds,n}R_s+r_{ds,n}+R_s\right]\right)}{1+\left(g_{m,n}+g_{mb,n}\right)R_s} \quad (2)$$

Differential-Mode
Equivalent Circuit.

Where

$$CMMR = \frac{A_{df}}{A_{cm}}$$

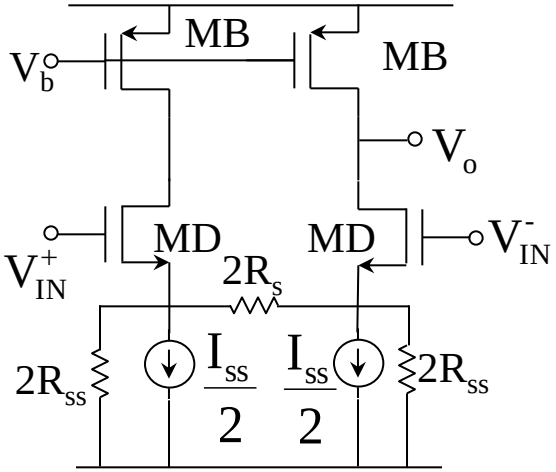
Assume

$$\left(g_{m,n} + g_{mb,n}\right) r_{ds,n} \left(R_s + 2R_{ss}\right) >> R_s, R_{ss}, r_{ds,n}, r_{ds,p}$$

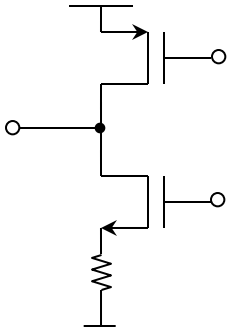
$$\left(g_{m,n} + g_{mb,n}\right) r_{ds,n} R_s >> R_s, r_{ds,n}, r_{ds,p}$$

$$\frac{1}{\mathrm{g_{m,n}} + g_{mb,n}} << R_s \ , R_s << R_{ss}$$

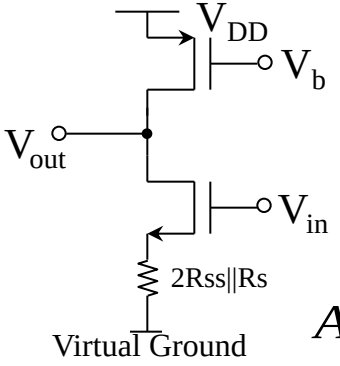
$$A_{cm} \approx \frac{r_{ds,p}}{2R_{ss}} \ , A_{df} \approx \frac{1}{2}\frac{r_{ds,p}}{2R_s} \ , CMRR \approx \frac{R_{ss}}{R_s}$$



Source Degenerated OTA-2



CM Equivalent Circuit



$$A_{cm} = \frac{g_{m,n} \cdot \left(r_{ds,p} \,||\, \left[\left(g_{m,n} + g_{mb,n}\right) r_{ds,n} 2R_{ss} + r_{ds,n} + 2R_{ss}\right]\right)}{1 + \left(g_{m,n} + g_{mb,n}\right) 2R_{ss}} \quad (3)$$

$$A_{df} = \frac{1}{2} \frac{g_{m,n} \cdot \left(r_{ds,p} \,||\, \left[\left(g_{m,n} + g_{mb,n}\right) r_{ds,n} \left(R_s \,||\, 2R_{ss}\right) + r_{ds,n} + R_{ss} \,||\, 2R_{ss}\right]\right)}{1 + \left(g_{m,n} + g_{mb,n}\right)\left(R_s \,||\, R_{ss}\right)} \quad (4)$$

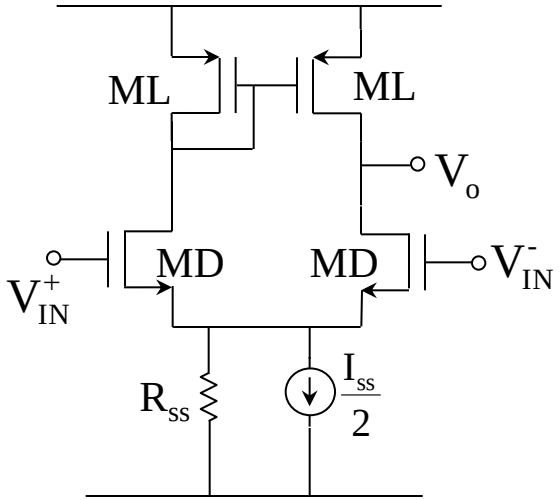
Differential-Mode
Equivalent Circuit

Where

$$CMRR = \frac{A_{df}}{A_{cm}}\ , A_{cm} \approx \frac{r_{ds,p}}{2R_{ss}}\ , A_{df} \approx \frac{r_{ds,p}}{2R_s}$$

Then

$$CMRR \approx \frac{R_{ss}}{R_s}$$



$$A_{cm} = \frac{g_{m,n} \cdot \left(\left(\frac{1}{g_{m,p}} \,||\, r_{ds,p} \right) || \left[\left(g_{m,n} + g_{mb,n} \right) r_{ds,n} 2R_{ss} + r_{ds,n} + 2R_{ss} \right] \right)}{1 + \left(g_{m,n} + g_{mb,n} \right) 2R_{ss}} \qquad (5)$$

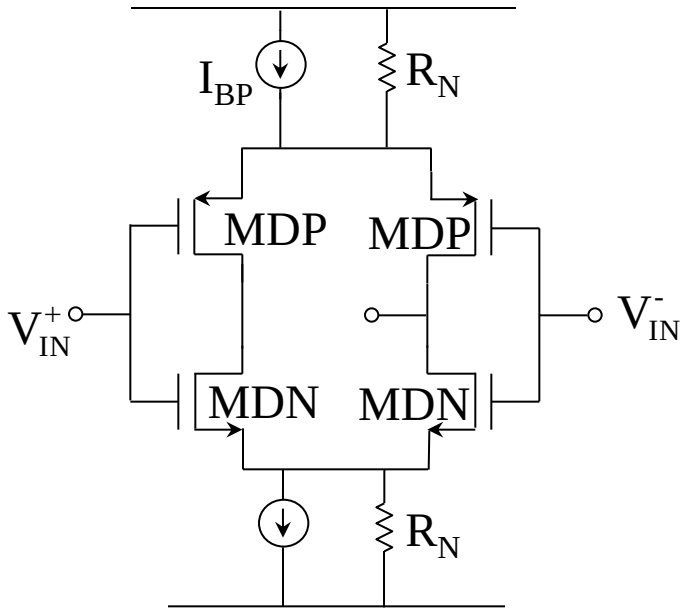
$$A_{df} = g_{m,n} \left(r_{ds,p} \,||\, r_{ds,n} \right) \qquad (6)$$

Where

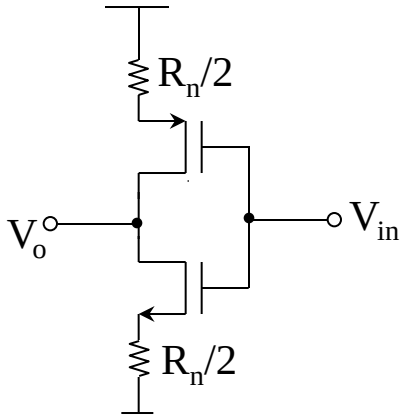
$$CMRR = \frac{A_{df}}{A_{cm}}, \quad A_{cm} \approx \frac{1}{g_{m,p} \cdot 2R_{ss}} \quad , \quad A_{df} = g_{m,n}\left(r_{ds,p} \,||\, r_{ds,n}\right)$$

Then

$$CMRR = g_{m,n}\left(r_{ds,p} \,||\, r_{ds,n}\right) g_{m,p} \cdot 2R_{ss}$$



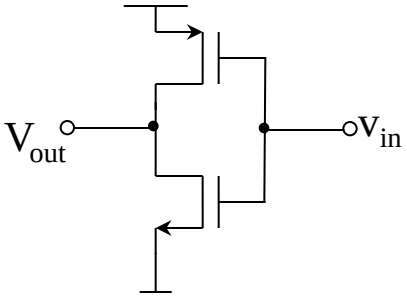
Complementary OTA



CM Equivalent Circuit

$$A_{cm} = \frac{\left[\left(g_{m,p}+g_{mb,p}\right)r_{ds,p}\,2R_N + r_{ds,p} + 2R_N\right] \,||\, \left[\left(g_{m,n}+g_{mb,n}\right)r_{ds,n}\,2R_N + r_{ds,n} + 2R_N\right]}{\left(\frac{1+\left(g_{m,n}+g_{mb,n}\right)2R_N}{g_{m,n}}\right) \,||\, \left(\frac{1+\left(g_{m,p}+g_{mb,p}\right)2R_N}{g_{m,p}}\right)}$$

Virtual Ground



Virtual Ground

$$A_{df} = \frac{1}{2}\left(g_{m,n}+g_{m,p}\right)\left(r_{ds,p} \,||\, r_{ds,n}\right)$$

DM Equivalent Circuit

Where

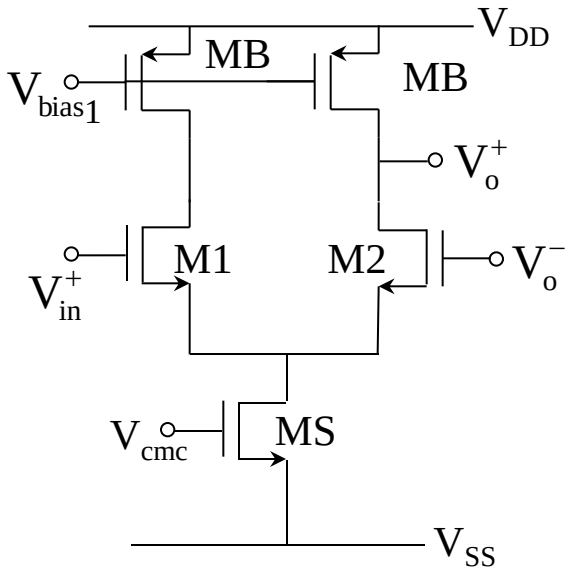
$$CMRR = \frac{A_{df}}{A_{cm}} \quad , \quad A_{cm} \approx 2\left\{\left[\left(g_{m.p} + g_{mb,p}\right)r_{ds,p}\right] || \left[\left(g_{m,n} + g_{mb,n}\right)r_{ds,n}\right]\right\} \quad ,$$

$$A_{df} = \frac{1}{2}\left(g_{m,n}+g_{m,p}\right)\left(r_{ds,p} \,||\, r_{ds,n}\right)$$

Then

$$CMRR = \frac{\left(g_{m,n} + g_{m,p}\right)\left(r_{ds,p} \,||\, r_{ds,n}\right)}{4\left\{\left[\left(g_{m,p} + g_{mb,p}\right)r_{ds,p}\right] || \left[\left(g_{m,n} + g_{mb,n}\right)r_{ds,n}\right]\right\}}$$

$$T_1 = \left.\frac{V_o^+ - V_o^-}{v_{cmc}}\right|_{v_i^+ = v_i^- = 0} = 0$$



Simple Differential OTA

$$T_2 = \left.\frac{V_o^+ + V_o^-}{2v_{cmc}}\right|_{v_i^+ = v_i^- = 0} = \frac{g_{m,MS}}{2}\left\{r_{ds,MB} \,||\left[\left(g_{m,M1} + g_{mb,M1}\right)r_{ds,M1}2r_{ds,MS} + r_{ds,M1} + 2r_{ds,MS}\right]\right\}$$

$$A_{dm} = T_3 = \left.\frac{V_o^+ - V_o^-}{v_i^+ - v_i^-}\right|_{v_{cmc} = V_{bias}} = g_{m,M1,2}\left(r_{ds,MB} || \, r_{ds,M1}\right)$$

$$A_{cm} = T_4 = \left.\frac{V_o^+ + V_o^-}{v_i^+ + v_i^-}\right|_{v_{cmc} = V_{bias}} = \frac{r_{ds,MB} \,||\left[2\left(g_{m,M1} + g_{mb,M1}\right)r_{ds,M1}r_{ds,MS} + r_{ds,M1} + 2r_{ds,MS}\right]}{\dfrac{1 + 2\left(g_{m,M1} + g_{mb,M1}\right)r_{ds,MS}}{g_{m,M1}}} \approx \frac{r_{ds,MB}}{2r_{ds,MS}}$$

Folding Cascode Amplifier Architecture

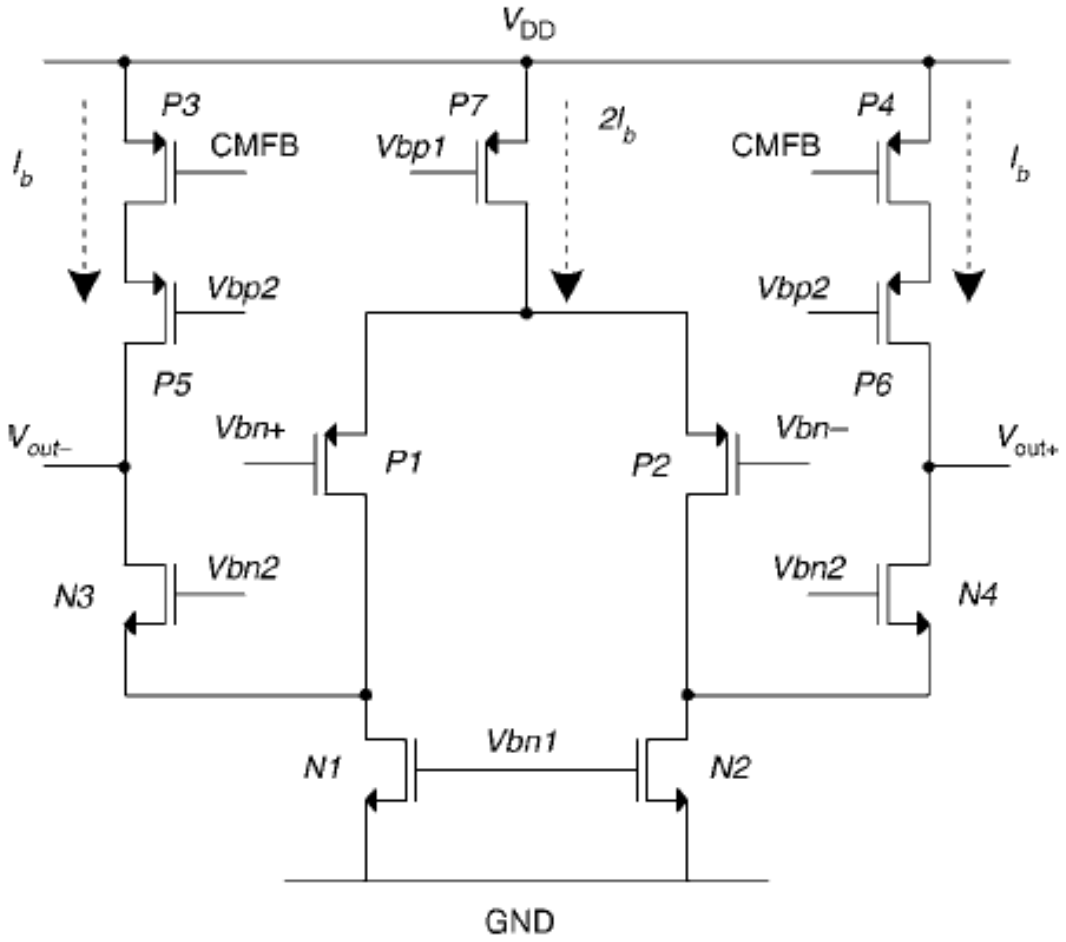


Fig. 1 *Conventional folded cascode*

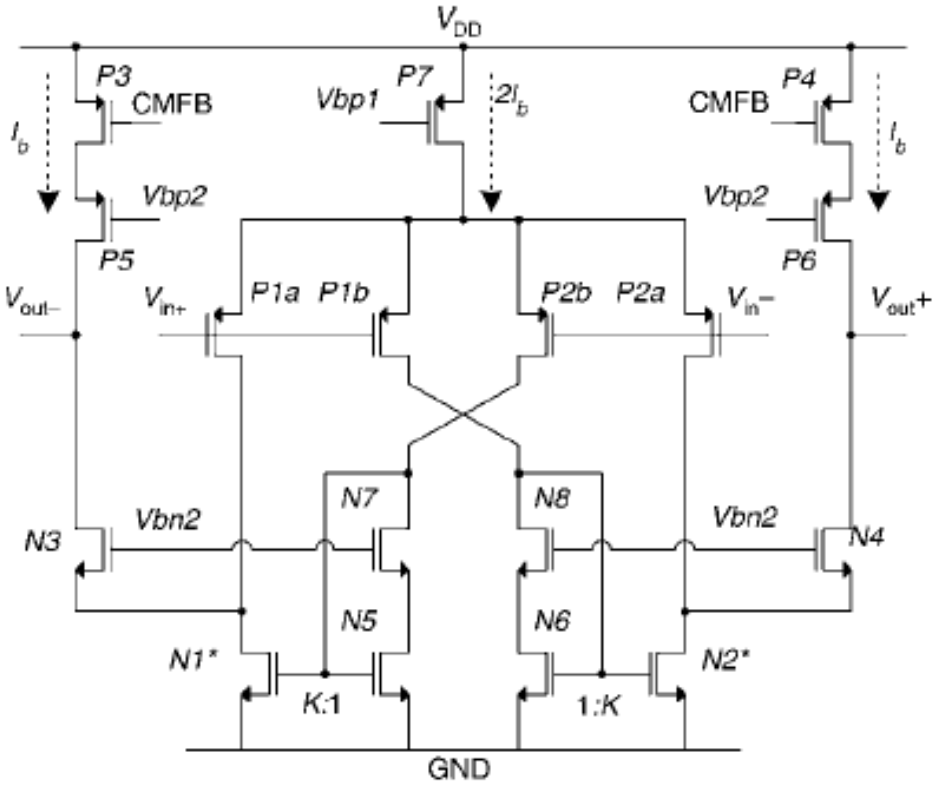


Fig. 2 *Recycling folded cascode*

Recycling folded cascode (RFC): The conventional FC is shown in Fig. 1. Note that transistors *N1* and *N2* conduct the most current and thus have the largest transconductance, yet act as current sinks only. Previous work to enhance the performance of the FC exploited multipath schemes [3]. However, *N1* and *N2* were left unexplored.

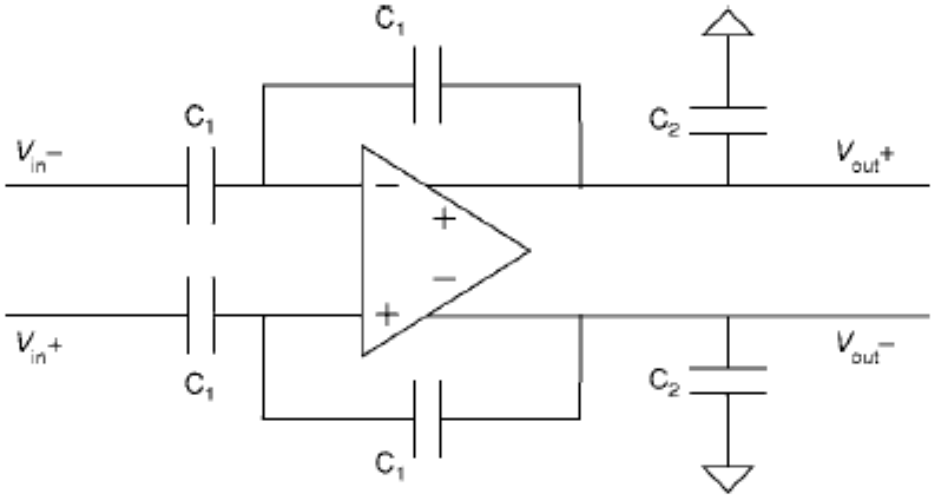


Fig. 3 *Unity gain capacitive buffer*

Table 1: Performance summary of conventional folded cascode and recycling folded cascode

Parameter	Folded cascode	Recycling folded cascode
C_L (pF)	1	1
GBW (MHz)	467.7	**489.8**
Power (μA)	1185	**551**
Gain (dB)	41.1	**50.9**
Phase margin (deg)	**85.1**	77.2
0.1% setting time (ns)	5.7	**5.1**
Static error (%)	2.04	**0.61**

Cascode with positive feedback and bulk-driven input stage

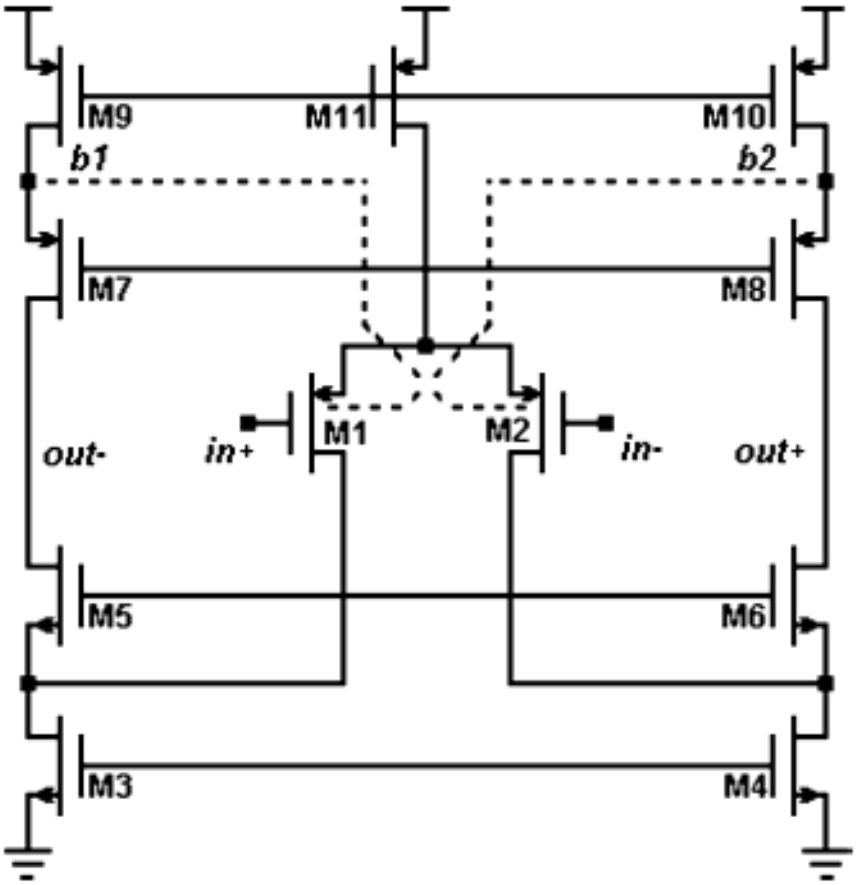


Fig. 1 Scheme of the initial idea to use of bulk and positive feedback.

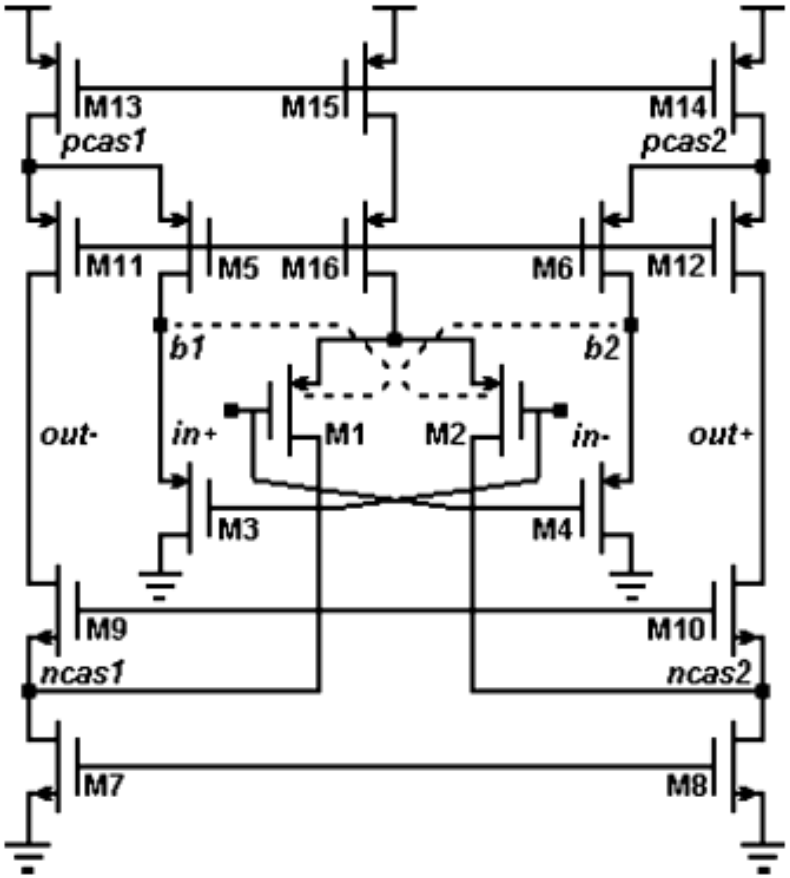


Fig. 2 Scheme of the proposed op-amp.

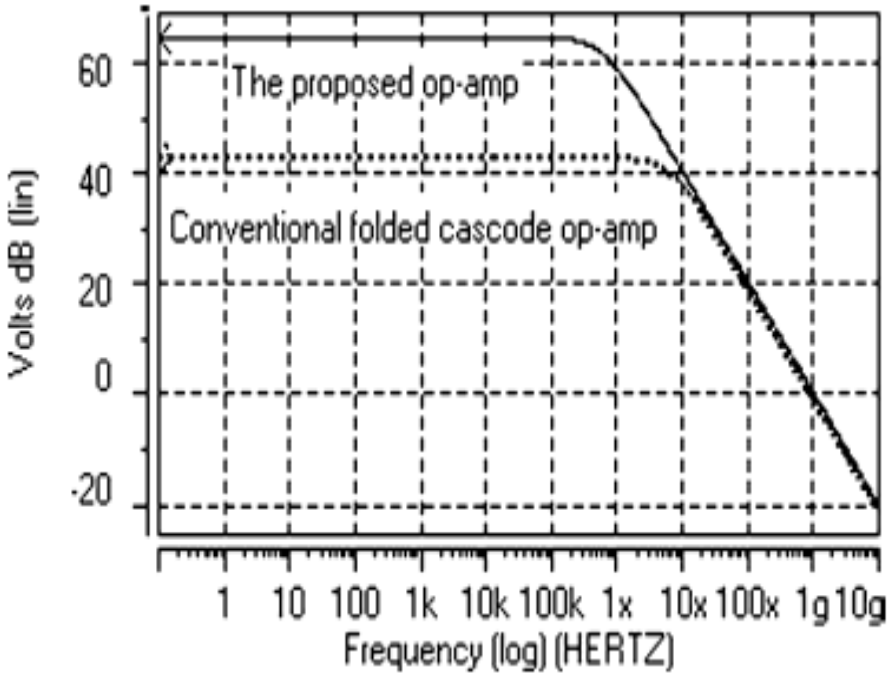


Fig. 3 Gain of the proposed and conventional folded cascode op-amp.

1V CDB Folded Cascode OTA

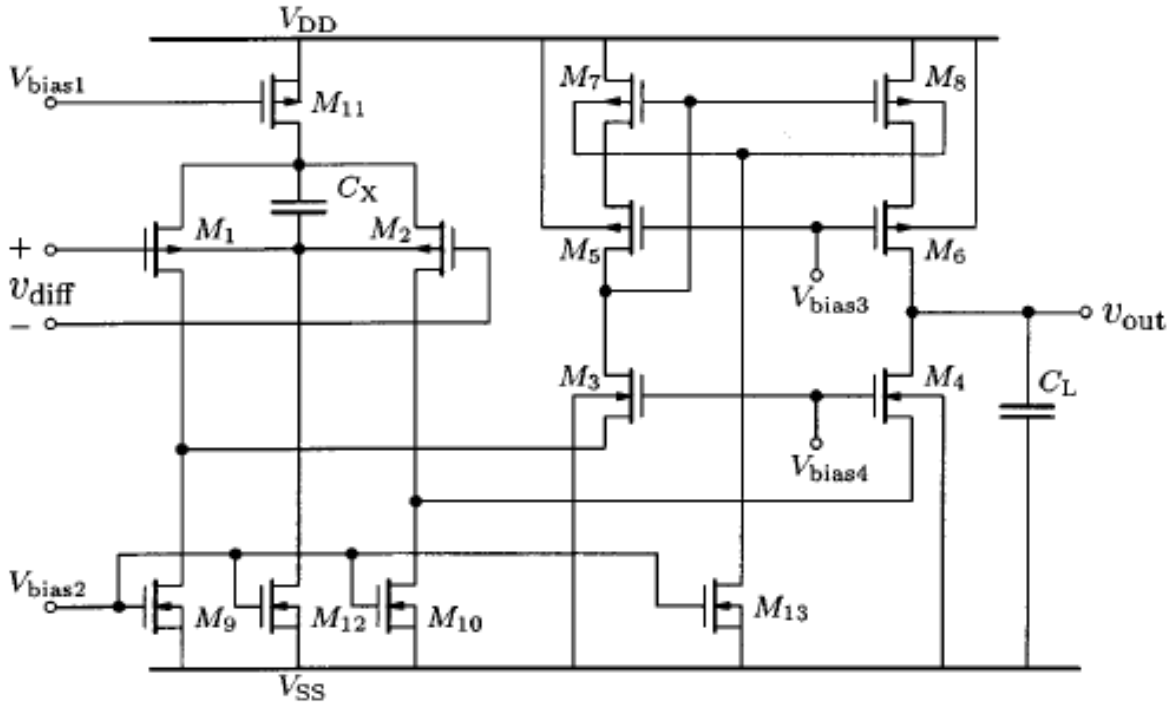


Fig. 6. 1-V CDB folded cascode OTA.

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• **Folded cascode** amplifier with rail-to-rail common-mode range - all 2 versions »
WC Hsu, WR Krenik, JR Hellums - US Patent 4,797,631, 1989 - Google Patents
Page 1. [54] **FOLDED CASCODE** AMPLIFIER WITH RAIL-TO-RAIL COMMON-MODE RANGE [75] Inventors: Wei-ChanHsu,Piano;WilliamR. Krenik, Dallas; James R. Heliums, **...**

Design of a New Folded Cascode Op-Amp Using Positive Feedback and Bulk Amplification

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- R. Assaad and J. Silva-Martinez, "Enhancing General Performance of the Folded-Cascode Amplifier by Recycling Current", *IEEE Electronics Letters. Vol. 43, Issue 23, November 2007*.

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