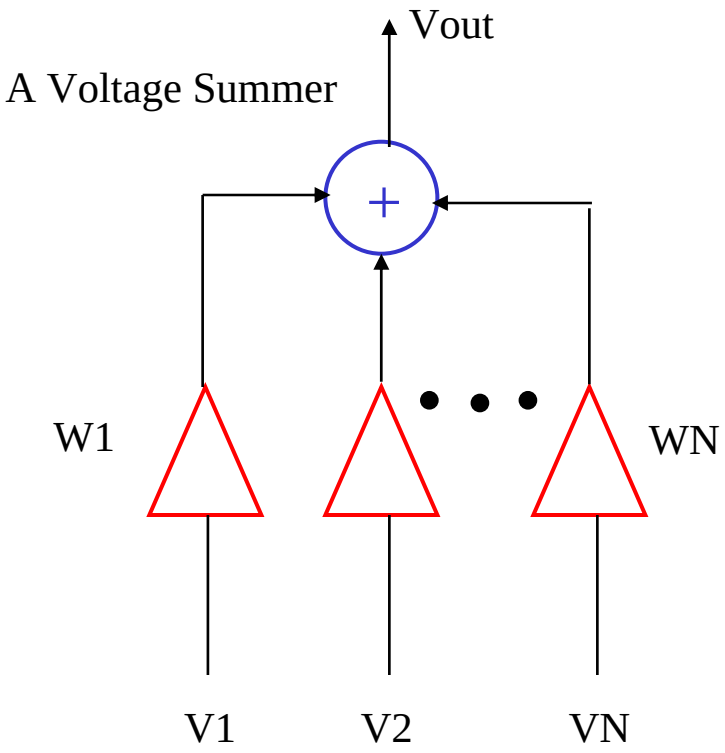
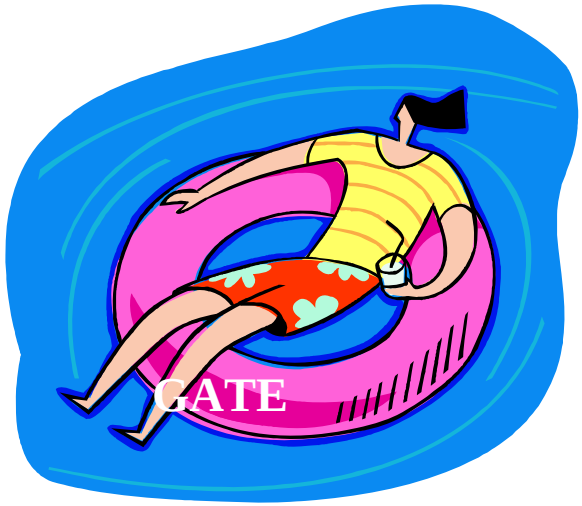
Floating Gate Techniques and Applications

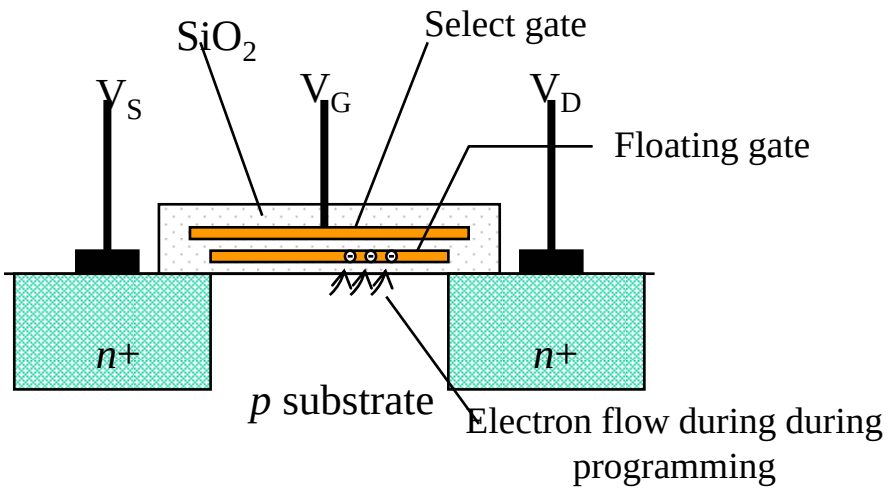




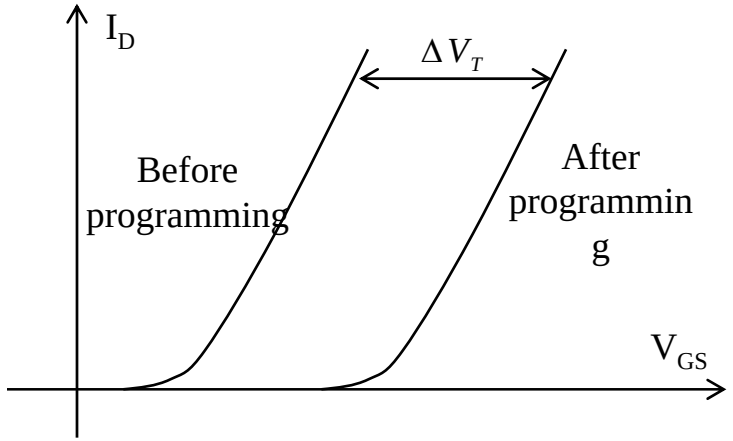
Introduction to Floating Gate MOS transistors

- Floating gate MOS transistors are widely used in digital world as EPROMs (Erasable Programmable Read Only Memories) and EEPROMSs (Electrically Erasable Programmable Read Only Memories).
  - How to program a floating gate transistor in PROMs .
    - To program the device, a high voltage (16V for instance) is applied between the drain and source, this causes electron to avalanche through the source towards the drain.
    - As the SiO_2 layer is very thin, electrons travels through this SiO_2 layer to the floating gate, give the floating gate electrode an electrical charge. Hence the threshold voltage of the floating gate transistor is increased. The change of V_T is given by

$$\Delta V_T = -\frac{\Delta Q_{FG}}{C_{FG}}$$



Multiple-Input Floating Gate MOS Transistors

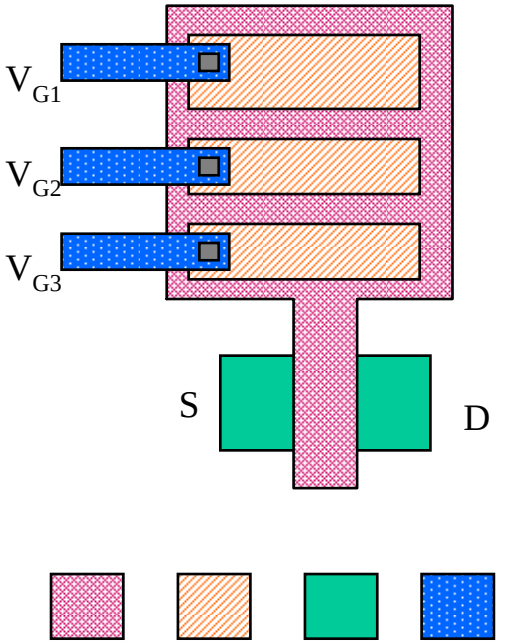


I_D vs. V_{GS} characteristics of the floating gate transistor before and after programming

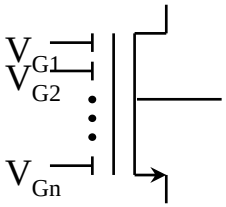
- The above mentioned programming technique is based on hot-electron injection, this method can only introduce electrons ONTO the floating gate. There is another program method which is based on tunneling effect, and can induce positive or negative charge on the floating gate. When the floating gate transistor is bathed in UV light for some time, the charge on the floating gate will disappear.
- Because of the very good insulation properties of SiO_2, the charge on the floating gate leaks away very slowly, and the V_T will keep high for a long time (for decades in room temperature).
- For analog circuits, there are some applications of this programming property of floating gate MOS transistors, such as circuit trimming and neural networks. Practically it is hard to control the charge on the floating gate exactly. In the following, we will not discuss this property, we just assume that the floating gate is without any charge, see Rodriguez-Villegas paper. E. Rodriguez-Villegas and H. Barnes, "Solution to the Trapped Charge in FGMOS Transistor", *IEE Electronic Letters* 39 (19) pp.1416-1417, Sep. 2003

Multiple-Input Floating Gate MOS Transistors

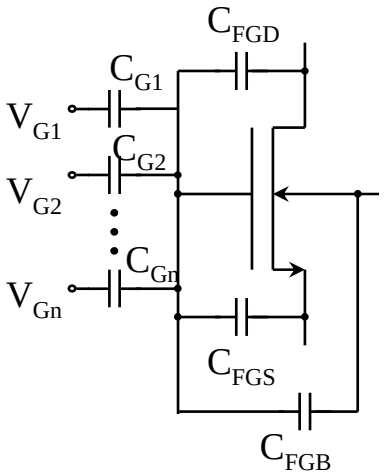
- Multiple-Input Floating Gate (MIFG) MOS Transistors
  - A Multiple-Input Floating Gate (MIFG) MOS Transistor is a floating gate transistor with mutiple control gate
  - The layout and symbol of an MIFG MOS transistor



(a) Layout



(b) Schematic Symbol



(c) Equivalent Circuit

Multiple-Input Floating Gate MOS Transistors

– The n input control gates are capacitively coupled to the floating gate.

Let's assume Q_{FG} is the net charge on the floating gate, V_{FG} is the voltage of the floating gate, and V_{gi} is voltage of the *i*th control gate, thus

$$V_{FG} = (Q_{FG} + C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi}) / C_{TOTAL}$$

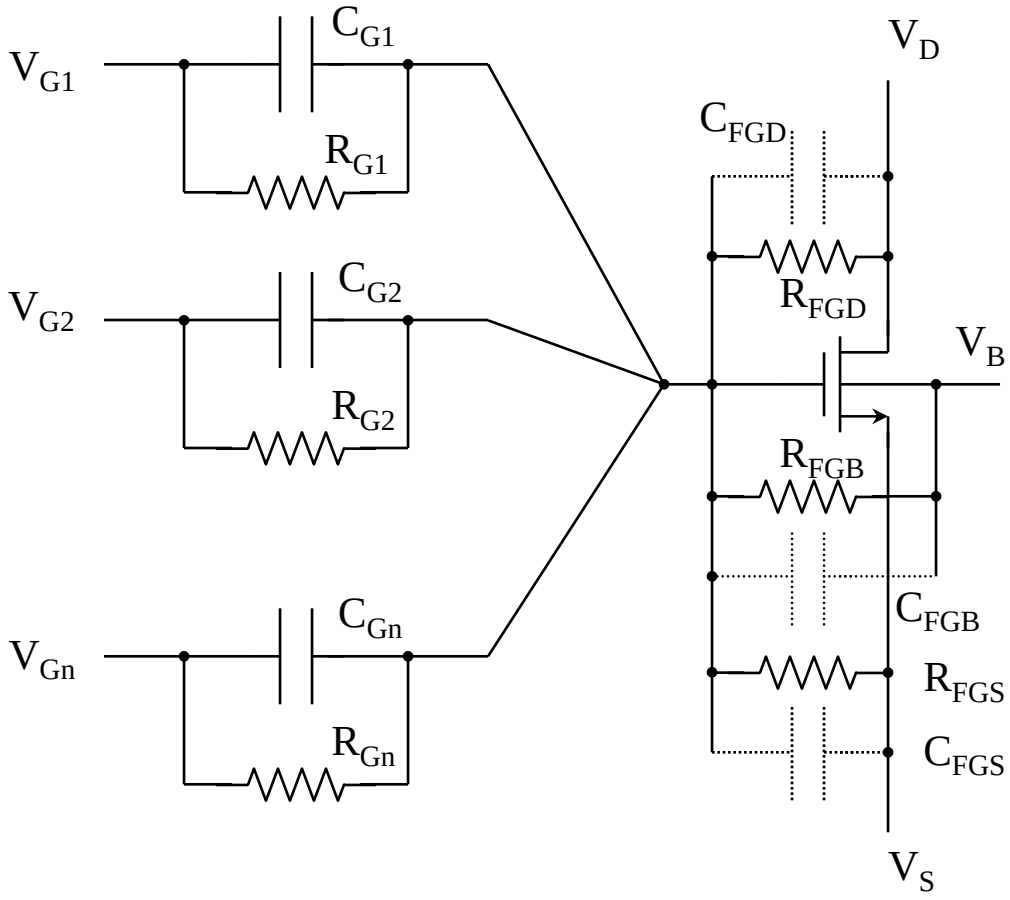
where

$$C_{TOTAL} = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{n} C_{Gi}$$

– If we do not considering the control gates, the physical structure of the floating-gate transistor is the same with conventional MOS transistor, so the I_D vs. V_{FGS} characteristics of a floating gate transistor is the same with that of a conventional MOS transistor. So we can model floating gate transistors using conventional MOS models in HSPICE.

Modeling Multiple-Input Floating Gate MOS Transistors

- SPICE simulation model of the MIFG MOS transistor



Modeling Multiple-Input Floating Gate MOS Transistors

- Because SPICE can not accept floating node which has no DC branch to ground, we have to add one resistor with each capacitor with a resistor, which should have a value more than 10^{18} to minimize the loading effect to the circuit.
- Every branch should have the same time constant - which is the product of R and C, i.e.,

  $R_{G1}C_{G1}= R_{G2}C_{G2}=\ldots= R_{Gn}C_{Gn}= R_{FGD}C_{FGD}= R_{FGS}C_{FGS}= R_{FGB}C_{FGB}$

  If the above condition stands, the DC voltage of the floating gate will not be affected by the introduction of the resistors. Which can be verified by f writing the DC nodal equation for the floating gate for DC (without considering the effect of the capacitors).

$$V_{FG}\left(\frac{1}{R_{FGD}}+\frac{1}{R_{FGS}}+\frac{1}{R_{FGB}}+\sum_{i=1}^{n}\frac{1}{R_{Gi}}\right)-V_D\frac{1}{R_{FGD}}-V_S\frac{1}{R_{FGS}}-V_B\frac{1}{R_{FGB}}-\sum_{i=1}^{n}V_{Gi}\frac{1}{R_{Gi}}=0$$

Modeling Multiple-Input Floating Gate MOS Transistors

Which is:

$$V_{FG} = (V_D \frac{1}{R_{FGD}} + V_S \frac{1}{R_{FGS}} + V_B \frac{1}{R_{FGB}} + \sum_{i=1}^{n} V_{Gi} \frac{1}{R_{Gi}}) / (\frac{1}{R_{FGD}} + \frac{1}{R_{FGS}} + \frac{1}{R_{FGB}} + \sum_{i=1}^{n} \frac{1}{R_{Gi}})$$

As $R_{G1}C_{G1} = R_{G2}C_{G2} = \ldots = R_{Gn}C_{Gn} = R_{FGD}C_{FGD} = R_{FGS}C_{FGS} = R_{FGB}C_{FGB}$, the above equation is equivalent to

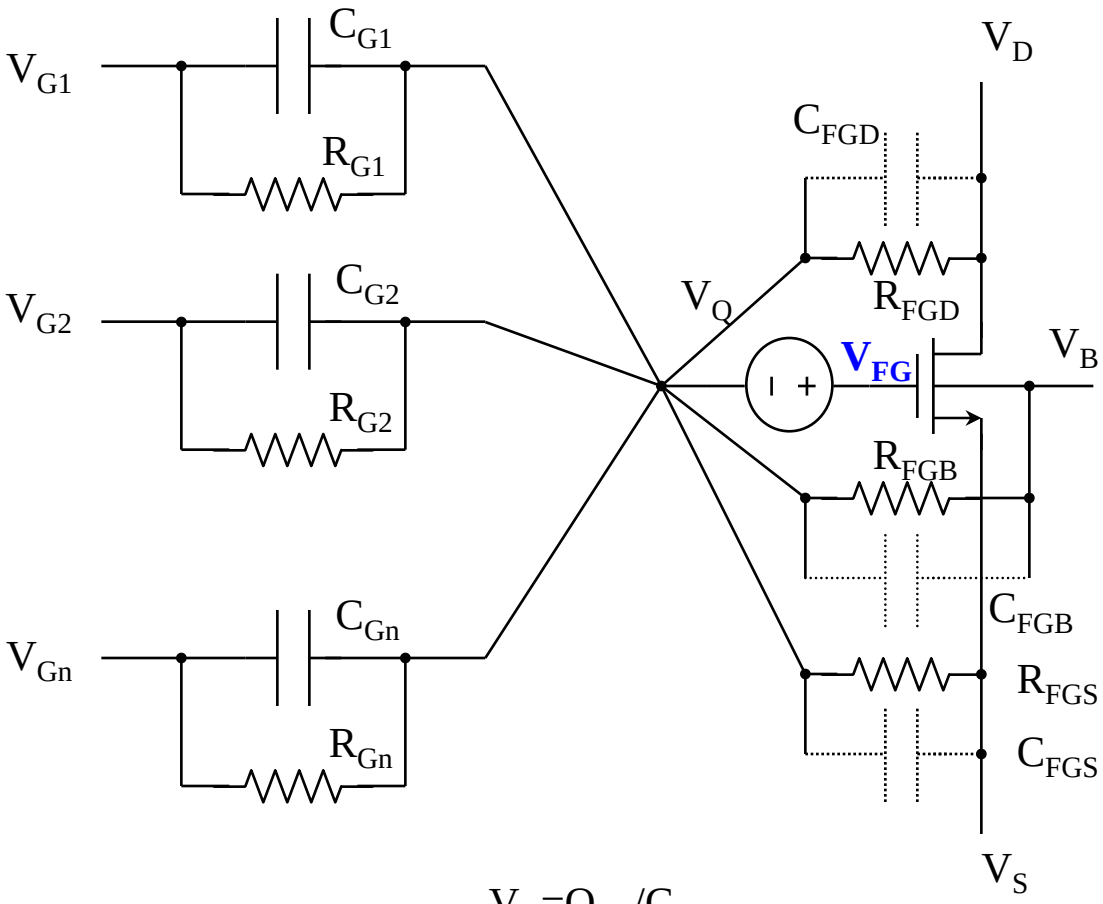
$$V_{FG} = (C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum_{i=1}^{n} C_{Gi}V_{Gi}) / C_{TOTAL}$$

- If there is some initial charge on the floating gate, the SPICE model can be modified to the following diagram (Please refer to the next slide).

- **Usually, for an MIFG MOS transistor, $C_{Gi} >> C_{FGD}, C_{FGS}, C_{FGB}$.**

Modeling Multiple-Input Floating Gate MOS Transistors

– Modified SPICE simulation model of the MIFG MOS transistor with initial charge on the floating gate



$V_Q = Q_{FG}/C_{TOTAL}$

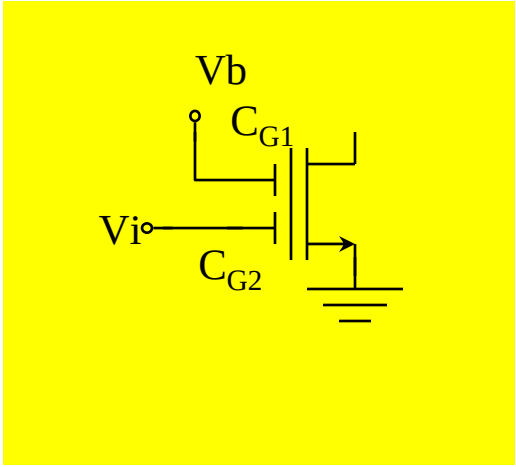
Characteristics of MIFG MOS transistors

- V_{FG} is a linear weighted sum of multiple input gates. It can be applied in A/D, D/A and multiple input amplifier applications.
- For a 2-input-gate MIFG MOS transistor, if we apply a higher DC biasing voltage at one gate, which we call bias gate, and the signal to another gate, the signal gate, we can effectively adjust the equivalent threshold voltage $V_{T,equ}$ seen from the signal gate. This property can be utilized in low voltage applications.

$$V_{FGS} \approx (C_{G1}V_b + C_{G2}V_i)/C_{TOTAL}$$
$$= k_1 V_b + k_2 V_i$$

where

$$k_1 = C_{G1}/C_{TOTAL}, \text{ and}$$
$$k_2 = C_{G2}/C_{TOTAL}$$



Characteristics of MIFG MOS Transistors

- The equivalent threshold voltage seen from Vi is given by

$$V_{T,equ} = \frac{V_T - V_b k_1}{k_2}$$

  which may less than V_T depending on the value of V_b, k_1 and k_2.

- The effective transconductance is given by

$$g_{m,eff} = k_2 g_{m,FG}$$

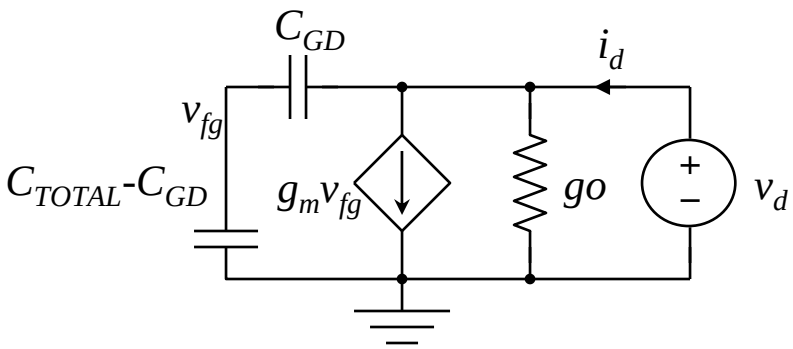
  where $g_{m,FG}$ is the transconductance seen from the floating gate.
  Note that $g_{m,eff}$ is less than $g_{m,FG}$ by a factor of k1.

- The output impedance

  As there is a DC and AC feedback from drain to floating gate through C_{GD}, the output impedance is less than that of an MOS transistor working in the same biasing condition.

Characteristics of MIFG MOS transistors

To get the output impedance of the floating gate MOS transistor, we connect all the inputs to AC ground, and apply a voltage source at the drain of the floating gate MOS transistor. We can get the following small signal circuit,



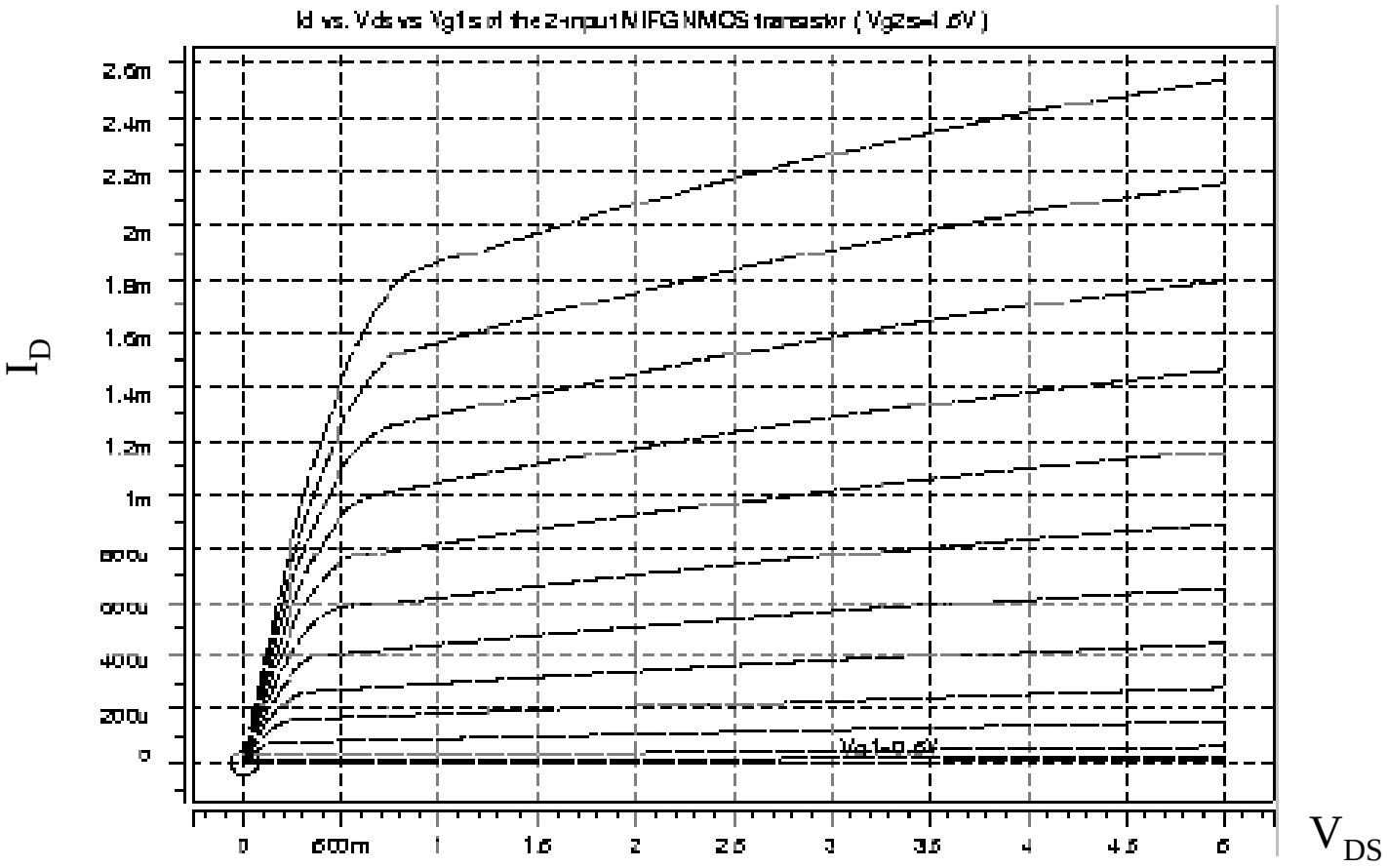
We can easily obtain the output conductance expressed as

$$g_{o,eff} = \frac{C_{GD}}{C_{TOTAL}} g_m + g_o$$

HSPICE simulation of the 2-input MIFG transistor

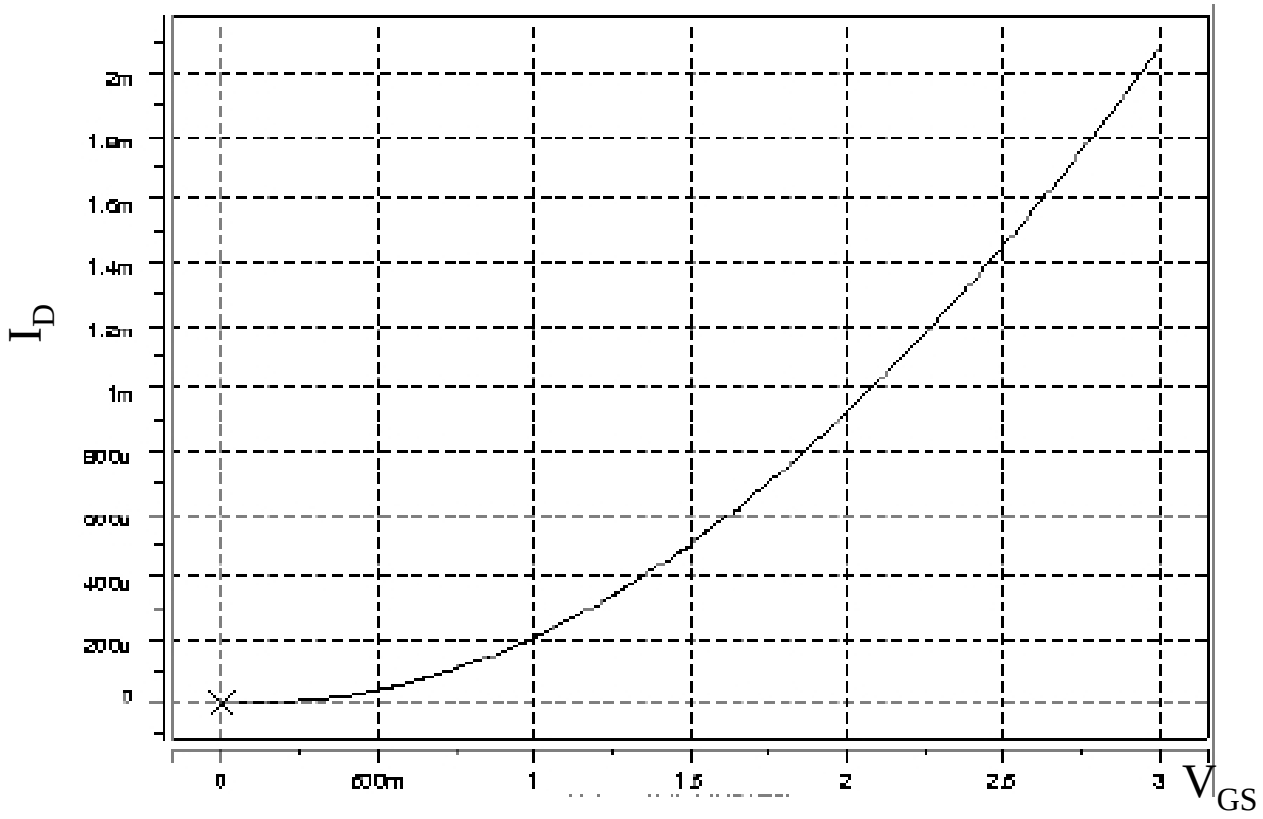
– CG1=4p, CG2=4p, W=200u, L=4u, (we can get CFGS=0.554p by HSPICE simulation, and CFGD=0.0592p by hand calculation)

I_D vs. V_{DS} vs. V_{GS} input output characteristics (V_{G2}=1.5V)



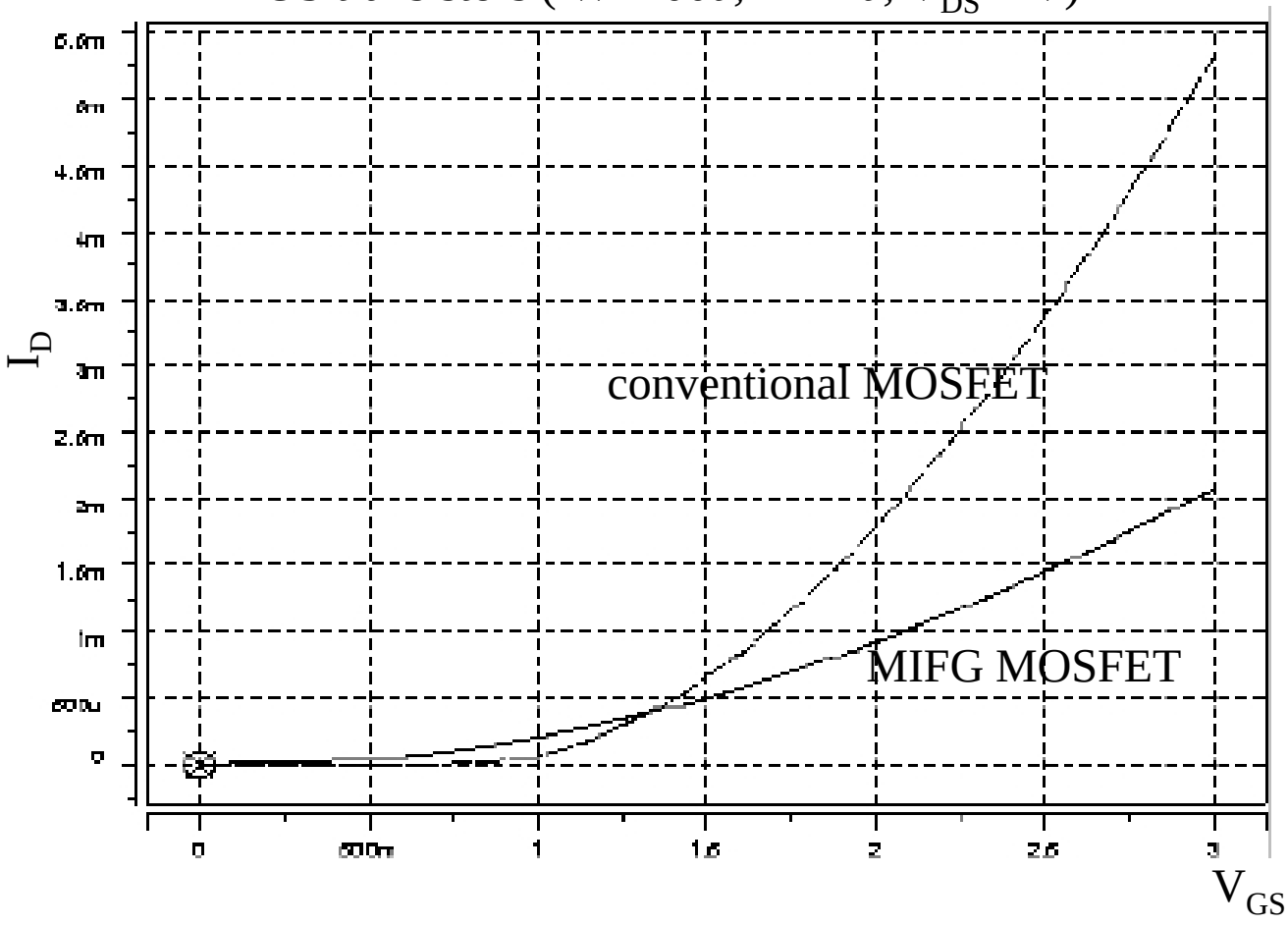
HSPICE simulation of the 2-input MIFG transistor (cont'd)

I_D vs. V_{GS} input output characteristics (V_{DS}=2V)



HSPICE simulation of the 2-input MIFG transistor (cont'd)

I_D vs. V_{GS} input output characteristics of MIFG and conventional MOS transistors (W=200u, L = 4u, V_{DS}=2V)



HSPICE simulation of the 2-input MIFG transistor (cont'd)

- HSPICE File

```
MIFG MOS transistor DC sweep

.options list node post captab
.include orbit_bsim.mod

* parameters
.param lam = 1u ln = 4u wn1 = 200u

* subcircuit for the 2-input floating gate transistor

* .subckt fgnmos drain gate1 gate2 source bulk
.subckt fgnmos d g1 g2 s b
m01 d fg s b cmosn W=wn1 L=ln AD='5*lam*wn1' AS='5*lam*wn1'
+ PS='2*wn1+10*lam' PD='2*wn1+10*lam'
cg1 g1 fg 4p
rg1 g1 fg 1e10
cg2 g2 fg 4p
rg2 g2 fg 1e10
cfgd fg d 59.24f
rfgd fg d 6.7522e11
cfgs fg s 0.5540p
rfgs fg s 7.2202e10
.ends
```

HSPICE simulation of the 2-input MIFG transistor (cont'd)

```
* the floating gate transistor

x01 d g1 g2 nvss nvss fgnmos

vg2 g2 nvss 1.5
vin g1 nvss 0

vd nvd nvss 2
vtest nvd d 0

vss nvss 0 0

* test cards
.op
.dc vd 0 5 0.01 sweep vin 0 3 0.25
.dc vin 0 3 0.01

.end
```

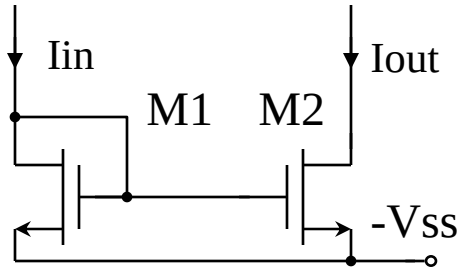
MIFG MOS Transistor Applications

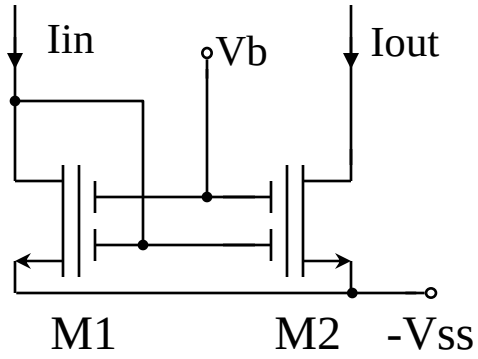
- MIFG MOS transistor application in analog circuit design
  - Many applications of floating gate MOS transistors in analog circuits have been reported in literature. These applications are based on the addition of the voltage signals applied at the input terminals of a MIFG MOS transistor, such as
    - D/A and A/D converter,
    - electronic programming,
    - multiple-input Op Amps and OTAs,
    - low voltage circuits, circuit trimming, and
    - neural networks
  - In the following sections, we will discuss some of these applications.

MIFG MOS Current Mirrors

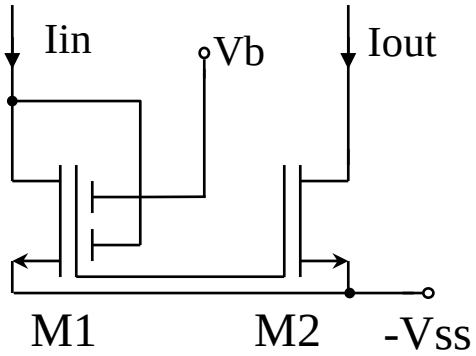
– Conventional current mirror
  - M1 has a voltage drop of V_{GS} which equals V_T+Vdsat, which is too large in some low voltage applications.

– MIFG MOS current mirror





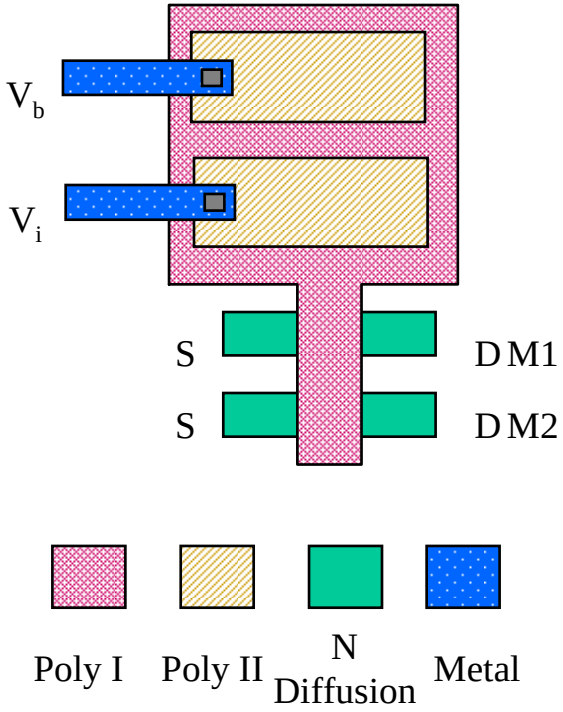
(a) MIFG current mirror I



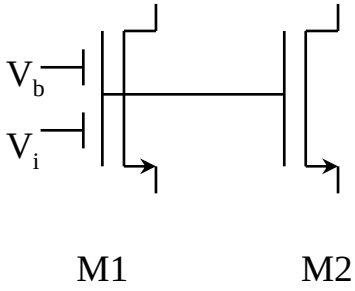
(b) MIFG current mirror II

MIFG MOS Current Mirrors

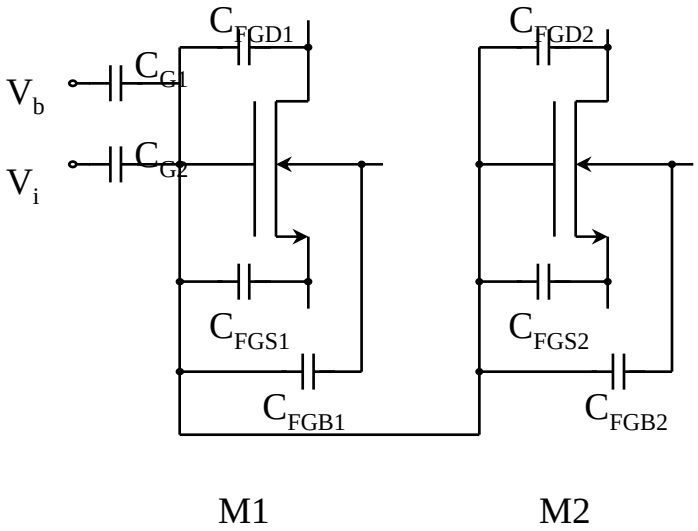
- MIFG current mirror I is easy to understand.
- The layout for the MIFG current mirror II is shown below, it is more compact than I



(a) Layout



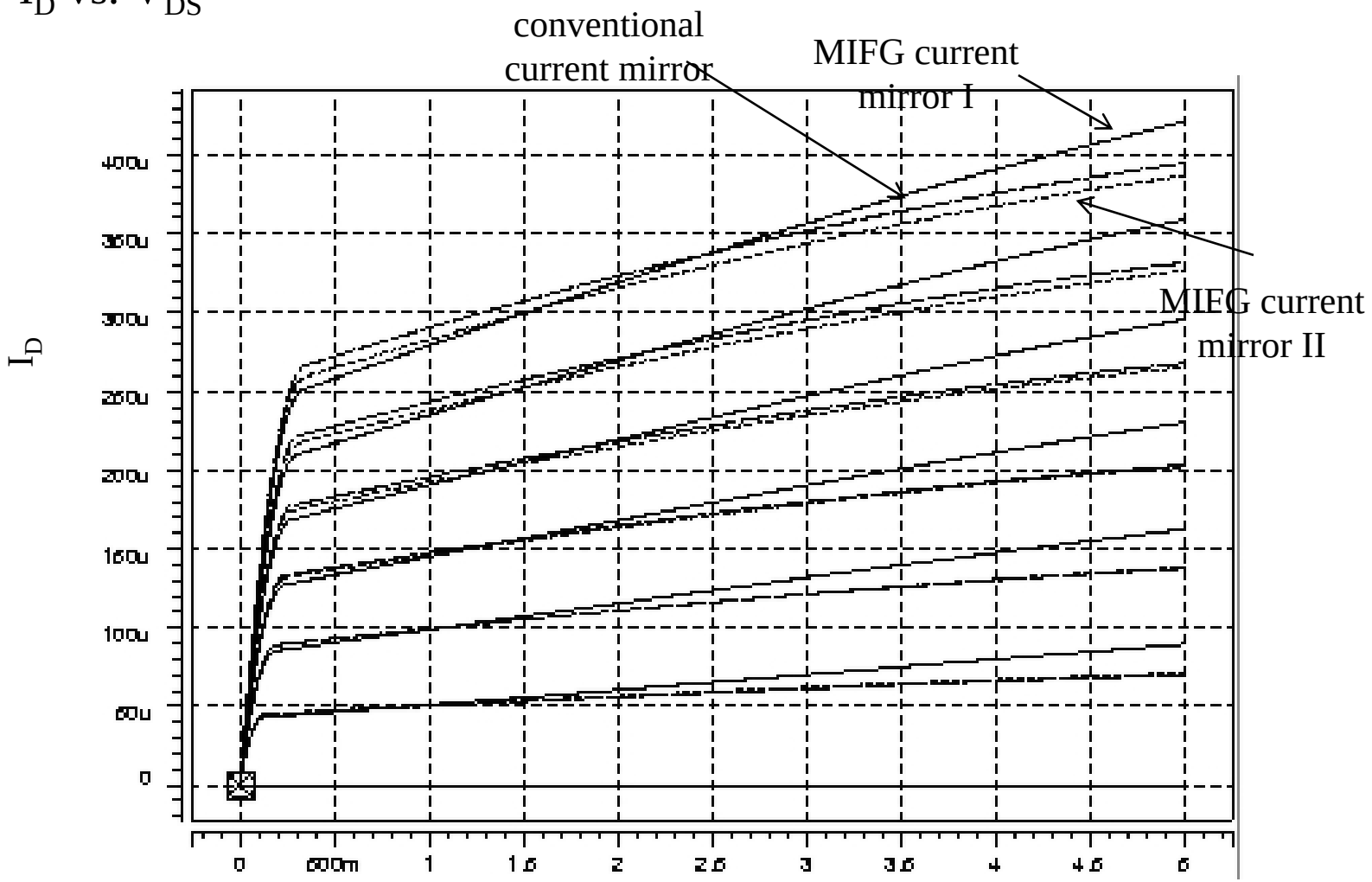
(b) Schematic Symbol



(c) Equivalent Circuit

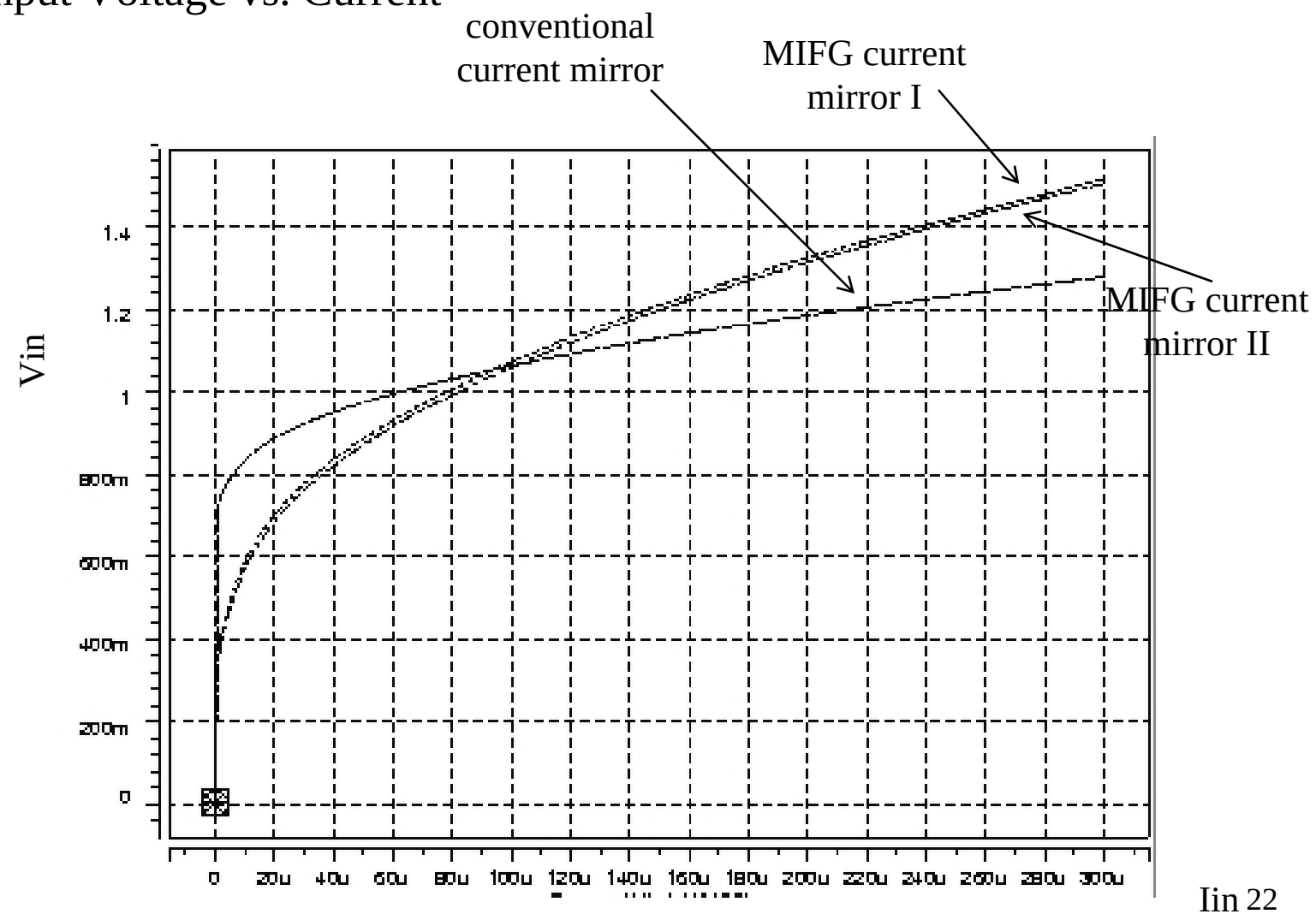
SPICE Simulation of MIFG MOS Current Mirrors

- I_D vs. V_{DS}



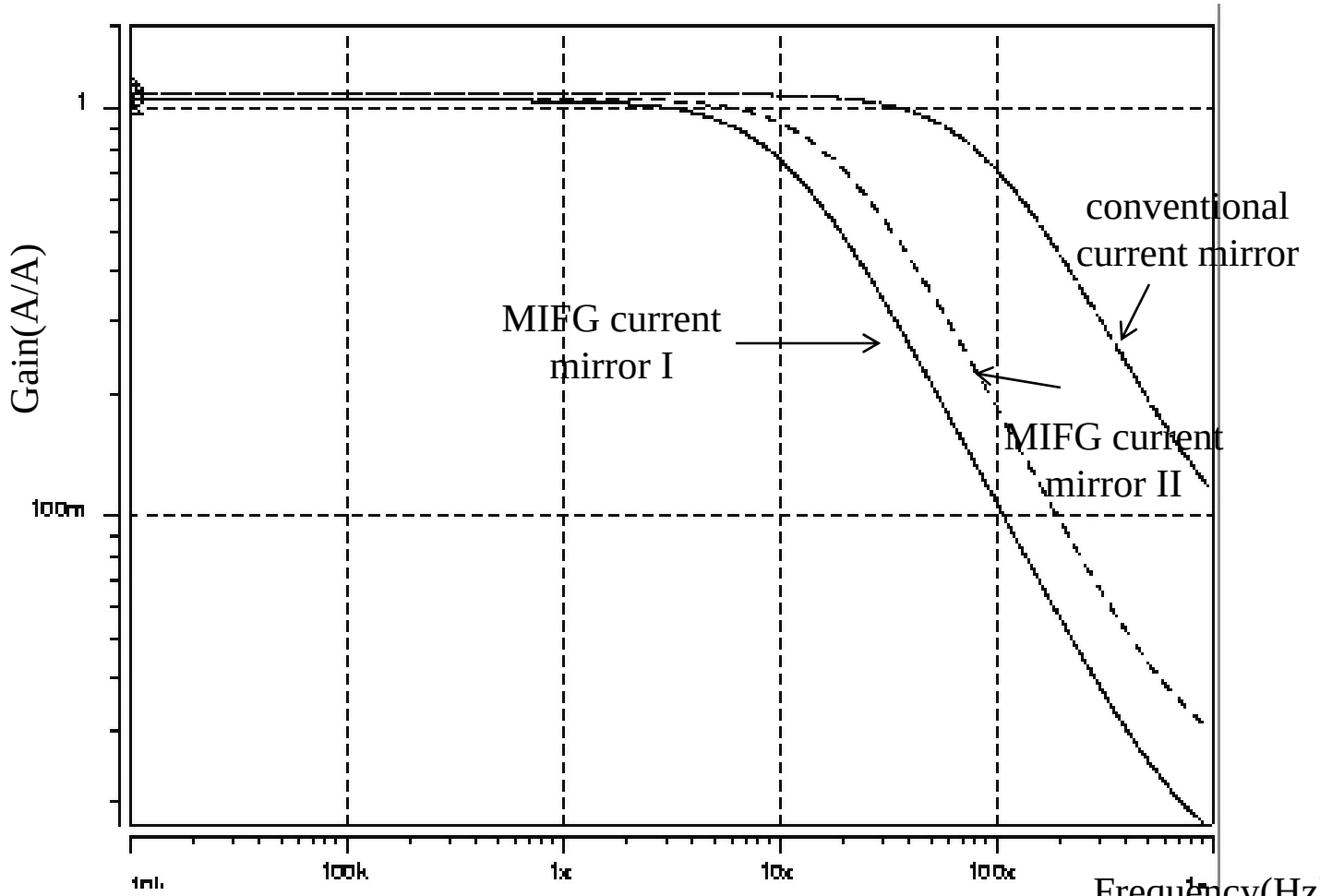
SPICE Simulation of MIFG MOS Current Mirrors

- Input Voltage vs. Current



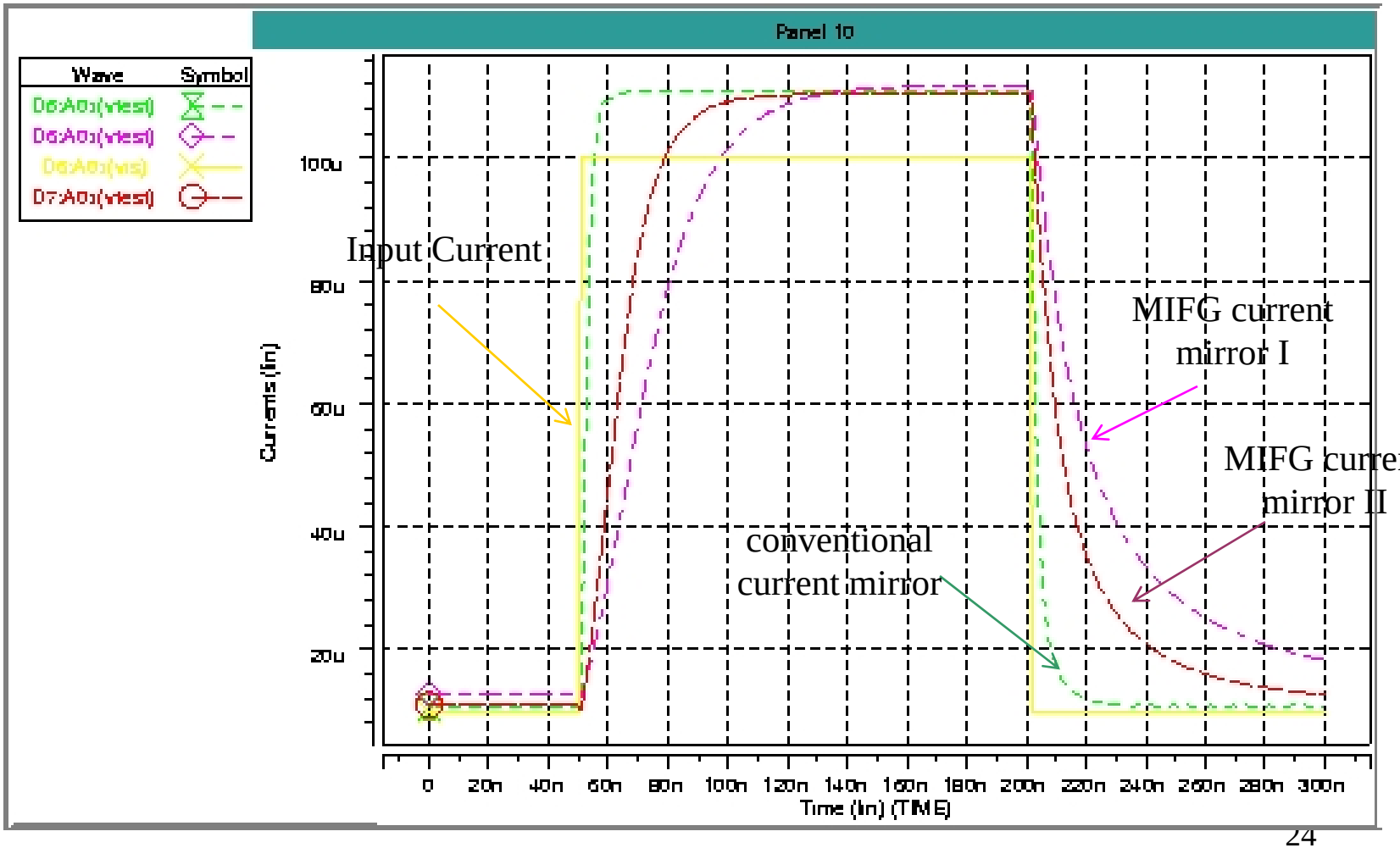
SPICE Simulation of MIFG MOS Current Mirrors

- Frequency Response



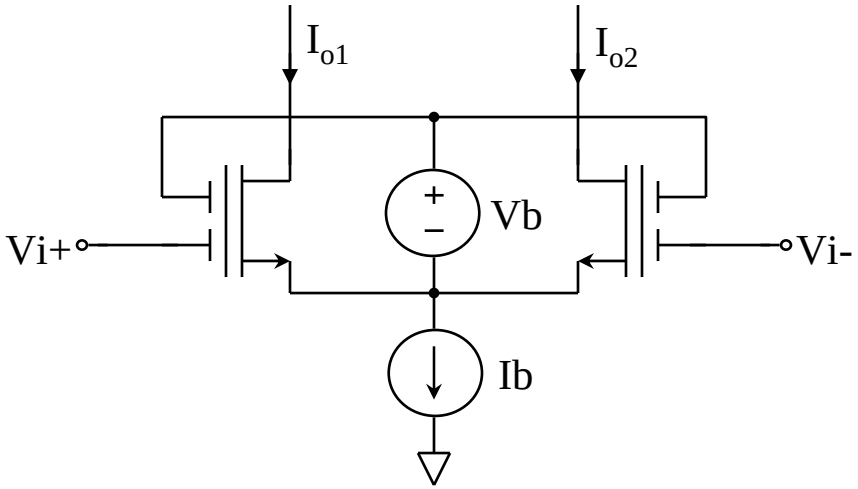
SPICE Simulation of MIFG MOS Current Mirrors

- Transient Response

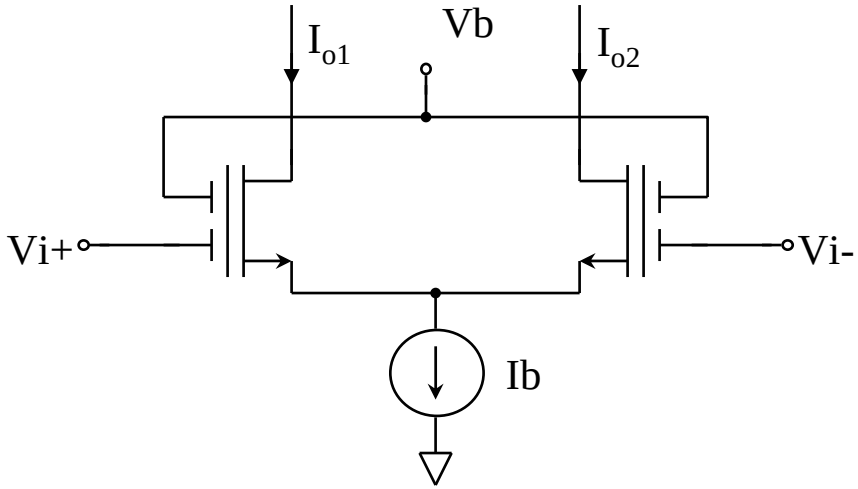


MIFG MOS Differential Pair

- There are 2 types of MIFG MOS differential pair
  - Differential pair I (Biased by floating voltage source)
  - Differential pair II (Biased by non-floating voltage source)



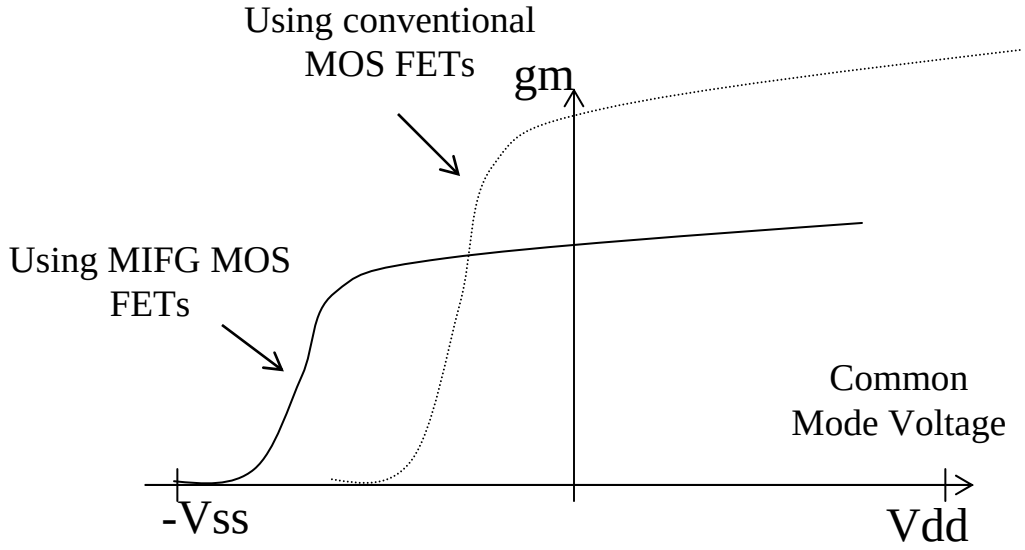
(a) Differential pair I
(Biased by floating voltage source)



(b) Differential pair II
(Biased by non-floating voltage source)

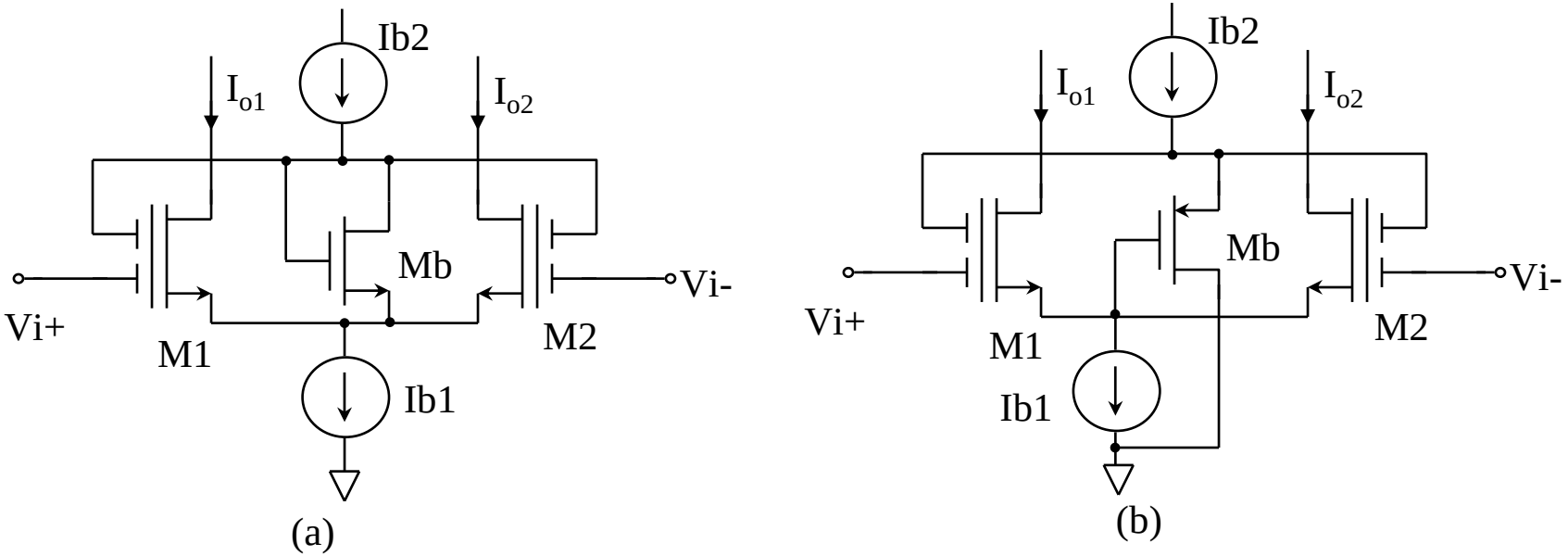
MIFG MOS Differential Pair

- Differential pair I (Biased by floating voltage source)
  - MIFG differential pair I is equivalent to a differential pair with low V_T transistors. It can not have a rail-to-rail range. And the floating voltage source may limit its common mode swing range if the floating voltage source can not swing out of the supply rails .
  - Tthe gm vs. common mode input voltage diagram of MIFG differential pair I and conventional differential pair is shown next. Because of the floating gate, gm is attenuated. The DC bias Vb introduce a DC shift in the curve below.



MIFG MOS Differential Pair

– Usually the floating voltage source is implemented as follows.



In (a) the floating voltage source is implemented by a diode connected MOS transistor biased by a current source Ib2.
In (b) the floating voltage source is implemented by a common drain connected PMOS transistor biased by a current source Ib2.

We may notice that, for both of these two circuits, when the input common mode voltage is approaching Vdd, Ib2 can be driven out of saturation region, because the low resistance of diode connected Mb and current Ib2 which is working ohmic region, the PSRR and CMRR may be degraded.

MIFG MOS Differential Pair

- Differential Pair II (Biased by non-floating voltage source)

  In the following, we will derive under what condition we can get a rail-to-rail input common mode range for the Differential Pair II

  – We know that for 2-input floating gate transistors

    $V_F = w_0 V_0 + w_1 V_1 + w_2 V_2$

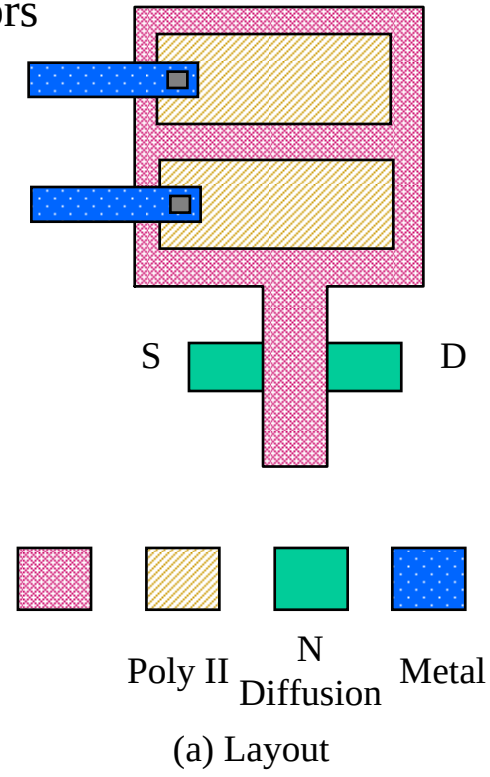
    where

    $w_i = C_i / C_{TOT}$, $i = 0, 1, 2$

    Normally, C_i (i = 1,2) is much larger than C_0, which means *w0* is very small and we can get the following approximation

    $w_1 + w_2 = 1$

  – When Vicm (common mode input voltage) is Vdd, for N type transistor, the floating gate can be Vdd, as long as the V_{DRAIN} is greater than V_{DD}-V_{TN}. So, for the diagram of Differential Pair II shown in previous slides, Vb can directly be Vdd.



(a) Layout

MIFG MOS Differential Pair

– When Vicm (common mode input voltage) is at the negative rail -Vss, for N type differential pair, there is a tendency that tail current transitor will have no room to work in saturation region. We should try to increase $V_{FG,cm}$, the common mode voltage on the floating gate. $V_{FG,cm}$ is given by

$$V_{FG,cm}=w_1 Vicm+w_2 Vb$$

That is, we should have a high Vb, which has the maximum value of Vdd. Let Vb=Vdd.

So, when *Vicm* = -Vss,

$$V_{FG,cm}=w_1 Vicm+w_2 Vb=- w_1 Vss+w_2 Vdd=-w_1 Vss+(1-w_1)Vdd$$

$$= Vdd-w_1(Vss+Vdd) \qquad (1)$$

MIFG MOS Differential Pair

– To make sure M1, M2 and tail current transistor work properly, the following inequality should be satisfied:

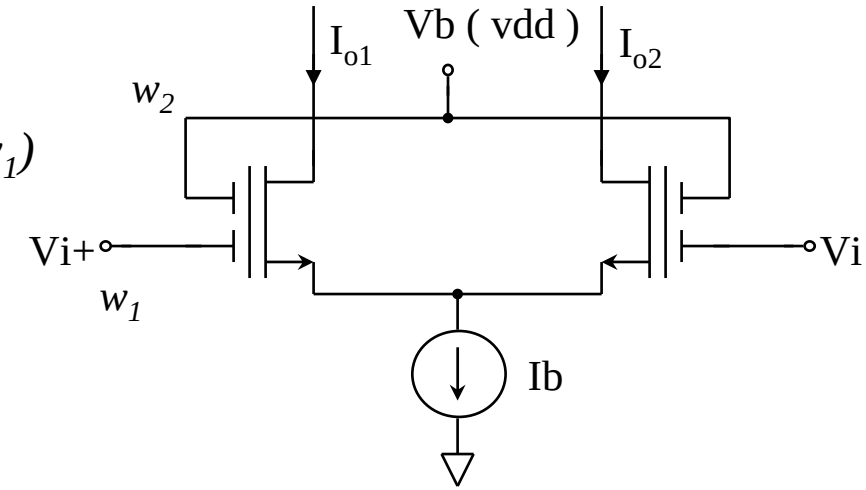
$$V_{FG,cm} >= -Vss + (V_{GS,M1,M2} + V_{dsat,MTAIL}) \qquad (2)$$

So, we can get from the above 2 equations,

$$(Vdd + Vss) >= (V_{GS,M1,M2} + V_{dsat,MTAIL})/(1-w_1)$$

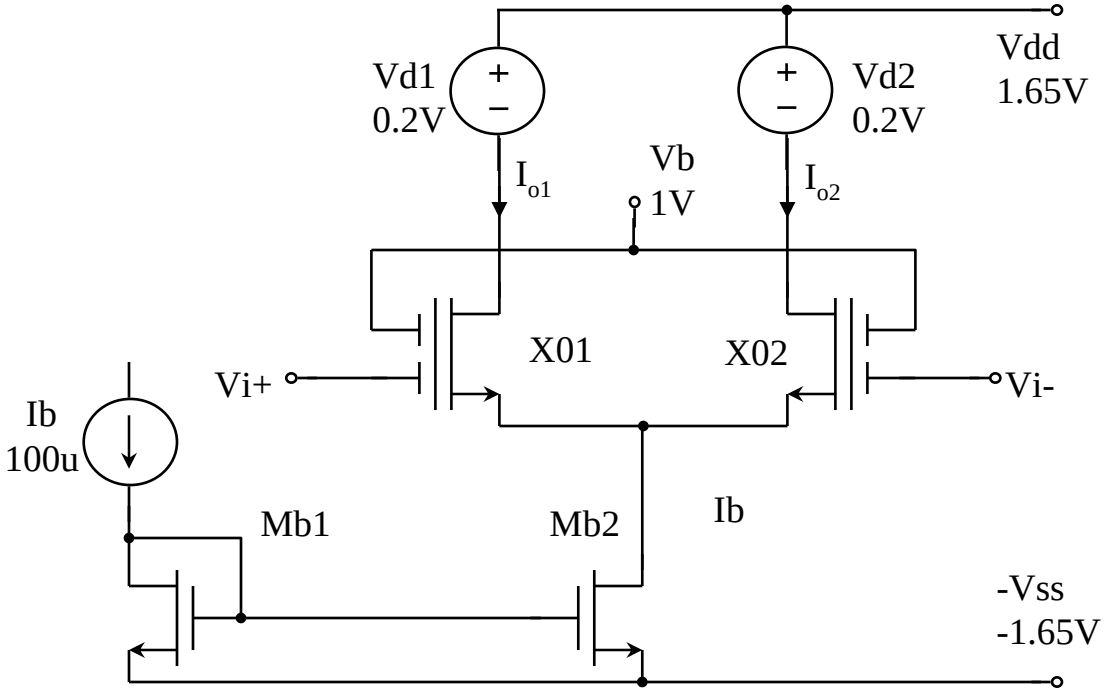
I.e. the minimum supply voltage Vsup is

$$(V_{GS,M1,M2} + V_{dsat,MTAIL})/(1-w_1)$$



HSPICE Simulation of MIFG MOS Differential Pairs

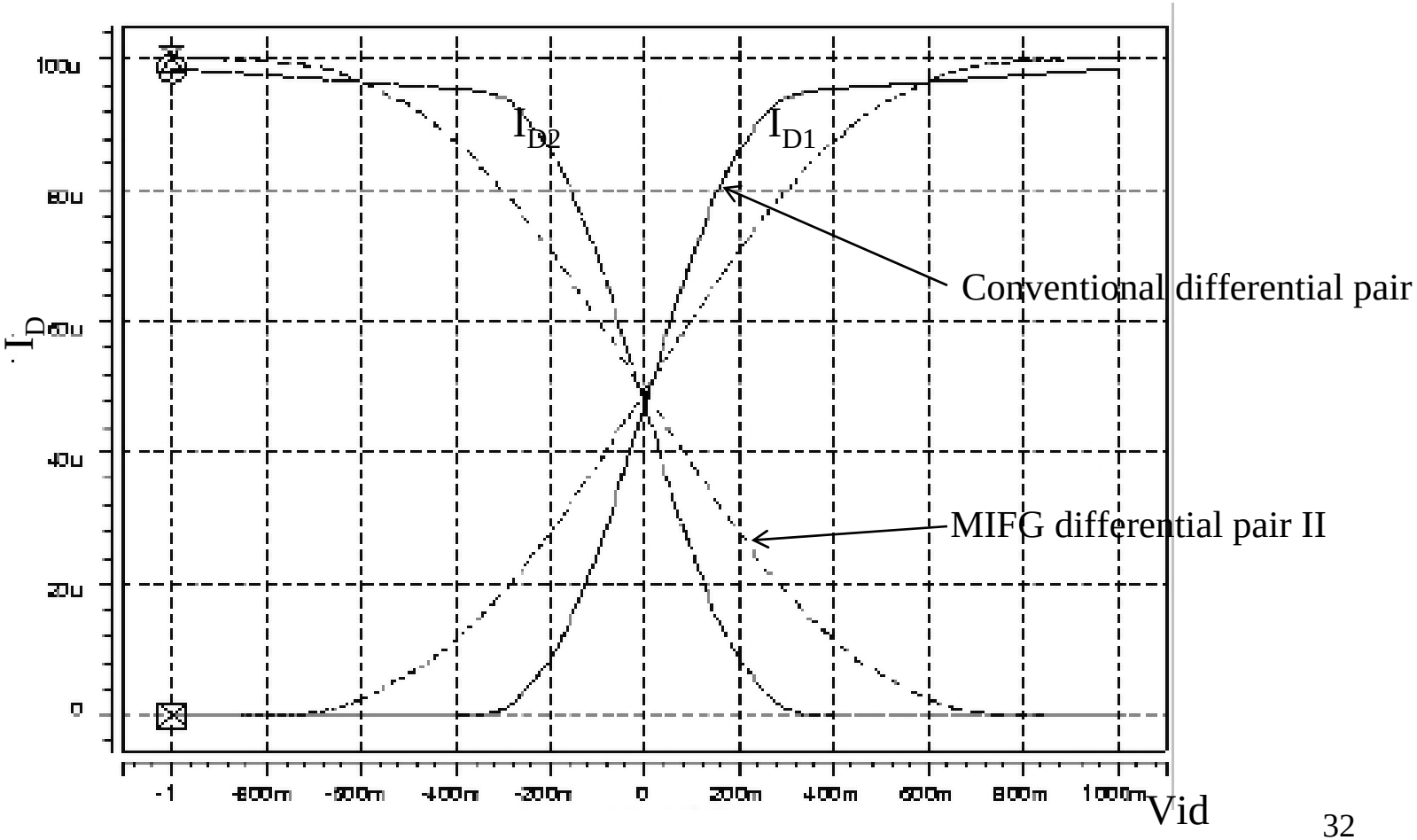
- HSPICE simulation for MIFG MOS differential pair II
  - For 2-input MIFG MOS transistor X01 and X02 (in HSPICE, they are defined by sub-circuit structure), CG1=4p, CG2=4p, W=200u, L=4u, (we can get CFGS=0.554p by HSPICE simulation, and CFGD=0.0592p by hand calculation, Vd1 and Vd2 are current indicators)



HSPICE simulation of MIFG MOS differential pair II (cont'd)

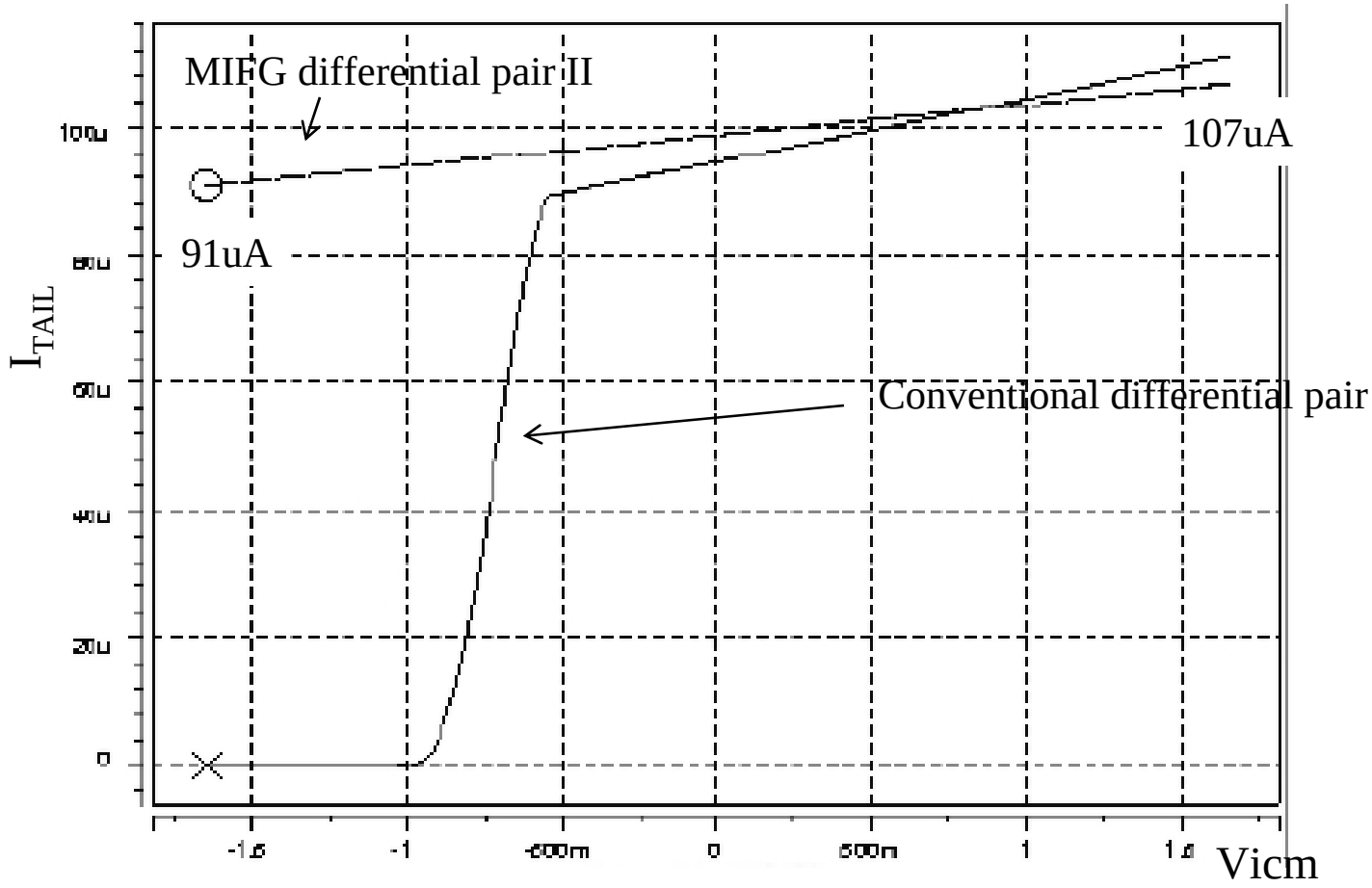
- Simulation results

Output drain current vs. input differential voltage



HSPICE simulation of MIFG MOS differential pair II (cont'd)

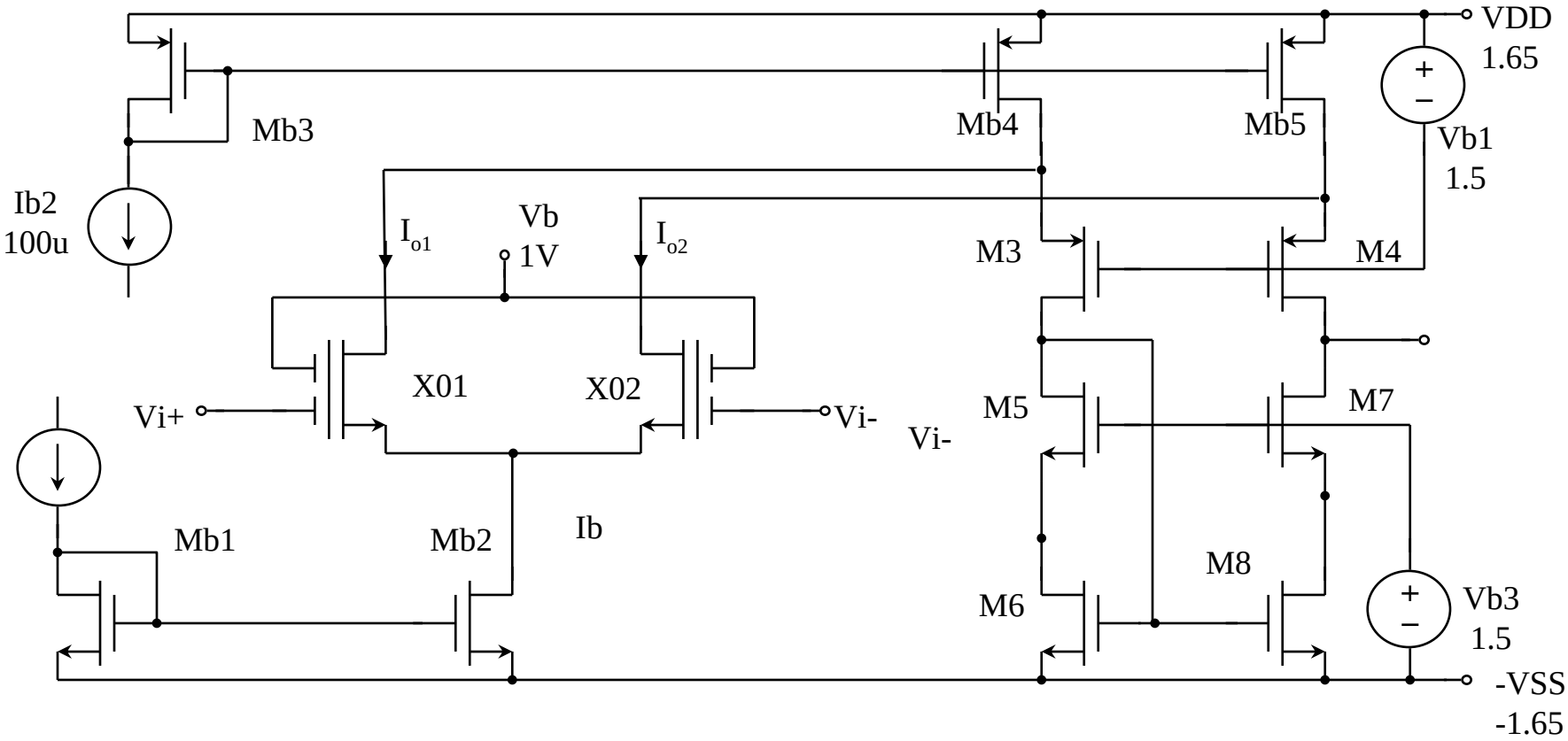
– Tail current vs. input common mode voltage



Observe that, the tail current changes from 91uA to 107uA (because of the output impedance of the tail current transistor!) when Vicm swings from rail-to-rail. The input stage has a rail-to-rail input range.

HSPICE simulation of MIFG MOS differential pair II (cont'd)

- The whole input stage (MIFG differential pair II with folded cascode)



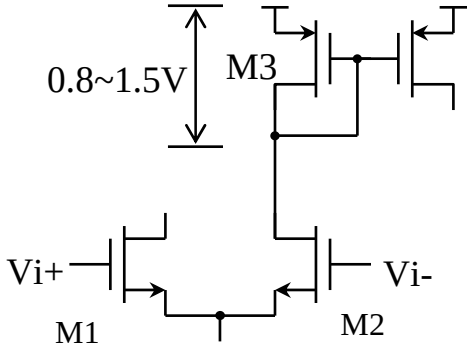
HSPICE simulation of MIFG MOS differential pair II (cont'd)

- Folded cascode circuit is frequently used in low voltage circuit design, because its special property compared with current mirror load for an differential input stage. As shown in the following.

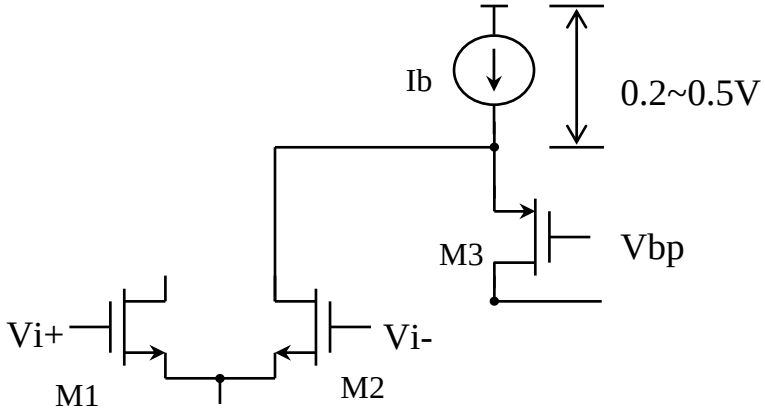
  If the input stage is loaded with a current mirror (Figure a), because the high $|V_{GS}|$ of M3, when the common mode input voltage is close Vdd, M2 may have no room to swing and be driven out of saturation region.

  If the input stage is loaded with a current mirror (Figure b), there is a low voltage drop on the current source transistor (Ib). When Vicm (input common mode voltage) = Vdd, the lowest drain voltage of M2 to keep it working in saturation region is Vdd-$V_{T,M2}$. Fortunately, this can be easily satisfied by using folded cascode circuit, as the current source transistor usually only needs 0.2 to 0.5V of $|V_{DS}|$ to keep it in saturation region.

  So folded cascode structure is widely used in low voltage input stage.



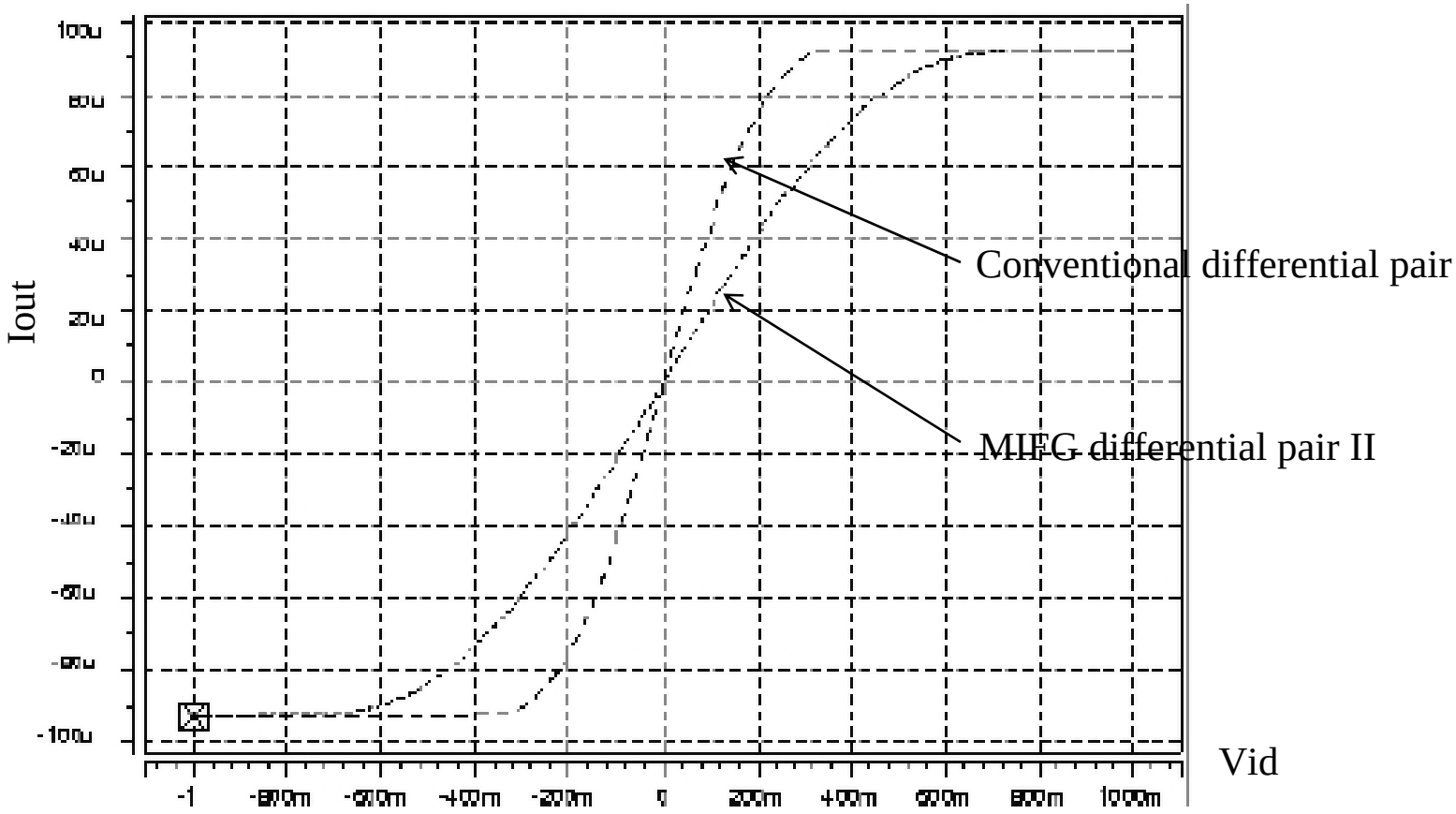
(a) Input stage loaded by a current mirror



(b) Input stage loaded by a folded cascode

HSPICE simulation of MIFG MOS differential pair II (cont'd)

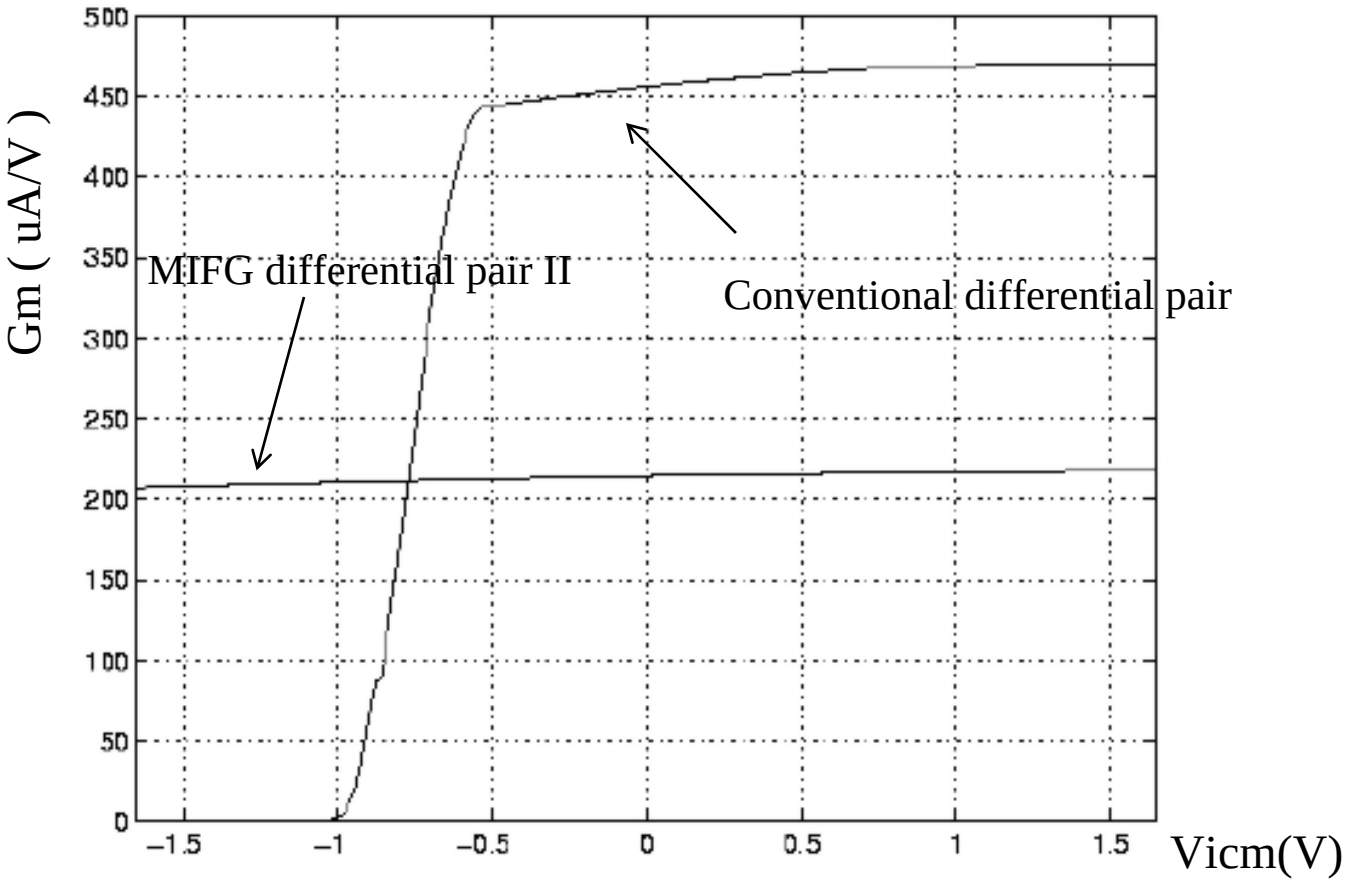
- Simulation results
  - Input output transfer characteristics



We may find out that the linear range is expanded by using MIFG differential stage, the price is that lower gm.

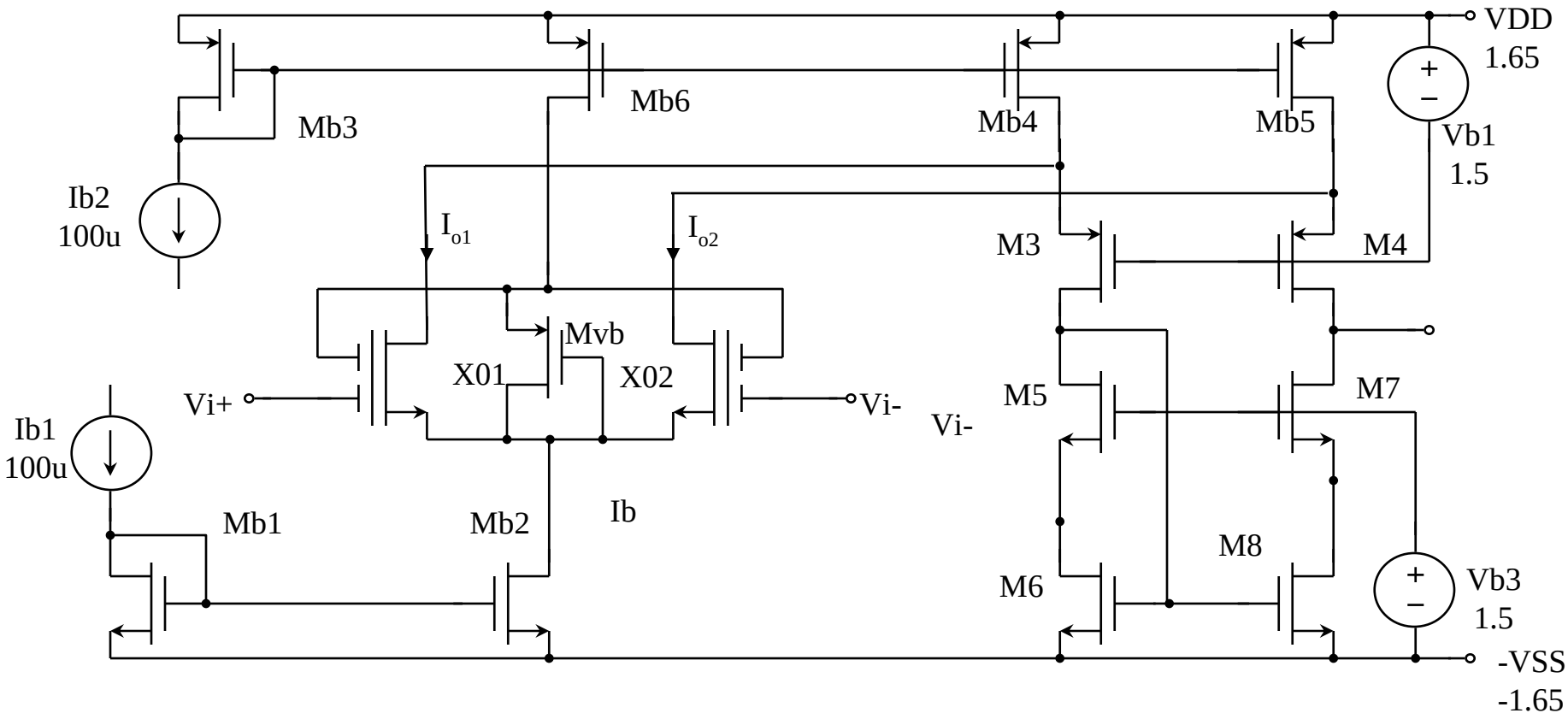
HSPICE simulation of MIFG MOS differential pair II (cont'd)

- Gm vs. Vicm



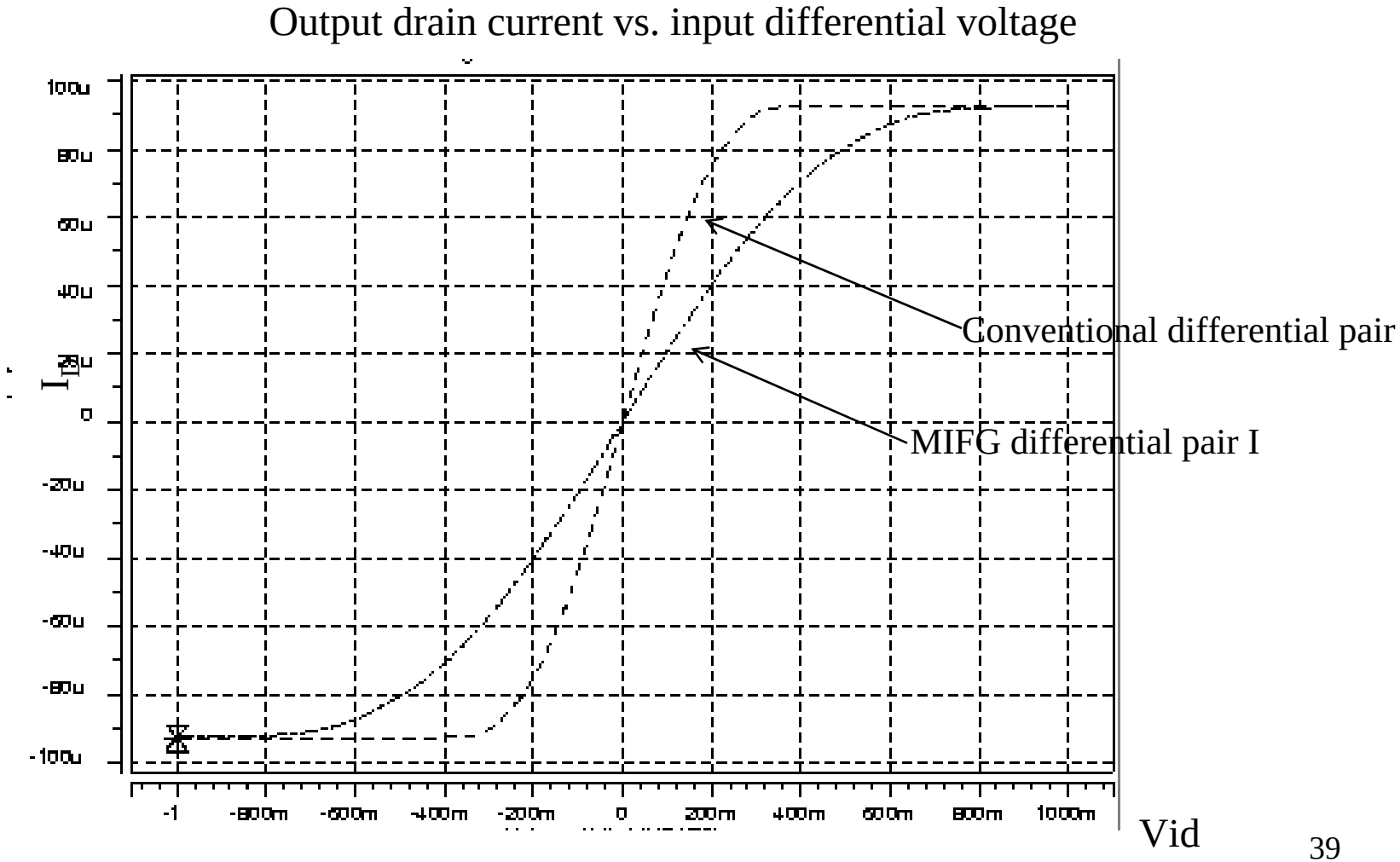
HSPICE simulation of MIFG MOS differential pair I

- The circuit



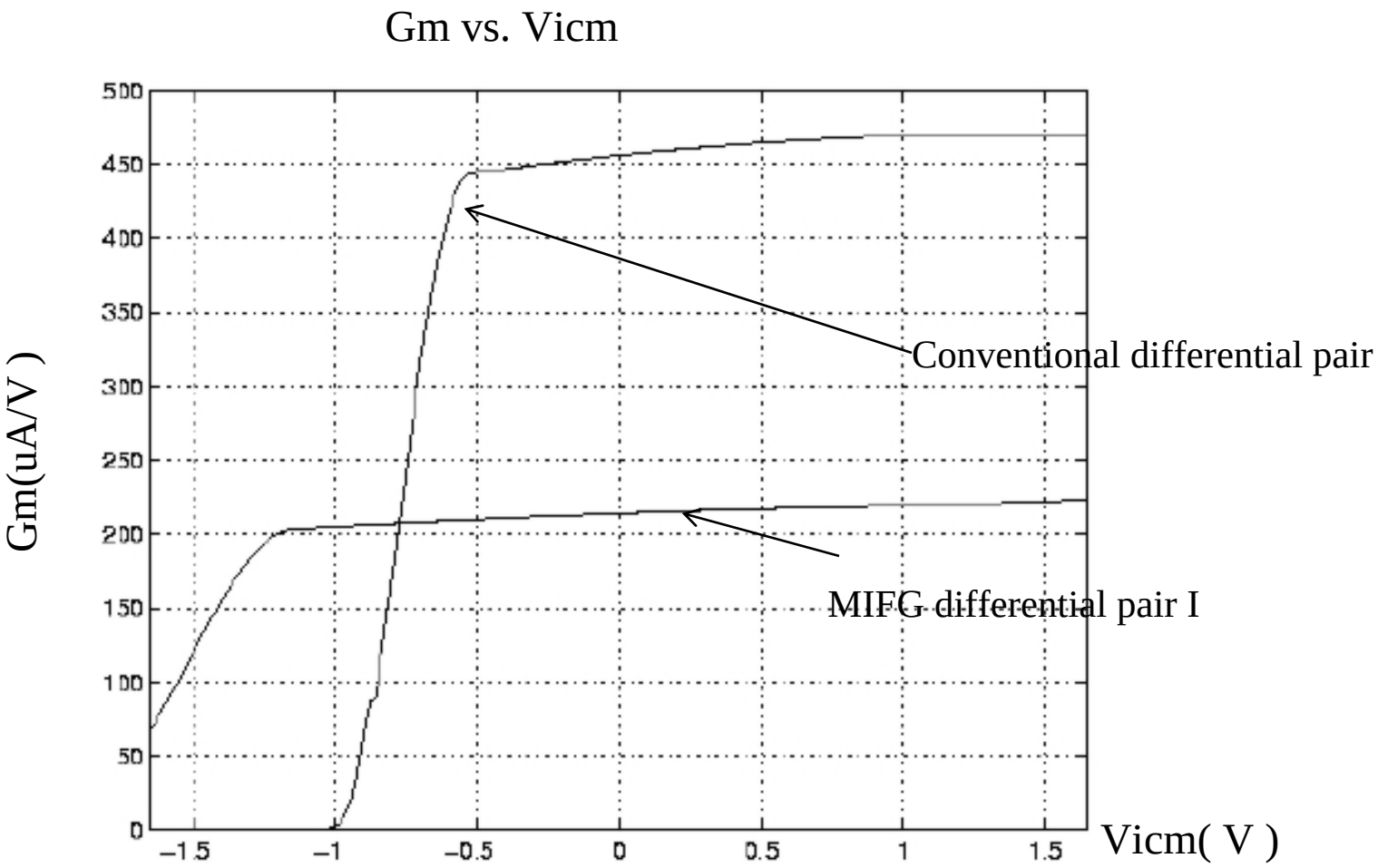
HSPICE simulation of MIFG MOS differential pair I

- Simulation results



HSPICE simulation of MIFG MOS differential pair I

- Simulation results



HSPICE simulation of MIFG MOS differential pair I (cont'd)

- HSPICE file

```
MIFG MOS transistor differential pair I with folded cascode load

.options list node post captab
.include orbit_bsim.mod

* parameters
.param lam = 1u ln = 4u wn1 = 200u wnb = 400u lp=4u wpb=900u wp3=600u
+ wpb6=90u wpvb=32u

* subcircuit for the 2-input floating gate transistor

* .subckt fgnmos drain gate1 gate2 source bulk
.subckt fgnmos d g1 g2 s b
m01 d fg s b cmosn W=wn1 L=ln AD='5*lam*wn1' AS='5*lam*wn1'
+ PS='2*wn1+10*lam' PD='2*wn1+10*lam'
cg1 g1 fg 4p
rg1 g1 fg 1e10
cg2 g2 fg 4p
rg2 g2 fg 1e10
cfgd fg d 59.24f
rfgd fg d 6.7522e11
cfgs fg s 0.5540p
rfgs fg s 7.2202e10
.ends
```

HSPICE simulation of MIFG MOS differential pair I (cont'd)

```
* Transistors of the differential pair
x01 2 ninp nvb 1 nvss fgnmos
x02 3 ninm nvb 1 nvss fgnmos

mb3 20 20 nvdd nvdd cmosp W=wpb L=lp AD='5*lam*wpb' AS='5*lam*wpb'
+ PS='2*wpb+10*lam' PD='2*wpb+10*lam'
mb4 2 20 nvdd nvdd cmosp W=wpb L=lp AD='5*lam*wpb' AS='5*lam*wpb'
+ PS='2*wpb+10*lam' PD='2*wpb+10*lam'
mb5 3 20 nvdd nvdd cmosp W=wpb L=lp AD='5*lam*wpb' AS='5*lam*wpb'
+ PS='2*wpb+10*lam' PD='2*wpb+10*lam'
mb6 nvb 20 nvdd nvdd cmosp W=wpb6 L=lp AD='5*lam*wpb6' AS='5*lam*wpb6'
+ PS='2*wpb6+10*lam' PD='2*wpb6+10*lam'

mvb 1 1 nvb nvb cmosp W=wpvb L=lp AD='5*lam*wpvb' AS='5*lam*wpvb'
+ PS='2*wpvb+10*lam' PD='2*wpvb+10*lam'

m03 4 nvbp 2 nvdd cmosp W=wp3 L=lp AD='5*lam*wp3' AS='5*lam*wp3'
+ PS='2*wp3+10*lam' PD='2*wp3+10*lam'
m04 nout nvbp 3 nvdd cmosp W=wp3 L=lp AD='5*lam*wp3' AS='5*lam*wp3'
+ PS='2*wp3+10*lam' PD='2*wp3+10*lam'

m05 4 nvbn 5 nvss cmosn W=wnb L=ln AD='5*lam*wnb' AS='5*lam*wnb'
+ PS='2*wnb+10*lam' PD='2*wnb+10*lam'
m06 5 4 nvss nvss cmosn W=wnb L=ln AD='5*lam*wnb' AS='5*lam*wnb'
+ PS='2*wnb+10*lam' PD='2*wnb+10*lam'
m07 nout nvbn 6 nvss cmosn W=wnb L=ln AD='5*lam*wnb' AS='5*lam*wnb'
+ PS='2*wnb+10*lam' PD='2*wnb+10*lam'
m08 6 4 nvss nvss cmosn W=wnb L=ln AD='5*lam*wnb' AS='5*lam*wnb'
+ PS='2*wnb+10*lam' PD='2*wnb+10*lam'
```

HSPICE simulation of MIFG MOS differential pair I (cont'd)

```
* Bias current mirror
mb0 10 10 nvss nvss cmosn W=wnb L=ln AD='5*lam*wnb' AS='5*lam*wnb'
+ PS='2*wnb+10*lam' PD='2*wnb+10*lam'
mb1 100 10 nvss nvss cmosn W=wnb L=ln AD='5*lam*wnb' AS='5*lam*wnb'
+ PS='2*wnb+10*lam' PD='2*wnb+10*lam'

* bias current source
ibn nvdd 10 110u
ibp 20 nvss 100u

* Bias voltage for the float gate

* Curent detector
* vd1 nvdd nd1 0.2
* vd2 nvdd nd2 0.2

* Tail current detector
vtail 1 100 0

vtest nout 0 0

vbn nvbn nvss 1.5
vbp nvdd nvbp 1.5
vdd nvdd 0 1.65
vss nvss 0 -1.65
```

HSPICE simulation of MIFG MOS differential pair I (cont'd)

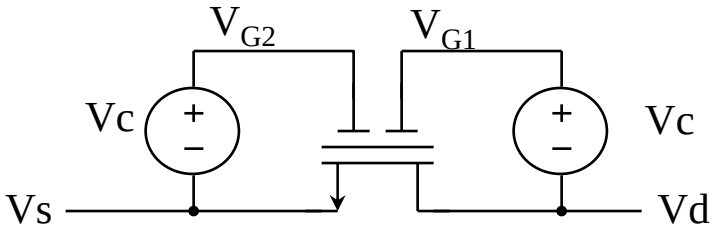
```
* differential input signal source with common mode voltage source
einp ninp ncm input 0 0.5
einm ninm ncm input 0 -0.5
vcm ncm 0 0
vin input 0 0

* test cards
.op
.dc vin -1 1 0.01
.dc vcm -1.65 1.65 0.01

.end
```

Linear floating gate MOS transistor

- The circuit is shown at right

  $V_{G1}=V_C+V_D$, and $V_{G2}=V_C+V_S$, the floating gate voltage can be expressed by

  $V_F=k_1(V_C+V_D)+k_2(V_C+V_S)$,



If we keep the transistor working in ohmic region,

$$I_{DS} = K_P \frac{W}{L}(V_{FGS} - V_T - \frac{V_{DS}}{2})V_{DS}$$

$$= K_P \frac{W}{L}[(k_1 + k_2)V_C + (k_1 - \frac{1}{2}) + (k_2 - \frac{1}{2})V_S - V_T]V_{DS}$$

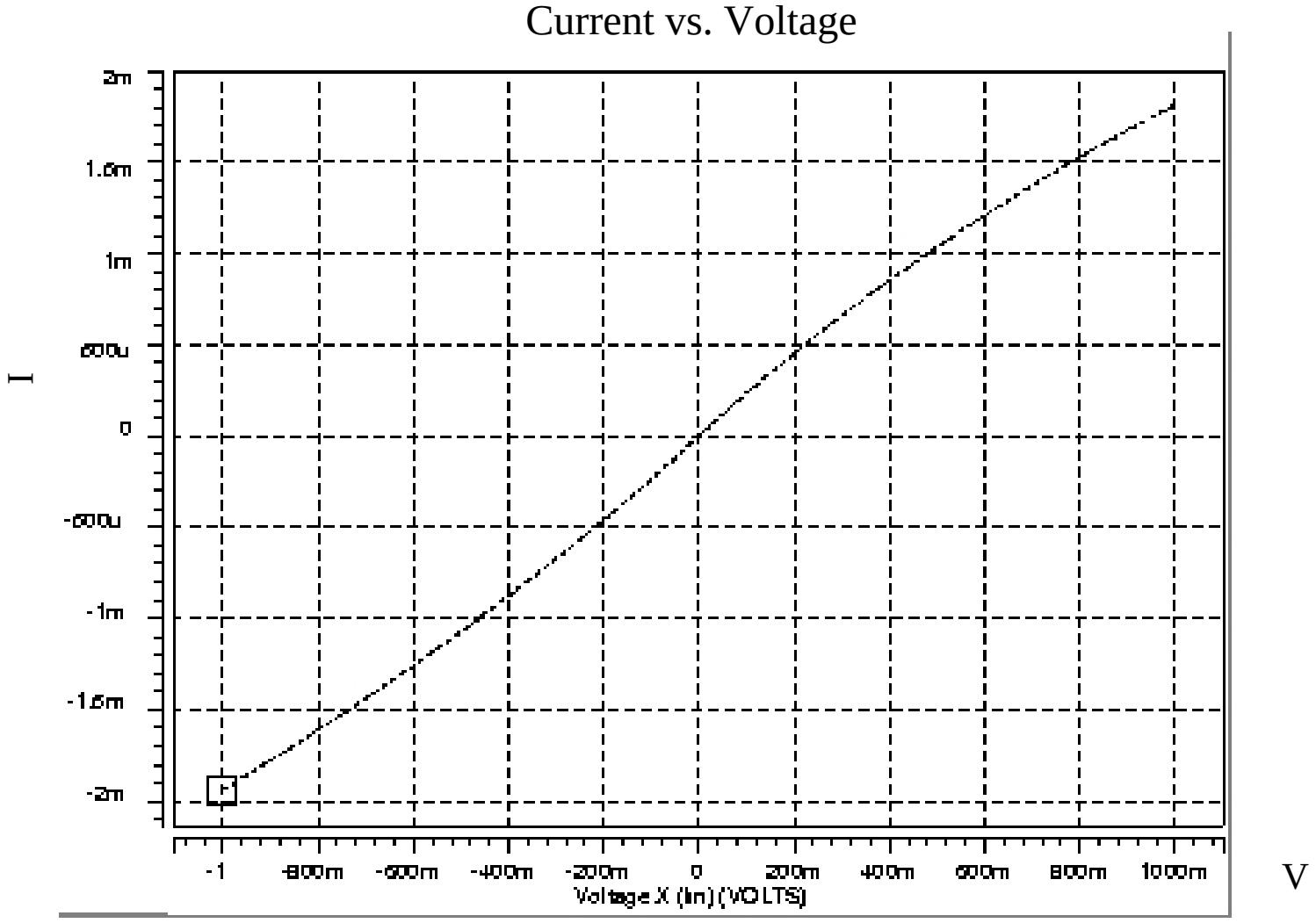
If $k_1 = k_2 = 1/2$, then we can get,

$$I_{DS} = K_P \frac{W}{L}(V_C - V_T)V_{DS}$$

It is a linear V-I reationship!

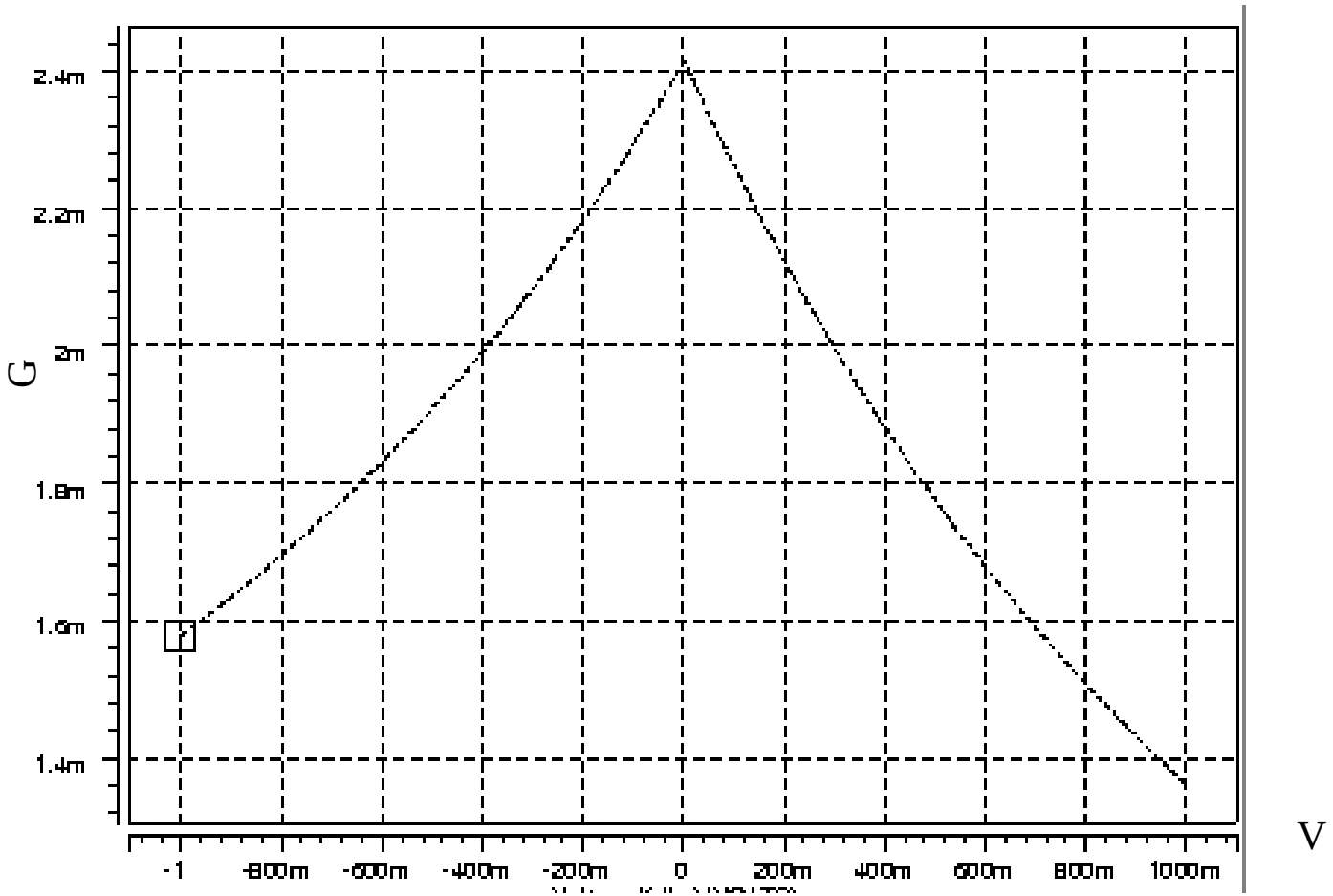
Linear floating gate MOS transistor

- HSPICE simulation results

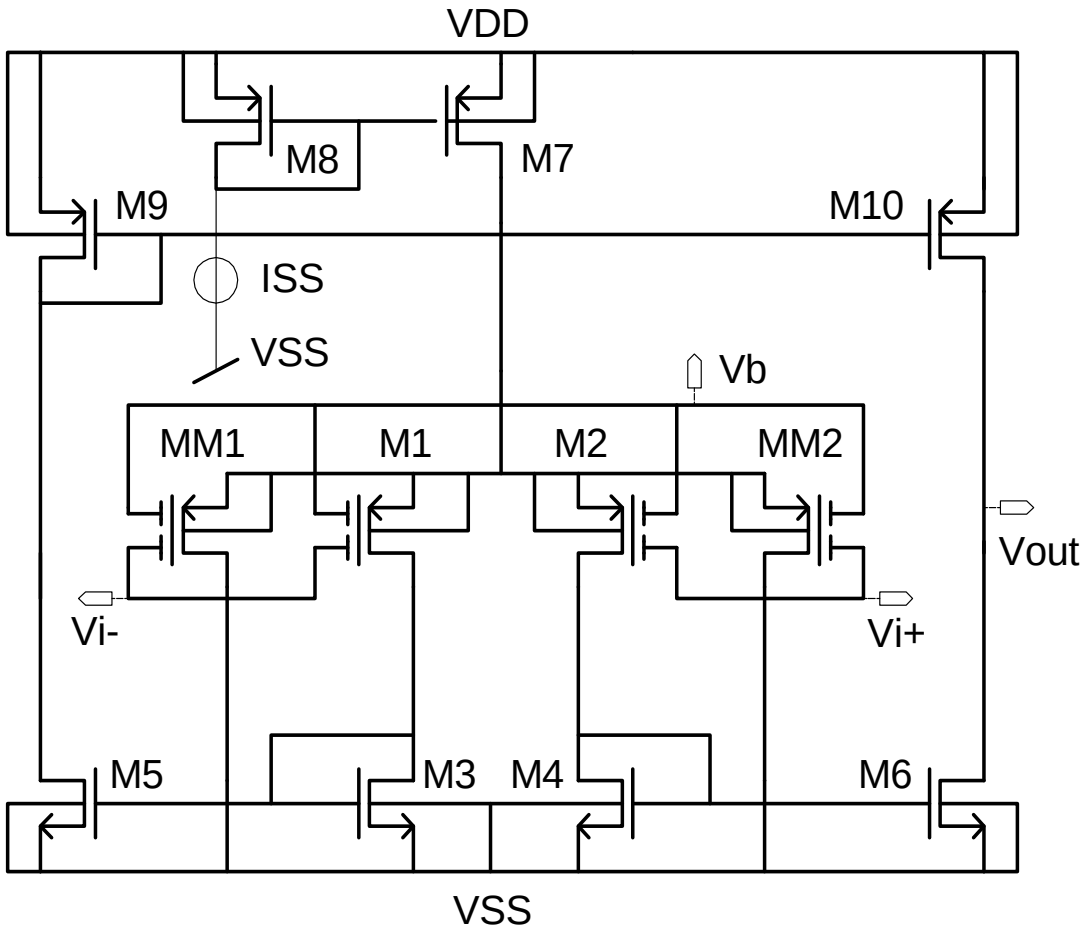


Linear floating gate MOS transistor

G vs. Voltage



FLOATING GATE OTA for LOW Gm



DESCRIPTION AND GOVERNING EQUATIONS

- Features
  1) MM1, MM2, M1and M2 are each now two input floating gate MOSFETS with the common input tied to a fixed bias voltage
  2) MM1 and MM2 are bigger than M1 and M2 by a factor M, which reduces the G_m by about the same factor M, of current division

- Transconductance of the OTA, G_m is given by

$$G_m = \left(\frac{C_{IN}}{C_B + C_{IN}} \right) g_{m\_FGM1}$$

where C_{IN} and C_B are the capacitors from the floating gate to the two inputs of the FGMOS respectively

DESIGN PROCEDURE

- Sizes of M1(M2) are fixed by specifying G_m, $I_{SS}(i_f)$, M and the POLY I-II input caps C_{IN}, C_B

$$\left(\frac{W}{L}\right)_{M1,M2} = \frac{Gm}{2n\mu C_{ox}\varphi_t\left(\frac{C_{IN}}{C_{IN}+C_B}\right)\left(\frac{I_{SS}}{2(M+1)n\varphi_t\left(\frac{Gm}{\left(\frac{C_{IN}}{C_{IN}+C_B}\right)}\right)}-1\right)}$$

- Other transistors sized by specifying I and i_f

$$\left(\frac{W}{L}\right) = \frac{2I}{i_f n\mu C_{ox}\phi_t^{\,2}}$$

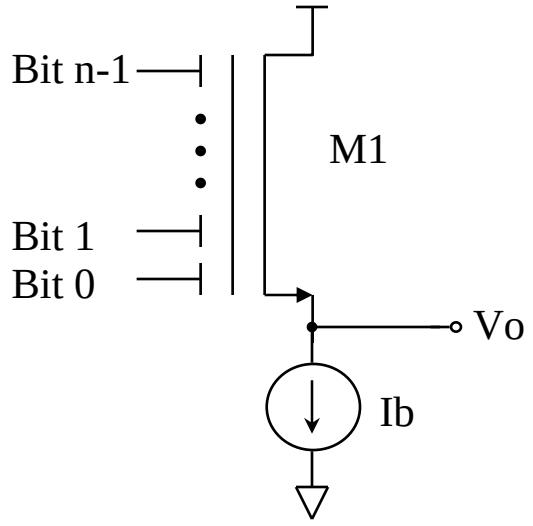
MIFG MOS D/A Converter

– Basic idea

- We know that the floating gate voltage V_{FG} is a weighted sum of the multiple inputs, it is possible to read out the V_{FG}. We can utilize the characteristic of floating MIFG MOS transistors to build D/A converters. Practically, we can have a good matching property of capacitors in conventional CMOS processes. These are the starting point of realizing a MIFG MOS D/A converter.
- It is possible to realize a n-bit D/A converter using one floating gate MOS transistors as shown below.

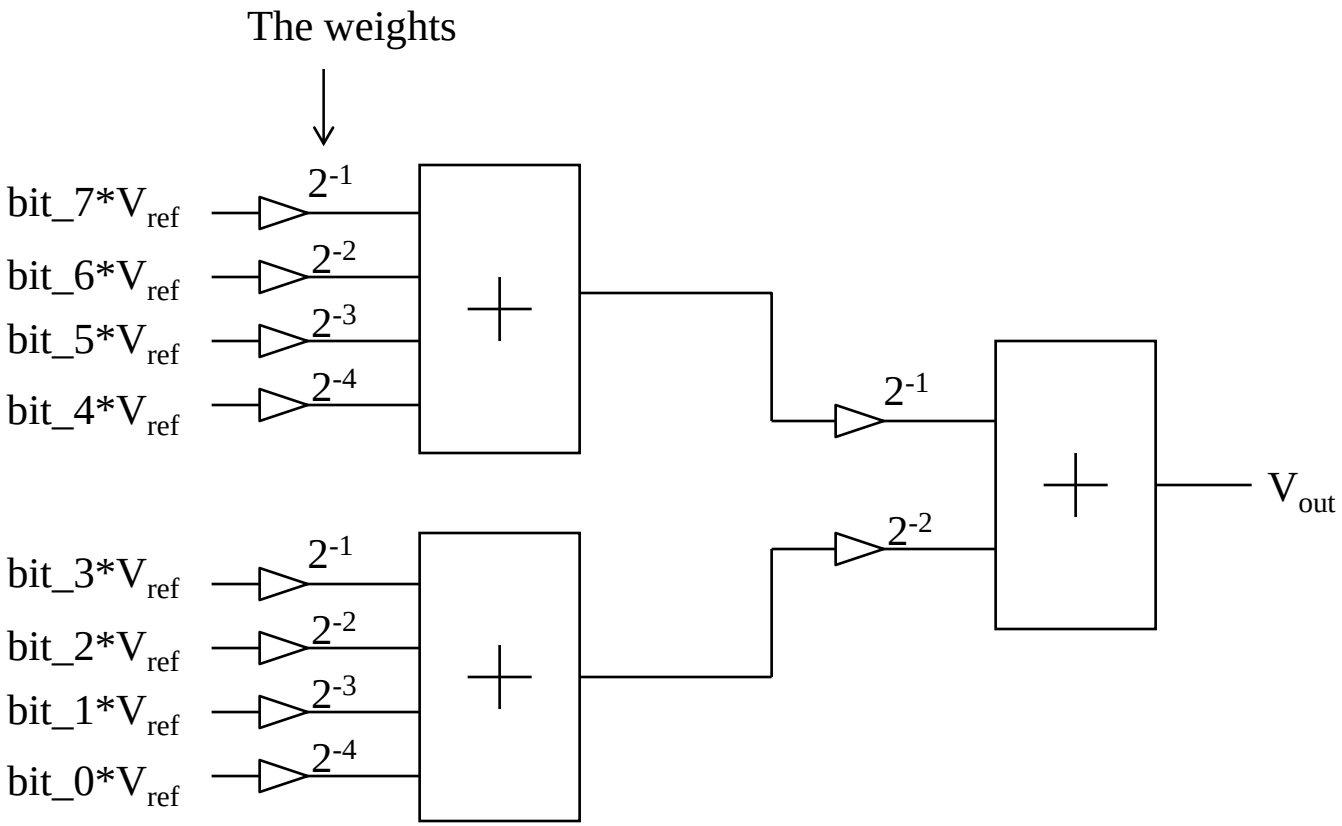
  The main problem of this implementation is that the larger of n, the larger ratio of the biggest capacitor C_{Gn-1} over C_{G0}. That is

$$\frac{C_{Gn-1}}{C_{G0}} = 2^{n-1}$$



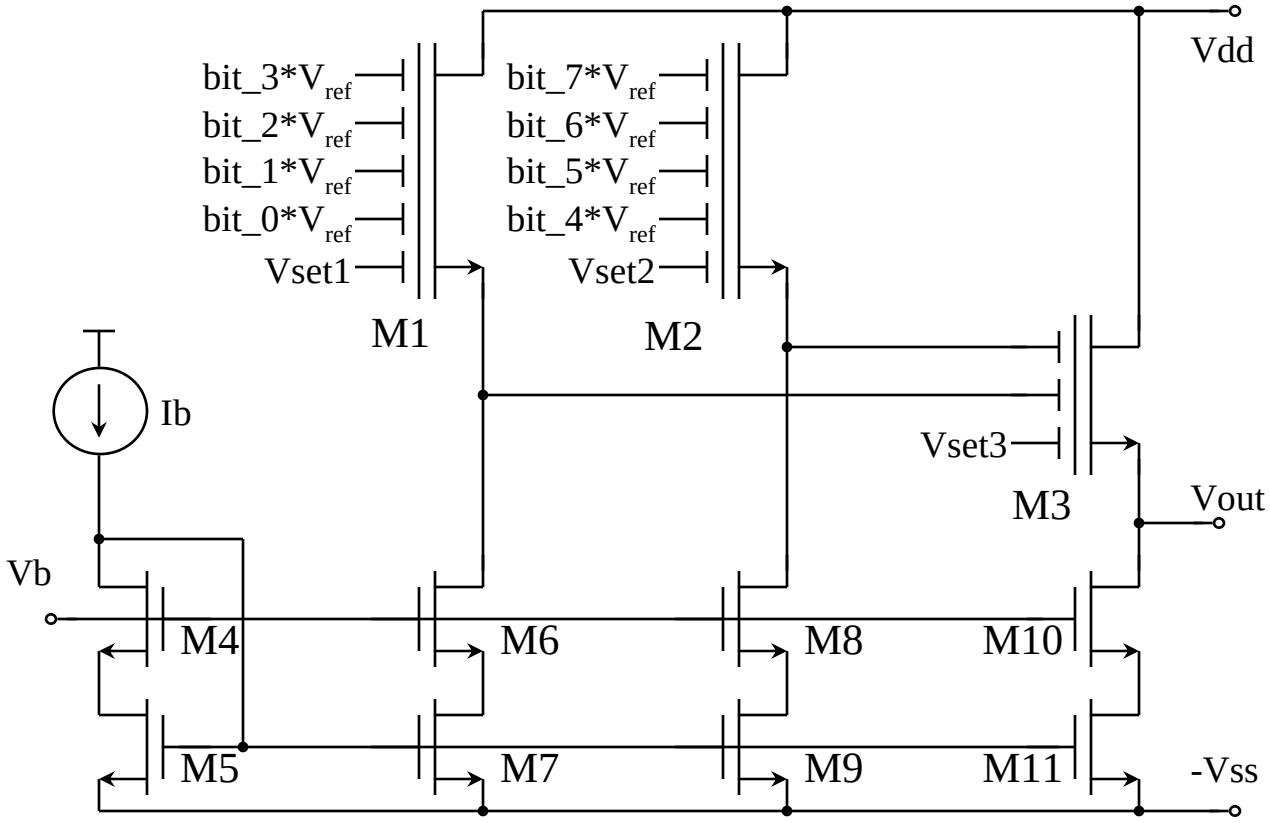
Multiple-Input Floating Gate MOS Transistors

- How about to realize several small D/A converter with fewer bits, such as 3 to 5 bits, and then add the outputs of these small D/A converters together by different weights, as shown in the following diagram (a 8-bit D/A converter).



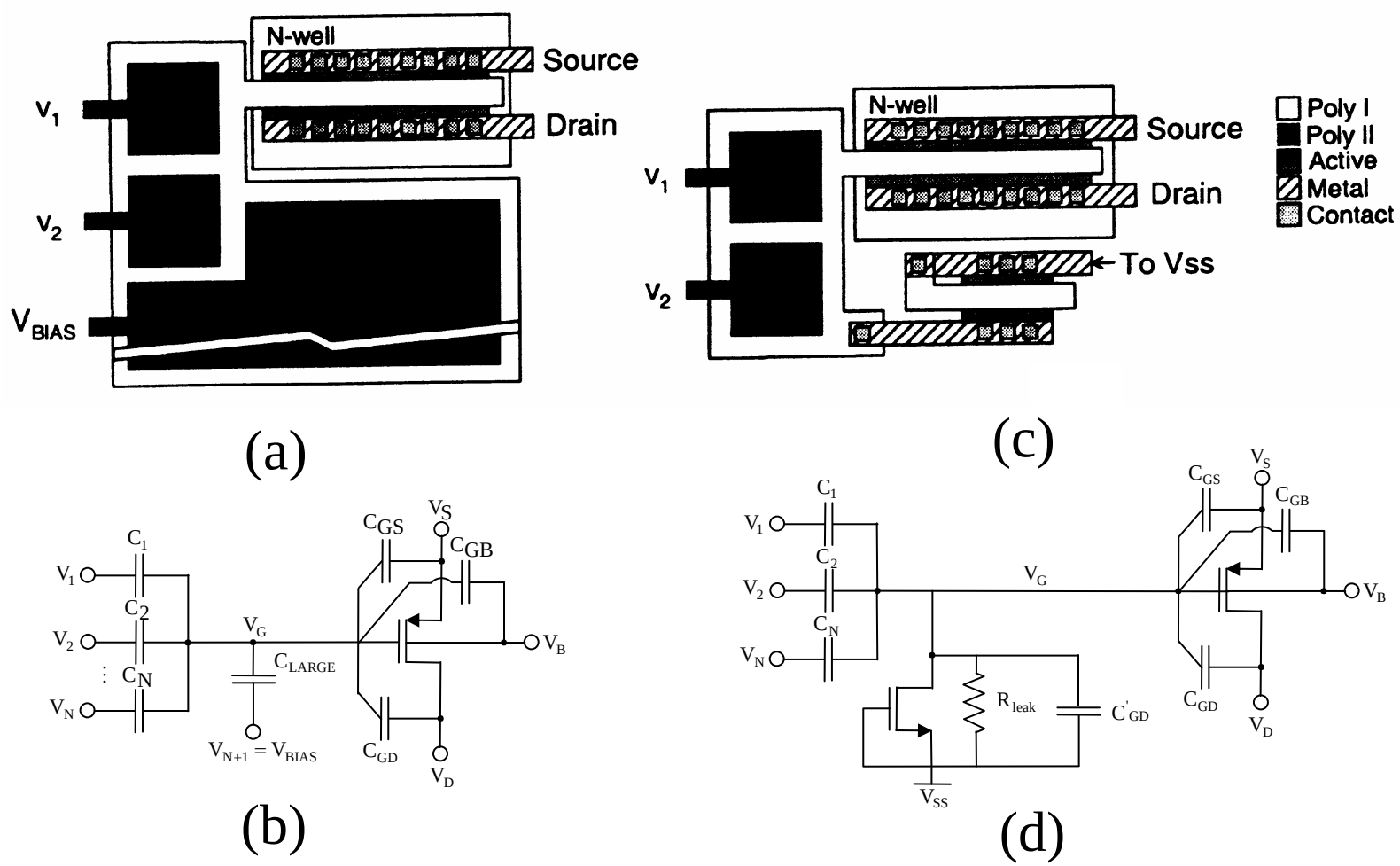
Multiple-Input Floating Gate MOS Transistors

– The circuit



Vset1~Vset3 are used to tune the zero point of the D/A converter.

Multiple Input Floating Gate Transistors



MIFG pMOS transistor. (a) Layout. (b) Equivalent circuit. QFG pMOS transistor. (c) Layout. (d) Equivalent circuit.

Conventional Floating Gate Transistors

$$v_G = \frac{1}{C_T}\left(\sum_{k=1}^{N+1} C_k v_k + C_{GS} v_s + C_{GD} v_D + C_{GB} v_B\right)$$

$$C_{LARGE} = C_{N+1} >> C_N, C_{N-1}, \ldots C_1$$

Thus ,

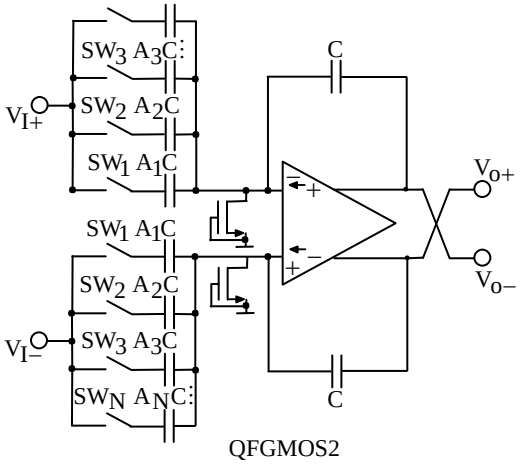
$$v_G = \frac{C_{LARGE}}{C_T} V_{BIAS}$$

$$+ \frac{1}{C_T}\left(\sum_{k=1}^{N} C_k v + C_{GS} v_S + C_{GD} v_D + C_{GB} v_B\right)$$

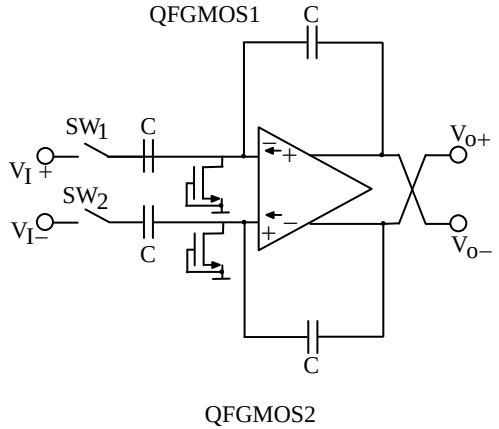
Where

$$C_T = \sum_{k=1}^{N+1} C_k + C_{GS} + C_{GD} + C_{GB}$$

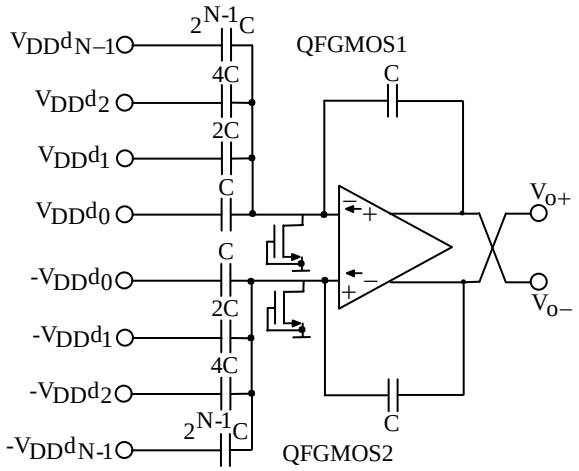
Examples of QFG Structures



(a)



(b)



(c)

Fig. 4. Feedback QFG topologies. (a) PGA. (b) Track and hold. (c) *N*-bit DAC.

For QGG Transistors.

Adding a large resistor from gate connected to Vss for a NMOS transistor (in cut-off) in reverse bias, then:

$$v_G \approx \frac{sR_{leak}}{1 + sR_{leak} C_T} \left(\sum_{k=1}^{N} C_k v_k + C_{GS} v_S + C_{GD} v_D + C_{GB} v_B \right)$$

Where

$$C_T = \sum_{k=1}^{N+1} C_k + C_{GS} + C_{GD} + C_{GB} + C_{GD}'$$

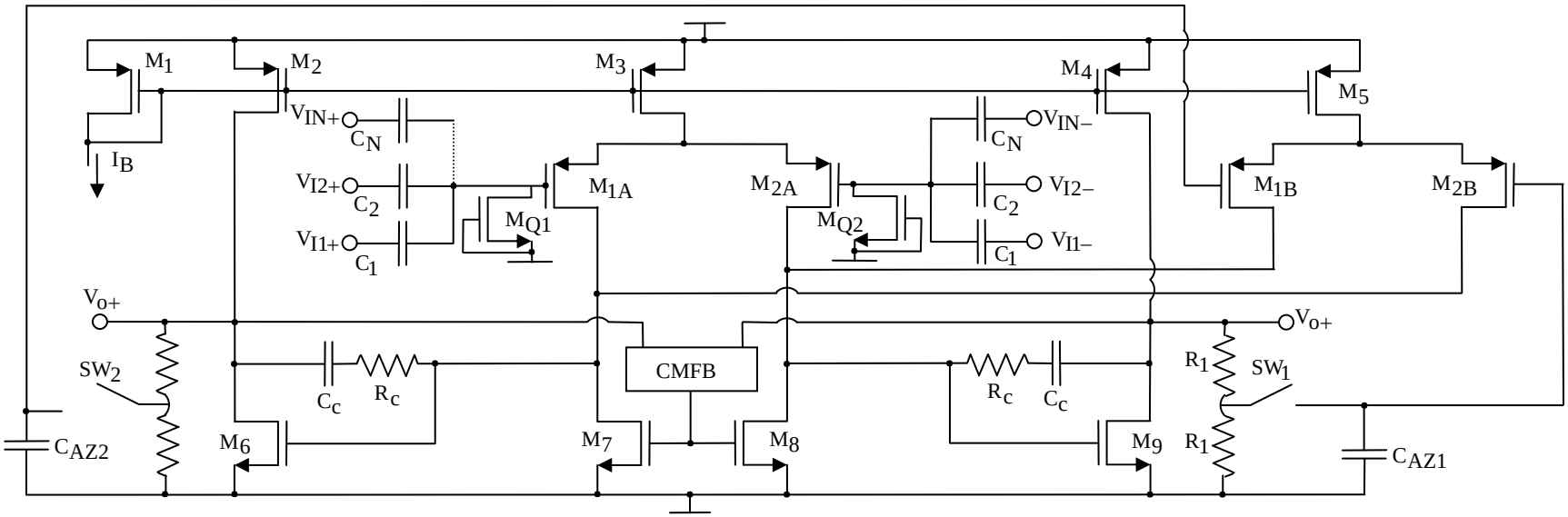
Quasi floating Gate Closed-Loop, via a feedback capacitor, Circuits

- Due to the symmetry of a differential amplifier the effects of the parasitic capacitors are canceled out.

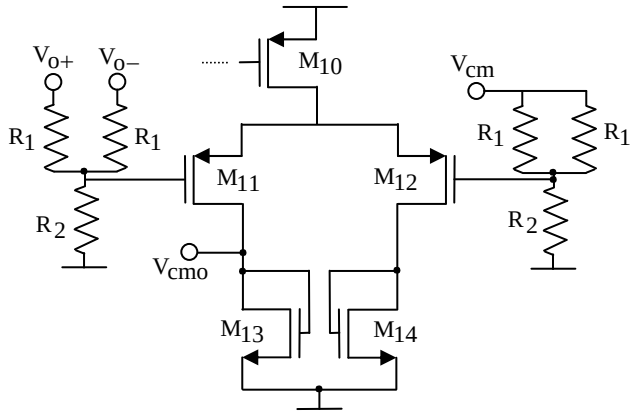
$$v_{G+} - v_{G-} \approx \frac{sR_{leak}}{1 + sR_{leak} C_T} \sum_{k=1}^{N} C_k (v_{k+} - v_{k-})$$

- Feedback reduces the input swing and consequently improves linearity.

- The DC input is set by one of the supply rails that is independent of the feedback network or on the DC output. This however since no Dc path exists, brings the need of an autozeroing circuit.



(a)



(b)

Fig. 5. (a) Amplifier schematic. (b) CMFB circuit

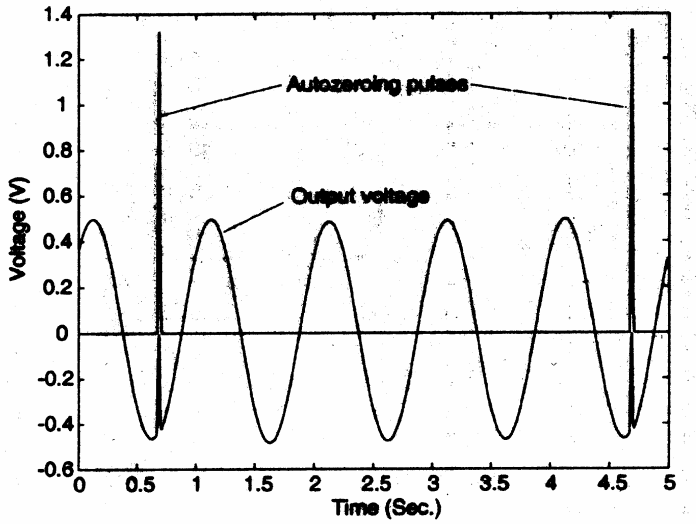


Fig. 7(a)

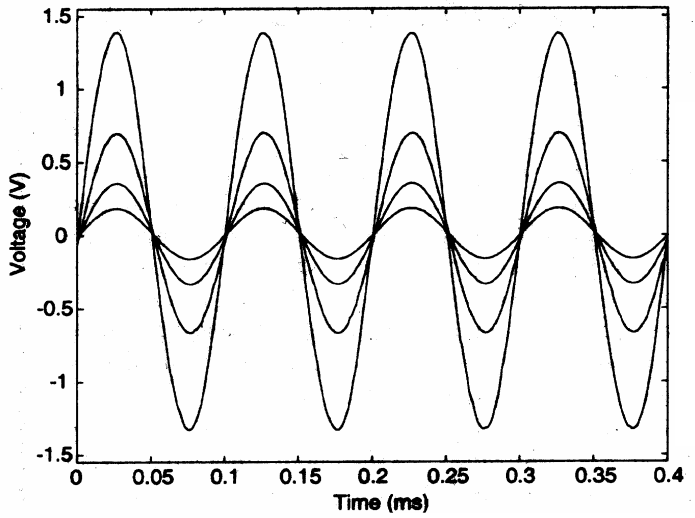


Fig. 7(b)

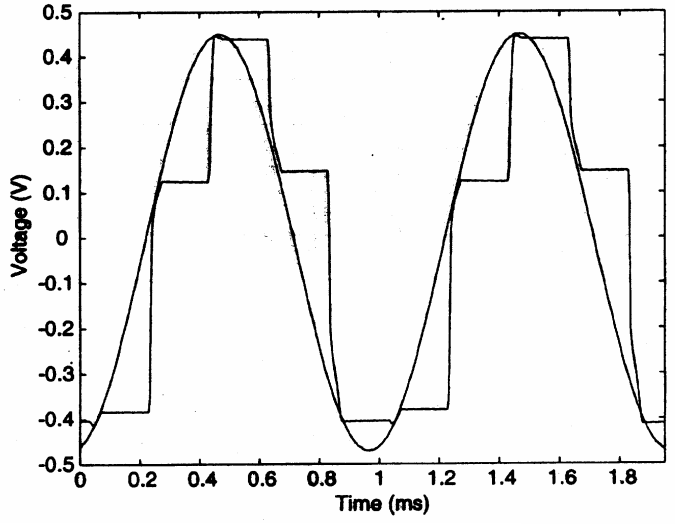


Fig. 8

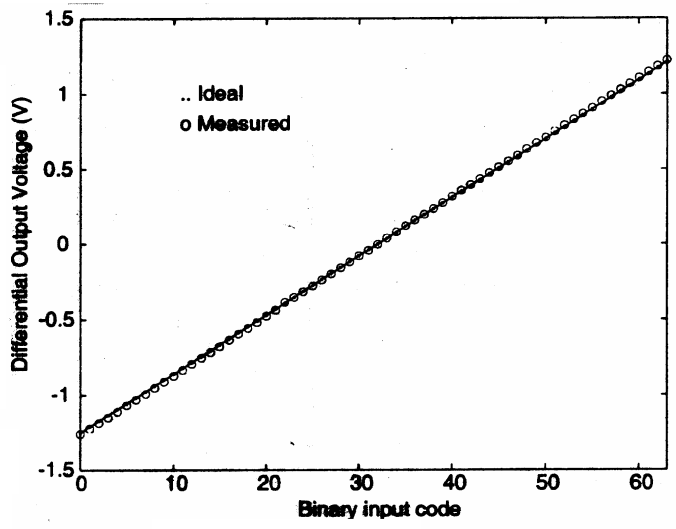


Fig. 9

Fig. 7. (a) Amplifier output voltage and autozeroing clock phase. (b) Amplifier output waveforms for a 10-kHz 0.35-V_{pp} input and different gain values. **Fig. 8.** Measured T/H_{60} output for a 1-kHz input sinusoid. **Fig. 9.** Measured output voltage of the 6-bit DAC.

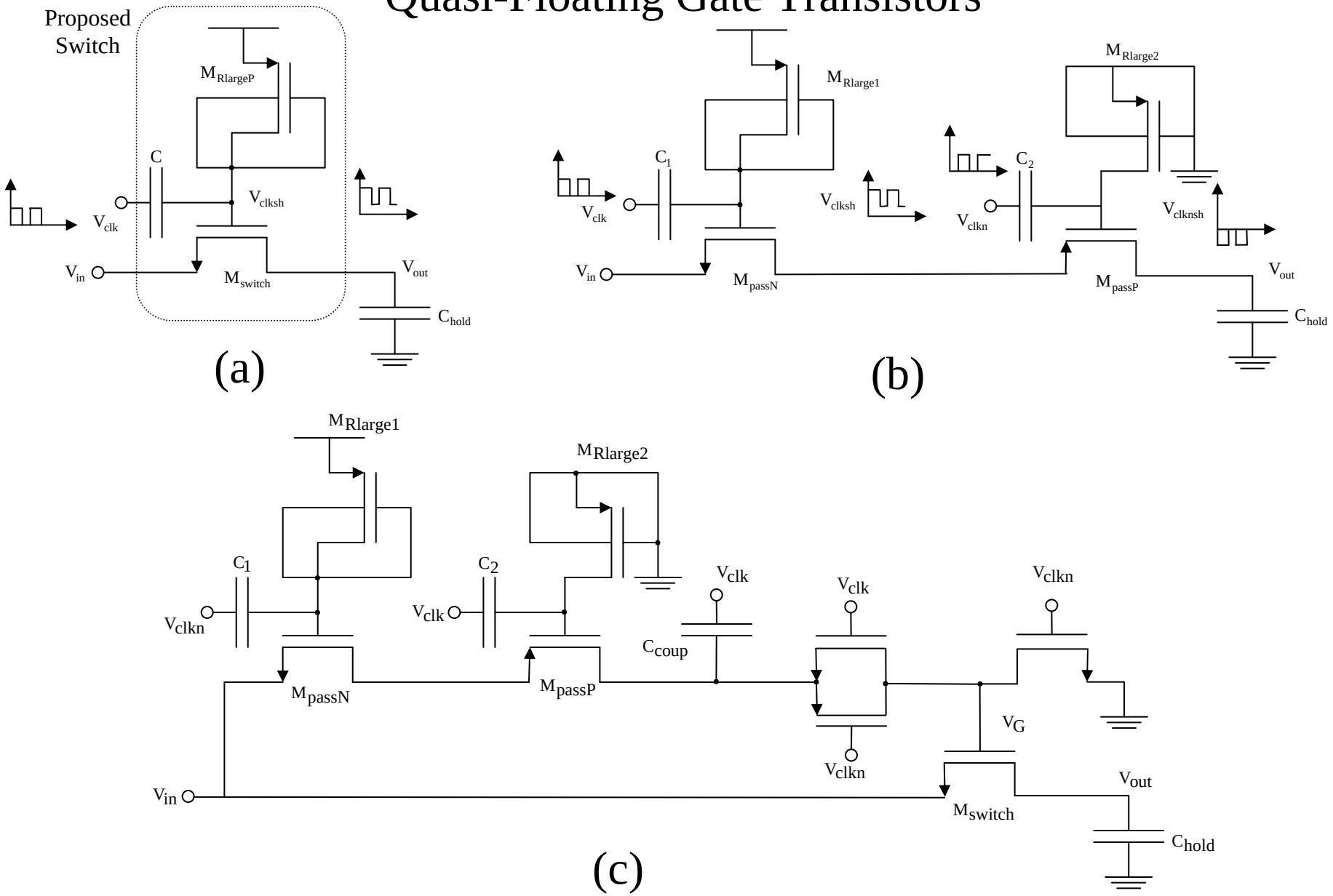
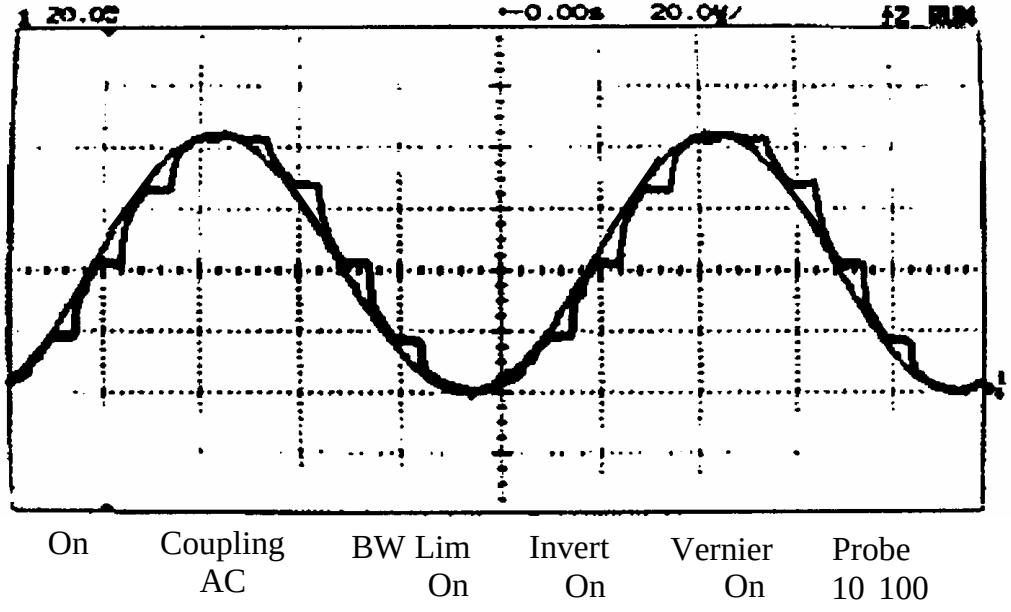
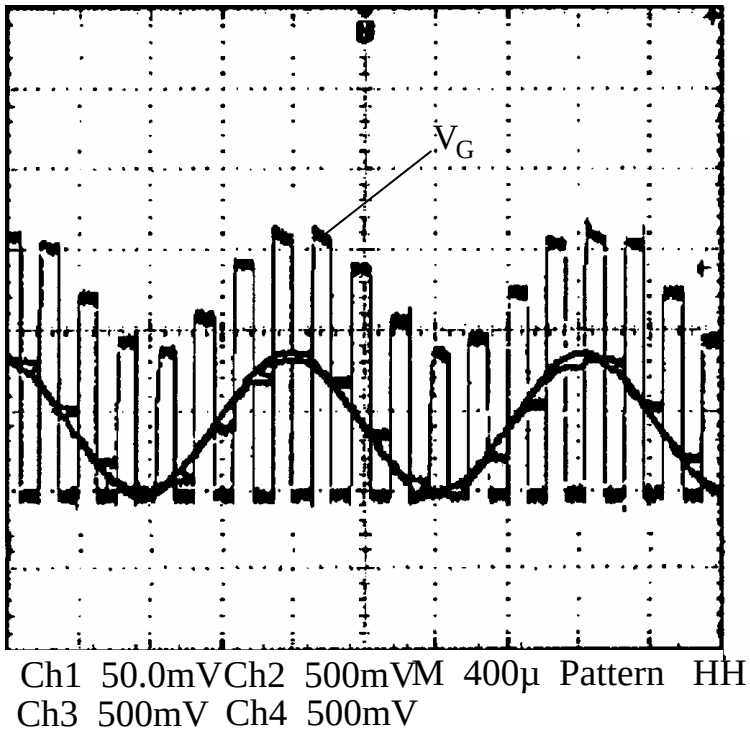


Fig. 2. (a) Almost rail-to-rail T/H with QFG switch. (b) Rail-to-rail T/H with QFG switch. (c) Rail-to-rail T/H with bootstrapped QFG switch.

Experimental Results



(a)



(b)

Fig. 3. (a)Measured input and output waveforms of the circuit of fig. 2(b). (Vertical scale 0.2 V/div). (b) Measured results for the circuit of fig. 2(c). (Vertical scale 0.5 V/div).

Table II

Main Parameters of the Circuits of Fig. 4

PGA		T/H		DAC	
PARAMETER	VALUE	PARAMETER	VALUE	PARAMETER	VALUE
Technology	0.5 μm	Technology	0.5 μm	Technology	0.5 μm
Supply Voltage	1.5 V	Supply Voltage	±0.75 V	Supply Voltage	±0.75 V
Gain error (G=1)	0.11%	Acquisition time	1.2 μs	Resolution	6 bit
Bandwidth (G=1)	4 MHz	Overshoot	85 mV	Max. INL	0.15 LSB
THD @ 10kHz, 2.8V_{pp}	0.65%	Settling time	750 ns	Max. DNL	0.12 LSB
Input equiv. noise (10kHz)	182nV/$\sqrt{Hz}$	Bandwidth	4 MHz	Settling time	400 ns
Static power consumption	0.78 mW	Pedestal error	8 mV	Offset error	0.07 LSB
Silicon area	0.20 mm^2	Static power consumption	0.40 mW	Gain Error	1.1%
		Silicon area	0.16 mm^2	SFDR (10kHz)	64 dB
				Static power consumption	0.80 mW
				Silicon area	0.38 mm^2

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