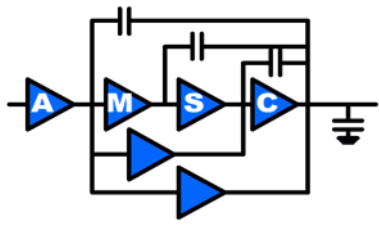
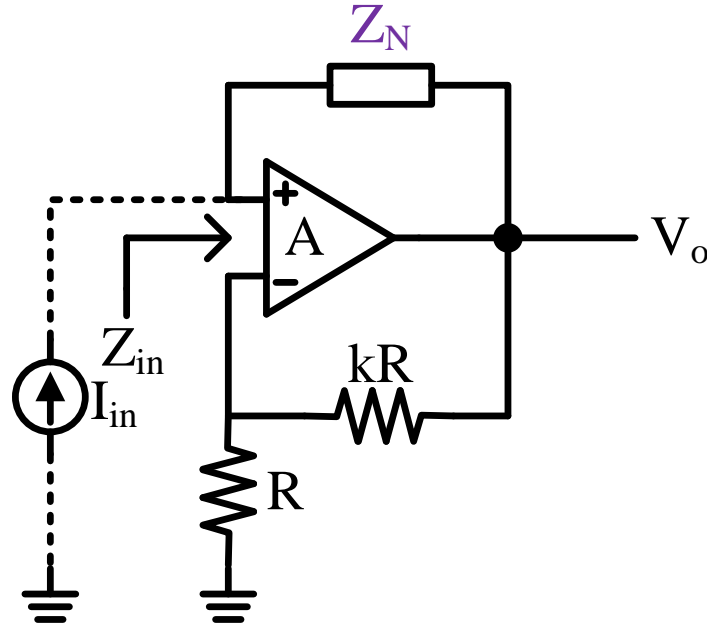


# Negative Impedance Converter (NIC) and Applications

Edgar Sánchez-Sinencio  
TI J. Kilby Chair Professor



# NEGATIVE IMPEDANCE CONVERTER (NIC)



$$\frac{V_+}{Z_N} - \frac{V_o}{Z_N} = I_{in} \quad (1)$$

$$-\frac{V_o}{kR} + \left( \frac{1}{R} + \frac{1}{kR} \right) V_- = 0 \quad (2)$$

$$V_o = (A)(V_+ - V_-) \quad (3)$$

Yields

$$Z_{in} = -Z_N \frac{1+k+A}{k(A-1)+1} = -Z_N \frac{1+\frac{1+k}{A}}{k-\frac{1-k}{A}}$$

$$Z_{in} \Big|_{A \rightarrow \infty} \cong -\frac{Z_N}{k}$$

For  $A(s) \cong \frac{GB}{s}$

$$Z_{in} = -\frac{Z_N}{k} \frac{1+s/\omega_Z}{1+s/\omega_p} \quad ; \quad \omega_Z = \frac{GB}{1+k} \quad ; \quad \omega_p = \frac{GB}{-1+\frac{1}{k}} : k < 1$$

# Negative Impedance Implementations

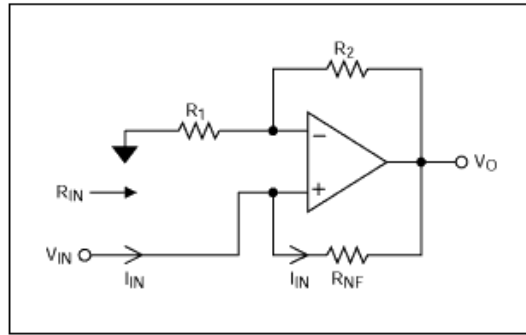


Figure 1. This circuit produces a negative resistance of  $R_{in} = -R_n f(R_1/R_2)$ .

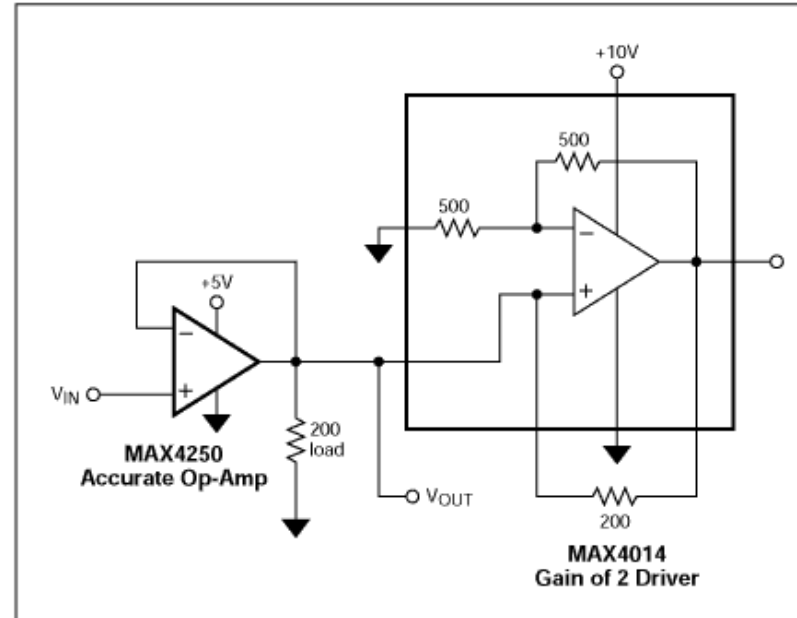


Figure 2. Connecting a load-cancelling negative resistor in parallel with the load.

Reference:

<https://www.maximintegrated.com/en/app-notes/index.mvp/id/1868>

# Negative Resistance Applications

## Gm with negative resistor

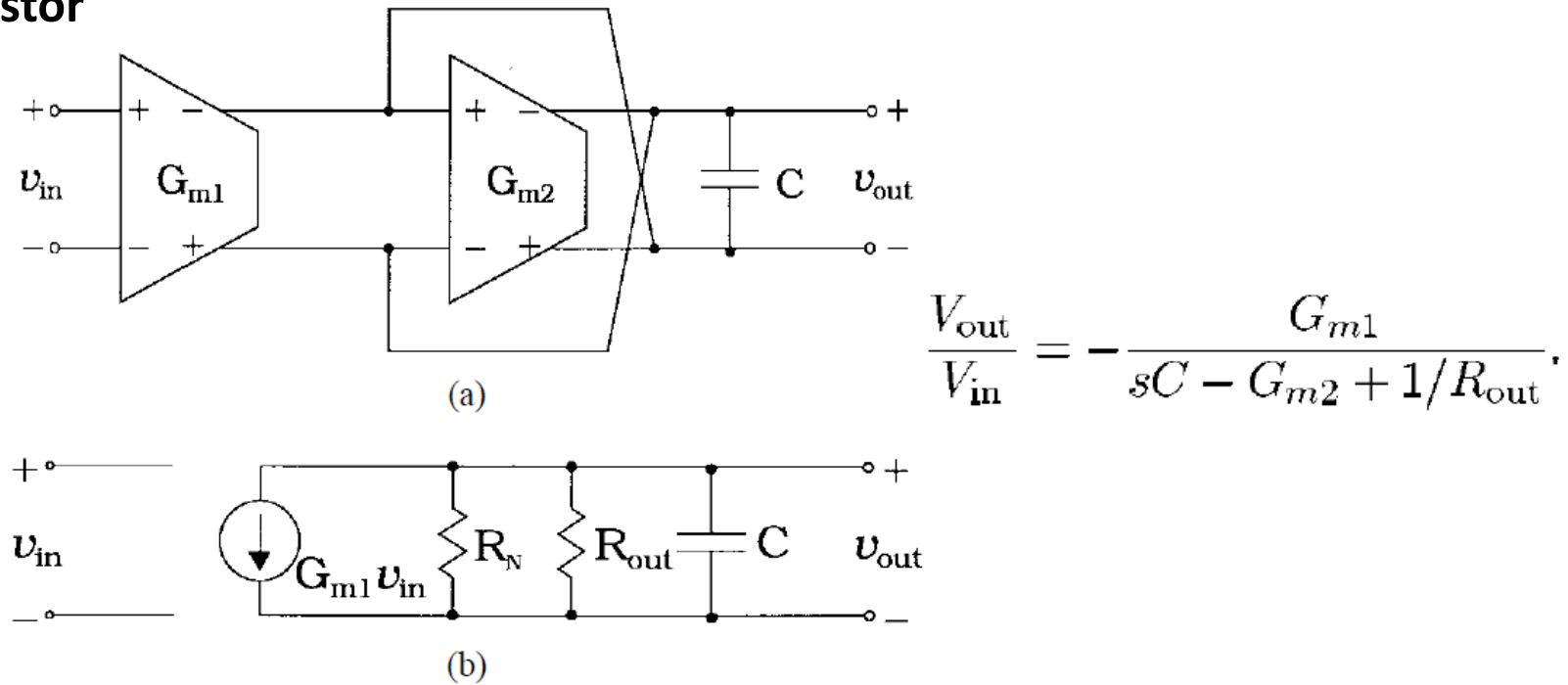
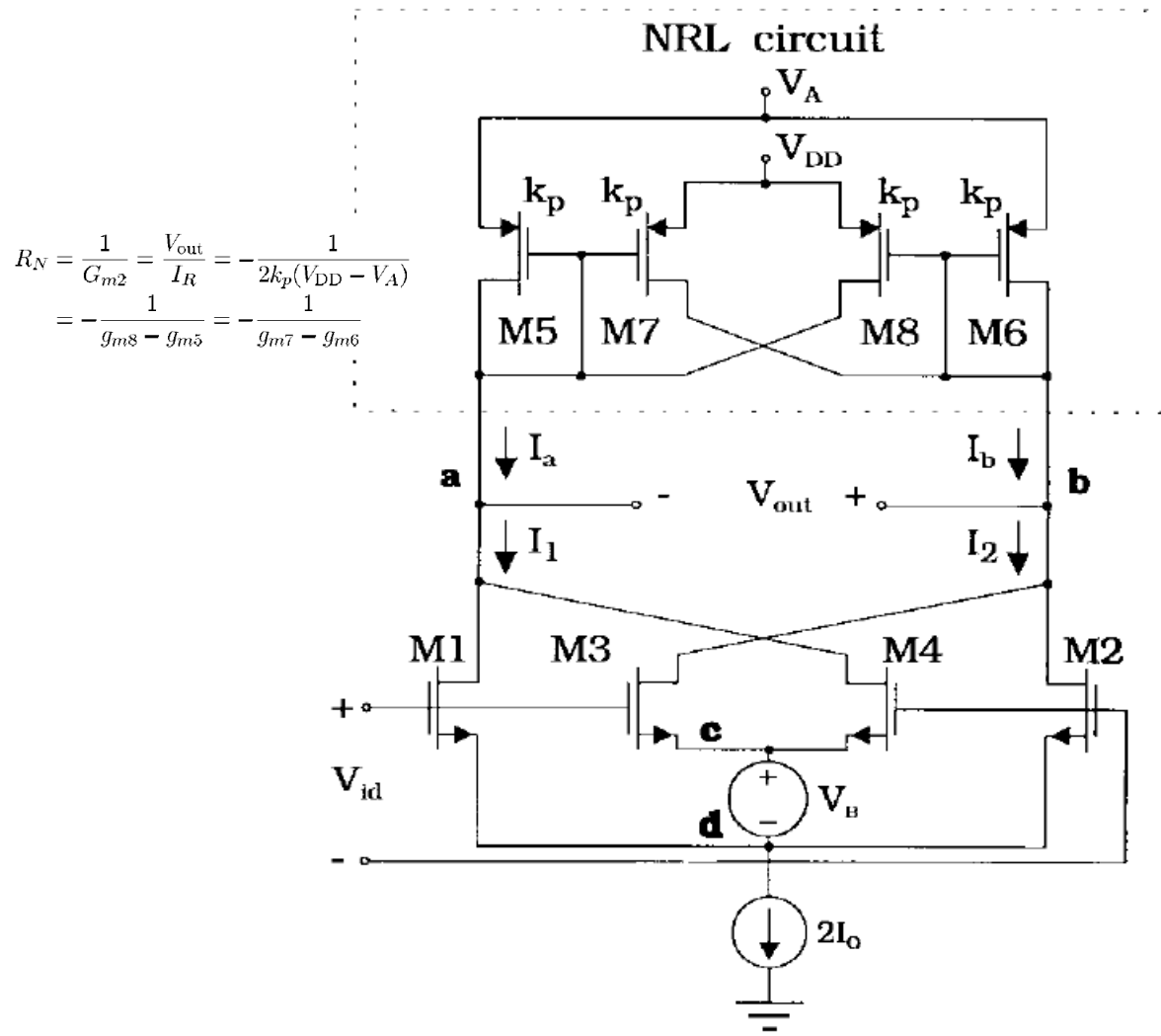


Fig. 1. (a) Conceptual block diagram of the OTA-C integrator with high dc gain. (b) Small-signal macromodel including parasitic output resistance  $R_{out}$  in parallel with a negative resistance  $R_N$ .

Reference: S. Szczepanski, J. Jakusz and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 3, pp. 174-187, Mar 1997.



$$I_1 = I_0 + \frac{I_{out}}{2} = k_n(V_P - V_{Tn})^2 + k_n(V_Q - V_B - V_{Tn})^2 \quad (4)$$

$$I_2 = I_0 - \frac{I_{out}}{2} = k_n(V_Q - V_{Tn})^2 + k_n(V_P - V_B - V_{Tn})^2 \quad (5)$$

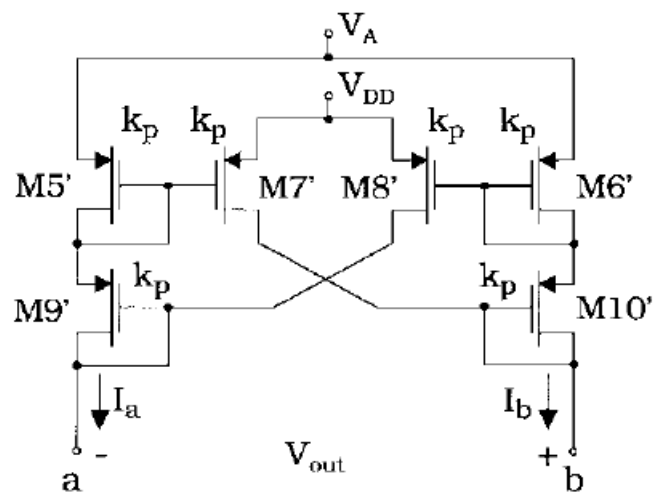
$$I_{out} = I_1 - I_2 = 2k_n V_B (V_P - V_Q) = 2k_n V_B V_{id} \quad (6)$$

$$I_{out} = 2k_n [V_{Boc} + r_{outB}(I_{d3} + I_{d4})] V_{id} \quad (7)$$

$$|V_{id}| \leq \sqrt{I_0/k_n - 3V_B^2/4} - V_B/2 \quad (9)$$

which requires that the common-mode voltage  $V_{ic} \geq V_{Tn} + V_B + V_{DSsat}$ , where  $V_{DSsat}$  is the minimum voltage required for the current source  $2I_0$  to operate in saturation.

Fig. 3. Simplified scheme of the proposed CMOS OTA with a voltage-variable NRL circuit.



(a)

(v)

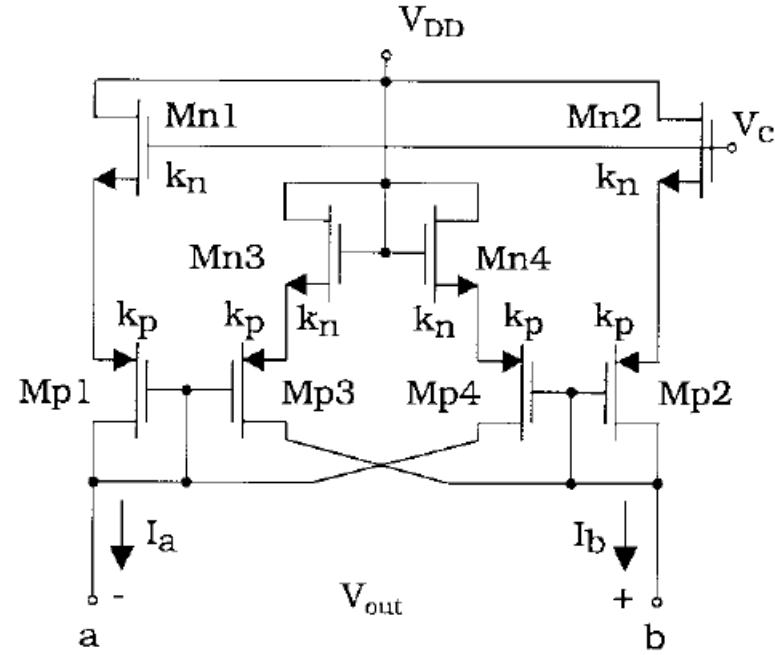


Fig. 12. Alternative topology for an NRL element based on two CMOS double pairs.

$$I_R = I_a - I_b = 2k_{\text{eff}}(V_C - V_{DD})V_{\text{out}} \quad (35)$$

$$R_N = \frac{V_{\text{out}}}{I_R} = -\frac{1}{2k_{\text{eff}}(V_{DD} - V_C)}. \quad (39)$$

To keep this circuit working linearly, the following conditions should be satisfied

$$|V_{\text{out}}| \leq \sqrt{\frac{I_o}{k_{\text{eff}}} - \frac{3}{4}(V_{DD} - V_C)^2} - \frac{V_{DD} - V_C}{2} \quad (40)$$

$$|V_{\text{out}}| \leq V_{T\Sigma} \quad (41)$$

Floating bias source: Ma1-  
Ma3 & Mb1-Mb3

$$V_B = V_{gsMa3} + \sqrt{\frac{I_{CF}}{k_n Ma2}} - \sqrt{\frac{I_S - I_{CF}}{k_n Ma1}} \quad (50)$$

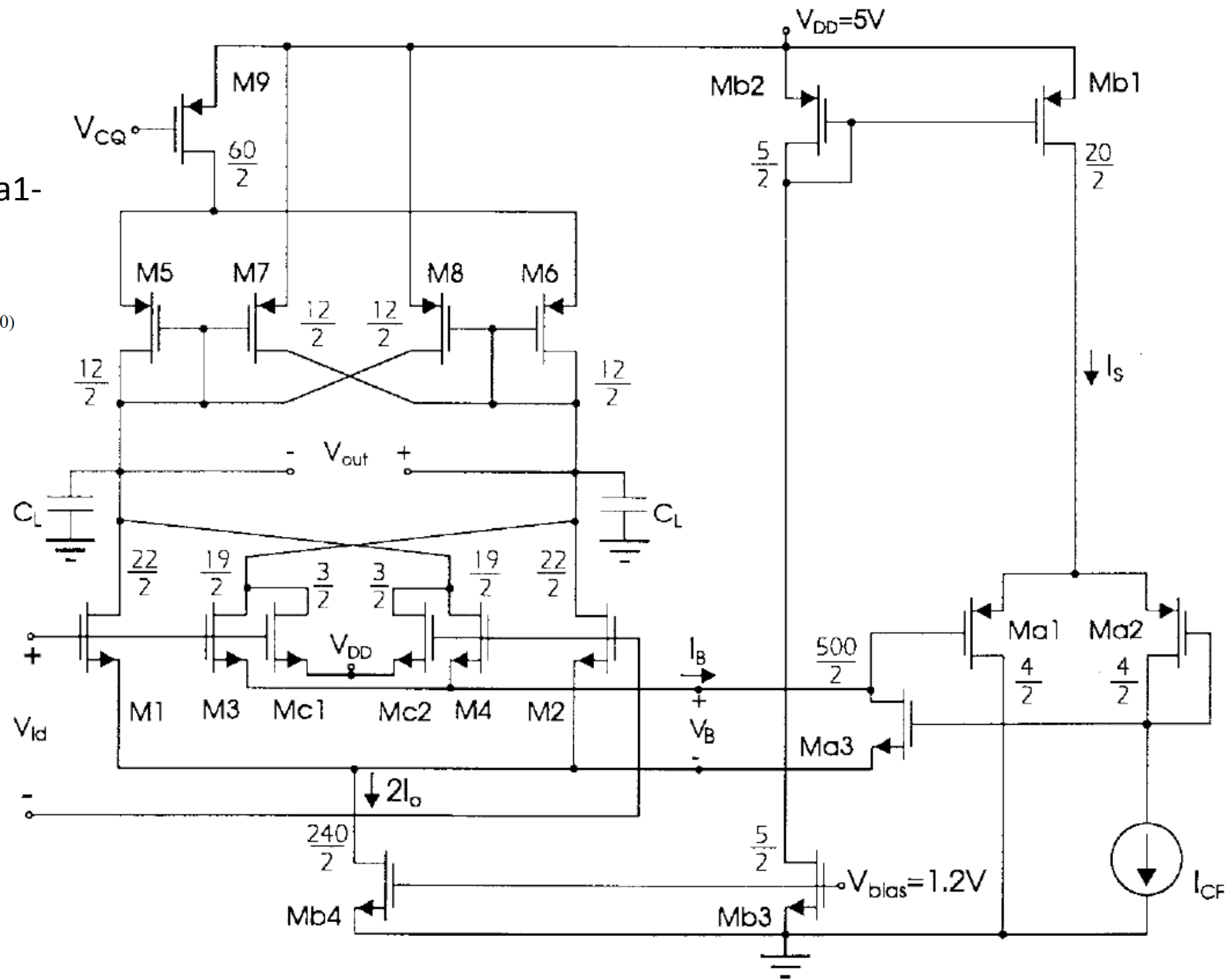
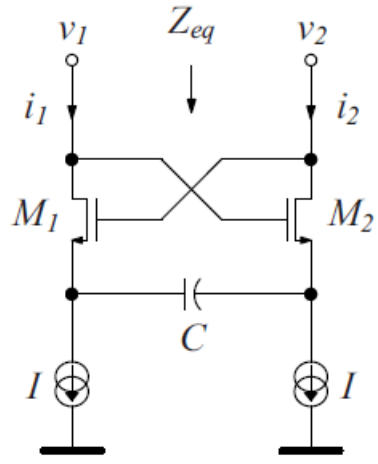


Fig. 14. Complete circuit diagram of the CMOS OTA with the NRL.



The simple negative capacitance generator

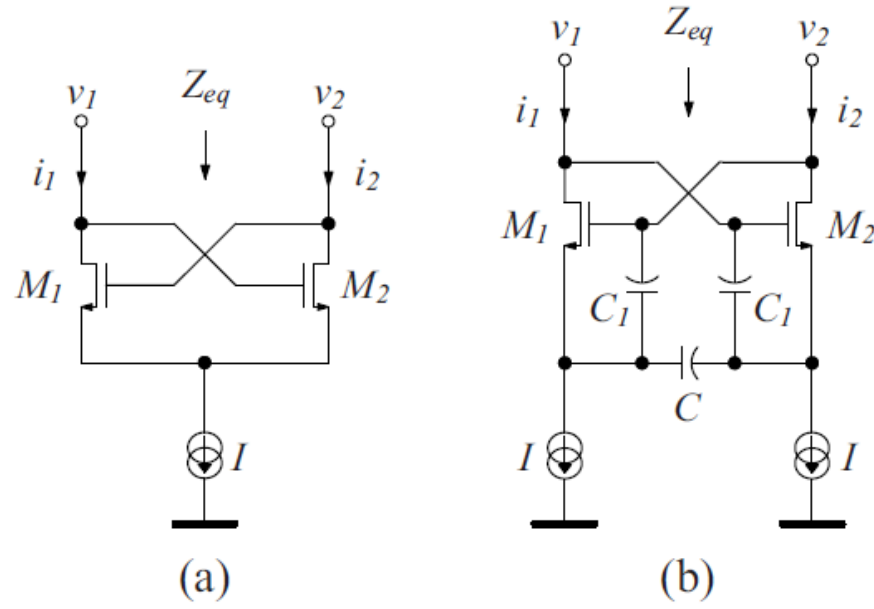
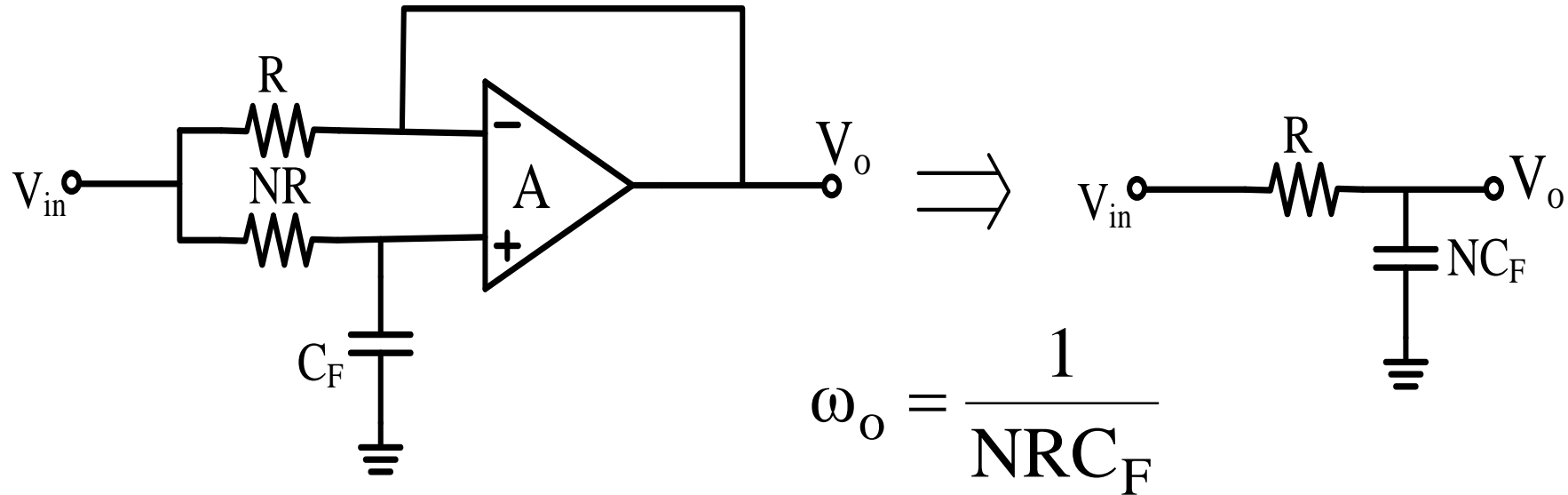


Figure 2. Schematic diagrams of (a) negative resistance and (b) negative inductance generators

$$Z_{equ} = -\frac{1}{sC} \frac{g_m + s(C_{GS} + 2C)}{g_m - sC_{GS}}$$



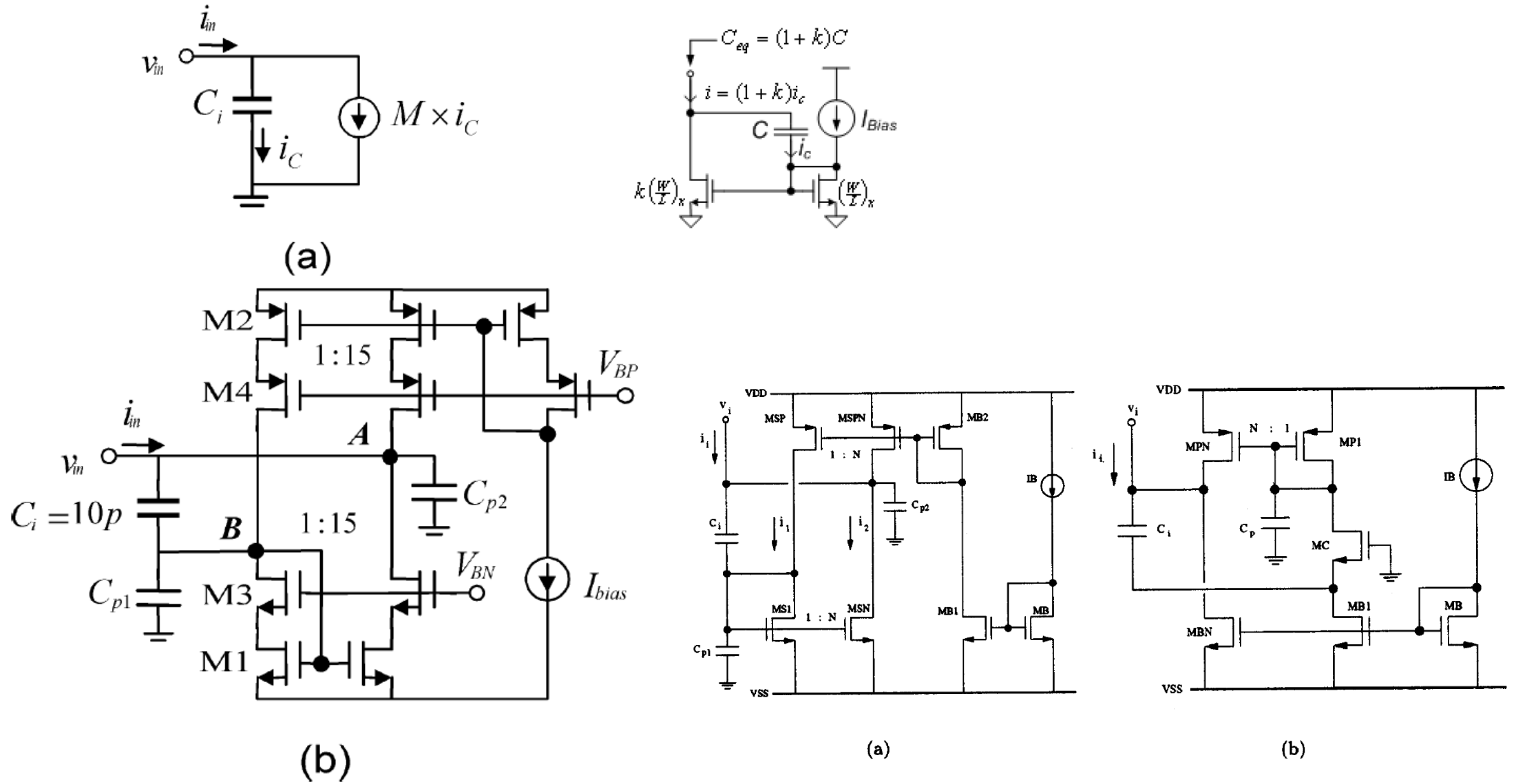
# CAPACITANCE MULTIPLIER



$$\omega_o = \frac{1}{NRC_F}$$

$$\frac{V_o}{V_{in}} = \frac{1}{(1 + sR(NC_F))(1 + 1/A)}$$

# CAPACITANCE MULTIPLIER



Scaling up a grounded capacitance. (a) Basic circuit. (b) Capacitance scaler using a cascode transistor.

Fig. 6. Capacitance multiplier. (a) Principle. (b) Circuit implementation.

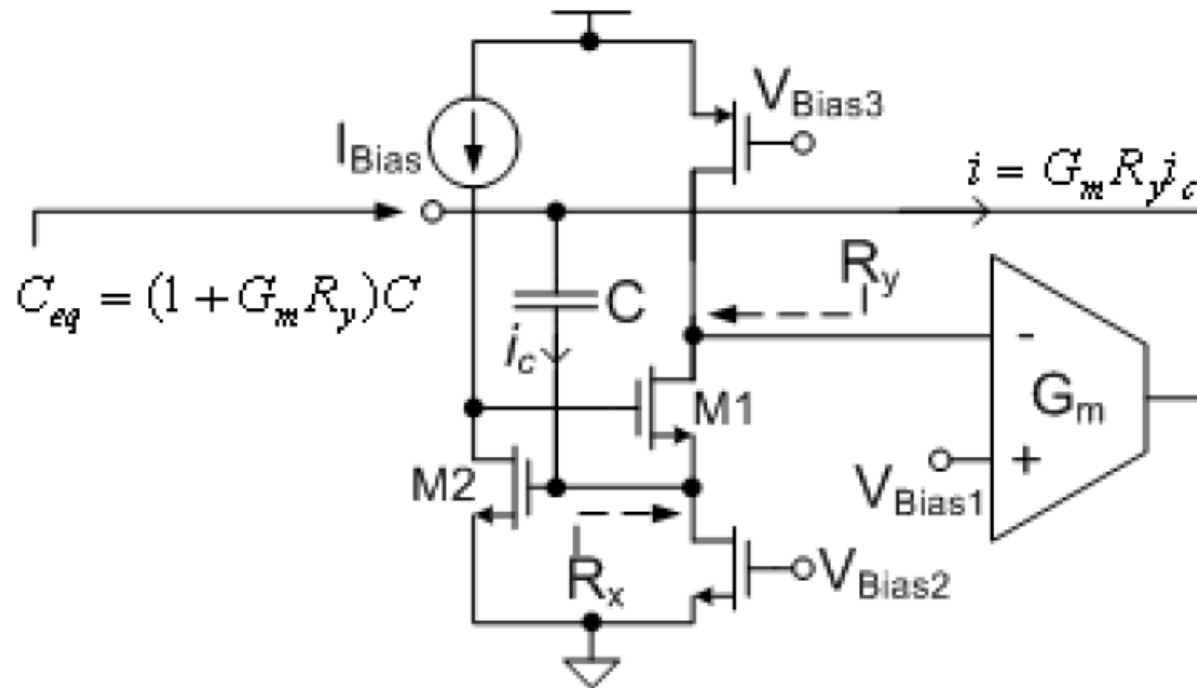


Figure 3. Linearly bidirectional current-mode capacitor multiplier

Reference:

[http://users.ece.gatech.edu/rincon-mora/publicat/trade\\_jrnls/pmdl\\_0706\\_cx.pdf](http://users.ece.gatech.edu/rincon-mora/publicat/trade_jrnls/pmdl_0706_cx.pdf)

# Using negative capacitance for LDO applications

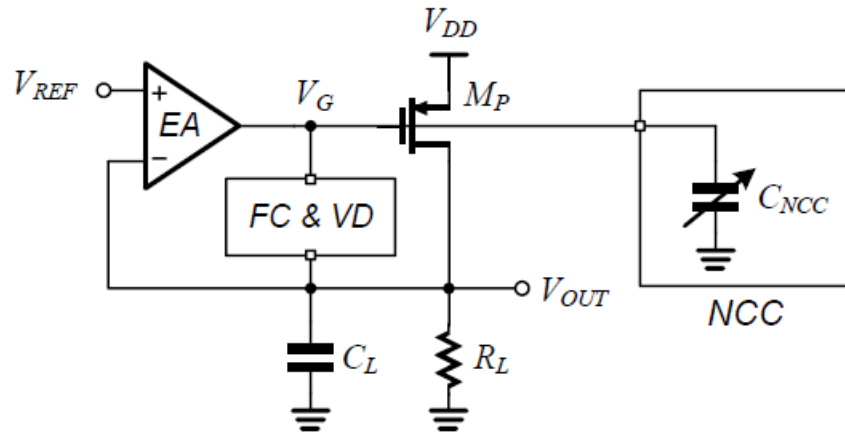


Fig. 1. Fundamental blocks of the proposed LDO regulator

If  $C_{NCC}$  cancels out the parasitic capacitances  $C_p$  and  $C_{gd}$  as

$$C_{NCC} = -(C_p + C_{gd}), \quad (3)$$

then  $v_g$  can be simply approximated as

$$v_g \cong \frac{C_{gs}}{C_{gs} + C_p + C_{gd} - (C_p + C_{gd})} v_{dd} = v_{dd}. \quad (4)$$

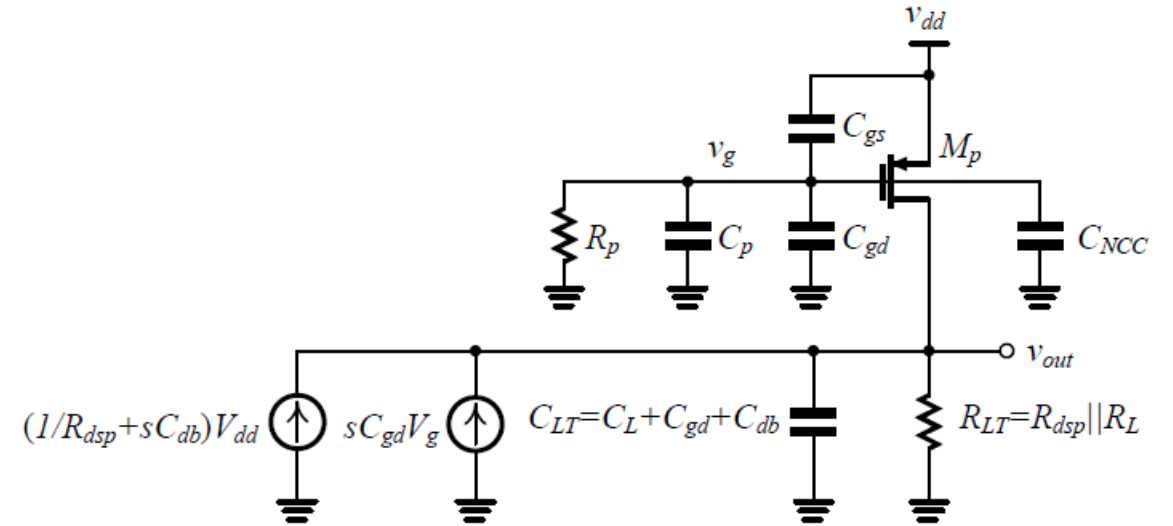


Fig. 2. Small-signal equivalent circuit of the proposed LDO regulator

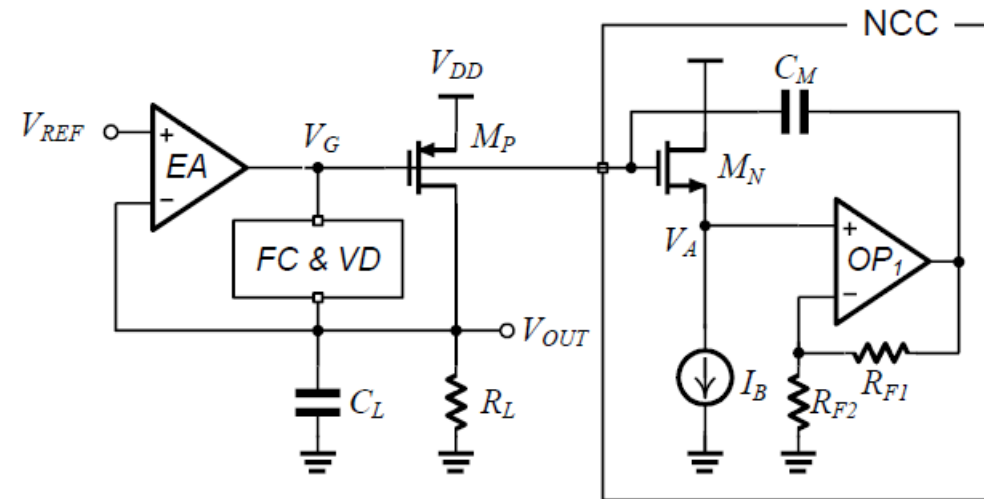


Fig. 3. Implementation of NCC with fundamental blocks