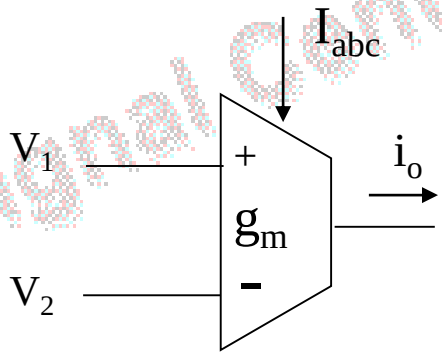
Nested G_m-C Compensation Amplifier.



Voltage Multistage Transconductance Amplifier Topologies for LV Power Supply.

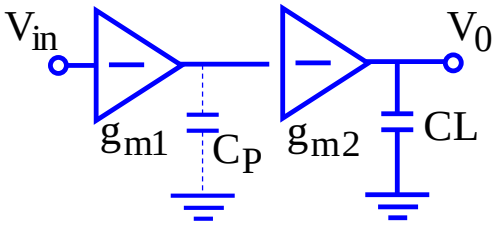
- Good voltage gain can be obtained using cascode stages. But these stages are not amenable for LV power supply.

- Under LV conditions, high voltage can be obtained using cascade amplifiers. That is growing horizontally, rather than vertically.

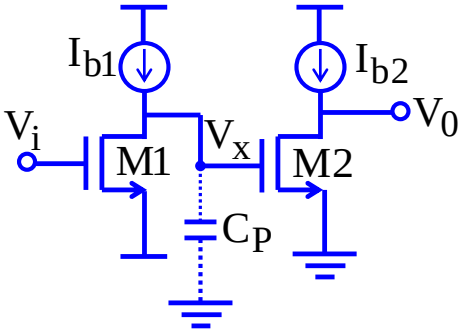
- Direct Cascade of simple (inverting) stages gives the required voltage gain without control of poles and zeroes.

- Dynamic behavior for optimal performance requires feedback (and feedforward) circuits.

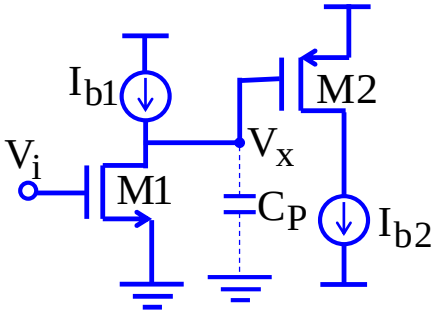
First Approach: Direct Cascade



Symbolic Representation



(a)



(b)

Two Possible Implementations

$$H(s) = \frac{V_0(s)}{V_{in}(s)} \cong \frac{+g_{m1}g_{m2}/C_pC_L}{1 + s\left(\frac{C_L}{g_{02}} + \frac{C_p}{g_{01}}\right) + \frac{C_pC_L}{g_{01}g_{02}}s^2}$$

The poles are located at

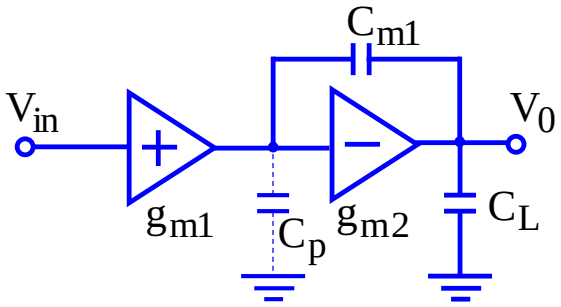
$$\omega_{p_1} = \frac{g_{01}}{C_p}\ ,\ \omega_{p_2} = \frac{g_{02}}{C_L}$$

i.e., 1 MHz and 10 MHz

$$H(o) = \frac{g_{m1}g_{m2}}{g_{01}g_{02}}$$

How do you bring one pole close to the origin?

-Use feedback, i.e. Miller effect



Neglect C_p (i.e., $C_p << C_{m1}$)

$$H(s) = \frac{V_0(s)}{V_{in}(s)} = \frac{g_{m1}(g_{m2} - sC_{m1})/C_L C_{m1}}{s^2 + s\left(g_{01}(C_L + C_{m1})/C_L C_p + g_{m2}/C_L + g_{02}/C_L\right) + g_{01}g_{02}/C_L C_{m1}}$$

The poles locations are approximately at:

$$\omega_{p_2} \cong (g_{m2} + g_{02})/C_L \quad \text{and} \quad \omega_{p_1} \cong \left(\frac{g_{01}}{C_{m1}}\right)\frac{g_{02}}{g_{m2}} = \left(\frac{g_{01}}{C_{m1}}\right)\frac{1}{A_{V_{02}}}$$

The good news is that: :

$\omega_{p_1} << \omega_{p_2}$ Good for stability

$H(o) = g_{m1}g_{m2}/g_{01}g_{02}$ Large DC voltage gain

The bad news is that a zero is at the RHP.

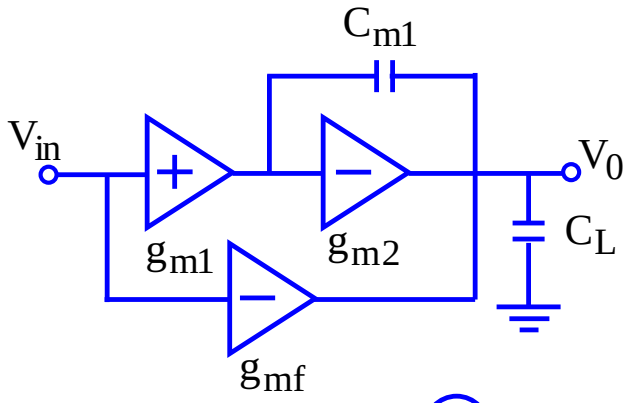
$$\omega_{z_1} = \frac{g_{m2}}{C_{m1}}$$

Now we will use a feedforward circuit to cancel the zero at the RHP.

This will impact the complexity and performance of the design.

Recall that before applying the feedforward we had:

$$H(s)=\frac{V_0(s)}{V_{in}(s)}=\frac{g_{m1}(g_{m2}-sC_{m1})/C_LC_{m1}}{s^2+s\left(g_{01}(C_L+C_{m1})/C_LC_p+g_{m2}/C_L+g_{02}/C_L\right)+g_{01}g_{02}/C_LC_{m1}}$$



No zero

Now the corresponding H(s) becomes:

For $g_{mf}=g_{m1}$

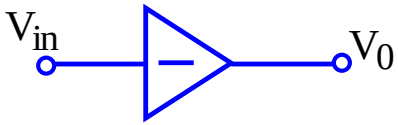
$$H(s)=\frac{V_o(s)}{V_{in}(s)}=\frac{-g_{m1}g_{m2}}{s^2C_LC_{m1}+s\left(C_{m1}g_{m2}+C_Lg_{o1}\right)+g_{o1}\left(g_{of}+g_{o2}\right)}$$

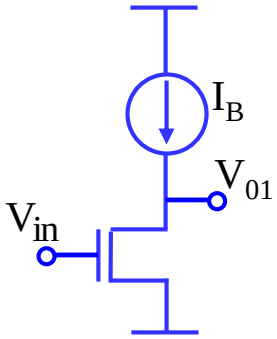
Assume a dominant pole, then

$$\omega_{p1} \cong \frac{g_{o1}\left(g_{o2}+g_{of}\right)}{g_{m2}C_{m1}} \quad ; \quad \omega_{p2} = \frac{g_{m2}}{C_L}$$

$$H(o) = A_{vo} = \frac{-g_{m1}g_{m2}}{g_{o1}\left(g_{o2}+g_{of}\right)} \quad ; \quad GB \cong A_{vo}\omega_{p1} = \frac{g_{m1}}{C_{m1}}$$

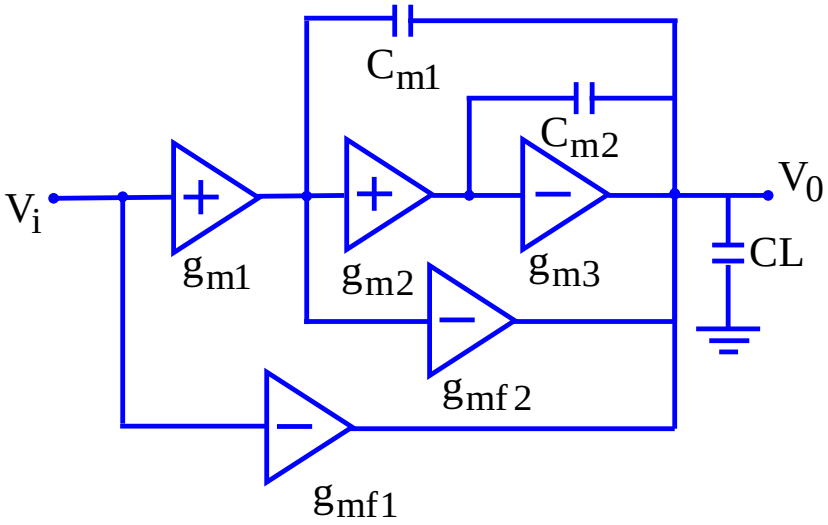
$$\frac{\omega_{p2}}{\omega_{p1}} = \frac{g_{m2'}g_{m2}C_{m1}}{C_L\left(g_{o2}+g_{of}\right)g_{o1}} \quad ; \quad C_{m1} \geq C_L$$





Let us consider a higher-order system, i.e. 3rd order.

Nested G_m-C Compensation Amplifier.



Three-stage amplifier topology with NGCC

$$H(s)=\frac{V_0(s)}{V_i(s)}=\frac{g_{m1}g_{m2}g_{m3}+sg_{m1}\left(g_{mf2}-g_{m2}\right)C_{m2}+\left(g_{mf1}-g_{m1}\right)C_{m1}C_{m2}S^2}{g_{01}g_{02}g_{03}+sg_{m2}g_{m3}C_{m1}+s^2\left(g_{m3}+g_{mf2}-g_{m2}\right)C_{m1}C_{m2}+s^3C_LC_{m1}C_{m2}}$$

By making $g_{mf1}=g_{m1}$ and $g_{mf2}=g_{m2}$,

$$H(s)=\frac{V_0(s)}{V_i(s)}=\frac{-g_{m1}g_{m2}g_{m3}}{g_{01}g_{02}g_{03}+sg_{m2}g_{m3}C_{m1}+s^2g_{m3}C_{m1}C_{m2}+s^3C_LC_{m1}C_{m2}}$$

Observe the regularity and simplicity of the reduced expression

This 3rd order H(s) assuming a dominant pole can be written as

$$H(s) = \frac{-A_0}{\left(1 + s\frac{A_0}{f_1}\right)\left(1 + \frac{s}{f_2} + \frac{s^2}{f_2 f_3}\right)}$$

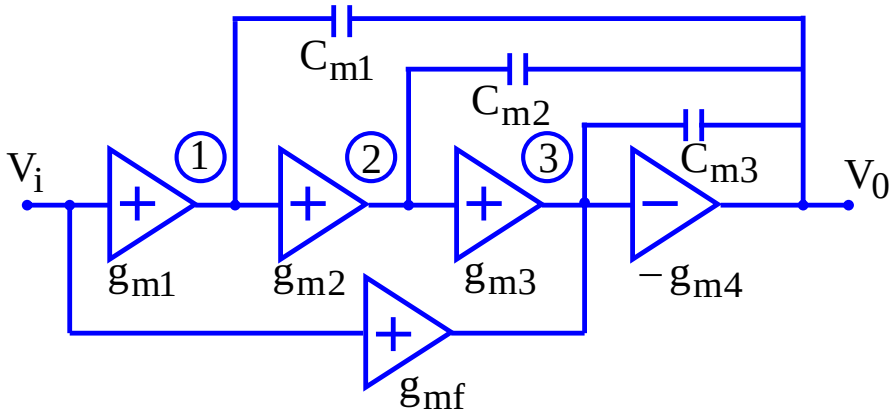
$$A_0 = \frac{g_{m1}g_{m3}g_{m2}}{g_{01}g_{03}g_{02}} \text{ and } f_1 = GB = \frac{g_{m1}}{C_{m1}}$$

$$f_2 = \frac{g_{m2}}{C_{m2}} \text{ , } f_2 f_3 = \frac{g_{m2}g_{m3}}{C_{m2}C_L} \text{ ; } f_i = \frac{g_{mi}}{C_{mi}}$$

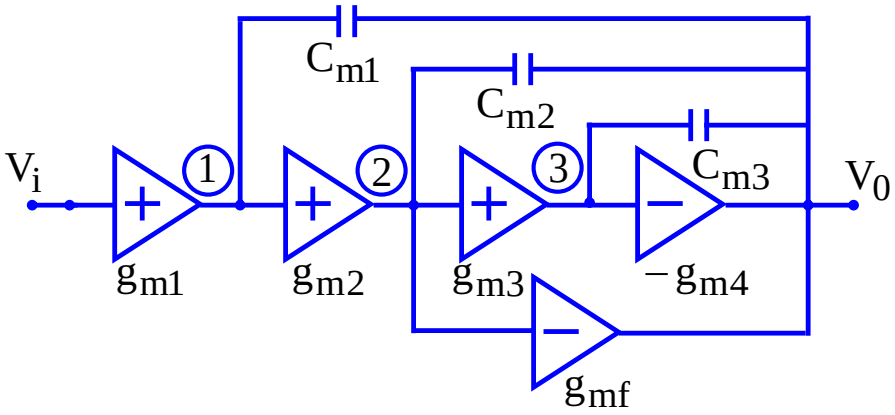
Note that the dominant pole is located at

$$P_1 = \frac{f_1}{A_0} = \frac{\frac{g_{m1}}{C_{m1}}}{\frac{g_{m1}g_{m2}g_{m3}}{g_{01}g_{02}g_{03}}} = \frac{g_{01}g_{02}g_{03}}{g_{m2}g_{m3}C_{m1}} = \left(\frac{g_{01}}{C_{m1}}\right)\frac{1}{A_{V0_2}A_{V03}}$$

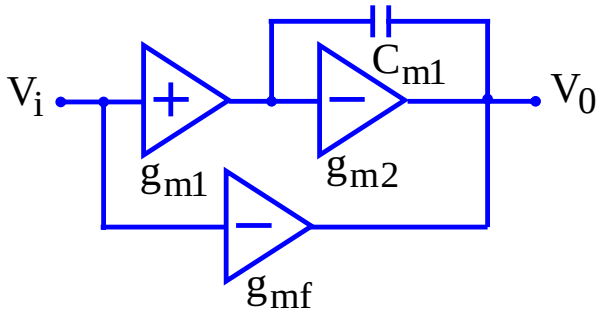
Multipath Nested Miller Compensation Technology
Potential Feedforward Schemes: An Amplifier Topologies Re-Visit.



(a) Multipath nested miller compensation topology. FF : NMC

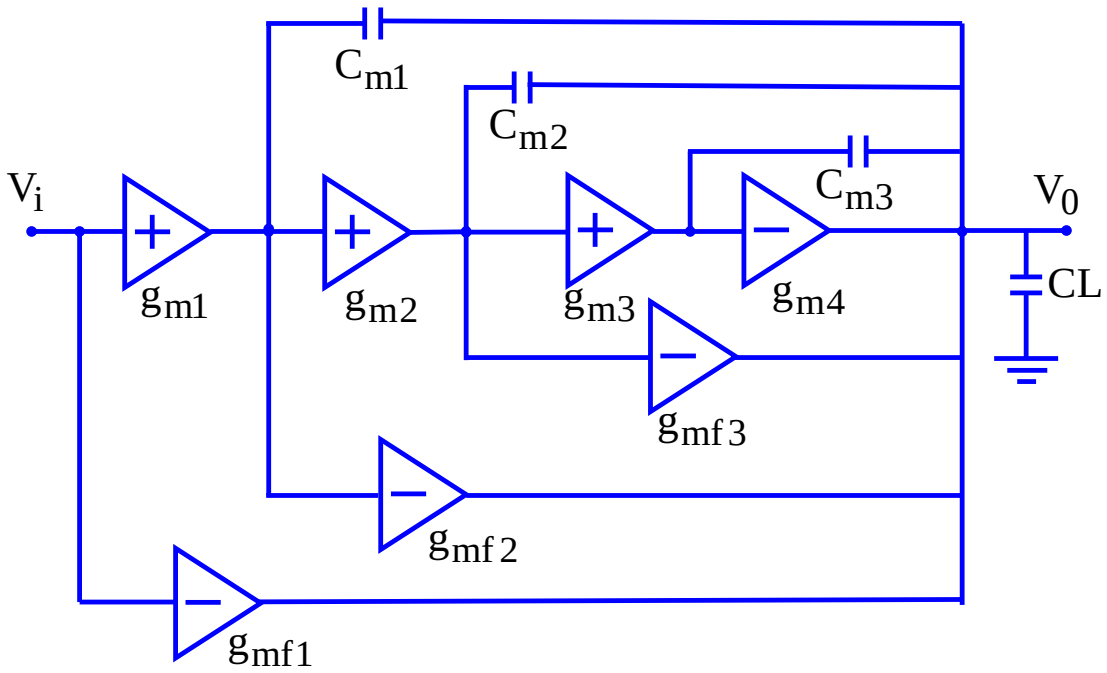


(b) An abstract model for the amplifier proposed by Castello, et.al.



(c) The amplifier with multipath miller zero cancellation.

Let Us Now Compare Several Four-Order Topologies



$$H(s) = \frac{-A_0}{\left(1+\frac{s}{P_1}\right)\left(1+a_1 s + a_2 s^2 + a_3 s^3\right)}$$

$$P_1 = \frac{GB}{A_0}$$

$$a_1 = \frac{1}{f_2}, a_2 = \frac{1}{f_2 f_3}\ ,\ a_3 = \frac{1}{f_2 f_3 f_4}$$

$$\frac{1}{f_2 f_3} = \frac{C_{m2} C_{m3}}{g_{m2} g_{m3}}\ ,\ \frac{1}{f_i} = \frac{C_{mi}}{g_{mi}}$$

Four stage amplifier topology with NGCC (Fan You et al)

$$f_1 < f_2 < f_3 \le f_4\ ,\ f_1 = GB$$

$$f_4 > \frac{f_2}{1 - f_2 / f_3}$$

- Power Comsumption : $P = (V_{dd} - V_{ss}) \sum_1^n I_i$

$$P = (V_{DD} - V_{ss}) I_n \left[1 + \sum_{i=1}^{n-1} \frac{\alpha_i f_i}{f_n}\right],\ \alpha_i = \frac{C_{mi}}{C_L}\ ,\ \alpha_i f_i = \frac{g_{mi}}{C_L}$$

I_n and f_n are current and frequency normalization factors, respectively.

Comparison of Several Topologies.

$$\frac{V_0(s)}{V_i(s)} = -A_0 \frac{1 - b_1 s - b_2 s^2 - b_3 s^3}{(1 + s/P_1)(1 + a_1 s + a_2 s^2 + a_3 s^3)}, \qquad k_i = \frac{g_{mi}}{g_{oi}}, i = 1,3 \quad \text{and} \quad f_i = \frac{g_{mi}}{C_{mi}}$$

Where

$$A_0 = k_1 k_2 k_3 k_4, \; P_1 = \frac{f_1}{A_0} = \frac{GB}{A_0}$$

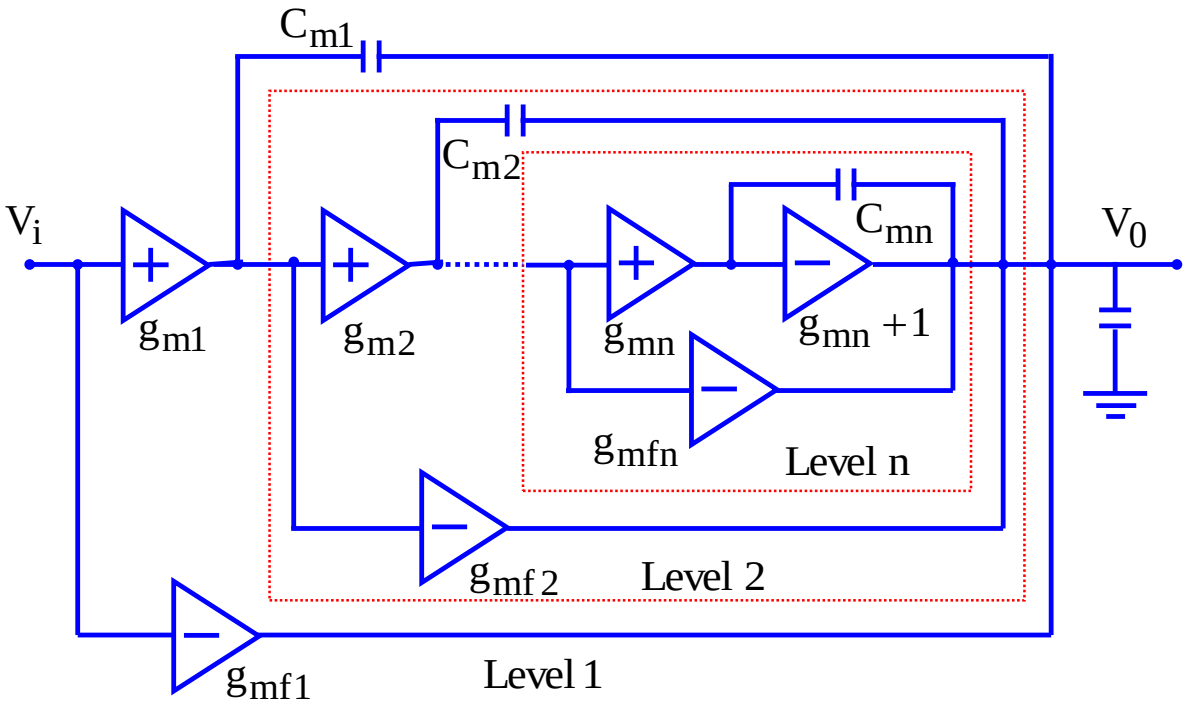
Comparison of Polynomial Coefficients for Four Stage NMC and NGCC Amplifier.

Design

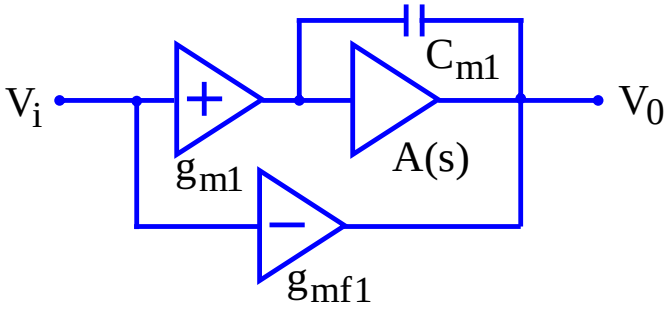
$P_h(s)$	a_1	a_2	a_3	
NMC	$\frac{(g_{m4}C_{m2} - g_{m2}C_{m3})}{g_{m2}g_{m4}}$	$\frac{(g_{m4} - g_{m2} - g_{m3})C_{m2}C_{m3}}{g_{m2}g_{m3}g_{m4}}$	$\frac{C_{m2}C_{m3}C_L}{g_{m2}g_{m3}g_{m4}}$	← **Complex**
NGCC	$\frac{C_{m2}}{g_{m2}}$	$\frac{C_{m2}C_{m3}}{g_{m2}g_{m3}}$	$\frac{C_{m2}C_{m3}C_L}{g_{m2}g_{m3}g_{m4}}$	← **Simple**

$Z(s)$	b_1	b_2	b_3
NMC	$\frac{C_{m3}}{g_{m4}}$	$\frac{C_{m2}C_{m3}}{g_{m3}g_{m4}}$	$\frac{C_{m1}C_{m2}C_{m3}}{g_{m2}g_{m3}g_{m4}}$
NGCC	0	0	0

Nested G_m-C Compensation (NGCC) N^{th}-Order

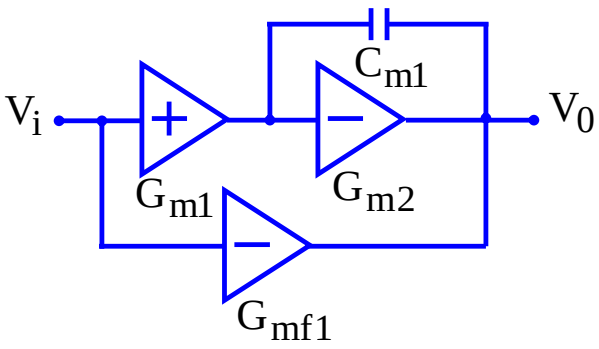


Conceptual multistage amplifier topology with NGCC.

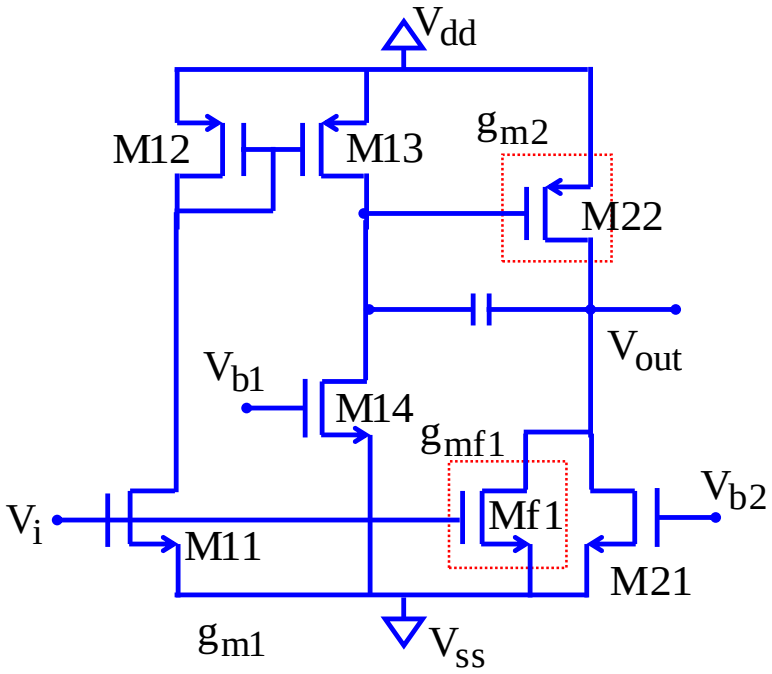


Abstract model.

How to Implement a Positive G_m?



(a) Representation



(b) Transistor Level

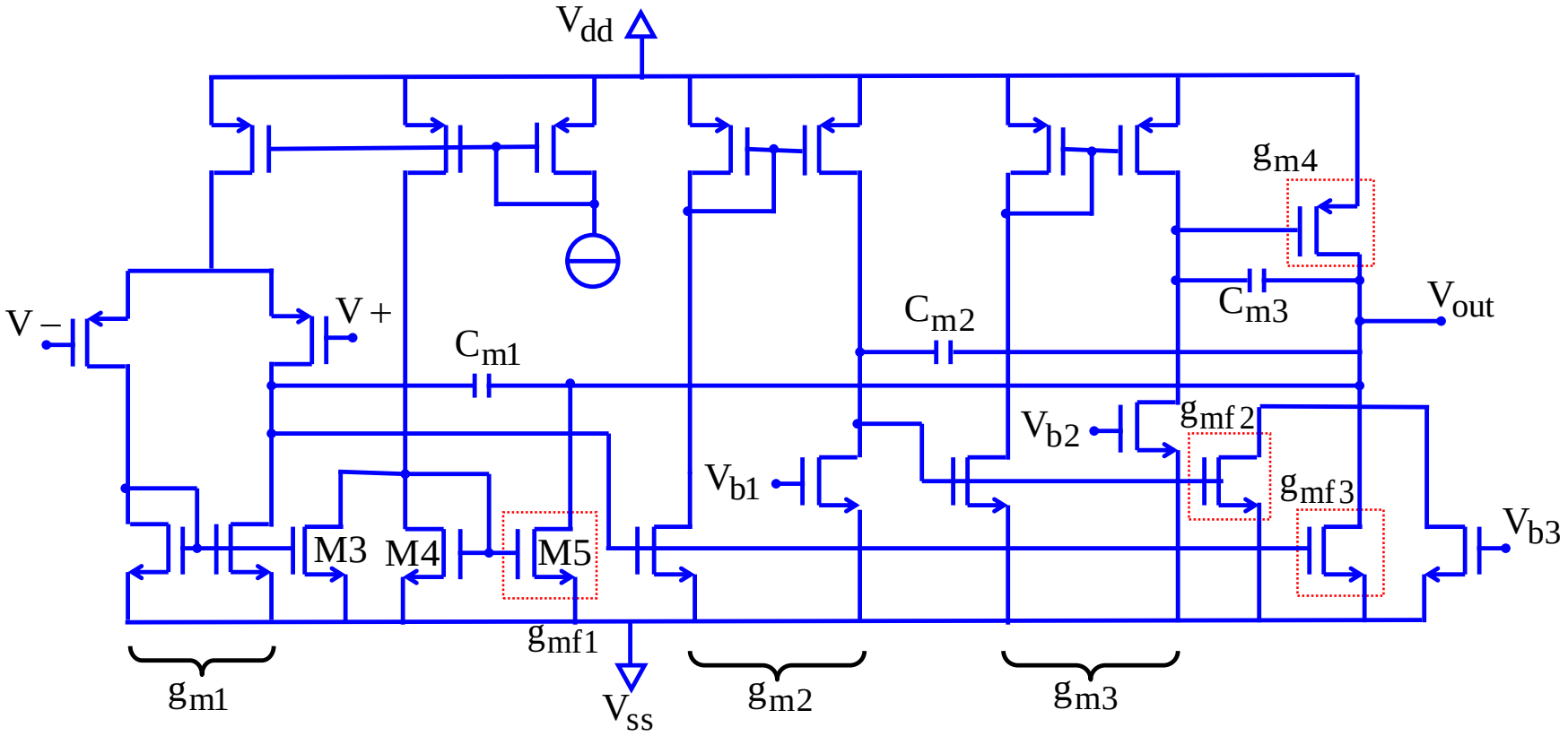
$G_{m1} \Rightarrow M11 - M14$, $g_{mM11} = g_{m1}$

$G_{m2} \Rightarrow M21 - M22$, $g_{mM22} = g_{m2}$

$G_{mf1} \Rightarrow Mf1$

- If $G_{m2} > G_{mf1}$, M22 current > Mf1 current, then add M21 to provide additional current.
- If $G_{m2} < G_{mf1}$, Remove M21 and add a PMOS transistor in parallel to M22.

Design Example of a Four-Stage Amplifier



Four stage operational amplifier with NGCC topology

- The dominant pole f_1 is determined by GB
- Phase margin (ϕ_m) is mainly determined by the high frequency poles

• The location of higher-order poles not only influence on the ϕ_m, but also in settling time and power consumption.

• For specification requiring $A_o > 80$ dB, a four-stage (n = 4) is usually required

• Stability considerations for n = 4 impose

$$f_4 > \frac{f_2}{1 - f_1 / f_3} \quad ; \quad f_1 = GB$$

$$f_1 < f_2 < f_3 \leq f_4$$

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{-A_o}{\left(1 + \frac{A_o}{GB} s\right)\left(1 + \frac{s}{f_2} + \frac{s^2}{f_2 f_3} + \frac{s^3}{f_2 f_3 f_4}\right)}$$

$$\frac{1}{f_i} = \frac{C_{mi}}{g_{mi}} \quad , \quad i = 1, \ldots 4$$

Design Approach

Step 1. Determine $\mathbf{f_1}$ based on **GB**

$$f_1 = GB$$

Step 2. Determine $\mathbf{f_2}$ based on **Phase Margin**

$$\phi_m = 90^o - \tan^{-1}\left(\frac{GB}{f_2}\left(\frac{1-GB^2/f_3 f_4}{1-GB^2/f_2 f_3}\right)\right) \approx 90^o - \tan^{-1}\left(\frac{GB}{f_2}\right)$$

Example:

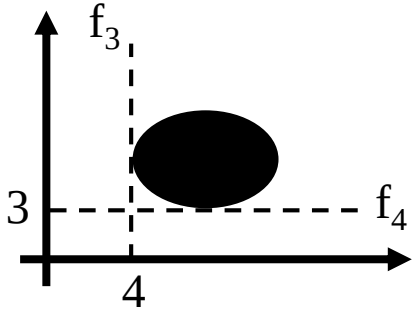
$f_2 = 2$ GB, $f_3 > f_2$, $f_4 > f_2$ $\rightarrow$ $\phi_m \cong 60^o$

However, this does not guarantee small settling time

Design Approach

Step 3. Determine **f_3, f_4** based on **settling time** and **power**

$$H(s) = \frac{A_o}{\left(1+\frac{A_o s}{f_1}\right)\left(1+\frac{s}{f_2}+\frac{s^2}{f_2 f_3}+\frac{s^3}{f_2 f_3 f_4}\right)}$$



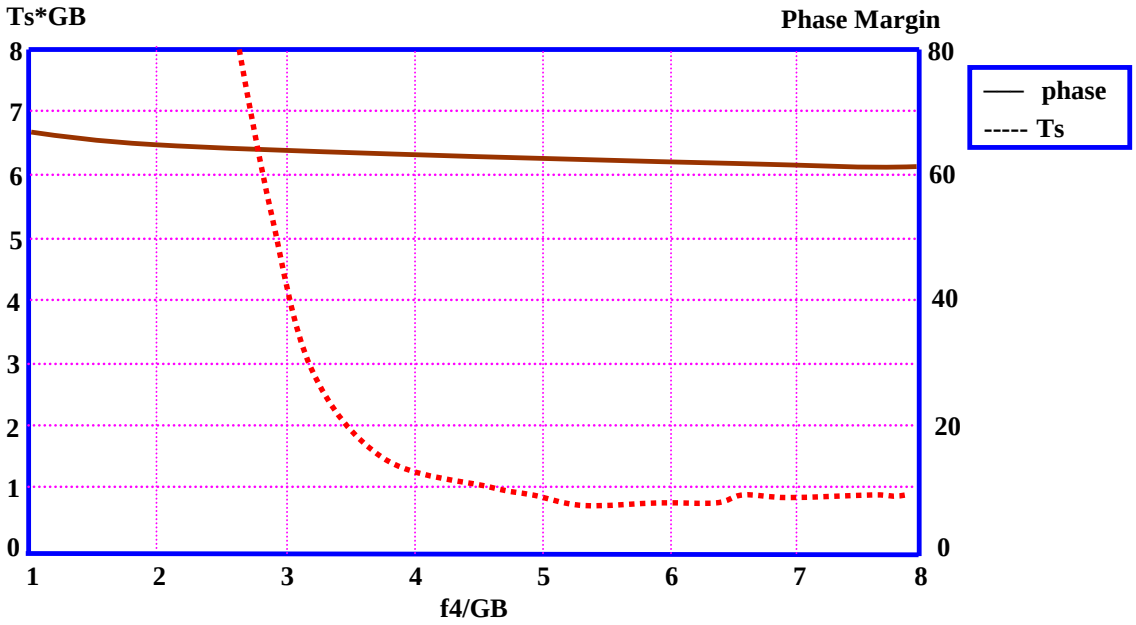
a. Sweep f_3 and f_4 **Ts?** (settling time)

Numerical Analysis (e.g. **MATLAB**)

b. Select a set of (f_3, f_4) with desired power and settling time

What is the effect of f_4 /GB?

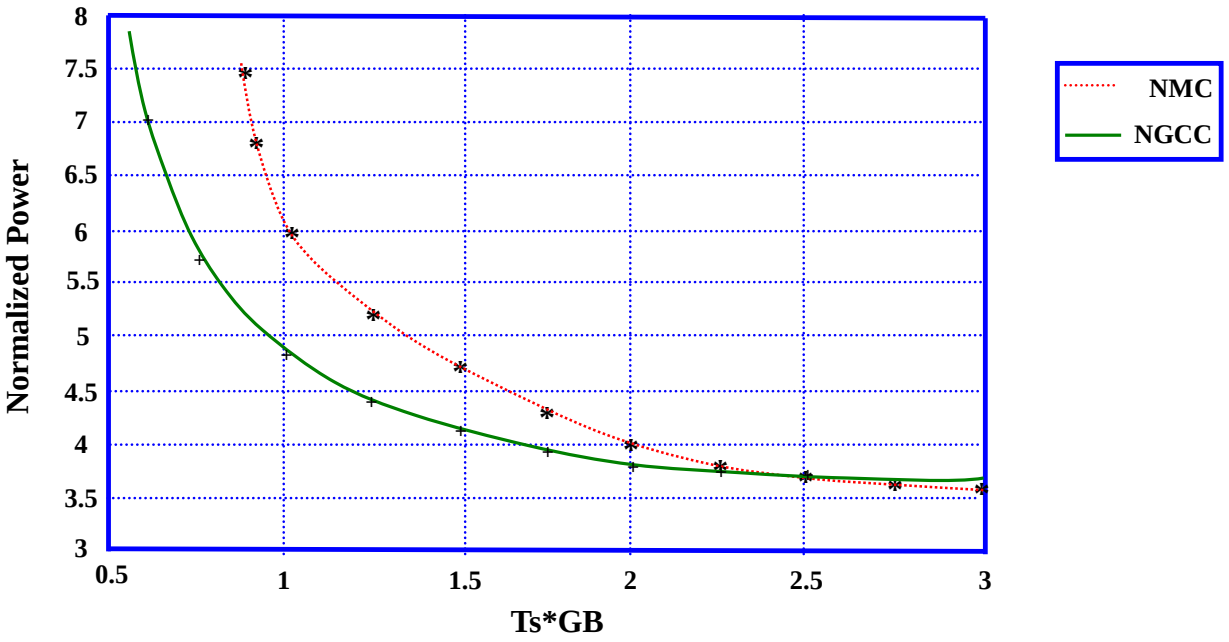
How far should one push f_4?



The phase margin and normalized settling time (TsGB) of an NGCC amplifier vs. f_4/GB.

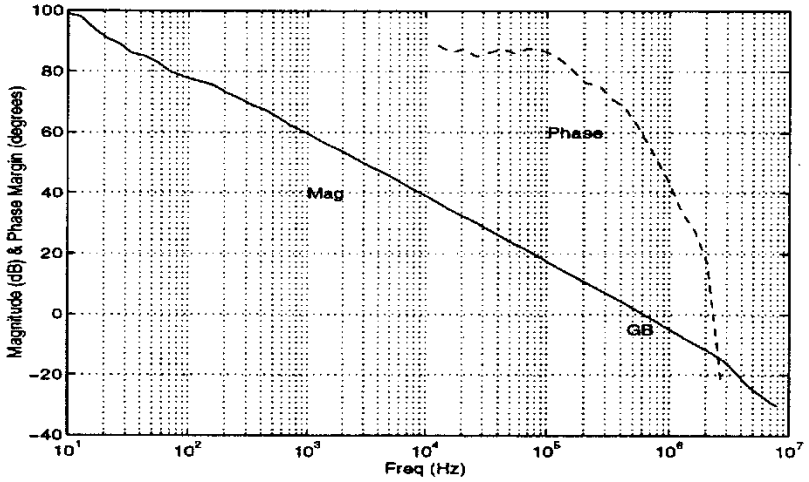
- **Trade-off between phase margin versus setting time.**

How do the Two Topologies Compare for Power Consumption?

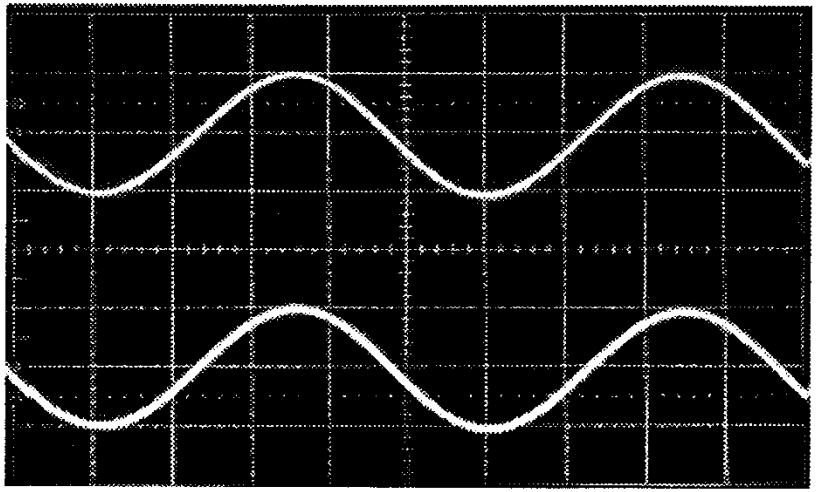


The normalized power consumption of the NGCC and the NMC amplifiers as a function of the normalized settling time.

More Experimental Results.



Measured frequency response of 4-stage NGCC amplifier

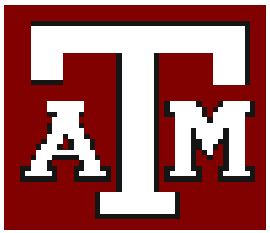


Measured 1.0Vp-p 100 KHz sin-wave at input and output nodes of a unity follower.

Measured Performance of the 4-Stage NGCC Op Amp.

Power Consumptio n	0.68mW	1.40mW
DC Gain	$\approx$100dB	$\approx$100dB
Gain Bandwidth	610kHz	1.0MHz
Phase Margin	60^{o}	58^{o}
Input Offset	5.2mV	5.2mV
Slew Rate	$2.5V/\mu S$	5.0V
Power Supply	$\pm$1.0V	$\pm$1.0V
Load Condition	$10k\Omega // 20\,pF$	10kΩ//20pF
Area	$0.22mm^{2}$	$0.22mm^{2}$

OPTIMAL DESIGN OF LOW POWER NESTED GM-C COMPENSATION AMPLIFIERS USING A CURRENT-BASED MOS TRANSISTOR MODEL



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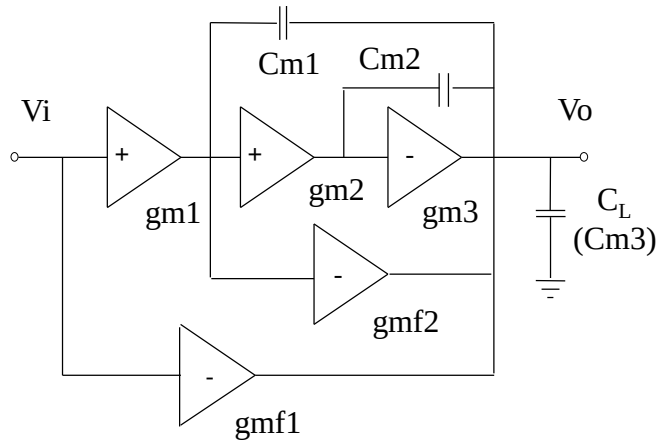
Low Power Operational Amplifiers

- Applications: mobile communication & portable devices
- Major concerns: power, stability, area and speed.
- Design approach:
  - Low voltage — multistage cascading.

    Techniques for solving stability problem:
    - Nested Miller Compensation (NMC)
    - Nested Gm-C Compensation (NGCC)
  - Low operating current — weak or moderate inversion.
    - Optimal design in moderate inversion
    - Continuous MOSFET model

Topology of Three-stage NGCC Amplifier



We define:

$$k_i = \frac{g_{mi}}{g_{oi}} \qquad f_i = \frac{g_{mi}}{C_{mi}}$$

$f_1 = \frac{g_{m1}}{C_{m1}}$ — unity gain frequency

$A_o = k_1 k_2 k_3$ — dc gain

- feedforward path g_{mf1} and g_{mf2} to cancel RHP zeros.
- Transfer function:

$$\frac{V_o(s)}{V_i(s)} = -\frac{g_{m1}g_{m2}g_{m3} + sg_{m1}(g_{mf2} - g_{m2})C_{m2} + s^2(g_{mf1} - g_{m1})C_{m1}C_{m2}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2(g_{m3} + g_{mf2} - g_{m2})C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}}$$

Making $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$ gives:

$$\frac{V_o(s)}{V_i(s)} = \frac{-g_{m1}g_{m2}g_{m3}}{g_{o1}g_{o2}g_{o3} + sg_{m2}g_{m3}C_{m1} + s^2g_{m3}C_{m1}C_{m2} + s^3C_LC_{m1}C_{m2}}$$

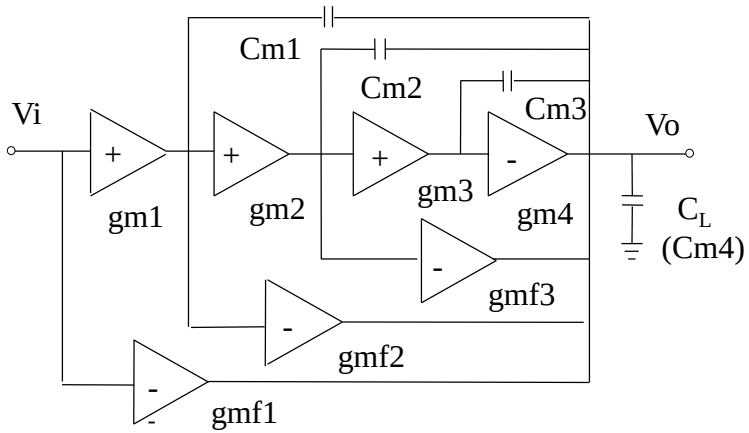
Rewritten as:

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-k_1k_2k_3}{\left(1 + s\frac{k_1k_2k_3}{f_1}\right)\left(1 + \frac{s}{f_2} + \frac{s^2}{f_2f_3}\right)}$$

Phase margin:

$$PM \cong 90^o - \tan^{-1}\frac{1}{\left(\frac{f_2}{GB} - \frac{GB}{f_3}\right)}$$

Topology of Four-stage NGCC Amplifier



Compared to three-stage NGCC:

- easier to obtain high dc gain,
- more complicated design,
- potentially more power consumption.

- Transfer function:

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_0}{\left(1+\frac{A_0 s}{f_1}\right)\left(1+\frac{s}{f_2}+\frac{s^2}{f_2 f_3}+\frac{s^3}{f_2 f_3 f_4}\right)}$$

- Phase margin:

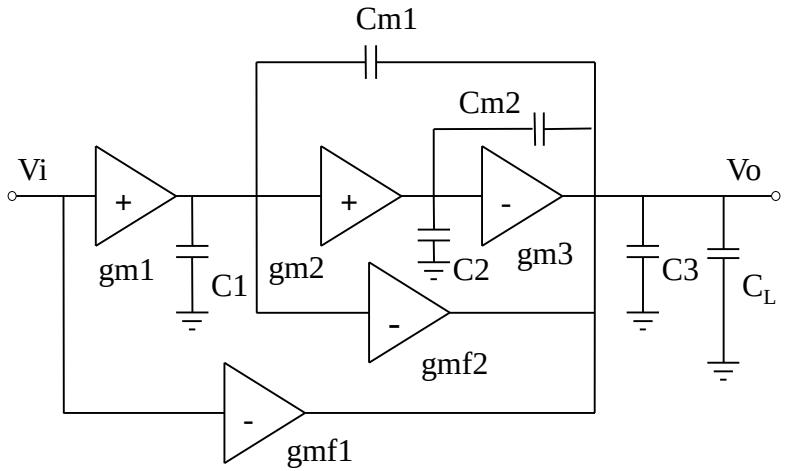
$$PM = 90^o - \tan^{-1}\left(\frac{GB}{f_2}\times\frac{1-GB^2/f_3 f_4}{1-GB^2/f_2 f_4}\right)$$

$$\approx 90^o - \tan^{-1}\left(\frac{GB}{f_2}\right)$$

- Transfer function of an n-stage NGCC amplifier:

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_0}{\left(1+\frac{A_0 s}{f_1}\right)\left(1+\frac{s}{f_2}+\frac{s^2}{f_2 f_3}+\ldots+\frac{s^{n-1}}{\prod_{i=2}^{n} f_i}\right)}$$

Modification on Low Power Three-stage NGCC



Significant parasitic effect:

— very large transistors for weak inversion design,

— long channel transistors used for high dc gain.

- Modified transfer function:
-

$$H'(s) = -\frac{A_0 + a_1 s + a_2 s^2}{\left(1 + s\frac{A_0}{f_1'}\right)\left(1 + \frac{s}{f_2'} + \frac{s^2}{f_2' f_3'}\right)}$$

where

$$a_1 = k_1 k_2 \left(\frac{C_2}{g_{o3}} - k_3 \tau\right)$$

$$a_2 = k_1 \left(\frac{C_1 (C_2 + C_{m2})}{g_{o2} g_{o3}} + k_2 \tau \frac{C_{m2}}{g_{o3}}\right)$$

- Ci — parasitic capacitance at each output node,
- τ — phase delay due to the current mirror at second stage.

Modification on Low Power Three-stage NGCC (cont.)

$$f_1' = f_1$$

$$f_2' = f_2 \frac{1}{1+\varepsilon_1+\varepsilon_2\frac{g_{m2}}{g_{m3}} - f_2\tau + \frac{g_{o3}}{g_{m3}}(1+\varepsilon_1)(1+\varepsilon_2)}$$

$$f_3' = f_3 \frac{\frac{1}{1+\varepsilon_2} - f_2\tau\frac{1}{1+\varepsilon_1}\frac{1}{1+\varepsilon_2} + \frac{g_{o3}}{g_{m3}} + \frac{g_{m2}}{g_{m3}}\frac{1}{1+\varepsilon_1}\frac{\varepsilon_2}{1+\varepsilon_2}}{1+\frac{C_3}{C_L}+\frac{C_2}{C_L}\frac{1}{1+\varepsilon_2}+\frac{C_1}{C_L}\frac{1}{1+\varepsilon_1}+\frac{g_{m2}\tau}{C_L}\frac{1}{1+\varepsilon_1}\frac{1}{1+\varepsilon_2}}$$

Moderate inversion:

— good stability,

— optimization of power, speed & area.

with $\varepsilon_1 = C_1/C_{m1}$ and $\varepsilon_2 = C_2/C_{m2}$

Ex: f_1 = GB, f_2 = 2GB, f_3 = 4GB, $C_{m1} = C_{m2}$ = 8 pF, C_L = 20 pF,

then g_{m1} = 50 μS, g_{m2}=100 μS, g_{m3}=500 μS,

For g_{o3}=100 μS (R_L), C_1=1 pF, C_2=3 pF, C_3= 6 pF

Assume τ = 0,

Then $f_2' = 0.66 f_2$ and $f_3' = 0.67 f_3$

Current-Based Transistor Model

- Features of ACM model:
  - physics-based model,
  - universal and continuous expression for any inversion,
  - independent of technology, temperature, geometry and gate voltage,
  - same model for analysis, characterization and design.
- Main design equations: (design parameters: I, g_m, i_f)

$$\frac{I}{\phi_t g_m n} = \frac{1+\sqrt{1+i_f}}{2}$$

$$f_T = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right)$$

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox}\phi_t} \frac{1}{\sqrt{1+i_f}-1}$$

$$\frac{V_{DSAT}}{\phi_t} \cong \left(\sqrt{1+i_f}-1\right)+4$$

$$\frac{W}{L} = \frac{g_m}{2\mu C_{ox}\phi_t\left(\frac{I}{\phi_t g_m n}-1\right)}$$

I — drain current in transistor
g_m — transconductance in saturation
n — slope factor
ϕ_t — thermal voltage
i_f — inversion level of the transistor defined as $i_f = I/I_s$, where $I_s = \mu n C_{ox} \frac{\phi_t^2}{2} \frac{W}{L}$ is the normalization current.

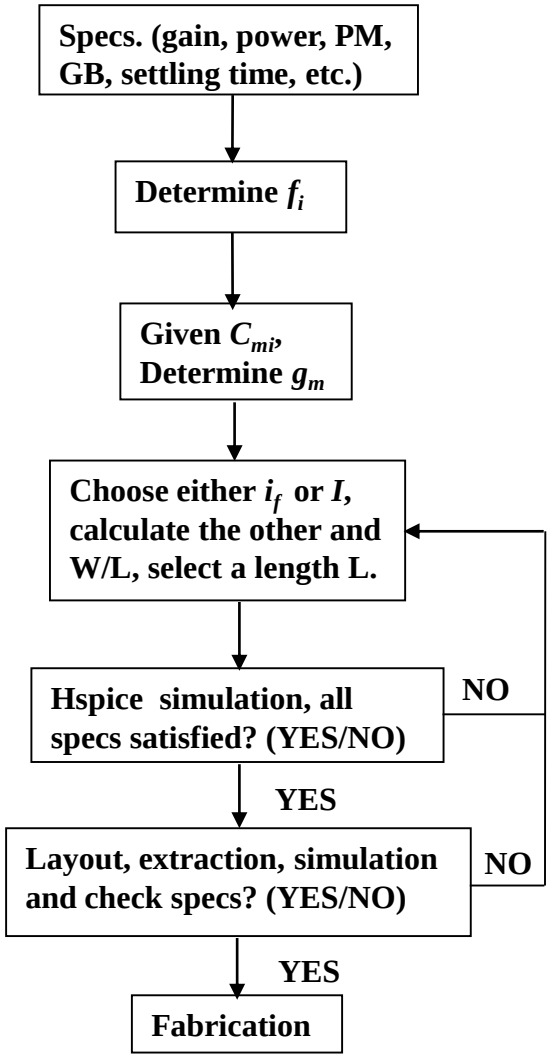
$i_f << 1$ — weak inversion,

$i_f >> 1$ — strong inversion.

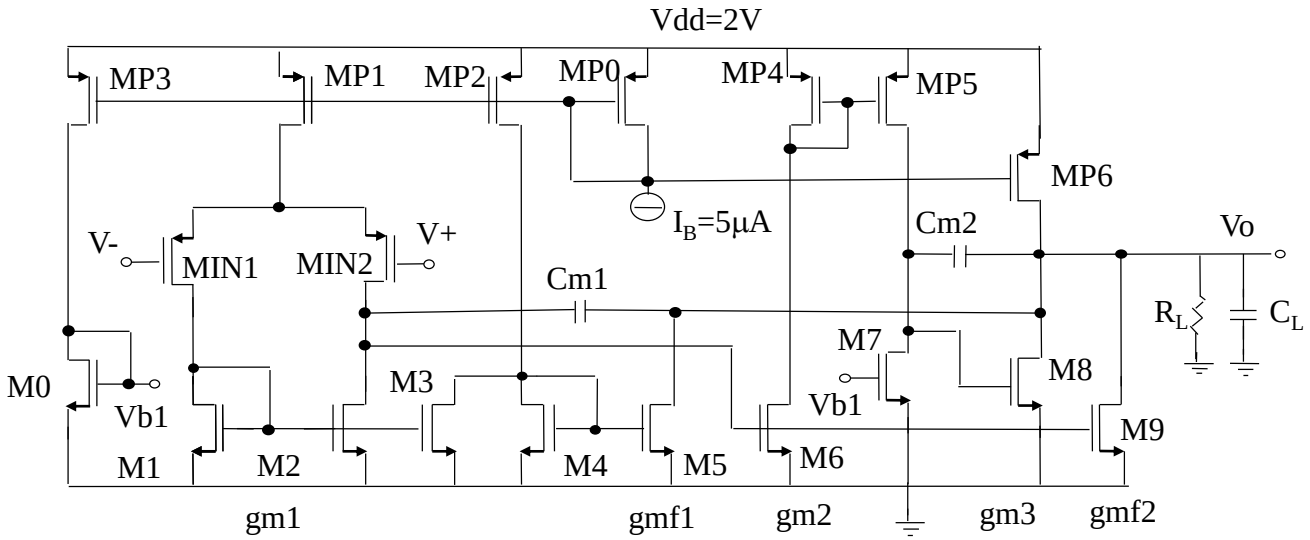
Specifications and Design Procedure

- Specifications:
  - load 10 kΩ/20 pF
  - gain bandwidth GB=1 MHz
  - dc gain $A_0 > 100$ dB
  - phase margin PM > 60^o
  - 0.2% settling time < 1μS
  - power consumption: minimum
- Other Specs can be included

  (if determined by g_m, I, and i_f):
  - noise,
  - slew rate,
  - common mode rejection.



Implementation of Three-Stage NGCC Amplifier

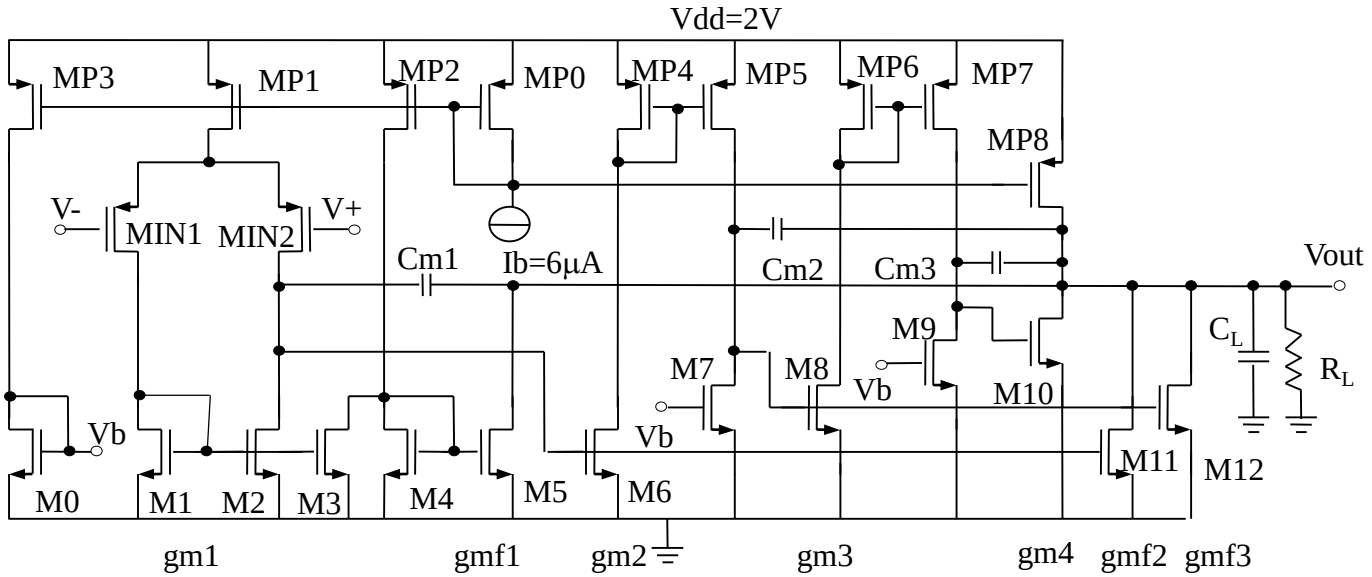


Remarks:

- Ideally, f_1 = GB, f_2 = 2GB, f_3 = 4GB, Choose f_2=3GB, f_3=5GB to compensate large parasitic effect.
- Long channel to obtain adequate gain — cause large parasitic effect.

Transistor NO.	W(μm)	L(μm)	i_f
M_1 — M_4	1×18	4.2	20
M_0, M_5	2×18	4.2	20
M_6, M_7, M_9	6×18	4.2	20
M_8	25×18	4.2	20
M_{IN1}, M_{IN2}	20×18	4.2	4
M_{P0} — M_{P3}	2×18	4.2	80
M_{P4}, M_{P5}	6×18	4.2	80
M_{P6}	33×18	4.2	80

Implementation of Four-Stage NGCC Amplifier



Remarks:

- f_1=GB, f_2=2GB, f_3=5GB, f_4=6GB
- shorter length — small parasitic effect
- lower inversion level than 3-stage one.
- Same implementation and same f_i for reference opamp (low-voltage strong inversion 4-stage)

Transistor NO.	W(μm)	L(μm)	i_f
M_1 — M_4	4×10.8	1.8	6
M_0, M_5	8×10.8	1.8	6
M_6, M_7, M_{11}	8×10.8	1.8	6
M_8, M_9, M_{12}	20×10.8	1.8	6
M_{10}	60×10.8	1.8	6
M_{IN1}, M_{IN2}	8×18	1.8	6
M_{P0} — M_{P3}	2×18	1.8	30
M_{P4}, M_{P5}	2×18	1.8	30
M_{P6}, M_{P7}	5×18	1.8	30
M_{P8}	24×18	1.8	30

Simulation Results of NGCC Amplifiers

(V_{DD} = 2 V, Z_{LOAD} = 10 kΩ/20 pF)

	Specifications	Three-Stage	Four-Stage	Four-Stage(ref.)
Power Consumption	Minimum	0.28 mW	0.30 mW	0.93 mW
DC Gain	≥ 100 dB	~ 100 dB	~ 105 dB	~ 110 dB
Gain Bandwidth	1.0 MHz	1.08 MHz	1.03 MHz	1.09 MHz
Phase Margin	$> 60^o$	59.5^o	62.7^o	61.2^o
0.2% Settling Time (100 mV)	< 1 μS	0.77 μS	0.55 μS	0.53 μS
THD (1kHz $1V_{P-P}$)		- 84.8 dB	- 88 dB	- 55.8 dB
1% THD Input (1kHz)		1.36V	1.38V	1.26V
Active Area (relative area)		$0.01mm^2$ (1.75)	$0.0052\ mm^2$ (0.91)	$0.0057\ mm^2$ (1)
min i_f, max i_f		4 , 80	6 , 30	100 , 130

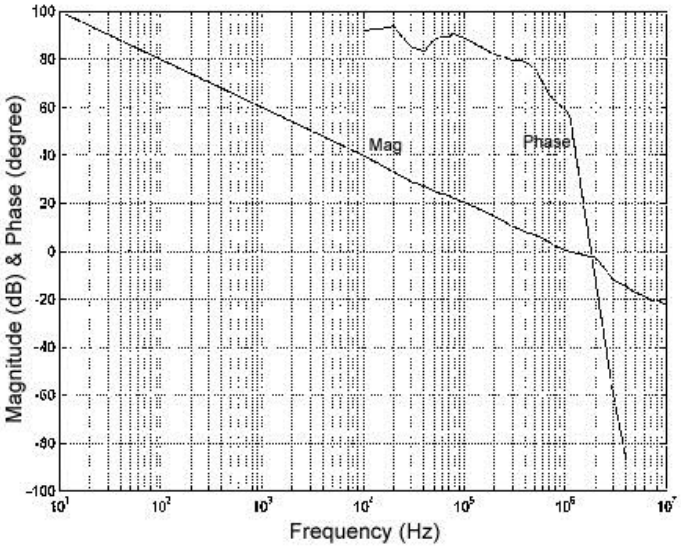
* 1.2 μm AMI n-well CMOS technology
* BSIM (HSPICE level 13) simulation

Experimental Results

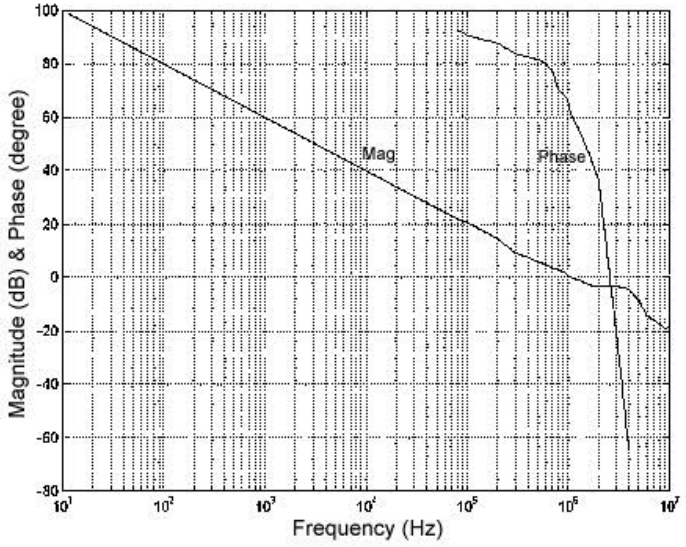
	Specifications	Three-Stage	Four-Stage	Four-Stage(ref.)
Power Consumption	Minimum	0.26 mW	0.28 mW	0.63 mW
DC Gain	≥ 100 dB	~ 96 dB	~ 105 dB	~ 100 dB
Gain Bandwidth	1.0 MHz	1.10 MHz	1.05 MHz	900 kHz
Phase Margin	$> 60^{o}$	56.7^{o}	62.0^{o}	63.6^{o}
THD (1kHz $1V_{P-P}$)		- 67.7 dB	- 67.5 dB	- 28.5 dB
1% THD Input (1kHz)		1.13 V	1.11 V	0.94 V
Active Area (Relative Area)		$0.01mm^2$ (1.49)	$0.0052\ mm^2$ (0.78)	$0.0067\ mm^2$ (1)

* The output stage of the reference op amp is realized with a PMOS transistor for reduction of power.

Frequency Response

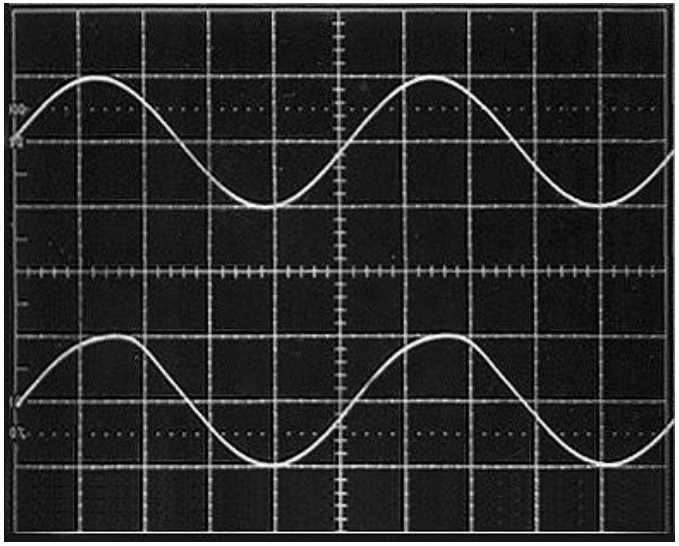


3-stage NGCC amplifier



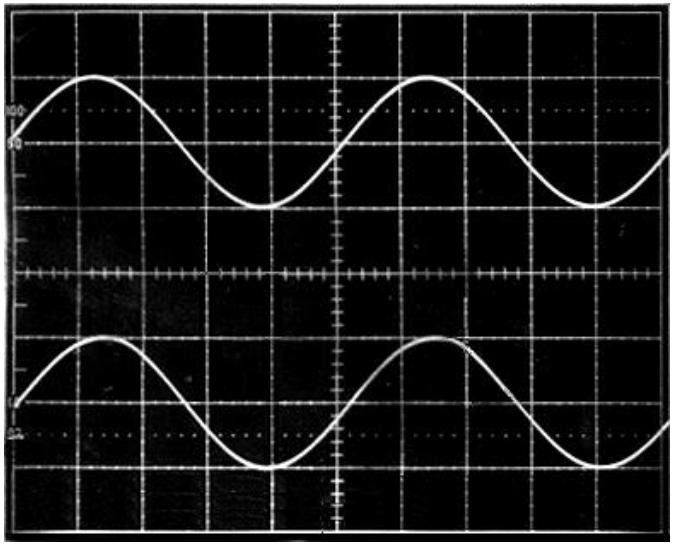
4-stage NGCC amplifer

Response to 100 kHz 1Vp-p sine wave



2 μS/DIV

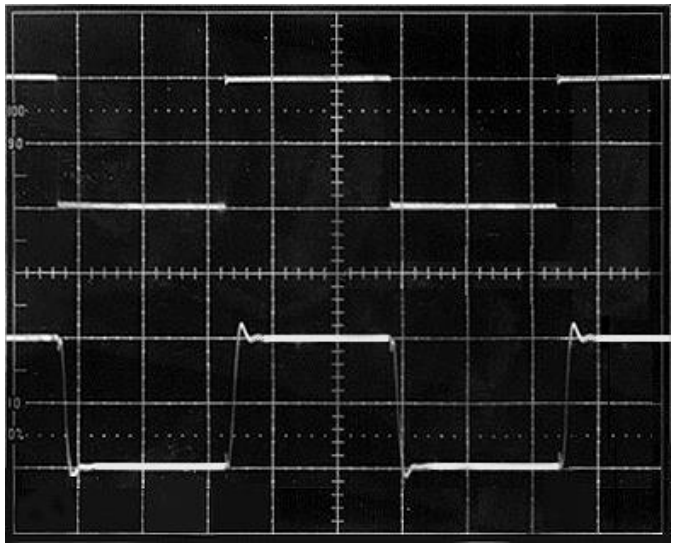
3-stage NGCC amplifier



2 μS/DIV

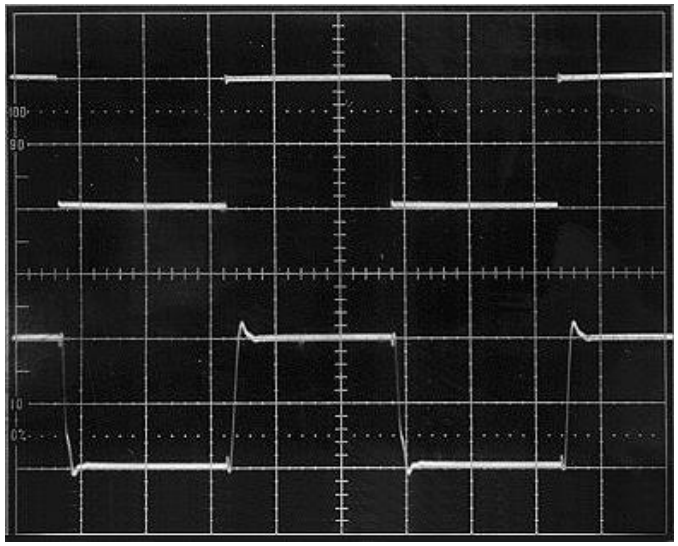
4-stage NGCC amplifier

Step Response with 100 kHz 100 mV Input



2 μS/DIV

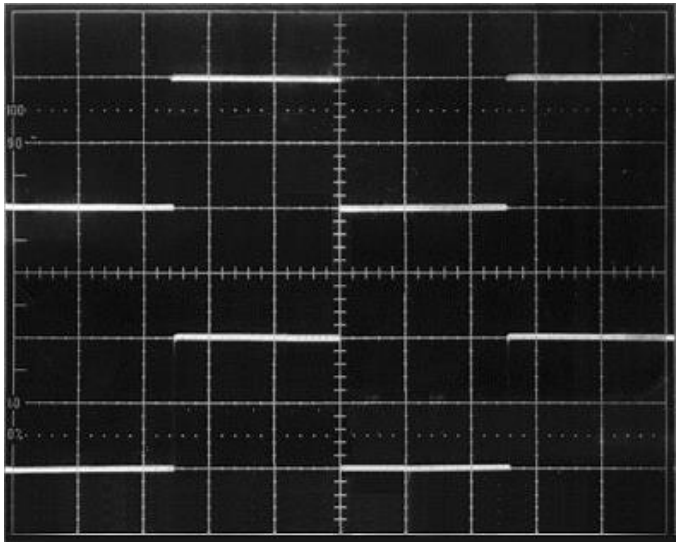
3-stage NGCC amplifier



2 μS/DIV

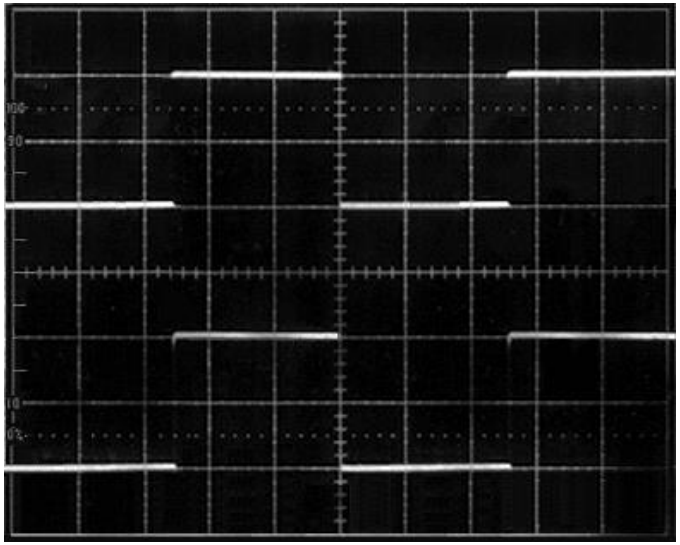
4-stage NGCC amplifier

Step Response with Large Signal (1 kHz 1V)



200 μS/DIV

3-stage NGCC amplifier



200 μS/DIV

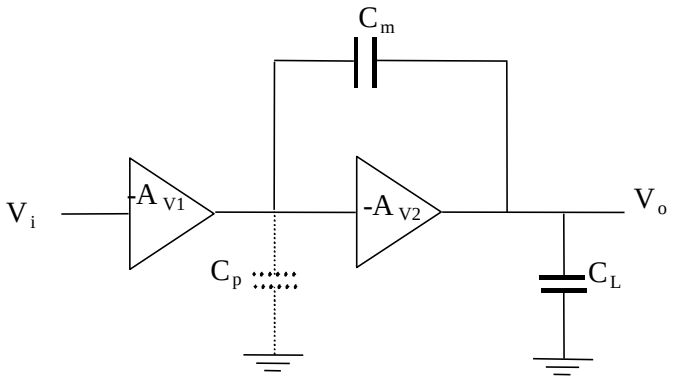
4-stage NGCC amplifier

Conclusions

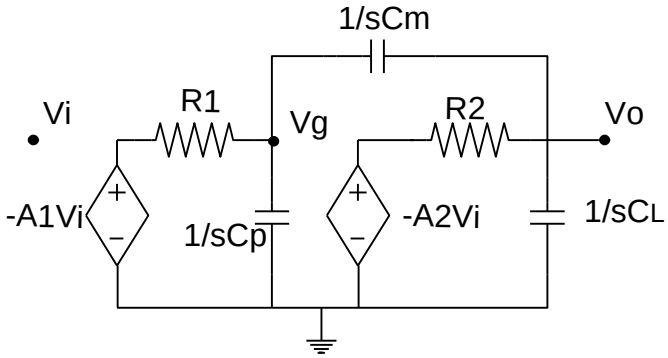
- Using a new MOSFET model, NGCC amplifiers can be designed in moderate inversion yielding optimal trade-off design.
- With same or better performance, low power amplifiers consume 65% less power than low voltage (strong inversion) design.
- Four-stage op amp has better overall performance with much less area and without dissipating evidently more power.
- Three-stage one benefits for the reduction of design complexity.

Alternative structures for the Nested Gm-C Architectures: Advantages and Disadvantages

Review: Cascade with Miller effect



(a)



$$\frac{Vo}{Vi} = \frac{A1(-A2 + sCmR2)}{1 + s(CpR1 + CLR2 + Cm(R1A1 + R1 + R2)) + s^2(CpCL + Cm(Cp + CL))R1R2}$$

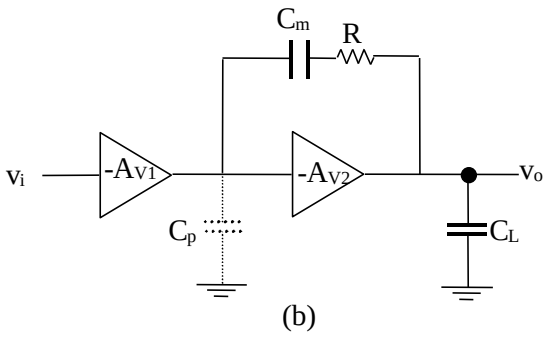
$$D(s) = 1 + \frac{s}{w_{p1}} + \frac{s^2}{w_{p1}w_{p2}}$$

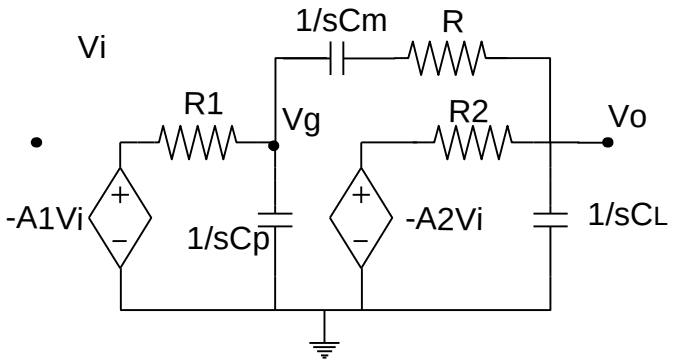
$$w_{p1} \approx \frac{-1}{CpR1 + CLR2 + Cm(A2R1 + R1 + R2)} \approx \frac{-1}{R1A2Cm} = -\frac{go1}{A2Cm}$$

$$w_{p2} \approx \frac{-CmA2 \cdot go2}{CpCL + Cm(Cp + CL)} \approx \frac{-gm2}{Cp + CL} \approx -\frac{gm2}{CL}$$

$$w_{z1} = +\frac{A2}{CmR2} = \frac{gm2}{Cm}$$

Pole splitting via RC feedback branch





$$\frac{Vo}{Vi} = \frac{\mathrm{A1(A2} + sCm(\mathrm{A2Rfs} - \mathrm{R2})}{(s^3\mathrm{CLR2CpR1RfCm} + s^2(\mathrm{Cm(CLR2Rf} + \mathrm{CpR1Rf} + \mathrm{CLR2R1} + \mathrm{R2CpR1}) + \mathrm{CLR2C}}$$

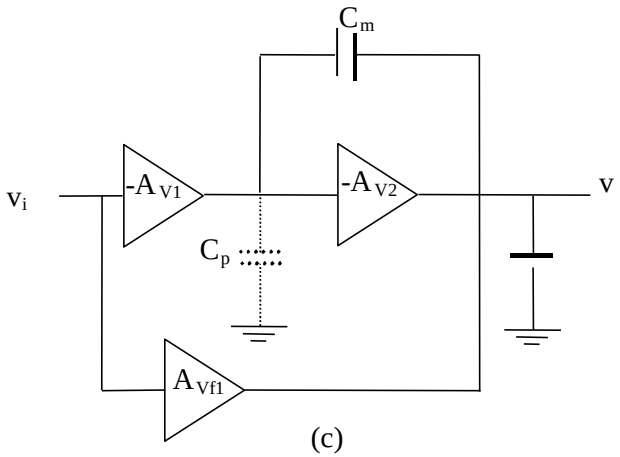
$$\frac{1}{+ s(\mathrm{RfCm} + \mathrm{A2CmR1} + \mathrm{CmR1} + \mathrm{CmR2} + \mathrm{CLR2} + \mathrm{CpR1}) + 1}$$

$$w_{p1} \approx \frac{-1}{CpR1 + CLR2 + Cm(A2R1 + R1 + R2)} \approx \frac{-1}{R1A2Cm}$$

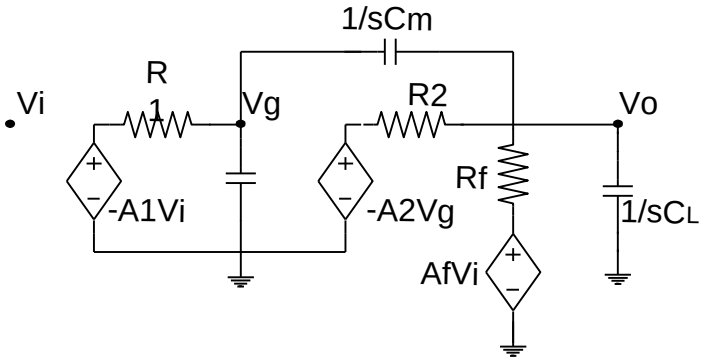
$$w_{p2} \approx \frac{-CmA2 \cdot go2}{CpCL + Cm(Cp + CL)} \approx \frac{-gm2}{Cp + CL}$$

$$w_{z1} = +\frac{1}{Cm(R2/A2 - R)} = \frac{1}{Cm(1/gm2 - R)}$$

Review: Feedforward compensation



(c)



° Transfer Function

$$\frac{Vi}{Vo} = \frac{-(-R2Af - A1RfA2 - s(CpR1R2Af + CmR2RfA1 - R2AfCmR1))}{s^2(CLR2RfCpR1 + CLR2RfCmR1 + CmR2RfCpR1 + s(RfCpR1 + RfCmR1)}$$

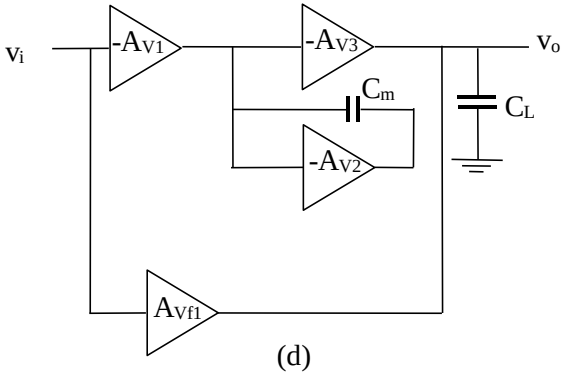
$$\frac{1}{+ s(CLR2Rf + CmR2Rf + R2CpR1 + R2CmR1 + RfA2CmR1) + Rf + R2}$$

$$\frac{Vo}{Vi} \approx \frac{-gm1gm2 + sCm(gm1 - gmf)}{go1go2 + s \cdot gm2Cm + s^2CLCm}$$

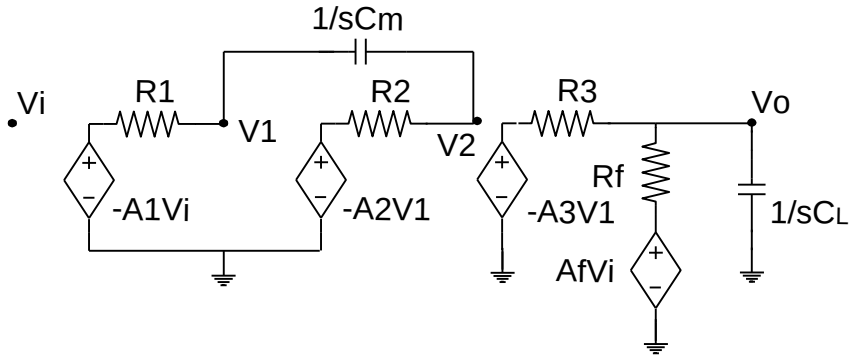
$$w_{p1} \approx \frac{-1}{gm2R2CmR1} \approx \frac{-1}{A2CmR1} \qquad w_{z1} \approx \frac{gm1gm2}{Cm(gm1 - gmf1)}$$

$$w_{p2} \approx \frac{gm2}{CL}$$

Creating and internal zero cancellation DFCFC



(d)



$$w_{p1} \approx \frac{-\mathrm{gm1}}{\mathrm{CmR2(gm1+gm2)}}\Big|_{gm1=gm2} = -\frac{g02}{2Cm}$$

$$w_{p2} \approx \frac{-(\mathrm{Rf}+\mathrm{R3})}{\mathrm{R3}\cdot\mathrm{Rf}\cdot\mathrm{Cm}}\Big|_{Rf=R3} = -\frac{2}{R3Cm}$$

$$w_{z1} \approx -\frac{\mathrm{R1gmfgm1}+\mathrm{gm3}}{\mathrm{Cm(R1gmfR2\,gm1}+\mathrm{R1gmfgm2R2}+\mathrm{gm3R1}+\mathrm{gm3R2)}}$$

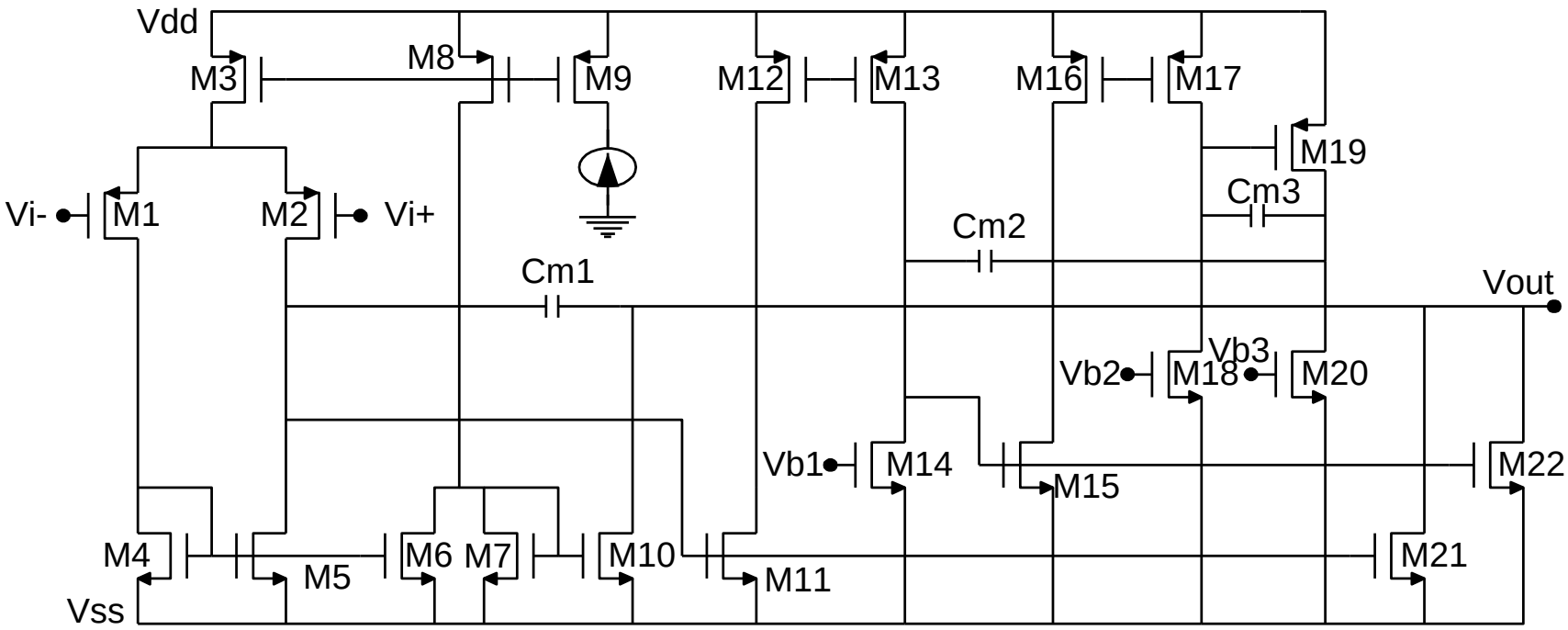
Damping factor frequency controlled compensation (DFCFC)

Amplifier Comparisons

- 4 stage NGCC Amplifier.
- 3 stage DFCFC Amplifier

Parameters	NGCC	DFCFC
Av (dB)	100.3	100.4
GBW (MHz)	8.21	8.23
Phase Margin(`)	70	75
0.2% Settling Time(ns)	373	398
Slew Rate(+) (V/us)	11.2	8.2
Slew Rate(-) (V/us)	-7.1	-6.7
CMR (V)	1.25	0.97
CMRR (dB)	63.02	28.55
PSRR+ (dB)	49.62	24.05
PSRR- (dB)	29.1	20.48
Input Referred Offset (v)	290n	-4.13u
Active Area (um^2)	233.4	228.88
Power Consumption (mW)	1.2	0.4

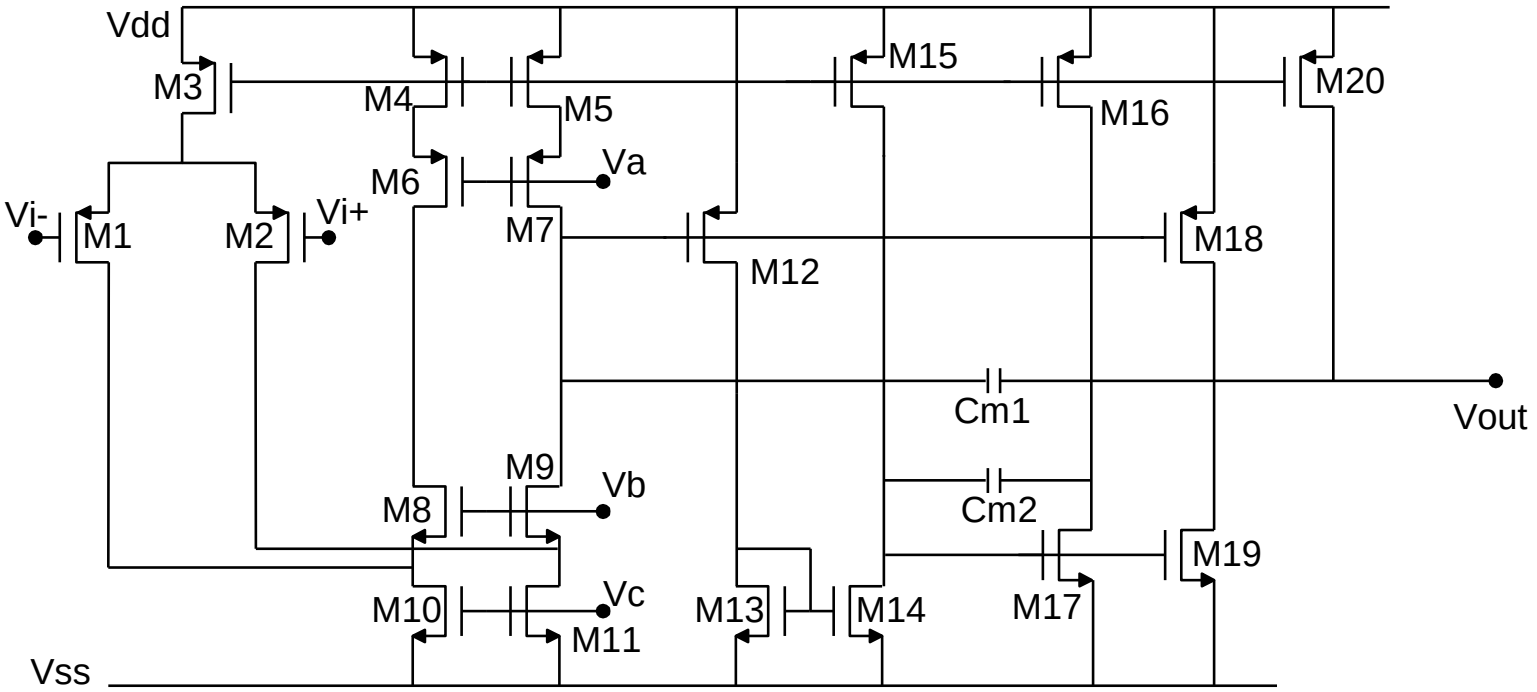
4 stage NGCC Amplifier.



Design Summary

#	M1	M2	M3	M4	M5	M6	M7	M8
Size	49/.4	46/.4	36/.4	10/.4	10/.4	38/.4	6.5/.4	38/.4
#	M9	M10	M11	M12	M13	M14	M15	M16
Size	38/.4	6.5/.4	22/.4	22/.4	22/.4	10/.4	20/.4	30/.4
#	M17	M18	M19	M20	M21	M22	•	•
Size	30/.4	20/.4	70/.4	20/.4	23/.4	44/.4		

3 stage DFCFC Amplifier



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#	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
Size	38/.4	38/.4	48/.4	1.2/.4	1.2/.4	1.2/.4	1.2/.4	1.2/.4	1.2/.4	18/.4
#	M11	M12	M13	M14	M15	M16	M17	M18	M19	M20
Size	18/.4	30/.4	22/.4	45/.4	45/.4	9/.4	3/.4	31/.4	95/.4	53/.4

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