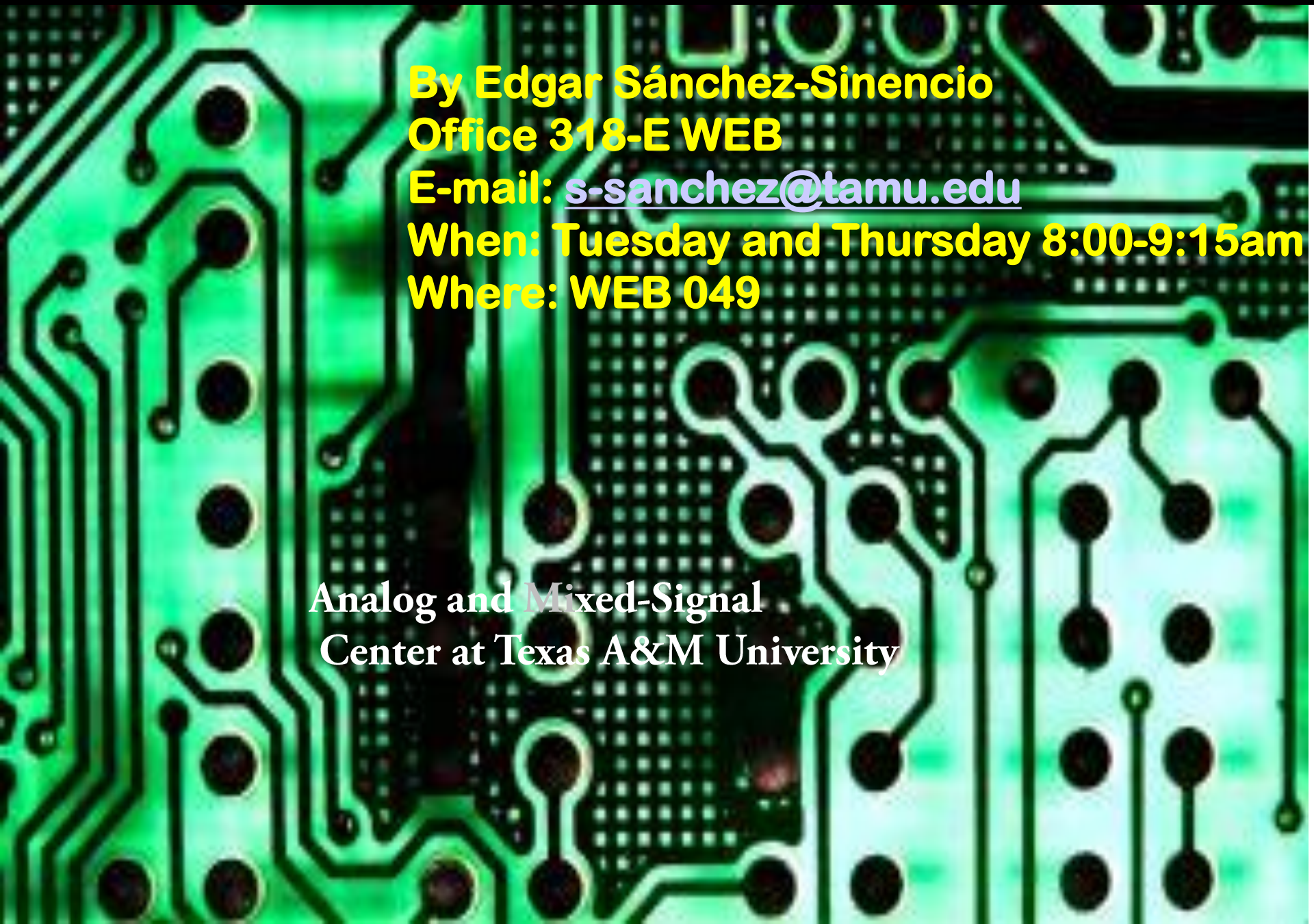
ADVANCED ANALOG CIRCUIT DESIGN TECHNIQUES



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Where: WEB 049

Analog and Mixed-Signal
Center at Texas A&M University

Advanced Analog Circuit Design Techniques

Required background:

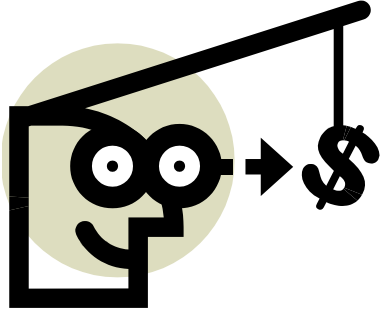
1. How to optimally bias your CMOS circuits
2. How to use MOS transistor models
3. Derive transfer functions from small signal circuits
   - Use of nodal admittance matrix
1. Stability Criteria.
   - How to determine pole and zeros.?
   - Routh Hurtwitz Criteria
   - Reduction of a higher-order system into a 2nd-order function
1. How to design:
   1. Inverting Amplifiers
   2. Current mirrors and current sources
   3. Differential pairs, and low noise amplifiers
   4. Simple Transconductor Amplifiers
   5. Two Stage Conventional Operational Amplifiers

6. Basic common-mode feedback structures for Fully Differential Operational Amplifiers
7 Common Mode Feedback Concept

Required background (continues):

- **Use CADENCE for**
  - **Noise Analysis**
  - **Monte Carlo Analysis**
  - **S/N ratio determination**
  - **Pole and zero determination**
  - **Temperature effects**
  - **Use of non-linear dependent sources**

- **Use of SIMULINK for systems analysis, modeling and characterization**



What is the motivation?

The knowledge and applications of analog circuits in medical electronics, modern mixed-signal IC chips for multimedia, energy harvesting , wearable devices, instrumentation and telecommunications are vital design element of any practical and commercial system.

- What are the challenges in designing low voltage circuits ?

  - To perform with technologies smaller than 40 nm

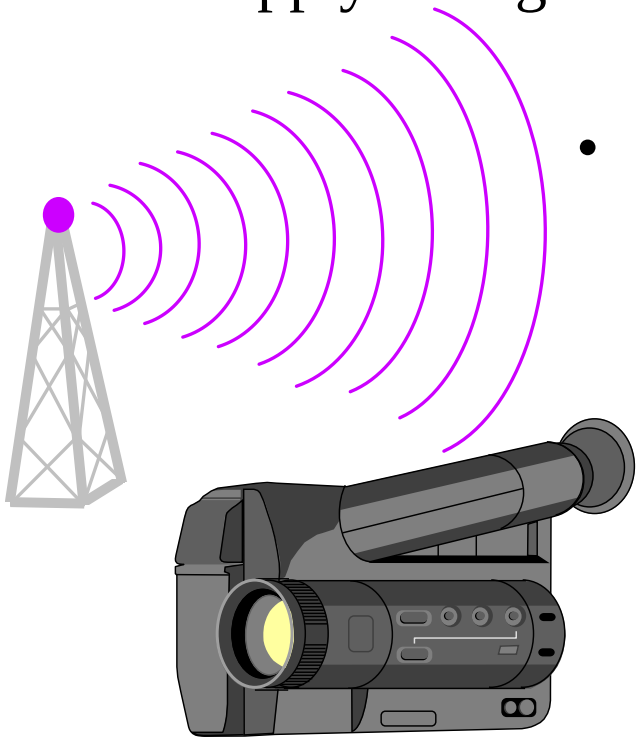
  - To operate with power supplies smaller than 1 volt

  - To design circuits with the same performance or better than circuits designed for larger power supplies

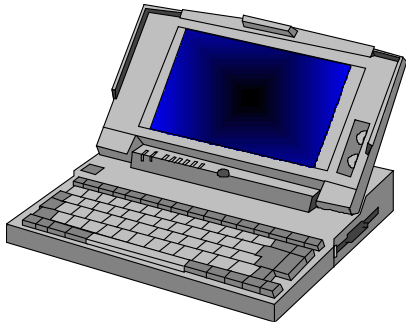
  -To generate new design alternatives

Why Low-Voltage Analog Integrated Circuits?

- Modern CMOS feature size is continuing to be scaled down to have a high f_T and large component density. In addition the maximum allowable power supply voltage continuously decreases.



- Therefore portable battery-powered equipment also necessitates low-voltage low-power circuit design.



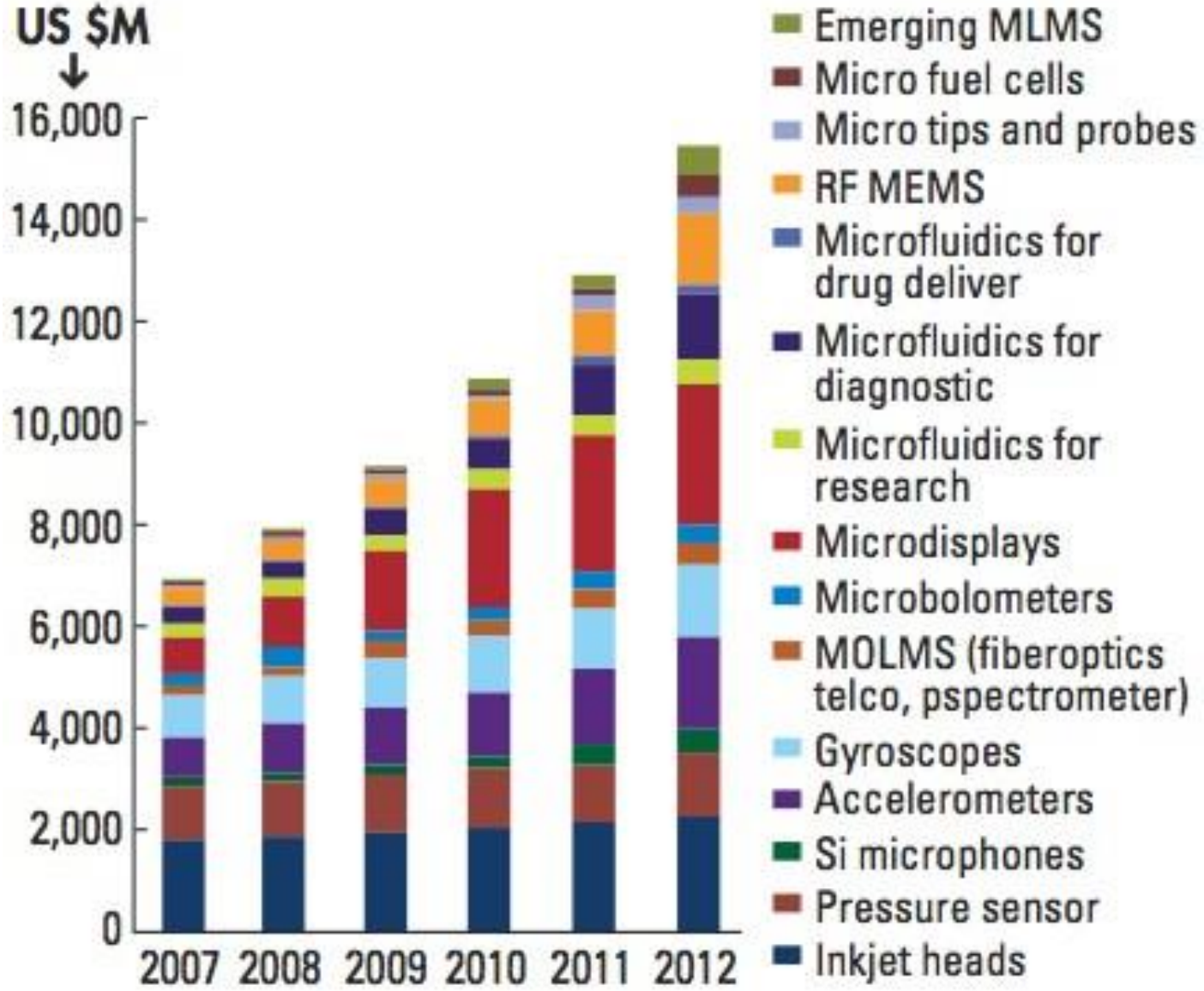
2014F Top 20 Semiconductor Sales Leaders ($M)

2014F Rank	2013 Rank	Company	Headquarters	2013 Total	2014 Total	2014/2013 % Change
1	1	Intel	U.S.	48,321	51,368	6%
2	2	Samsung	South Korea	34,378	37,259	8%
3	3	TSMC*	Taiwan	19,935	25,088	26%
4	4	Qualcomm**	U.S.	17,211	19,100	11%
5	5	Micron + Elpida	U.S.	14,294	16,614	16%
6	6	SK Hynix	South Korea	12,970	15,838	22%
7	8	TI	U.S.	11,474	12,179	6%
8	7	Toshiba	Japan	11,958	11,216	-6%
9	9	Broadcom**	U.S.	8,219	8,360	2%
10	10	ST	Europe	8,014	7,374	-8%
11	11	Renesas	Japan	7,975	7,372	-8%
12	12	MediaTek + MStar**	Taiwan	5,723	7,142	25%
13	14	Infineon	Europe	5,260	6,151	17%
14	16	NXP	Europe	4,815	5,625	17%
15	13	AMD**	U.S.	5,299	5,512	4%
16	17	Sony	Japan	4,739	5,192	10%
17	15	Avago + LSI**	Singapore	4,979	5,087	2%
18	19	Freescale	U.S.	3,977	4,548	14%
19	20	UMC*	Taiwan	3,940	4,300	9%
20	21	Nvidia**	U.S.	3,898	4,237	9%
Top 20 Suppliers				237,379	259,562	9%
Top 20 Suppliers Excluding Foundries				213,504	230,174	8%

*Foundry **Fabless

Source: IC Insights' Strategic Reviews Database

MEMS market forecast, 2007-2012



Technology Forecast (from http://www.itrs.net/ ITRS Roadmap 2009)

Year of Production	2009	2011	2013	2015	2017	2019
Supply Voltage(V)#	1/2.5	0.93/1.8	0.87/1.8	0.81	0.76	0.71
DRAM ½ Pitch (nm) (contacted)	52	40	32	25	20	15.9
Gate length(nm)	37/250	28/180	22/180			
Threshold Voltage (V)	0.33	0.31	0.29	0.27	0.25	0.23
Gm/gds at 5(10)Lmin	30(220)	30(160)	30(160)			
1/f noise ($uv^2.um^2/Hz$)	**100/500**	**80/180**	**70/180**			
NFmin(dB)	0.20	<0.2	<0.2			
Peak Ft (GHz)	240/40	320/50	400/50			
Peak Fmax (GHz)	370/40	480/50	590/50			

one data is for Performance RF/Analog and the other for Precision Analog/RF Driver

(continues)

- Why are we concerned in designing low voltage circuits ?

  - Designers could not use conventional cascode structures, and other conventional design methodologies yielding high signal swing.

  - Circuits must have the same performance or better than circuits designed for larger power supplies

  - Circuit performance with technologies smaller than 65 nm must be better than circuits for larger technologies.

  -Fourth-generation communication applications require circuits (and systems) with improved dynamic range over a much wider bandwidth.

  - New building blocks and systems must be designed to satisfy the needs of portable, lighter, cheaper and faster products

Remarks.-

- Power supply reduction helps digital circuits for power consumption but hurts analog voltage swing which should not be reduced.
- Inherent transistor voltage gain decreases with reduced size technology, this implies larger number of stages to compensate the overall voltage gain.
- Threshold voltages do not reduce linearly with size of technology, making the design with low V_{DD} harder for analog circuits

Year of Production	2009	2011	2013	2015	2017	2019
Threshold Voltage (V)	0.33	0.31	0.29	0.27	0.25	0.23

Concerns about low power supply voltage

Scaling down size technology and supply voltage does not scale linearly the " VTH hat "

Mister 3.3 volts IC

Mister 0.5 volts IC

- Also VDSAT does not scale down linearly with power supply nor with smaller size technologies.

Remarks on low power supply voltage integrated circuits

Technology trends show that in every generation:

- **Circuit delay is scaling down by 30%**
- **Supply voltages are also scaling by 30%**
- **Transistor's threshold voltage is reduced by nearly 15%**
- **Transistor density and digital performance are double approximately every two years.**
- **Higher power dissipation and temperature.**

Reference . W. M. Elgharbawy and M. A. Bayoumi, "Leakage Sources and Possible Solutions in Nanometer CMOS Technologies" *IEEE Circuits and Systems Magazine, pp. 6-15, Fourth Quarter 2005*

LOW VOLTAGE ANALOG DESIGN TECHNIQUES

- When transistors operate in saturation, how deep in saturation should they operate ? i.e. PMOS

Vds >Vgs-Vt ? By how much ? How can one answer this question?

- Can one model transistor with one equation valid for all regions of operation?
- If LV circuits do not allow cascode circuits, what are the alternatives?
  - *Floating Gate*
  - *Bulk Driven*
  - *Bulk Bias*
  - *Nested Gm-C (cascade plus optimal feedback compensation)*
  - *Self Cascode Transistor*
  - *NP Differential Pairs*

TRANSISTOR REGIONS OF OPERATION

- How to determine how much bias current is needed for certain application ?

- When a designer operates transistors in saturation, what does it mean VDS > VDS*(SAT)* ?

- Can a circuit have their transistors operating in the (moderate inversion) transition region ? What transistor model equation can be employed ?

One Equation-All Regions Transistor Model

- Features of ACM model:
  - physics-based model,
  - universal and continuous expression for any inversion level
  - independent of technology, temperature, geometry and gate voltage,
  - same model for analysis, characterization and design.
- Main design equations: (design parameters: I, g_m, i_f)

$$\frac{I}{\phi_t g_m n} = \frac{1+\sqrt{1+i_f}}{2}$$

$$f_T = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right)$$

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox}\phi_t} \frac{1}{\sqrt{1+i_f}-1}$$

$$\frac{V_{DSAT}}{\phi_t} \cong \left(\sqrt{1+i_f}-1\right)+4$$

$$\frac{W}{L} = \frac{g_m}{2\mu C_{ox}\phi_t\left(\frac{I}{\phi_t g_m n}-1\right)}$$

I — transistor drain current
g_m — transconductance in saturation
n — slope factor
ϕ_t — thermal voltage
i_f — inversion level of the transistor defined as $i_f = I/I_s$, where $I_s = \mu n C_{ox} \frac{\phi_t^2}{2} \frac{W}{L}$ is the normalization current.

$i_f << 1$ — weak inversion,

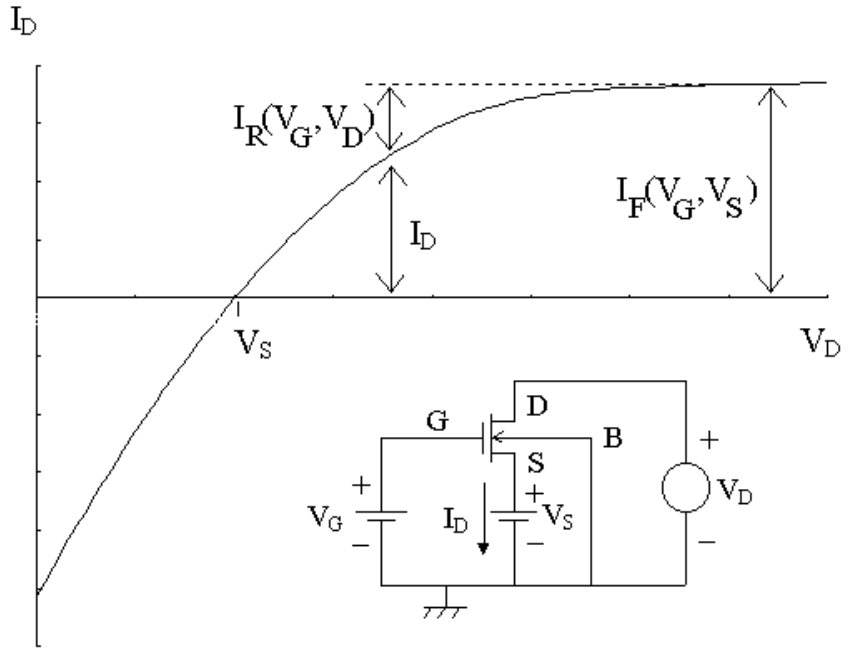
$i_f >> 1$ — strong inversion.

• Current-based MOSFET model(drain current split into a forward and a reversed term:

$$I_D = I_F - I_R$$

$$I_{F(R)} = \mu C_{ox} \frac{W}{L} \frac{1}{2n} \left(V_{GB} - nV_{SB(DB)} - V_{T0} \right)^2$$

$$V_{DB} = \frac{V_{GB} - V_{T0}}{n}$$



• Forward saturation

$I_F >> I_R$ and $I_D \cong I_F$

• Normalized output characteristic:

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f} - 1}{\sqrt{1+i_r} - 1} \right)$$

$$i_{f(r)} = \frac{I_{F(R)}}{I_S} \qquad I_S = I_{SQ}\left(\frac{W}{L} \right)$$

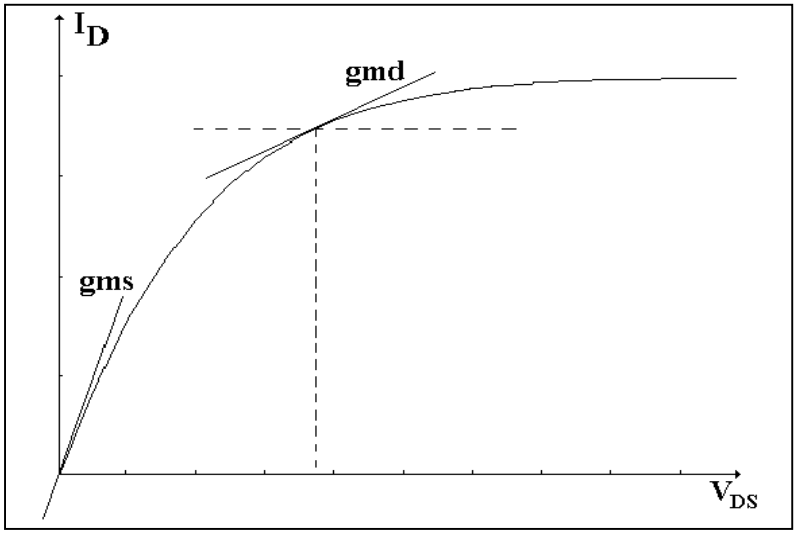
I_{SQ} =technological parameter (slightly dependent on V_G)

The Saturation Voltage

$$A = \frac{gms}{gmd} = \text{gain in CG configuration}$$

$$\frac{V_{DSSAT}}{\phi_t} = \ln(A) + \left(1 - \frac{1}{A}\right)\left(\sqrt{1 + i_f} - 1\right)$$

$\left(1 - \frac{1}{A}\right)$ — saturation level

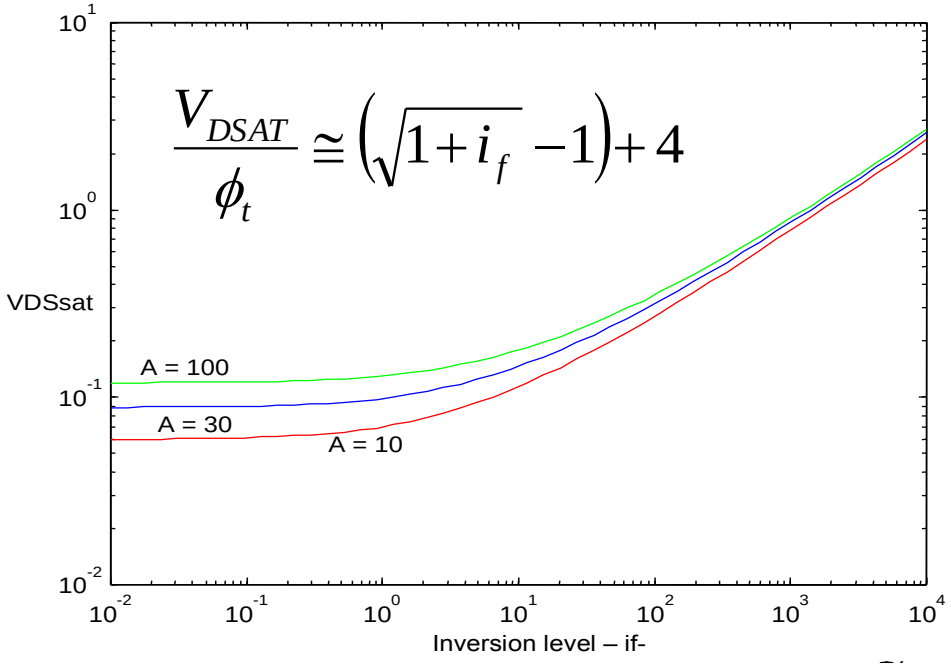


•Strong inversion

$$V_{DSSAT} \cong \phi_t \sqrt{i_t} = (V_G - V_T)/n$$

•Weak inversion

$$V_{DSSAT} \approx \phi_t . \ln(A)$$

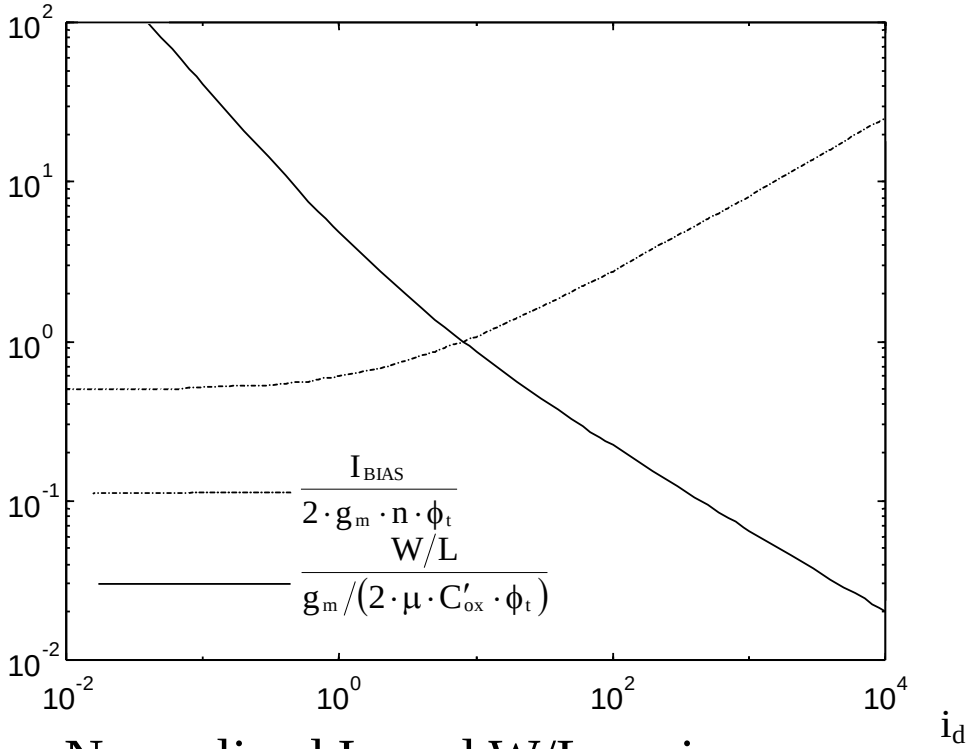


Drain Current and Aspect Ratio

$$g_m = 2\pi \cdot GBW \cdot CL$$

$$I_D = g_m \cdot n \cdot \phi_t \frac{1+\sqrt{1+i_f}}{2}$$

$$\frac{W}{L} = \frac{g_m}{\mu \cdot C'_{ox} \cdot \varphi_t}\left(\frac{1+\sqrt{1+i_f}}{i_d}\right)$$



Normalized I_D and W/L vs. i_f

	WI (i_f<<1)	**MI (i_f=8)**	**SI (i_f>>1)**
normalized I_D	**1/2**	**1**	$\sqrt{i_f}/4$
normalized W/L	$4/i_f$	**1**	$2/\sqrt{i_f}$

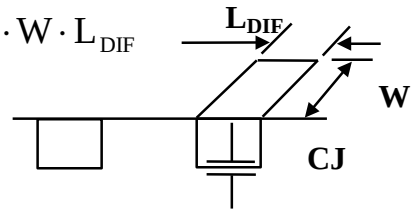
Correlation Between Area and Frequency Response

$$WL \cong 2\frac{CL}{C'_{ox}}\frac{GBW}{f_T}$$

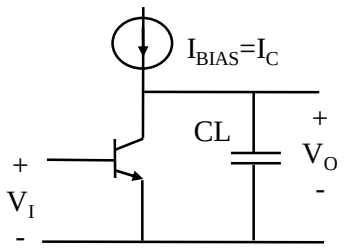
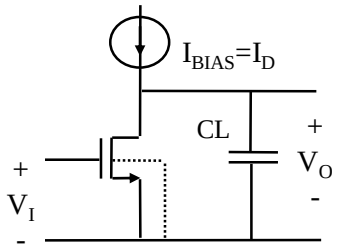
Correlation Between Junction Capacitance (CJ) and Frequency Response

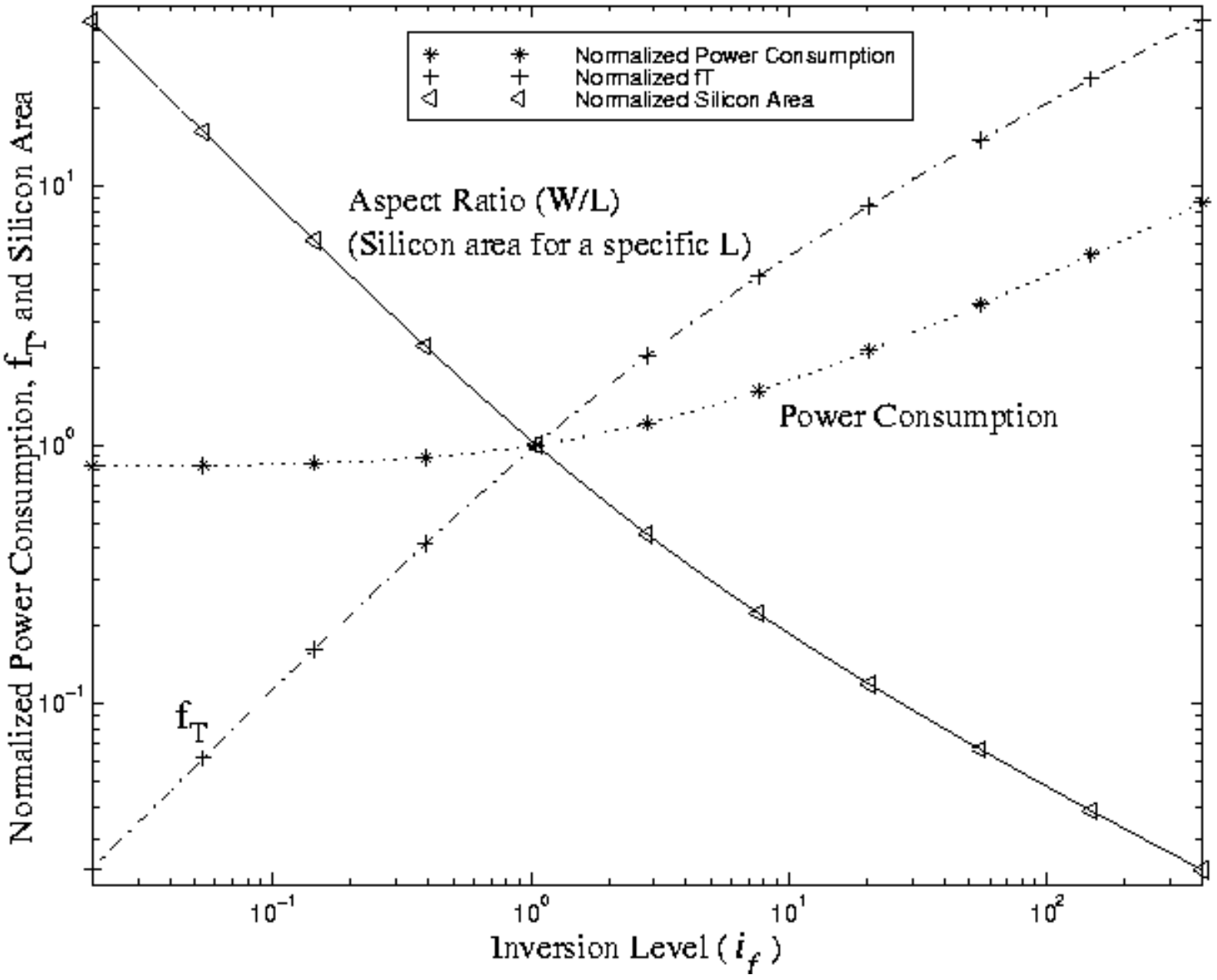
Parasitic capacitance α GBW/f_T

$$CJ = CJ' \cdot W \cdot L_{DIF}$$



$$\frac{CJ}{CL} \cong 2\frac{CJ'}{C'_{ox}}\frac{L_{DIF}}{L}\frac{GBW}{f_T}$$

	BIPOLAR	MOS
DC Circuit		
Transconductance -to-current-ratio (g_m/I_D)	$\frac{g_m}{I_C} = \frac{1}{\phi_t}$	$\frac{g_m}{I_D} = \frac{1}{\varphi_t}\left(\frac{2}{n\left(1+\sqrt{1+i_f}\right)}\right)$
DC Gain (A_{vo})	$A_{vo} = -\frac{VA}{\phi_t}$	$A_{vo} = -\frac{VA}{\phi_t}\left(\frac{2}{n\left(1+\sqrt{1+i_f}\right)}\right)$
Gain-Bandwidth Product (GBW)	$GBW = \frac{1}{2\pi CL}\frac{I_C}{\phi_t}$	$GBW = \frac{1}{2\pi CL}\frac{I_D}{\phi_t}\left(\frac{2}{n\left(1+\sqrt{1+i_f}\right)}\right)$
Intrinsic Cutoff Frequency (f_T)	$f_T \cong \frac{1}{2\pi\tau}$	$f_T \cong \frac{1}{2\pi\tau}2\left(\sqrt{1+i_f}-1\right)$
Minimum Output Voltage (V_O)	$\frac{V_{CEsat}}{\phi_t} \cong 6 \text{ to } 8$	$\frac{V_{DSsat}}{\phi_t} = \left(\sqrt{1+i_f}-1\right)+4$


Normalized Power Consumption
Normalized fT
Normalized Silicon Area
Aspect Ratio (W/L)
(Silicon area for a specific L)
Power Consumption
f_T
Normalized Power Consumption, f_T, and Silicon Area
Inversion Level (i_f)
10^{-1}
10^{0}
10^{1}
10^{2}

Design Methodology

1 - Select the inversion level (i_f) for 'optimal' design (I_D, W/L).

$$I_D = g_m \cdot n \cdot \varphi_t \frac{1+\sqrt{1+i_f}}{2}$$

$$\frac{W}{L} = \frac{g_m}{\mu \cdot C'_{ox} \cdot \varphi_t \left(\frac{1}{\sqrt{1+i_f}-1} \right)}$$

$$\frac{V_{DSsat}}{\phi_t} = \left(\sqrt{1+i_f} - 1 \right) + 4$$

2 - Choose both W and L. If $f_T \cong GBW$, add the parasitic capacitances (CJ, Cov) to CL.

$$\frac{CJ + Cov}{CL} = 2 \frac{1}{LC'_{ox}} \left(CJ'L_{DIF} + CGDO \right) \frac{GBW}{f_T}$$

3 - Verify if the spec for A_{vo} is met. Otherwise, increase the channel length and/or reduce i_d (cascode/cascade design can be necessary).

4 - Take into account V_{DSsat} and the parasitic capacitance of the current source.

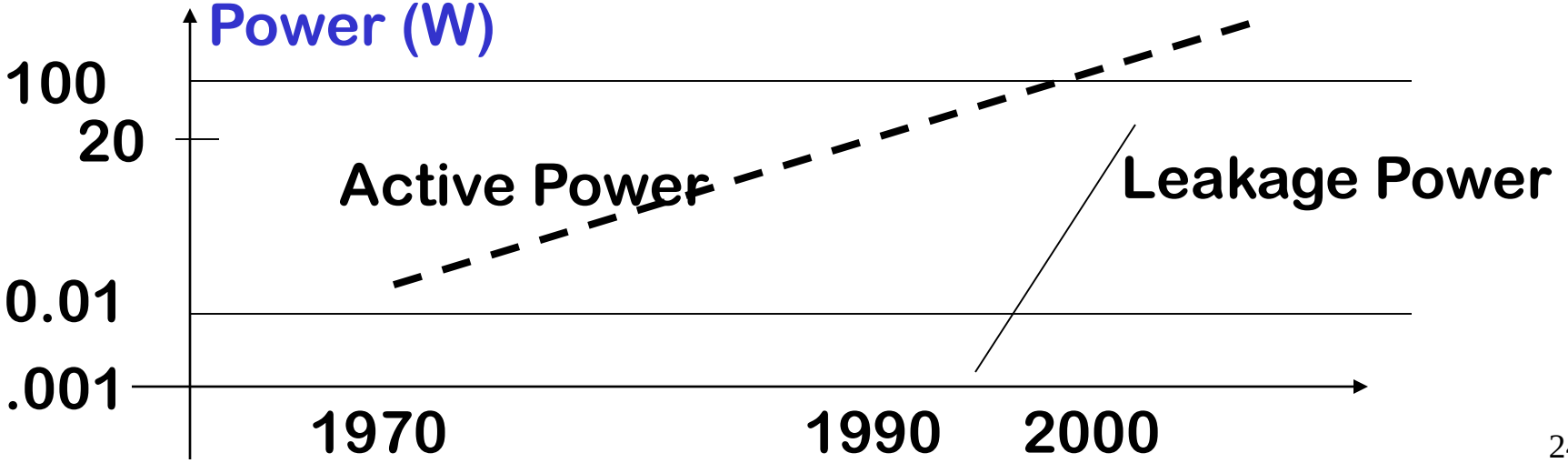
Analog and Mixed-Signal Circuit Design

- Process technology to choose
  - Cost
  - Performance
  - Compatibility
- Design approach and testing time
  - Floating Gate
  - Bulk-driven
  - LV techniques
- Region of operation
  - Weak inversion
  - Moderate inversion
  - Ohmic region
  - Saturation (strong inversion)

Small Size Technology

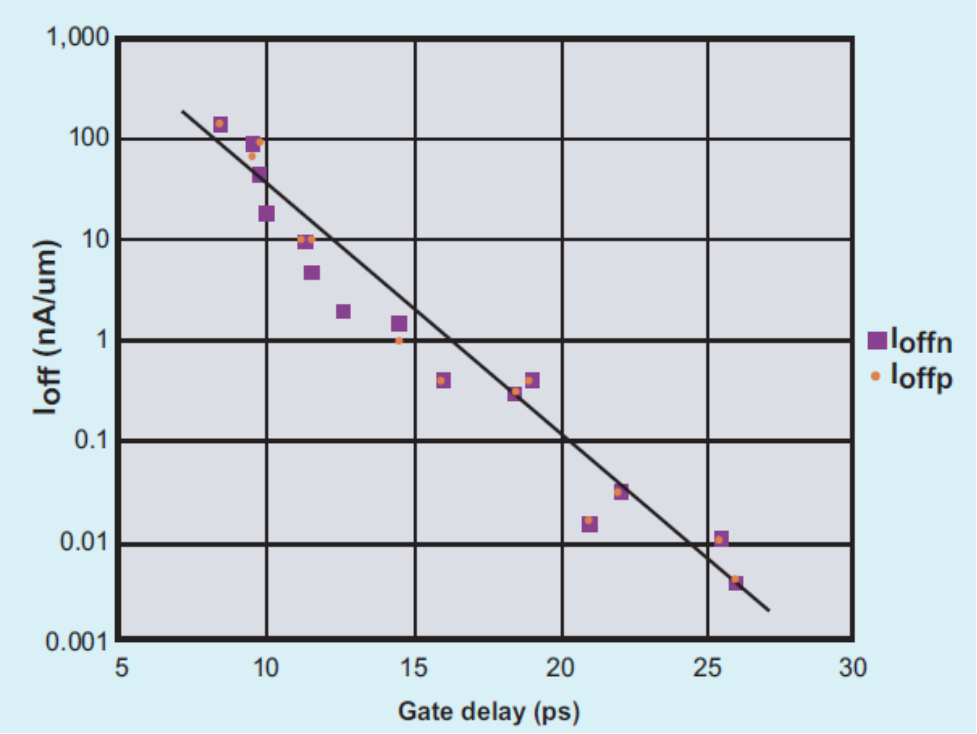
- The good news is that we will be able to run our ICs faster **i.e., circuit delay is scaling down by 30% every generation.**

- The bad news is that leakage power dissipation increases in a much faster rate than dynamic power



Example: 90nm

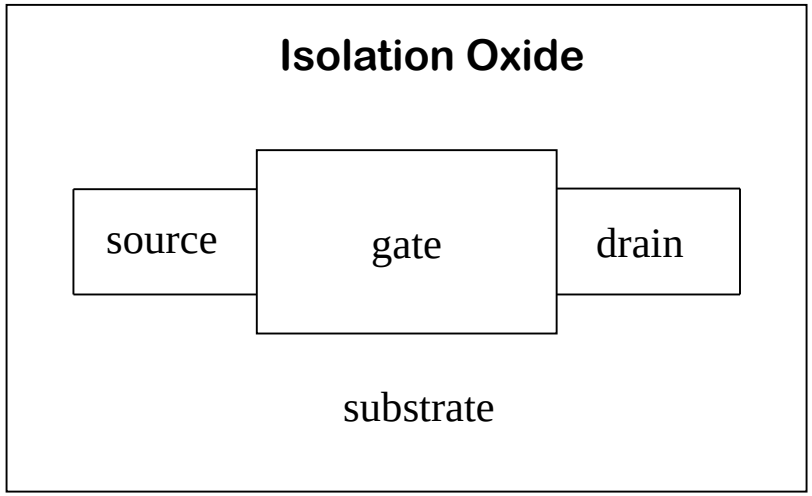
- sub-threshold leakage increases exponentially with every 65mV decrease in threshold voltage



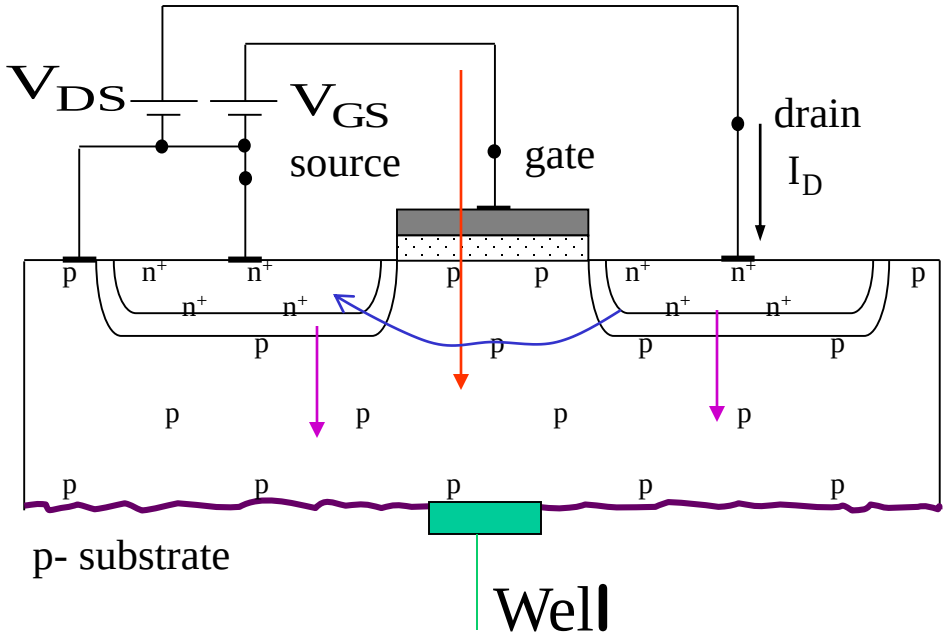
LEAKAGE SOURCES IN CMOS CIRCUITS

1. Subthreshold leakage in the channel in an OFF transistor between the source and drain terminals (I_{sub})
2. Reverse-bias source/drain junction leakage (I_{RB})
3. Gate leakage (I_{GATE})

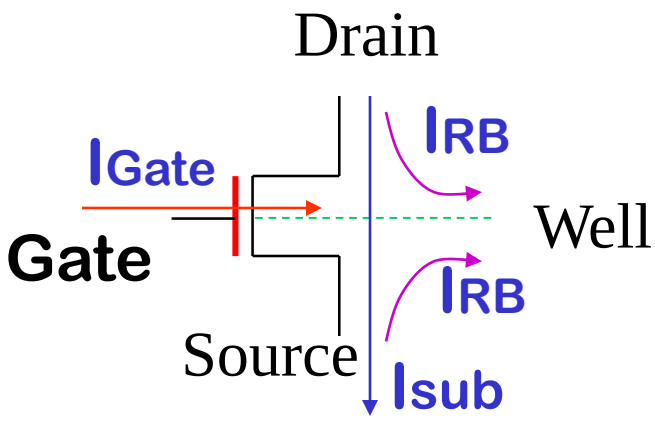
NMOS TRANSISTOR and ITS THREE MAIN LEAKAGE SOURCES



Top view



$V_{GS} = 0, V_{DS} = 0$ (cutoff)



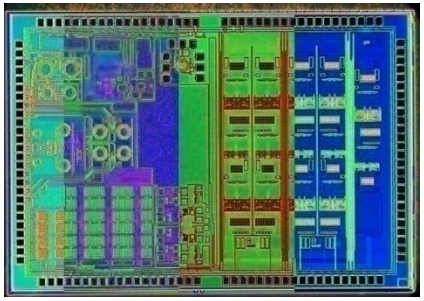
High Speed Amplifiers Remarks

- Op Amps usually have more than one high impedance node, this slow significantly the speed of amplifier. Recall that poles are inversely proportional to time constants. Thus large impedance node imply poles near the origin.
- Transconductance Amplifiers have ideally only one high impedance node, all the internal nodes are low impedance. This produces low voltage gains but the highest frequency response.

Course Objectives:

To understand at the macromodel level the circuit design parameter tradeoffs.

To design optimal circuits, that is circuits that meet the specifications with minimum area, design time and/or power.



To identify the effect of the non-idealities of actual circuits and how to overcome these problems.

Next we review the *conventional Op Amp Design frequency response compensation* techniques and also we introduced a simple LV Current-Mode based Op Amp using resistors as transconductors. Difference Differential Amplifiers are also introduced.