ELEN 607 (ESS) **Due: February 7, 2017**
SPRING '17

HOMEWORK ASSIGMENT #2

Prob. 1. a) Design, using macromodel of the Op Amp, a Negative Impedance Converter, for two cases: Z_N =R and Z_N =1/sC (see page 2 of notes). Use and ideal Op Amp with high Ao and no frequency dependence of the Op Amp. Determine the input impedances.
b) Assume A(s) =GB/s and obtain the corresponding Negative Impedance Converter Input impedance expressions for the two cases mentioned above. What are the bounds for a negative impedance converter, that is the frequency range where the input admittance behaves a –sC.
c) Use any of the Op Amp designed in HW 1, and implement the NIC for R=10K and C=6.28pF, Provide the frequency and step response of the input impedance. Make comments on the results and suggest improvements.

Prob. 2. This problem* has as a goal to increase the DC gain (Ao) and effectively reduce the effective output capacitance of any of your designed Op Amp in HW. 1 You can select the suitable NIC for this solution.

a) Select the best of your designed Op Amp in previous HW, then use a negative impedance* converter to reach this spec of an improvement of Ao of at least 20dB.
b) Repeat the operation to effectively reduce the load capacitance to 10pF instead of the original 25pF.
c) Provide in a Table form the specs obtained with and without the NIC. What are the parameters that change more significantly? Make comments.

*S. Szczepanski, J. Jakusz and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications," in IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, no. 3, pp. 174-187, Mar 1997. http://ieeexplore.ieee.org/document/558452/

"The great aim of education is not knowledge but action. "
-Herbert Spencer