ECEN 607 Due: **April 6, 2017**

Spring '17

HOMEWORK ASSIGNMENT #7

A team of 1 or 2 can submit the homework

Problem 1. Design an H-bridge as shown in Fig. 1 in a CMOS 0.13µm technology for the following specifications:

Specification	Value
Load	8 Ω
Output power	500 mW
VDD	1.2 V
Efficiency @ 500mW	95%
Switching frequency	1 MHz

Show your design procedure to minimize conduction losses and switching losses.

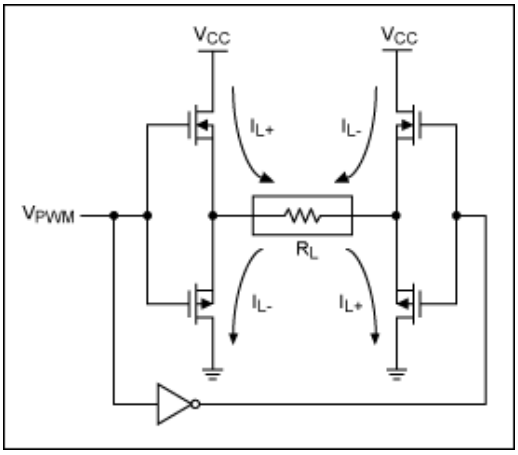

Fig. 1. H-bridge configuration.

Problem 2. Design a triangle waveform generator in CMOS 0.13µm for the following specifications:

Specification	Value
THD	23 dB
VDD	1.2 V
Switching frequency	1.2 MHz
Quiescent current	100 µA

Show your design procedure and minimize Cref.

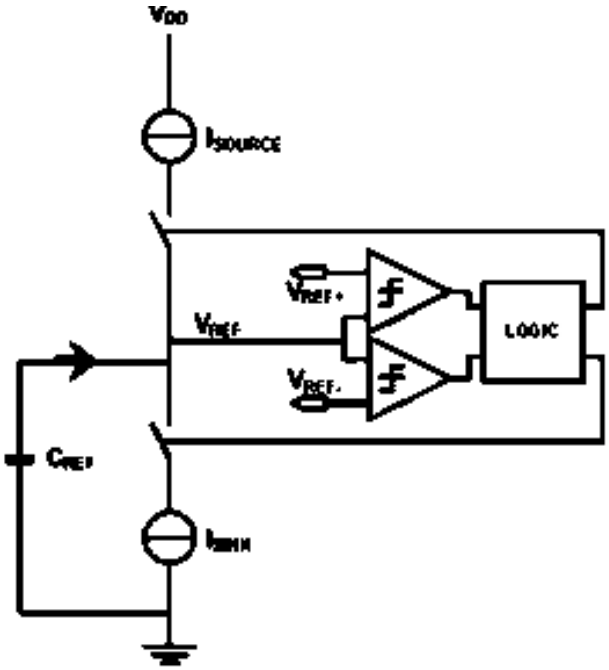

Fig. 2. Triangle-Wave topology.

Problem 3. Using macrodels for the opamp and comparators,

a) Design an open loop class-D amplifier using your designed H-bridge and reference generator. Perform THD, efficiency, and noise measurements.
b) Repeat a) in a close loop configuration.
c) Compare the two results in a table and comment about results.

Problem 4. Design a Class-D amplifier meeting the following specs. You can use any CDA topology including Hysteretic (self-oscillating) or the slide mode control. Use 130nm technology. Provide detail design procedure and discuss your final simulated results

Specification	
Load	8 Ω
Output power	0.5 W
VDD	1.2 V
Efficiency @ 500mW	95%
Switching frequency	1.2 MHz
Full Power THD	0.020 %