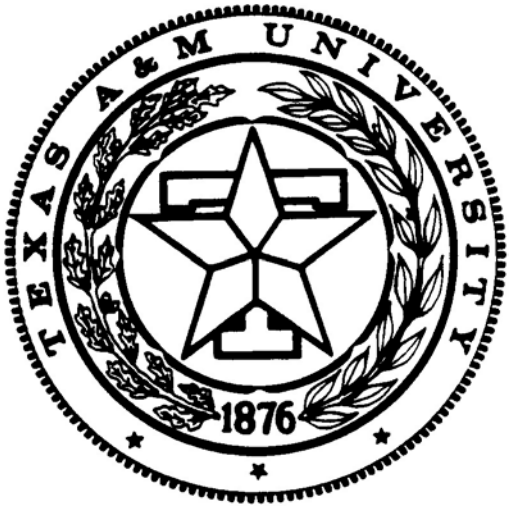
Electrical and Computer Engineering Department

Texas A&M University



ECEN 607

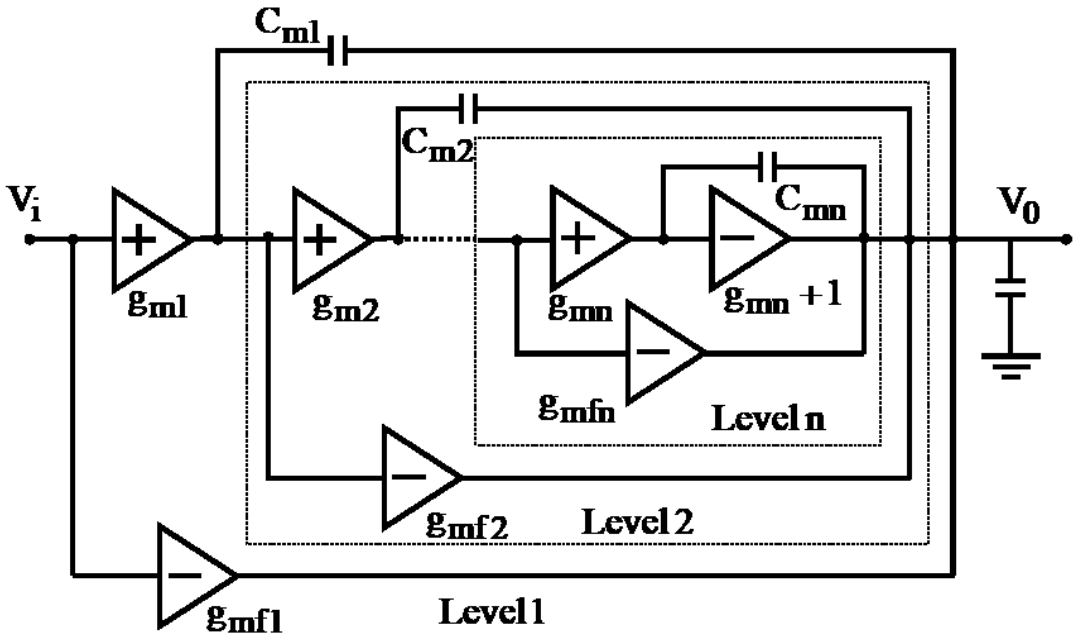
Advanced Analog Circuit Design

Homework 1

JESSE COULON

February 11, 2009

PROBLEM 1

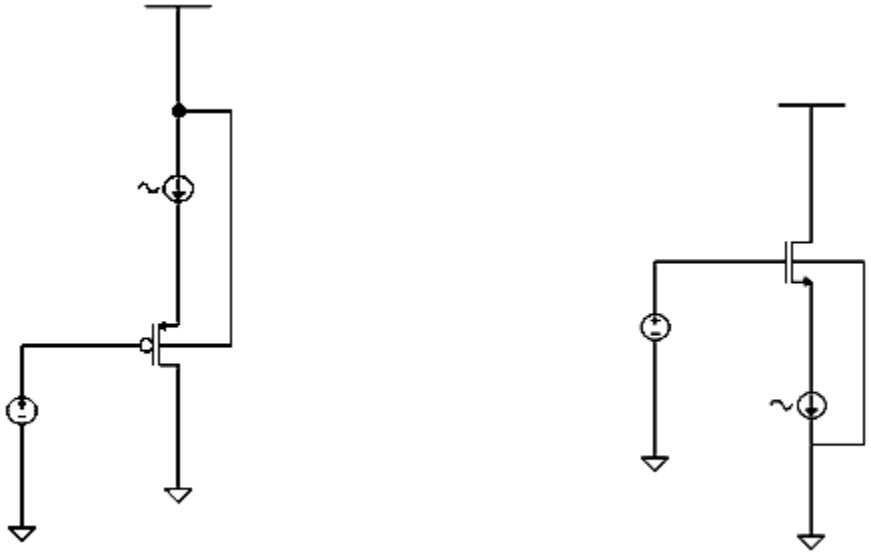


Determination of the Order of the Amplifier

Typically, when a dc gain of close to 80 dB or more is required from a multistage amplifier with simple, nancascode gain stages, people resort to using either 3 stage or 4 stage amplifiers. Any more than that would make the design very complex since there will be so many variables to so deal with. Even for the four stage amplifier, there is a relative difficulty because of the large number of variables required to optimize the design. Previous results from published works on NGCC amplifiers prove that both 3 and 4 stage amplifiers can attain very high dc gain with enough phase margins and good settling time. The 3 stage is likely to consume less power but at the cost of a very strict design to ensure that all the specifications are met, but makes stabilizing the amplifier easier. The 4 – stage although a little more complex, provides a little more freedom, relaxing a bit the design constraints for each stage while still achieving the desired specs. It is more difficult to stabilize the amplifier in this case.

Determination of Slope Factor "n"

To obtain the slope factor, first we need to determine the normalizing current of the ACM model. The circuit used is showing in the figure below.



(a) PMOS **(b) NMOS**

Schematic Setup for the Extraction of Is

The transistors are biased to be in the saturation region. A current with a small delta value is applied to each transistor and the corresponding change in source voltage of the transistors is measured. The normalization current (Is) is then computed as follows.

For NMOS:

$$I_s \cong I * \left(\frac{\frac{\Delta I}{I}}{2\Delta V_s / \phi_t} \right)^2 \qquad \Delta I = 4\mu A$$

$$I = 40\mu A \qquad \phi_t = 25.9mV$$

$$\Delta V = 0.5012 - 0.3529 = 0.01408$$

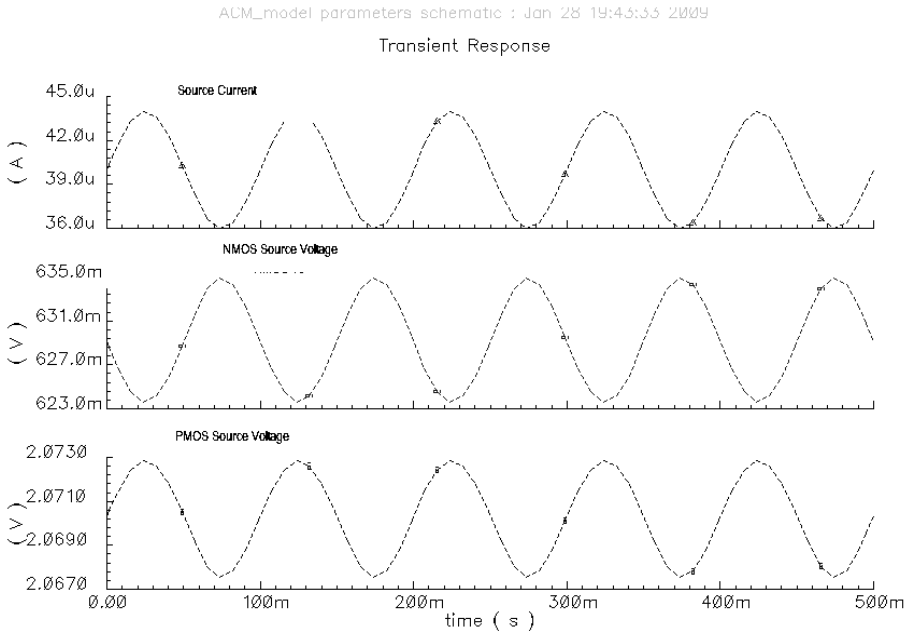
$$I_s = 307.37n$$

For PMOS

$$I = 40\mu A \qquad \phi_t = 25.9mV$$

$$\Delta V = 252m - 230.2m$$

$$I_s = 142.24\ nA$$

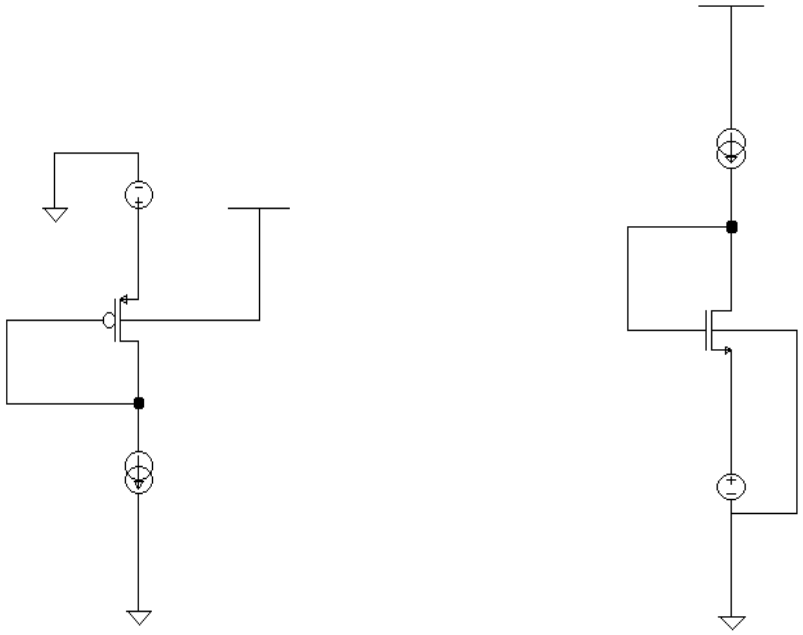


Plot showing delta Vs used for Extraction of Is

Next, the Vp parameter has to also be determined. From the ACM model

$$Vp - Vs = \emptyset t\left(\sqrt{1 + id}\right) - 2 + In\left(\sqrt{1 + id} - 1\right)$$

It is observed that with id = 3, Vp =Vs. Fig 2.4 is the setup for obtaining Vp and Fig 2.5 is the result from the dc sweep of the setup. A current of 3Is is used.

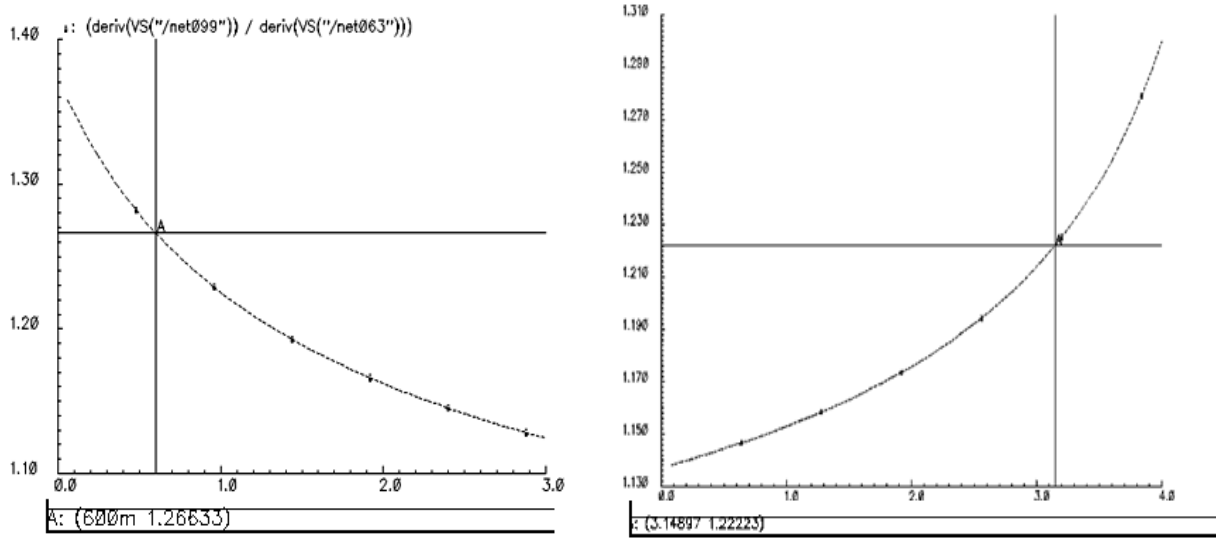


(a) PMOS **(b) NMOS**

Setup used for Obtaining Vp

With this parameter, the value of "n" can now be obtained. By ACM model definition, n is the derivative of Vg with respect to Vp. From the previous simulation, Vp = Vs.

$$n = \left(\frac{dVg}{dVp}\right)$$



Plot of n and V_D for NMOS and PMOS

From the plot the value of n is extracted at Vg = 0 for NMOS and Vg = Vdd = 2 for PMOS be obtained.

Transistor	n
PMOS	1.222
NMOS	1.266

General Design Procedure

A new variable which depends on the relative location of the poles of the system to each other will be used throughout the design. The general procedure for designing a 4^{th} order system is used here. The 3 stage is obtained by assuming f4 is at infinity. These are the 'f' variables. An N-stage NGCC has N 'f' variables, as such the following 4 are used henceforth, f1, f2, f3 and f4.

The transfer function for the 4 stage NGCC can be represented by the following equation

$$H(s) = \frac{A_o}{(1 + \frac{A_o}{f1})(1 + \frac{s}{f2} + \frac{s^2}{f2f3} + \frac{s^3}{f2f3f4})}$$

where A_o is the dc gain and $f1, f2, f3$ and $f4$ are the cut off frequencies of each stage

The stability criteria for this circuit can be fixed by using Routh-Hurwitz stability criterion on the unity-feedback transfer function which is given by the below equation

$$HCL(s) = \frac{1}{\frac{s}{f1} + \frac{s^2}{f1f2} + \frac{s^3}{f1f2f3} + \frac{s^4}{f1f2f3f4}}$$

We obtain the following conditions for stability

$$f4 > f2$$

$$f4 > \frac{f2}{1 - \frac{f1}{f3}}$$

Also phase margin can be approximated by the following equation if f3>f2 and f4>f2

$Ø_M = 90 - \arctan(GB/f2)$

- The cutoff of the first stage,f1 is set equal to the required GBW and f2 is obtained from the approximate expression of the phase margin.

$$\boldsymbol{f1 = GBW \cong 30MHz}$$

$$\emptyset m = 90^{\circ} - \tan^{-1}\left(\frac{GBW}{f2}\right) = 70^{\circ},\ \ GBW = 30MHz,$$

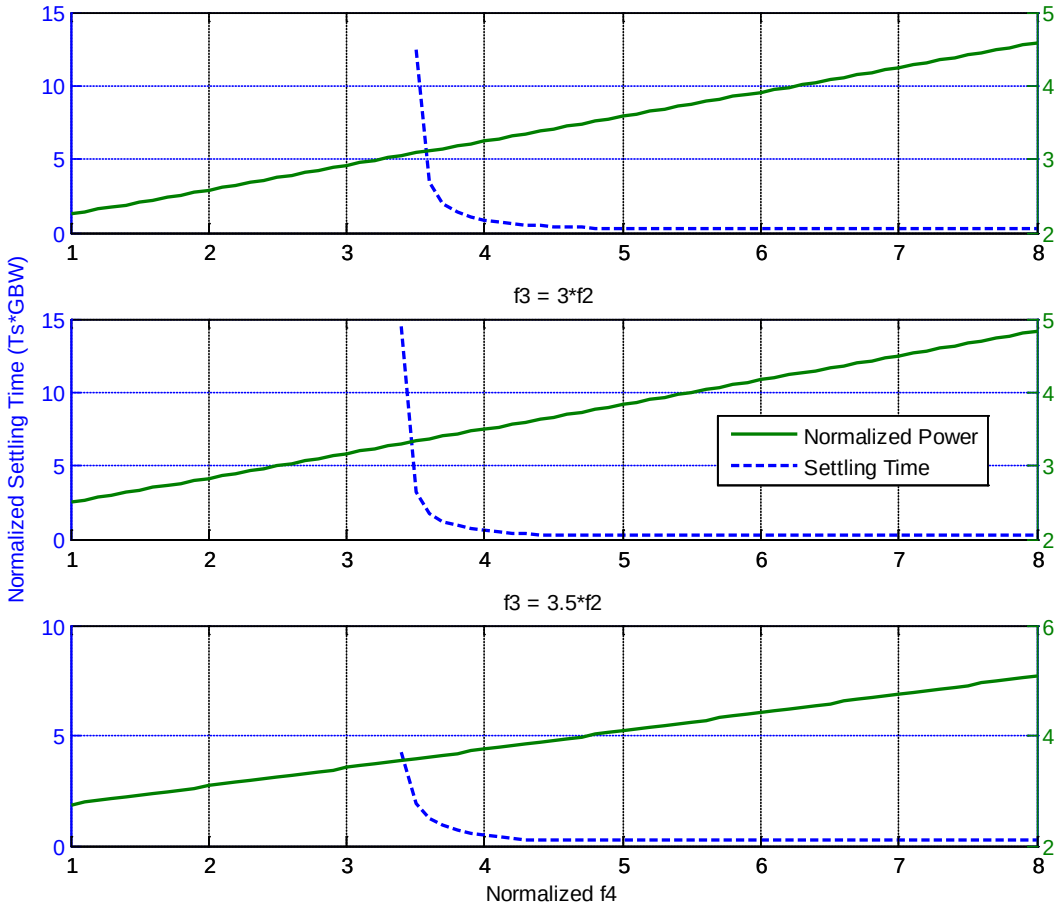
$$therefore, \qquad \boldsymbol{f2 \cong 3GBW = 90\ MHz}$$

- f3 and f4 are determined from the settling time and power requirement of the amplifier. A sweep of f3 and f4 can be done versus normalized power and settling power and the values of f3 and f4 that produces the minimum power and settling time and also meet the condition for phase margin >70deg is chosen. Using the full expression for the phase margin of the system, a numerical analysis can be performed to find optimum values of f3 and f4 such that settling time is minimized while the phase margin is not degraded. This can be performed using MATLAB. The code used is shown in Appendix A.
- To do that we need to choose values for the miller capacitors that we will use in the compensation. We require the ratios between the miller caps and the load cap to determine the normalized power for the MATLAB plots. For this design we use a miller caps of 2.5pF.

The phase margin is computed from the expression below:

$$\boldsymbol{\emptyset m = 90^{\circ} - \tan^{-1}\left[\frac{GBW}{f2}\left(\frac{1 - GBW^2/f3.f4}{1 - GBW^2/f3.f4}\right)\right]}$$

Settling time is obtained using the general transfer function of a 4th order NGCC, connecting it in unity feedback and taking the step response. The details are shown in the MATLAB code in the appendix. Fig 1.2 shows the results obtained.



From the plots, it is seen that when f3 = 2.5f1, which is the first plot above, the settling time and power can be optimized. The power and settling time in the other two cases are quite higher compared to the case when f3 =2.5f1. At that point the f4 is given by 3.5f1 and so we proceed with the design with these parameters

Next we can determine the transconductance of each stage from the following equation:

$$fi = \frac{gmi}{2\pi Cmi} \qquad \ldots\ldots\ldots\ldots 1$$

$$\boldsymbol{f1 = 30MHz,\ \ f2 = 90MHz,\ \ \ f3 = 225MH\ and\ f4 = 315MHz}$$

Substituting these values into eqn 1 *gives the following gms.*

$we\ choose\ Cm1 = Cm2 = Cm3 = 2.5\text{pF}$

$$\boldsymbol{gm1 = 471\mu S \quad gm2 = 1.41mS \ gm3 = 3.5mS \quad gm4 = 4.9mS}$$

- The ACM model for the transistor is defined by the following equations.

1. $Id = gm * n * \emptyset_t \dfrac{1+\sqrt{1+id}}{2}$
2. $W/_L = \dfrac{gm}{\mu C_{OX} \emptyset_t}\left(\dfrac{1}{\sqrt{1+id}-1}\right)$
3. $f_T = \dfrac{\mu \emptyset_t}{2\pi L^2}\left(2\sqrt{1+id}-1\right)$

For this design, we choose an appropriate Vdsat for each stage and compute the corresponding inversion level, then we can compute the respective W/L for each transistor.

Using this value and the gm_i computed above, the aspect ratios of the transistors all the transistors can be obtained from the equation 2 above.

$$W/_L = \frac{gm}{\mu C_{OX} \emptyset_t}\left(\frac{1}{\sqrt{1+id}-1}\right)$$

4th Stage – nmos input

$$\boldsymbol{\left(W/_L\right)4n = 91}$$

Hence,

$$\boldsymbol{\left(W/_L\right)4p = \left(W/_L\right)4n * 1/3 = 30}$$

3rd Stage – nmos input

$$\boldsymbol{\left(W/_L\right)3n = 79}$$

Hence,

$$\left(\frac{W}{L}\right)3p = \left(\frac{W}{L}\right)3n * 3 = 237$$

2nd stage nmos input

$$\left(\frac{W}{L}\right)2n = 23$$

Hence,

$$\left(\frac{W}{L}\right)2p = \left(\frac{W}{L}\right)2n * 3 = 69$$

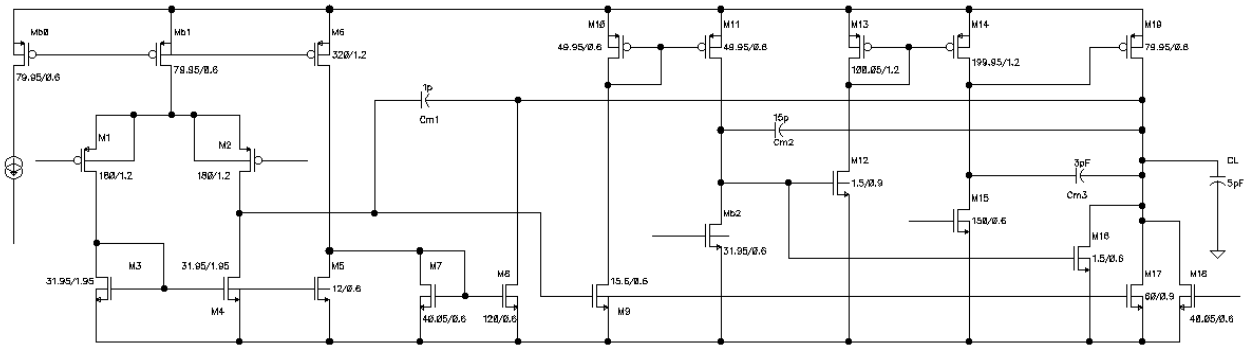
1st Stage – pmos input

$$\left(\frac{W}{L}\right)1p = 124$$

Hence,

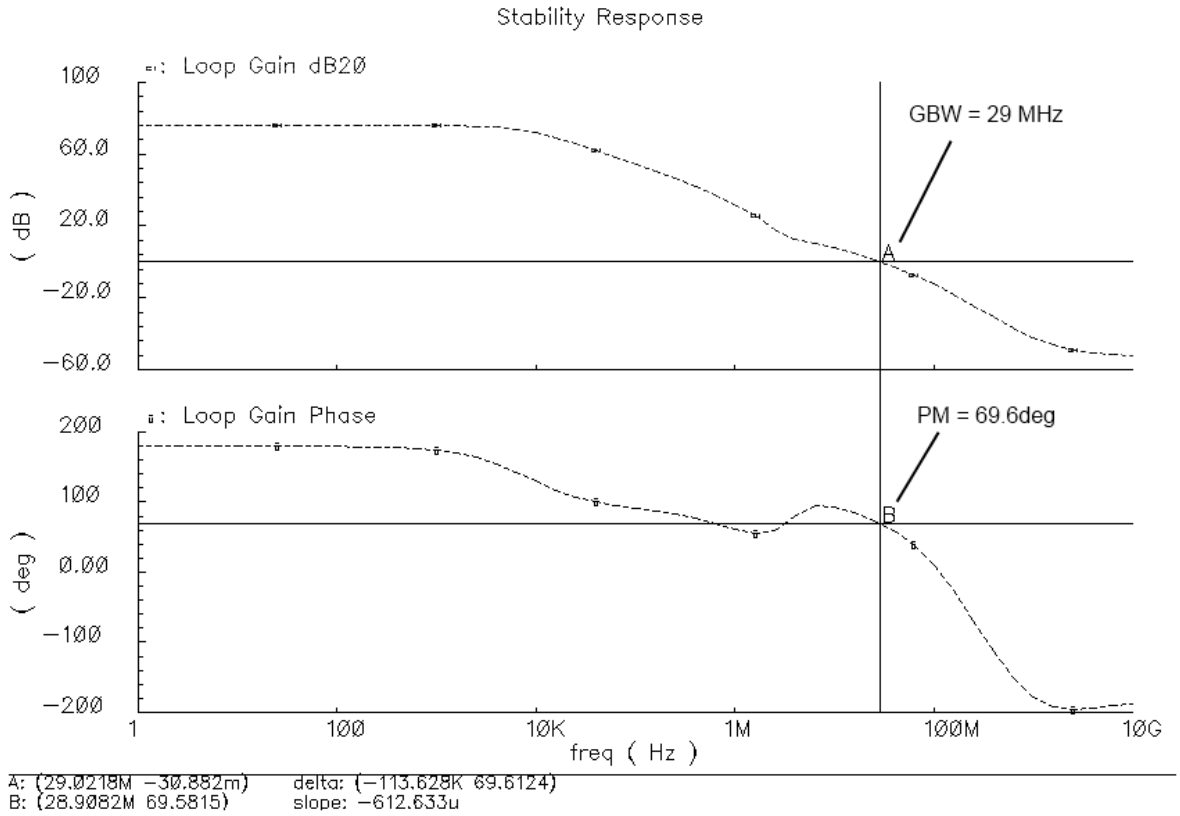
$$\left(\frac{W}{L}\right)1n = \left(\frac{W}{L}\right)1p * 1/3 = 42$$

These computed values are used for the first set of simulations of the amplifier, and are adjusted as necessary to meet the required specifications.

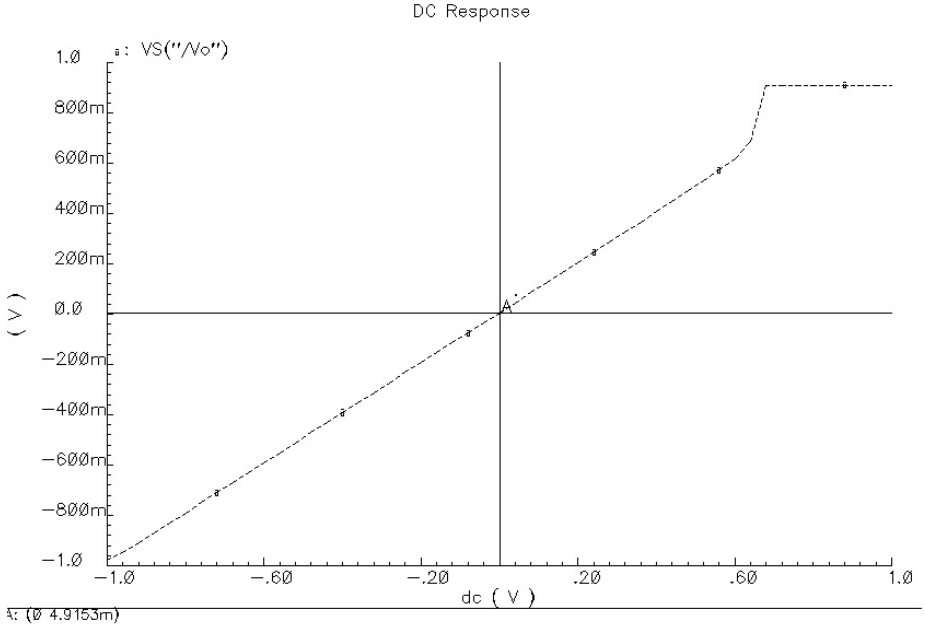


Schematic for the Four -Stage NGCC

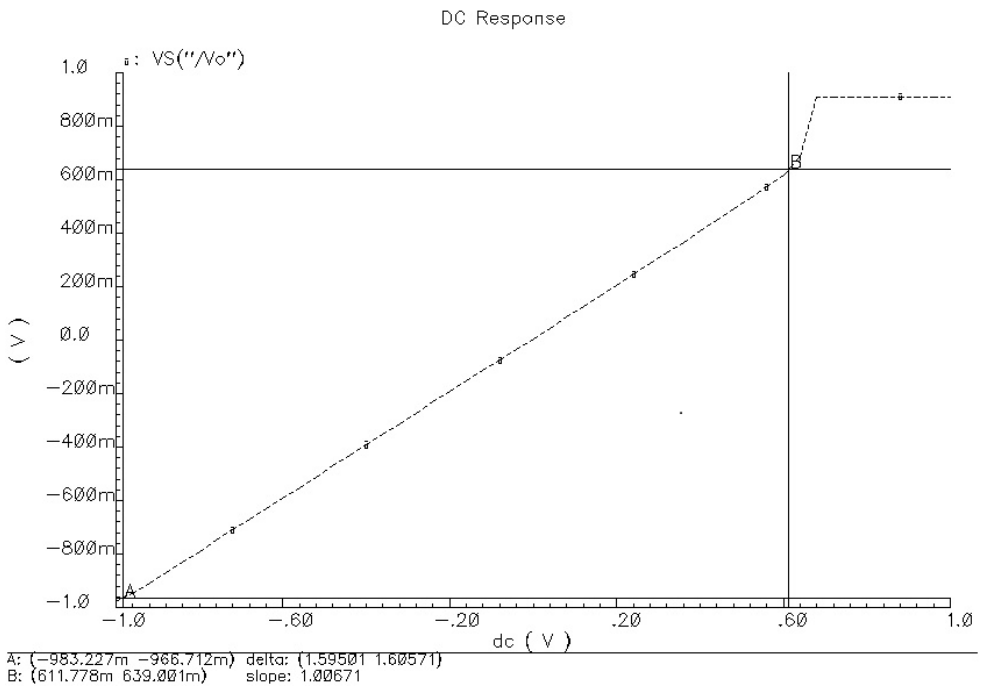
RESULTS



Magnitude and Phase Response, Gain = 76dB

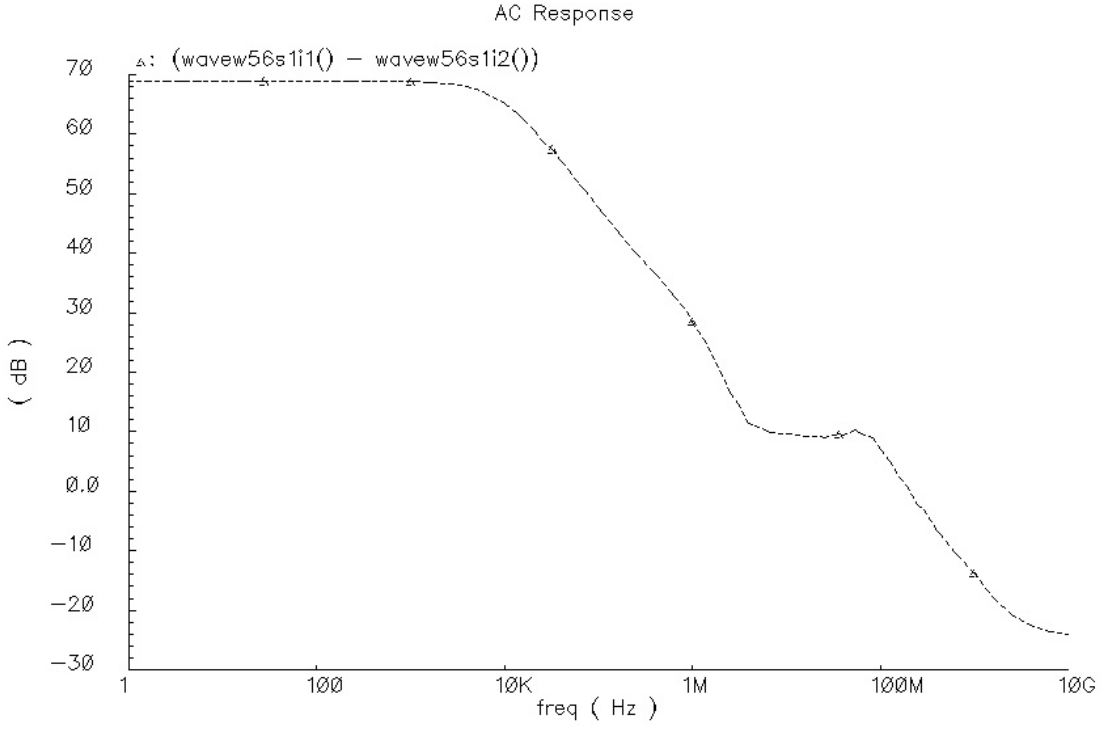


DC Response showing offset, Input referred offset = 4.9mV

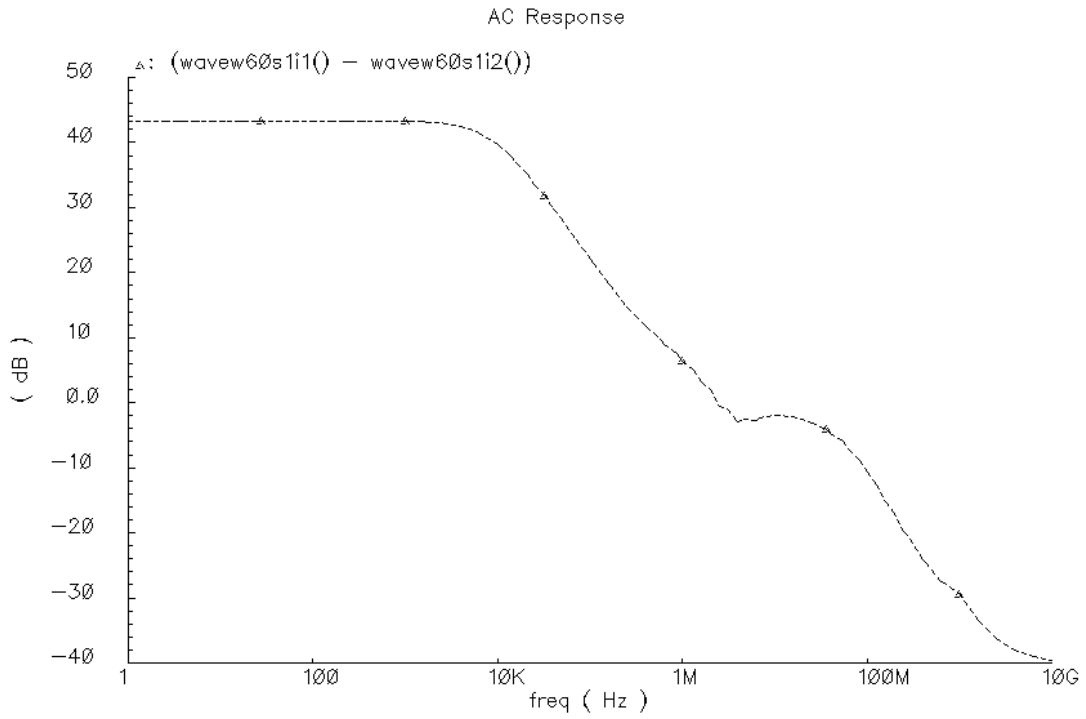


DC Response showing the Output swing and the Common mode Range

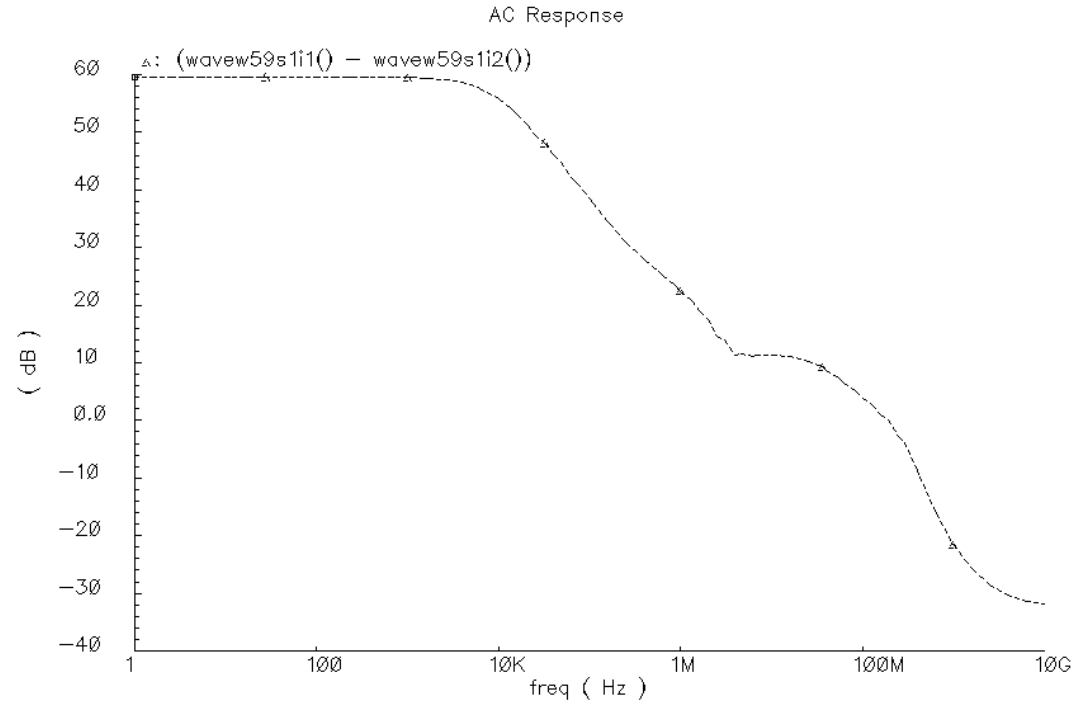
Output Swing = 1.61V and CMR = 1.6V



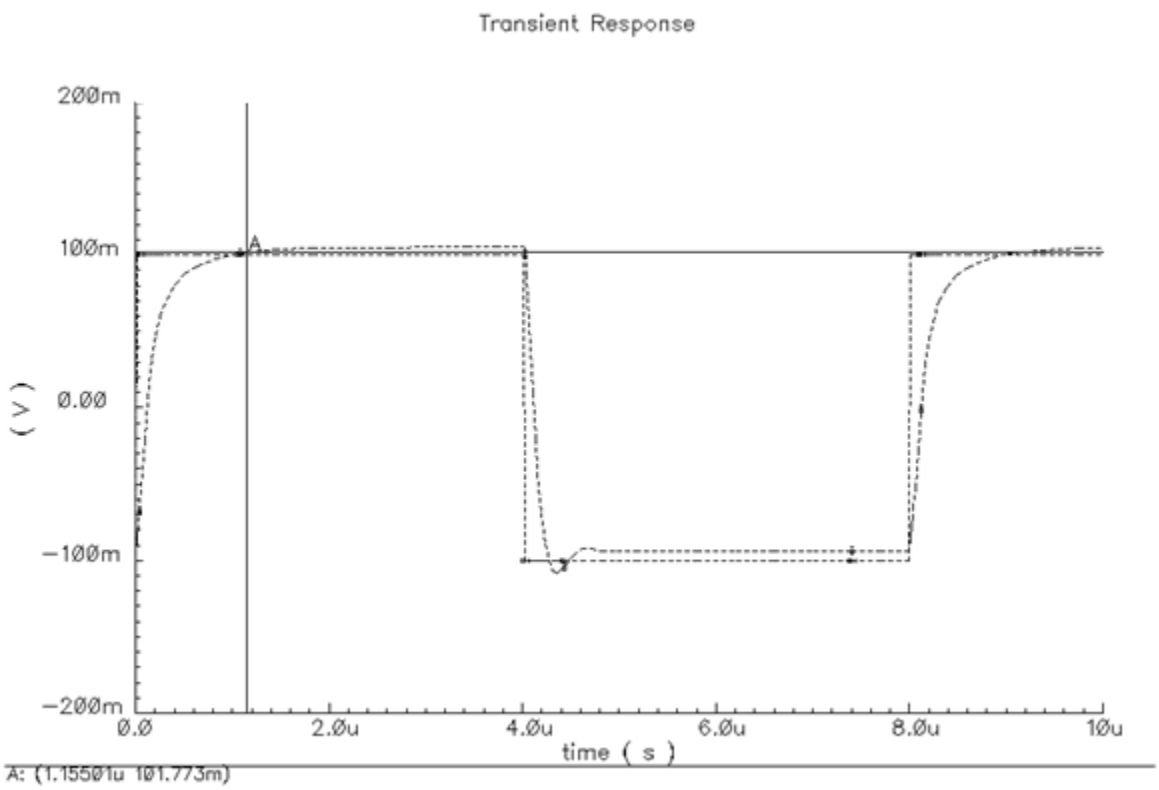
CMRR versus frequency, CMRR @dc = 68dB



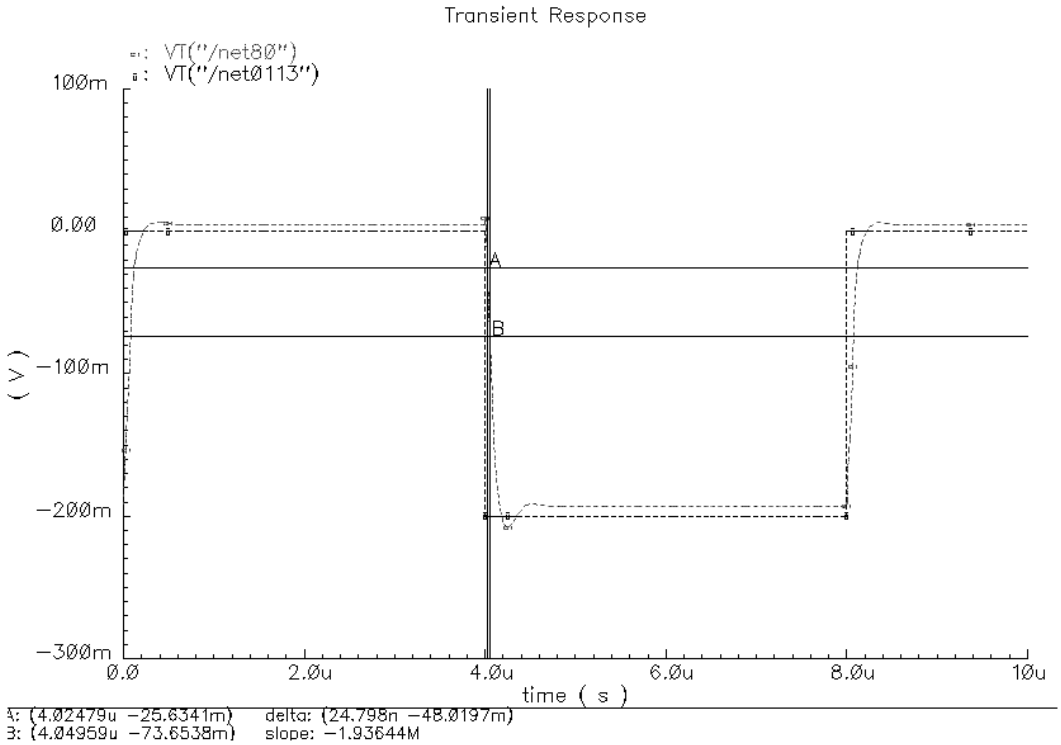
PSRR– versus frequency, PSRR @ dc = 44.3dB



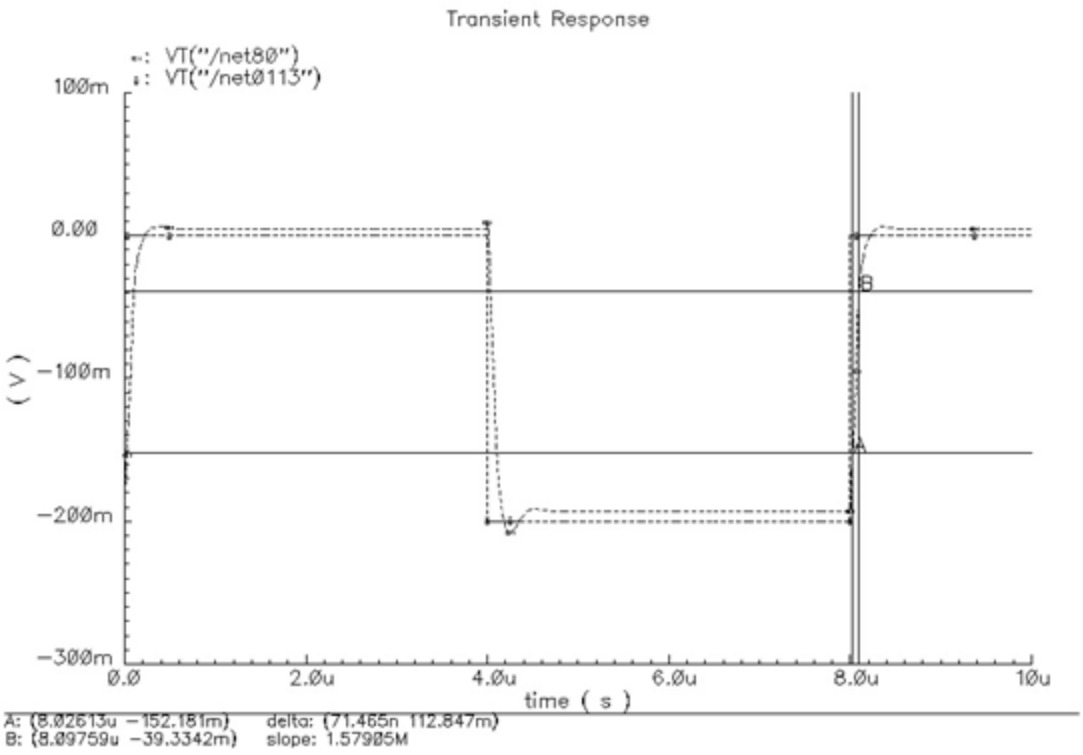
PSRR+ versus frequency, PSRR @ dc = 60dB



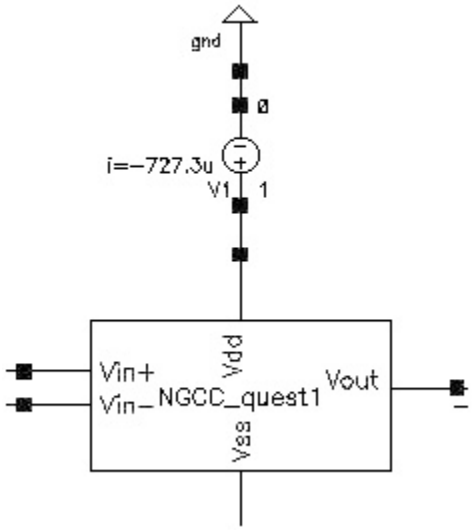
Transient response showing the settling time, Settling time = 1.155us



Negative Slew Rate, SR+ = 1.94V/us



Positive Slew Rate, SR+ = 1.58V/us

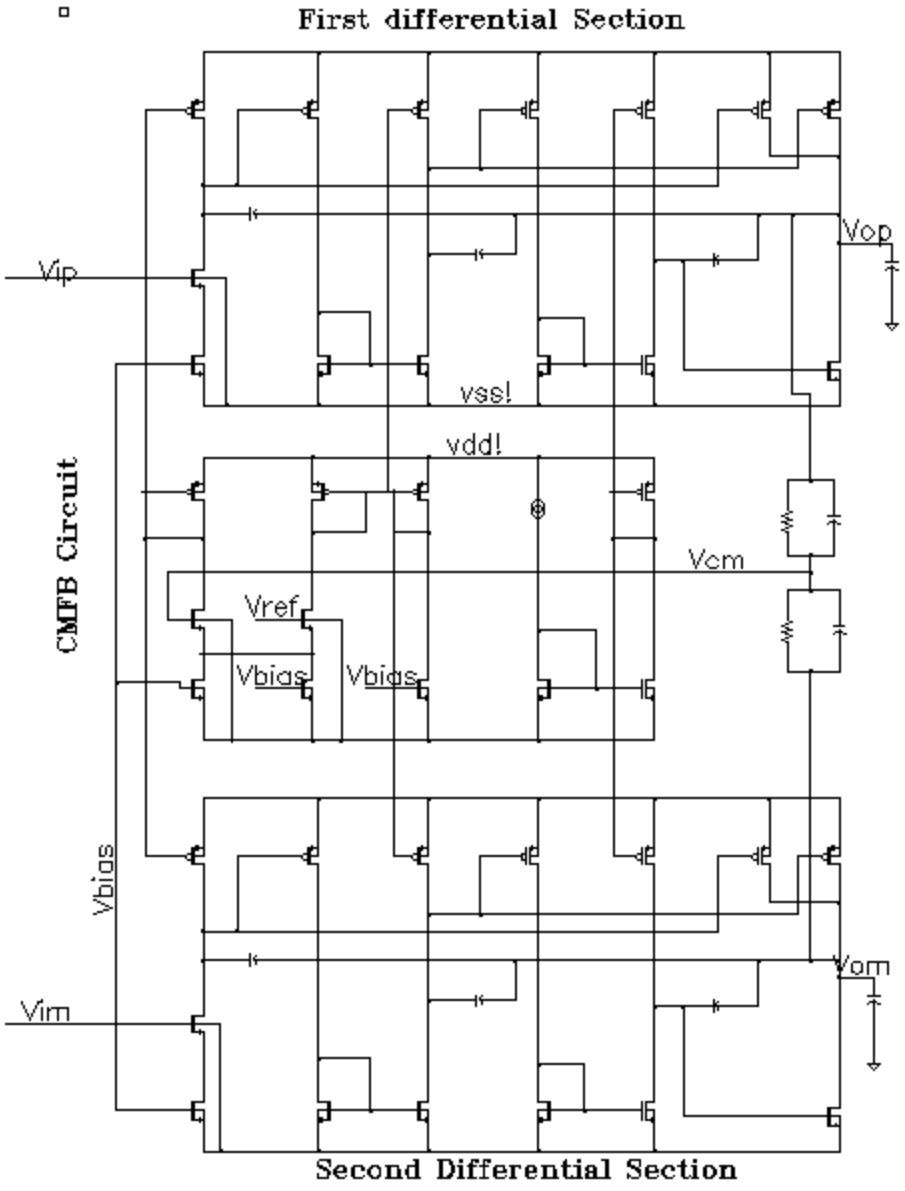


Current consumption in the design

Fully Differential Version

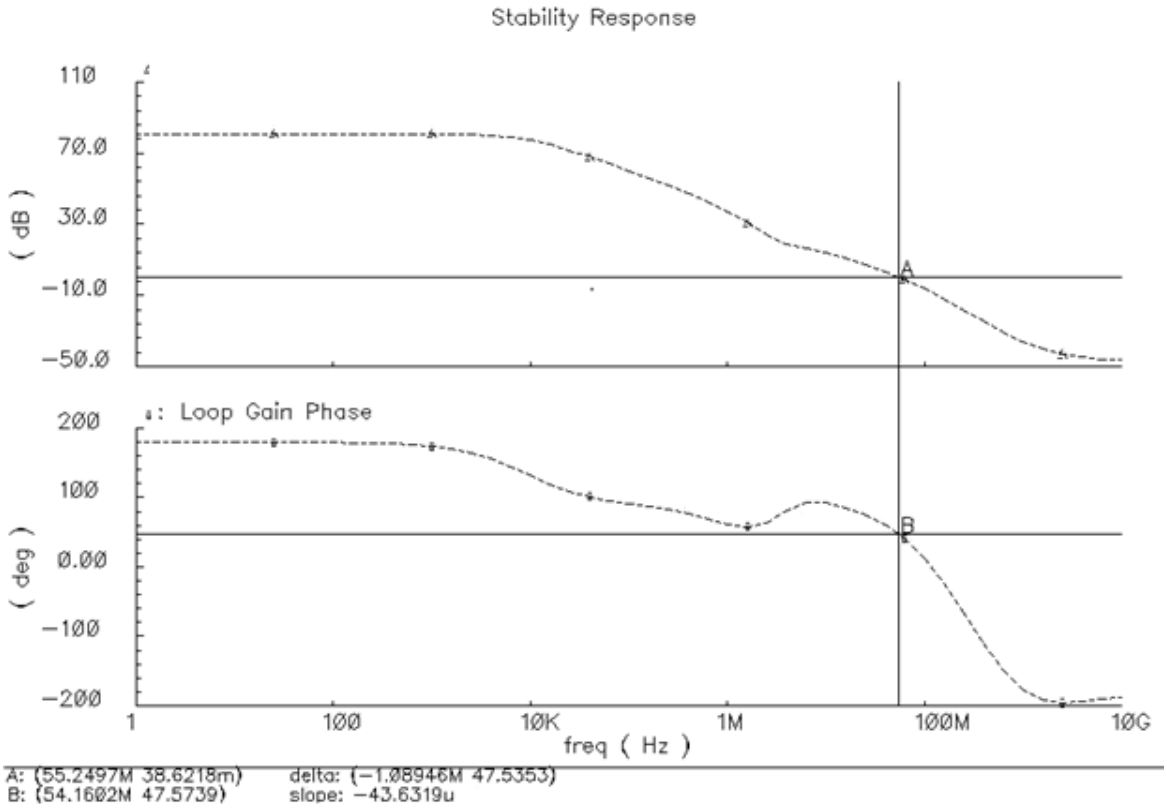
We implement two of the NGCC stages above together with a common mode feedback circuit to obtain the fully differential version of the four stage NGCC.

Schematic of the Fully Differential Block

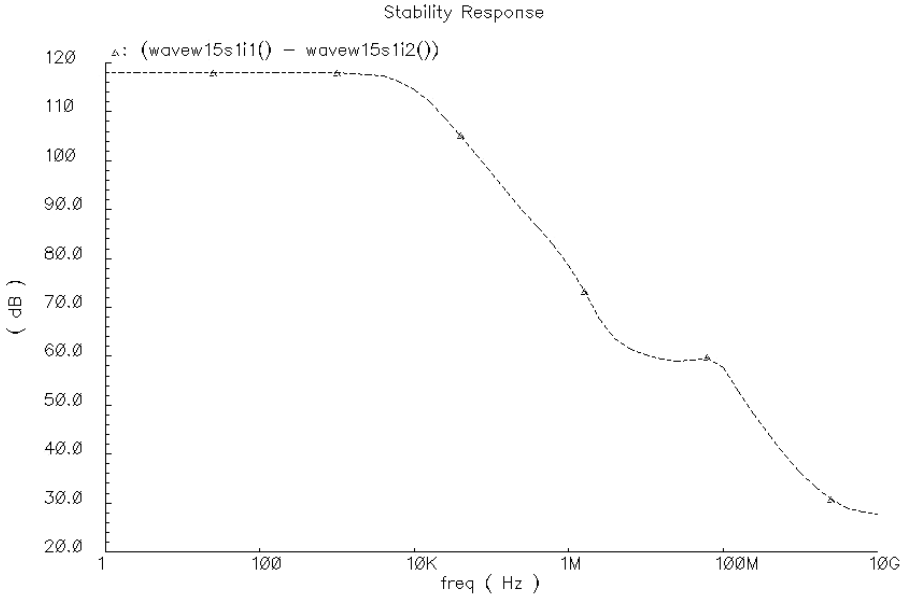


Implementation of the Fully Differential Four Stage NGCC Opamp

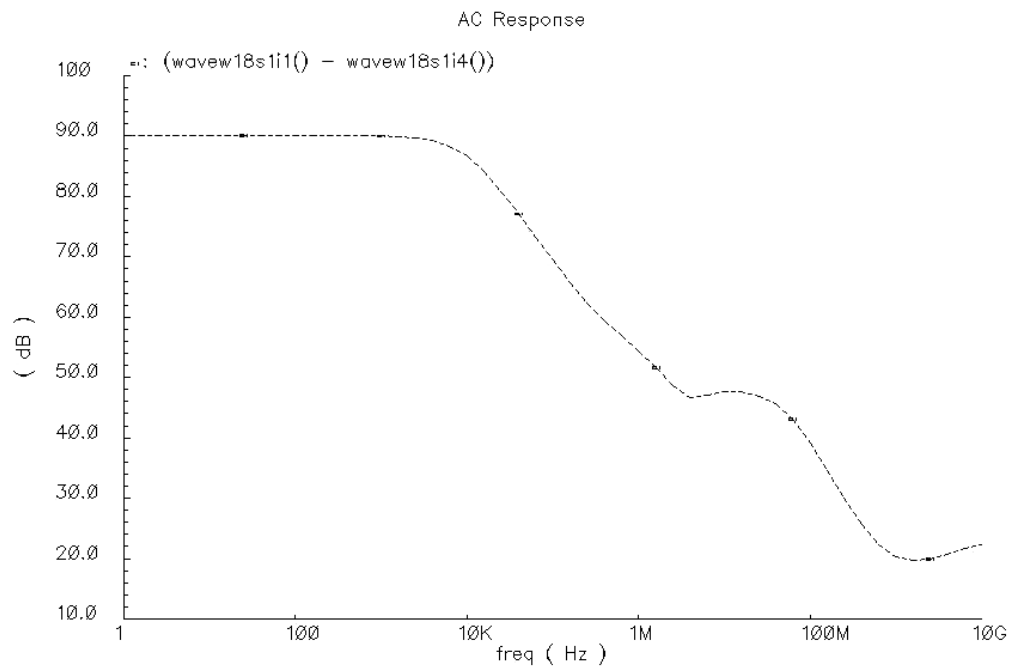
Results



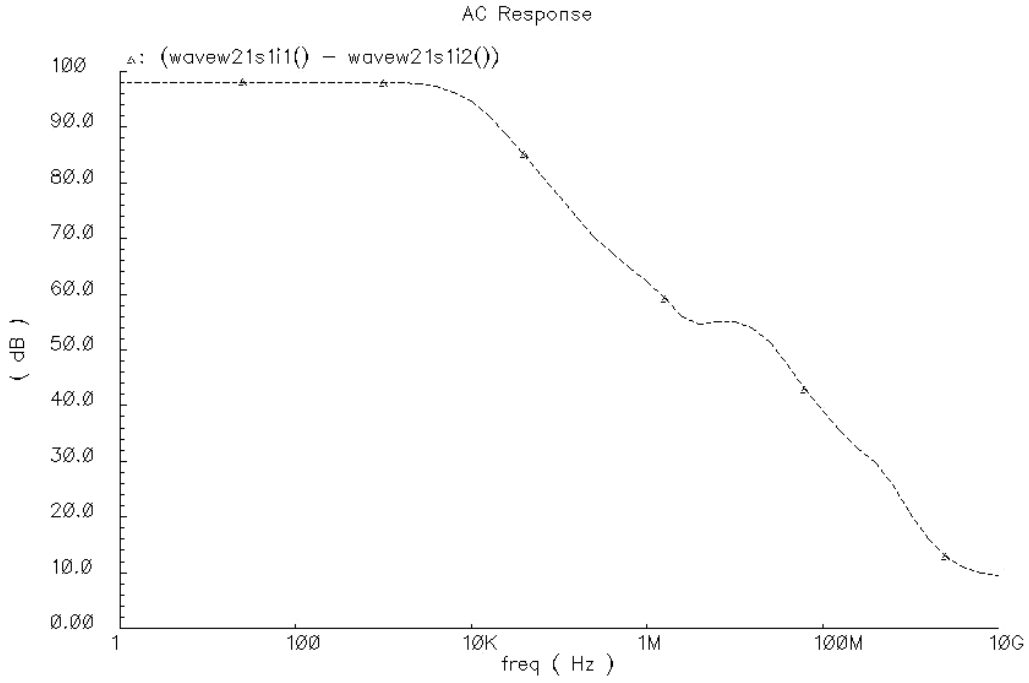
Magnitude and Phase Response, Gain = 80.9dB GBW = 55MHz PM = 47deg



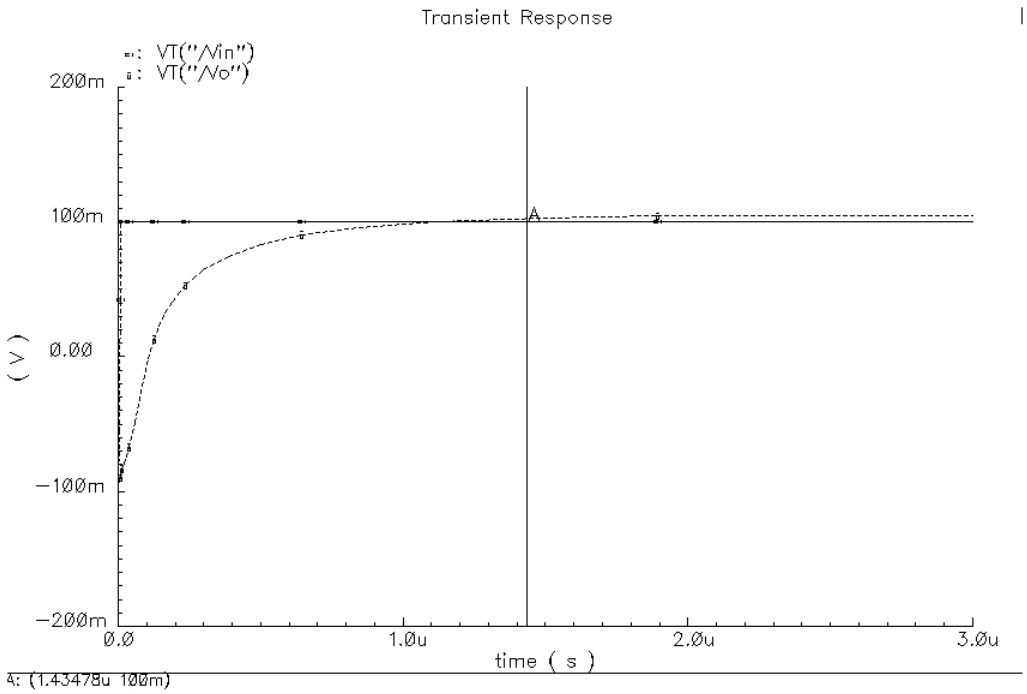
CMRR versus frequency, CMRR@dc = 117.2dB



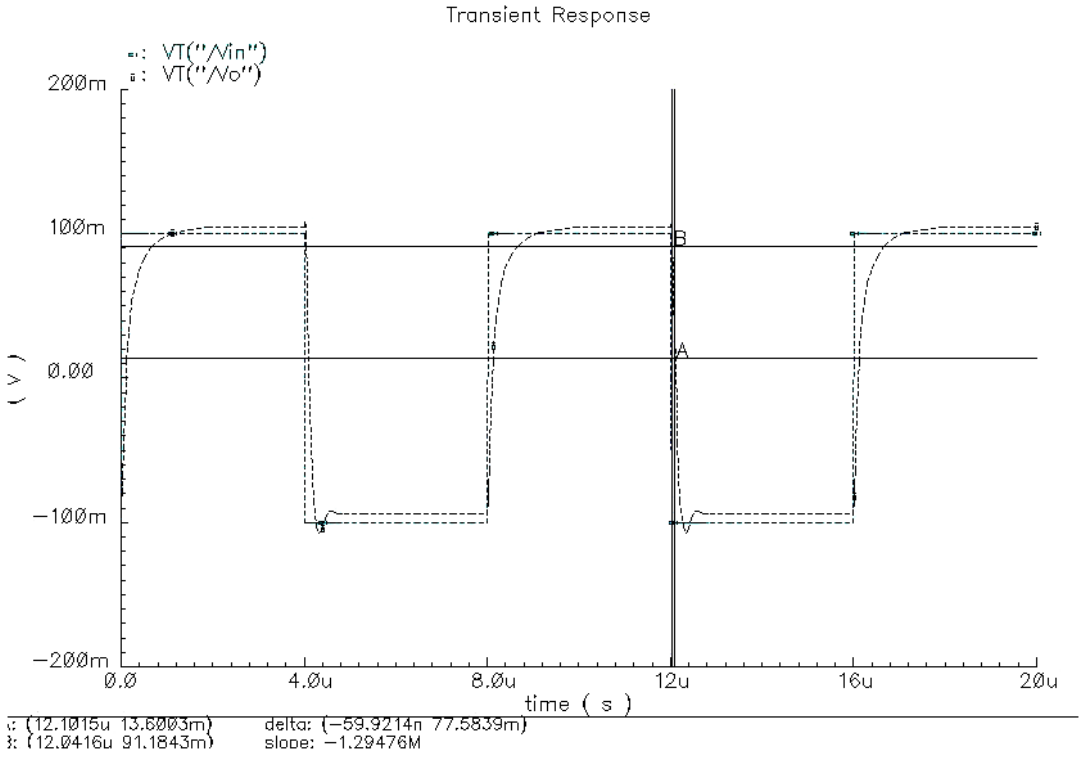
PSRR- versus frequency, PSRR-@dc = 89dB



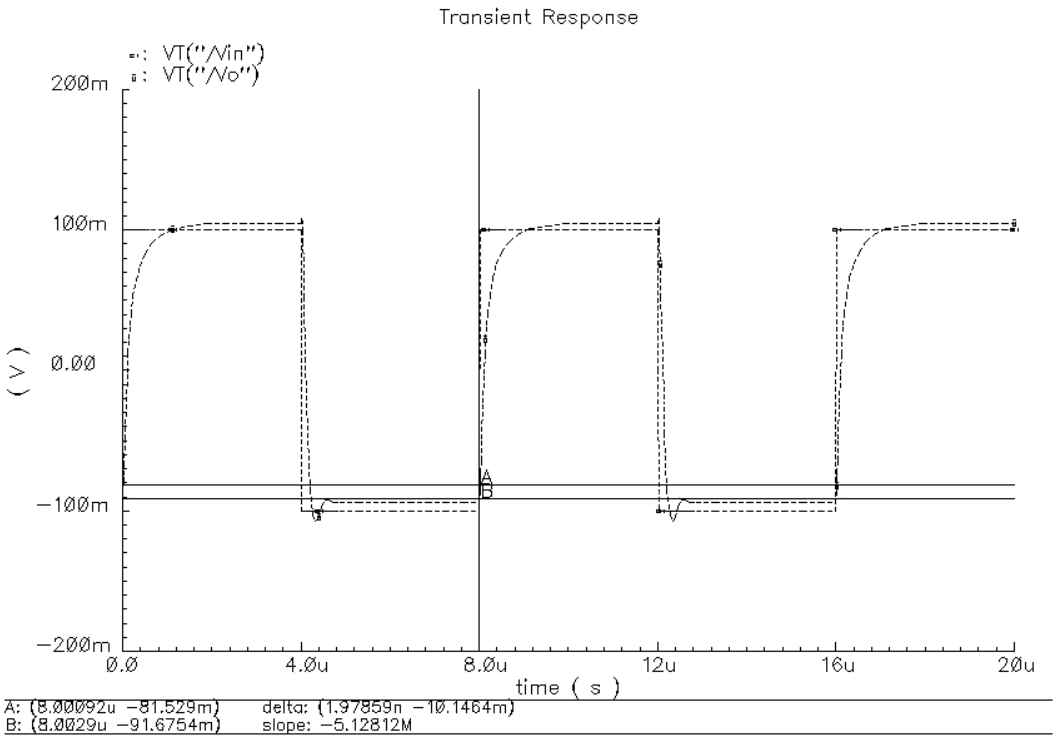
PSRR+ versus frequency, PSRR+@dc = 97dB



Transient Response, Settling time = 1.43u



Negative Slew Rate = -1.3V/us



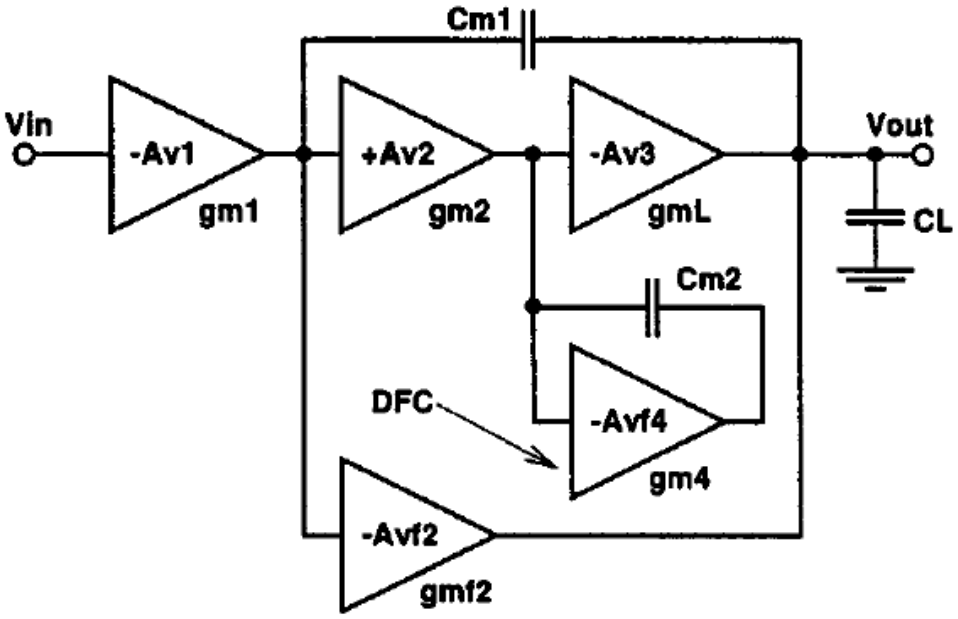
Positive Slew Rate = 5.12V/us

Specification	Required	Single output version	Fully Differential
Power Supply	**2V**	**2V**	**2V**
Load	**5pF**	**5pF**	**5pF**
GBW	**29MhZ**	**29MHz**	**55MHz**
DC Gain	**75dB**	**76dB**	**80.9dB**
Phase Margin	**70deg**	**69.6deg**	**47deg**
Settling time	**minimum**	**1.155us**	**1.43us**
Power Consumption	**minimum**	**1.38mW**	**2.59mW**
Slew Rate (+/-)	**10V/us**	**-1.5/1.94 V/us**	**-1.3/5.12 V/us**
CMRR @DC	**-**	**68dB**	**117.2dB**
PSRR(+/-)@DC	**-**	**60/44.3 dB**	**97/89 dB**

COMMENTS

From the results shown in the table above, it is observed that with the implementation of the fully differential version of the opamp, we boosted the GBW of the opamp and as well the DC gain shot up by about 6dB which is consistent with theoretical deductions. However, the phase margin is very bad for the fully differential version resulting in a longer settling time. It is also clear from the table how CMRR and PSRR are generally far better for the differential opamp than for the single ended. The fully differential is ideally balanced inherently so rejects all common mode inputs. But the cost of that is about a double pay in power consumption.

PROBLEM 2: DESIGN OF DAMPING FACTOR CONTROLLED FREQUENCY COMPENSATION AMPLIFIER (DFCFC1)



Topology of DFCFC1 Amplifier

General Design Procedure

The circuit has three gain stages with an extra two feed forward paths. The transconductances of each stage are obtained as follows. DFCFC1 is defined by the following main conditions

1. $\boldsymbol{gmf2 = gm3}$

2. $\boldsymbol{Cm1 = \left({}^{4}/_{\beta}\right).\left({}^{gm1}/_{gm3}\right)}$

3. $\boldsymbol{CL\ Cm1 \geq Cm2 > Cp}$

4. $\boldsymbol{gm4 = \beta.\left(\frac{Cp}{CL}\right).gm3}$

5. $\boldsymbol{\beta = \sqrt{1 + 2(CL/Cp).(gm2/gm2)}}$

- $GBW = \left(\boldsymbol{\beta}/_{4}\right).\left(gm3/_{CL}\right) = gm1/_{C1} \approx 29MHz \qquad Let\ Cm1 = 5pF,$

  $then\ \boldsymbol{gm1 = 900\mu S}$ &

  $\boldsymbol{\beta . gm3 = 0.0036} \qquad \ldots\ldots\ldots \mathbf{1}$

- $\boldsymbol{\beta}$ is a constant that depends on the capacitive load and the output parasitic capacitance. Assuming parasitic capacitance, Cp = 100fF, then

  $\boldsymbol{\beta = \sqrt{1 + 2(CL/Cp).(gm2/gm2)}} \qquad \boldsymbol{CL = 5pF,} \qquad \boldsymbol{Cp = 100fF}$

  $Setting\ gm1 = gm2\ and\ simplifying\ further\ gives$

  $$\boldsymbol{\beta^2 = 1 + \frac{0.2}{gm3}} \qquad \ldots\ldots\ldots\ldots \mathbf{2}$$

- Equations 1 & 2 are solved simultaneously to give

  $\boldsymbol{gm3 = 65\mu S} \qquad\qquad \boldsymbol{\beta = 55}$

- $gm4\ is\ also\ obtained\ from\ the\ follwing\ expression$

  $$\boldsymbol{gm4 = k.\left(\frac{Cp}{CL}\right).gm3,} \quad \boldsymbol{gm3 = 65\mu S} \quad \boldsymbol{Cp = 100fF} \quad \boldsymbol{CL = 5pF}$$

  $thefore \quad \boldsymbol{gm4 = 71.5\mu S}$

For this design, we choose an appropriate Vdsat for each stage and compute the corresponding inversion level, then we can compute the respective W/L for each transistor.

For the various stages and the gms associated with them, we can obtain the W/L for each transistor.

For the 3rd Stage – nmos input

$$\left(W/L\right)3n = 38$$

Hence,

$$\left(W/L\right)3p = \left(W/L\right)3n * 3 = 114$$

2nd stage nmos input

$$\left(W/L\right)2n = 30$$

Hence,

$$\left(W/L\right)2p = \left(W/L\right)2n * 3 = 90$$

1st Stage – pmos input

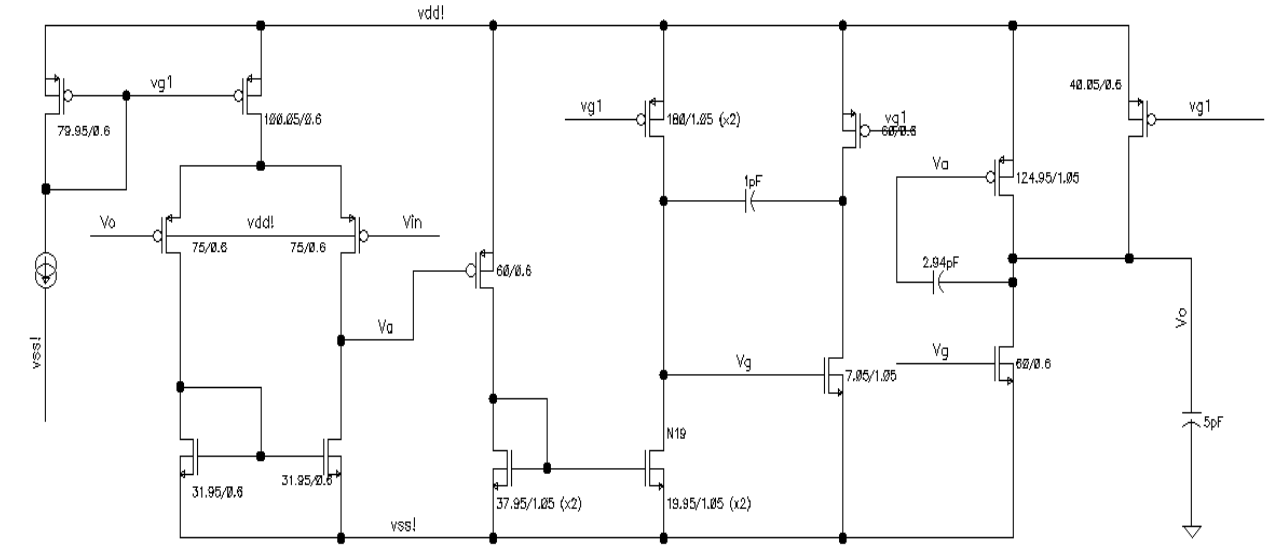
$$\left(W/L\right)1p = 109$$

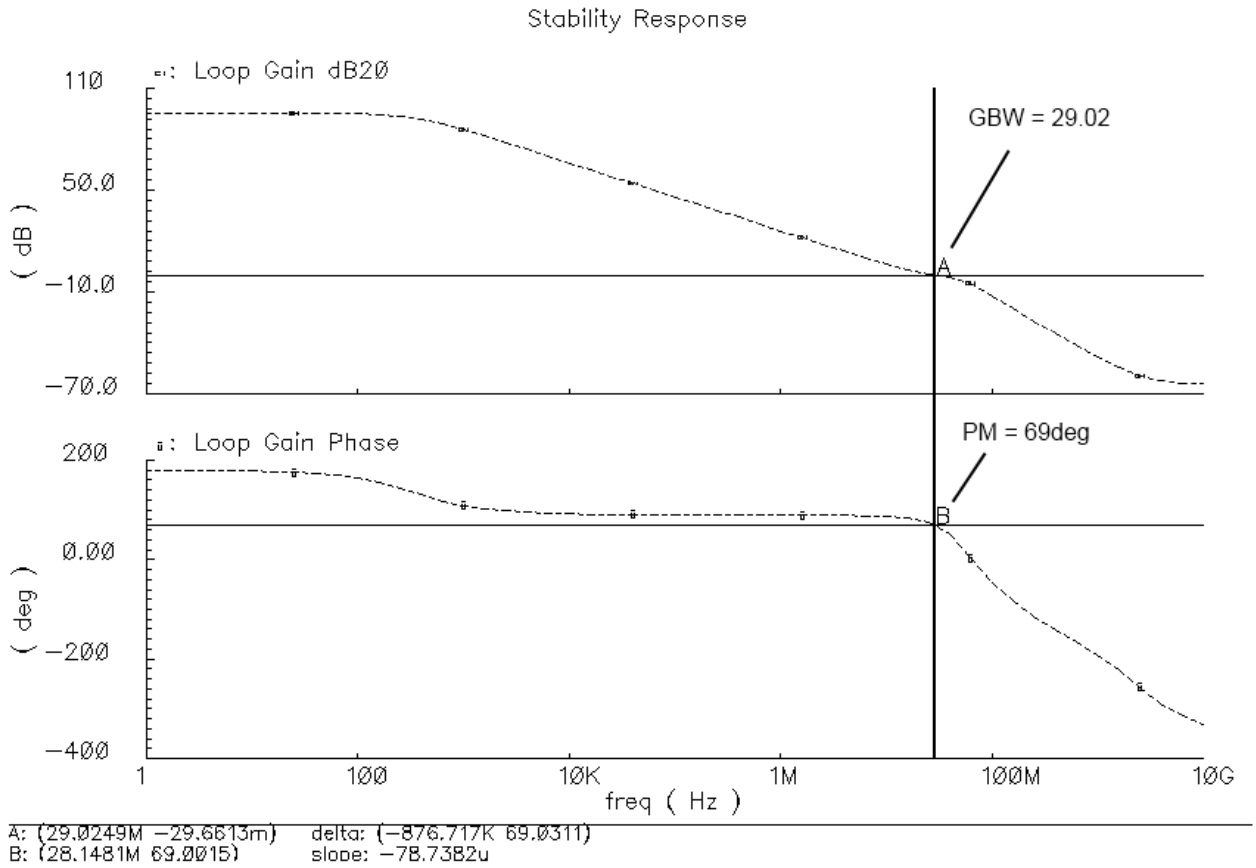
Hence,

$$\left(W/L\right)1n = \left(W/L\right)1p * \frac{1}{3} = 36$$

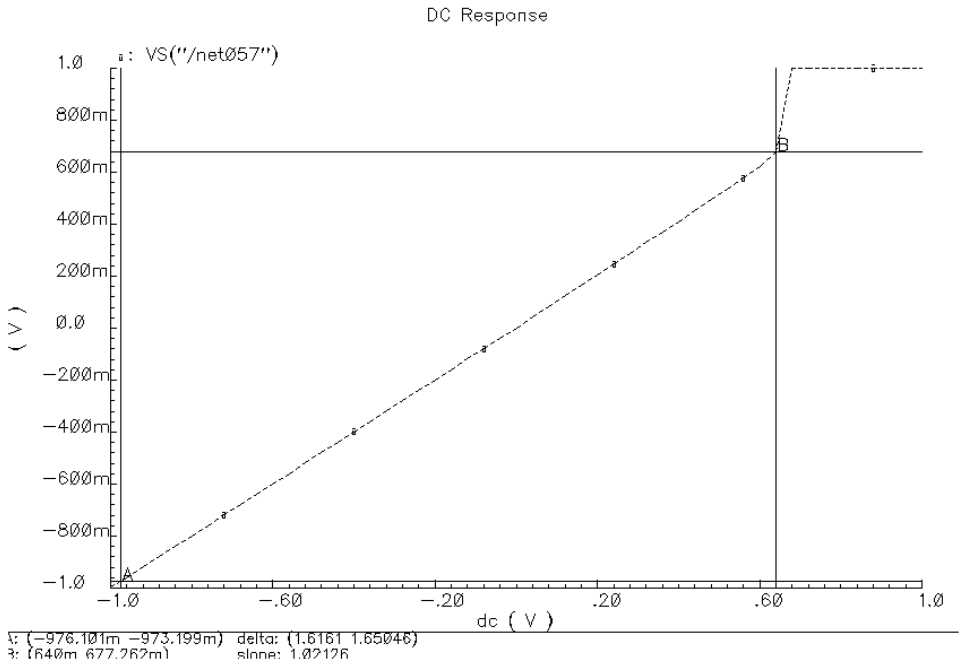
The design was done based on these aspect ratios obtained but a little fine tuning was done to meet the required specifications

Schematic of the DFCFC Opamp

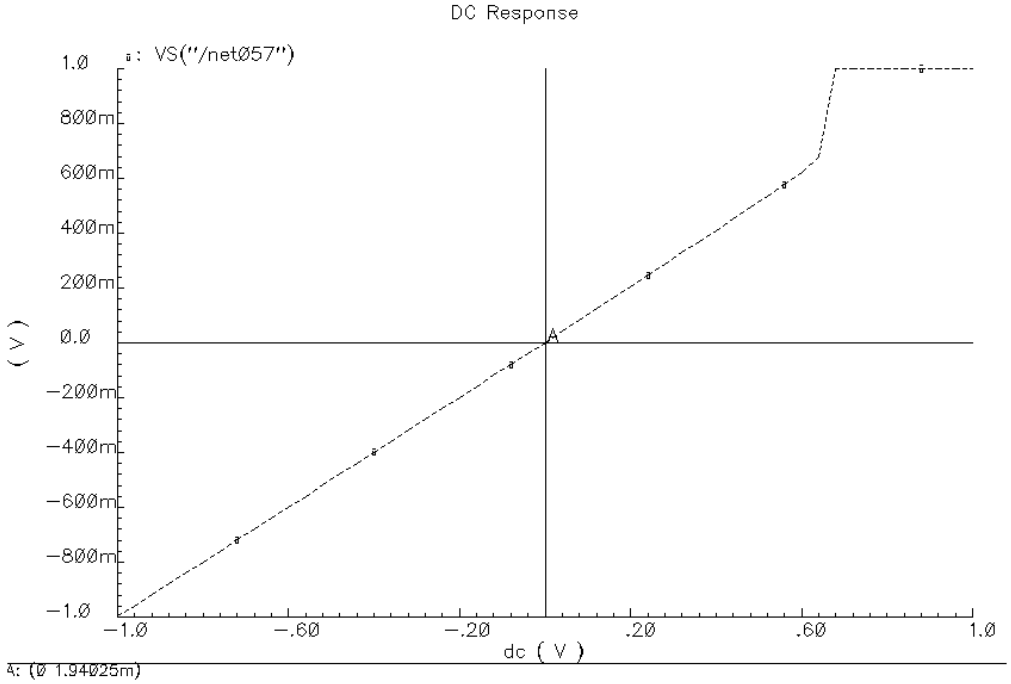




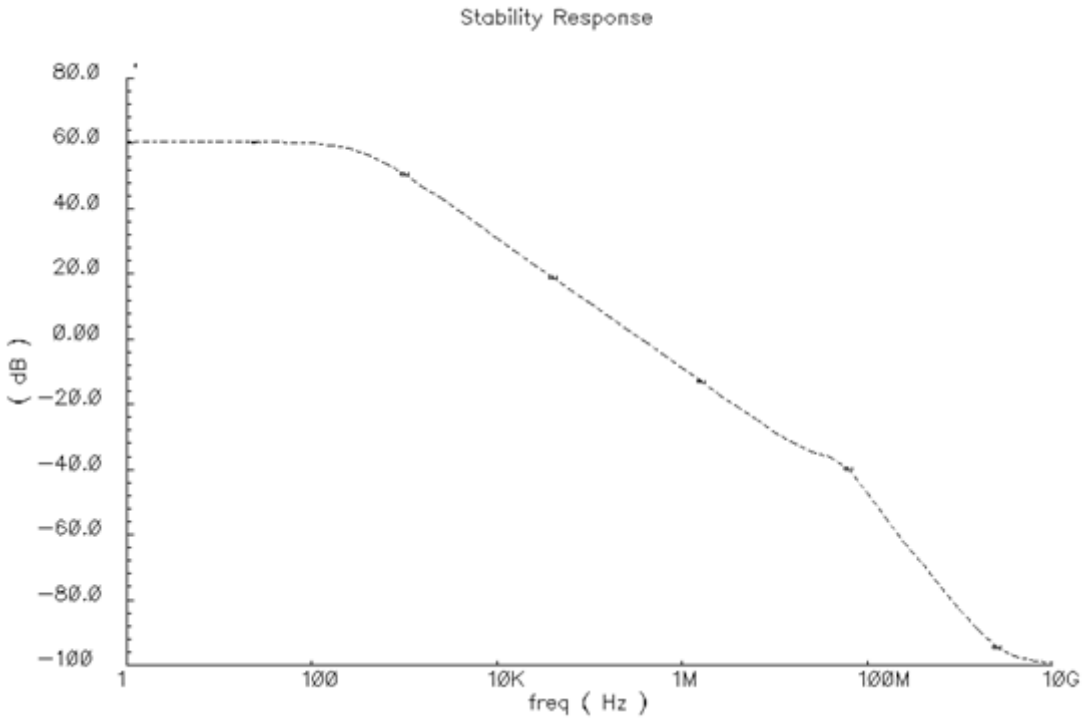
Magnitude and Phase Response, Gain = 101.3dB



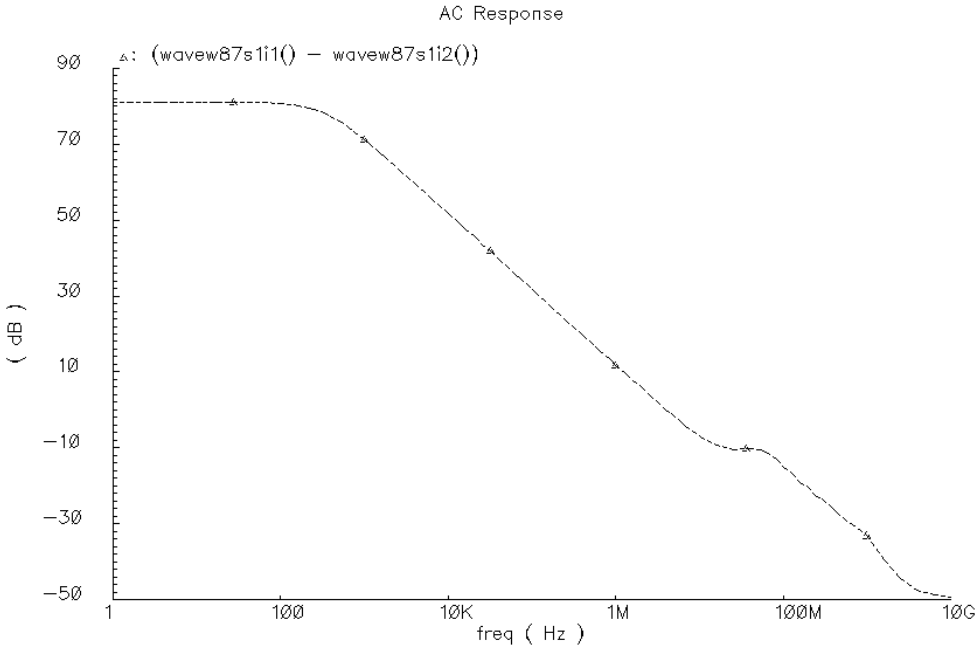
DC Response: Output swing = 1.65V, ICMR = 1.61V



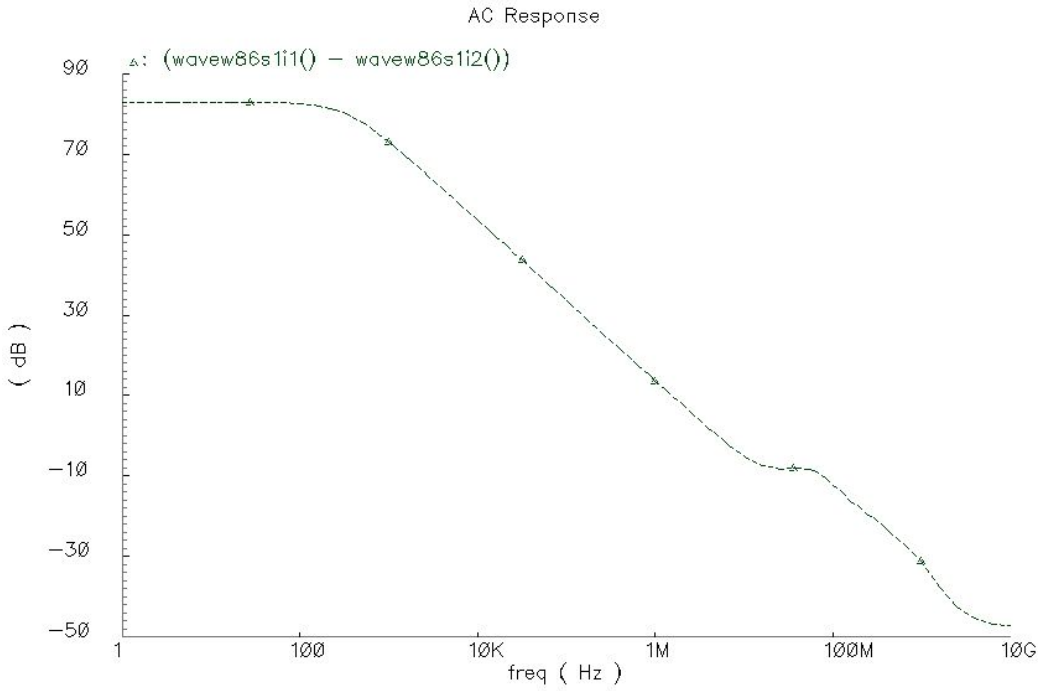
DC Response, Input referred offset = 1.94mV



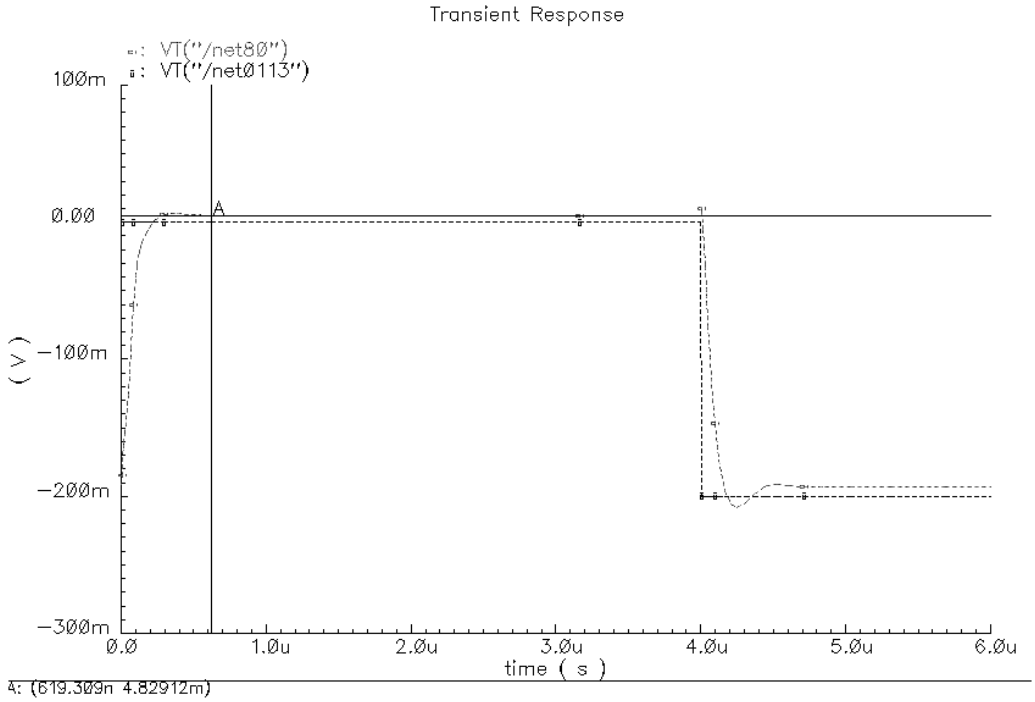
CMRR versus frequency, CMRR@ dc = 60dB



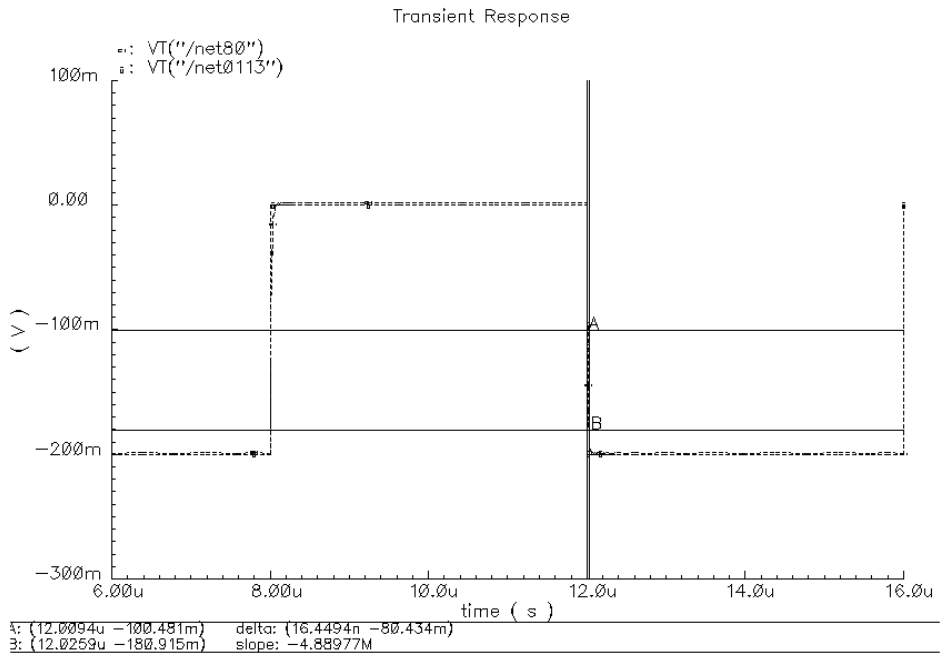
PSRR- versus frequency, PSRR- @ dc = 80dB



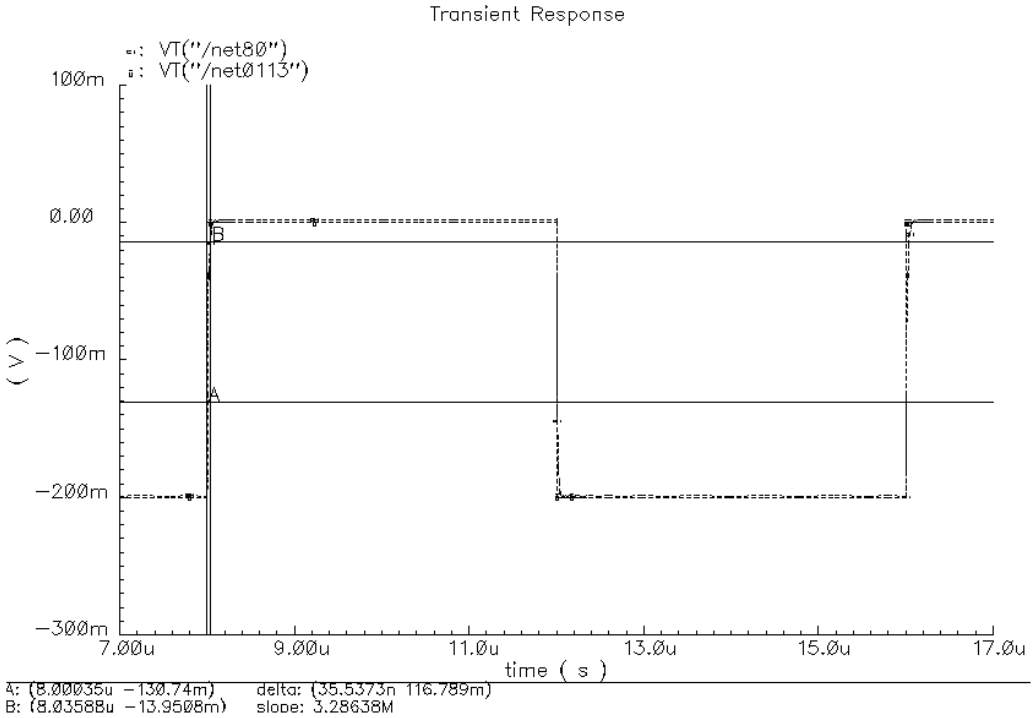
PSRR+ versus frequency, PSRR+ @ dc = 83dB



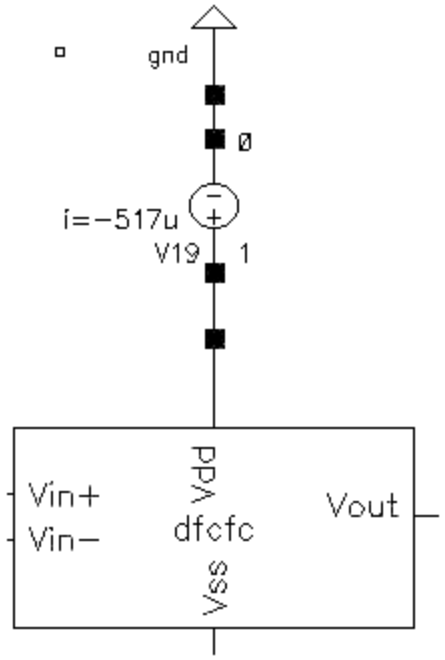
Transient Response, Settling time = 619ns



Negative Slew Rate = -4.9V/us



Positive Slew Rate = -3.3V/us



Current consumption

PARAMETER	SPECIFICATION	SIMULATION
Avo	75 dB	101.3 dB
GBW	29 MHz	29 MHz
Phase Margin	70 deg	69 deg
Slew Rate	10 V/µs	-4.9 V/µs (-ve)
		3.3 V/µs (+ve)
Settling Time	Minimum	619ns
CL	5 pF	5 pF
PSRR+	-	83 dB
PSRR-	-	80 dB
CMRR (0)	-	60 dB
Power Consumption	Minimum	0.914 mW
Total Compensation Capacitance	-	8pF

COMPARISON OF RESULTS – 3 STAGE DFCFC1 & 4 STAGE NGCC

PARAMETER	SPECIFICATION	DFCFC1	NGCC
Avo	75 dB	101.3 dB	76 dB
GBW	29 MHz	29 MHz	29 MHz
Phase Margin	70 deg	69 deg	69.6 deg
Slew Rate	10 V/µs	-4.9 V/µs (-ve)	1.94 V/us (+ve)
		3.3 V/µs (+ve)	1.5 V/us (-ve)
Settling Time	Minimum	619 ns	1.155u
CL	5 pF	5 pF	5 pF
PSRR+	-	83 dB	60 dB
PSRR-	-	80 dB	44.3 dB
CMRR (0)	-	60 dB	68 dB
Power Consumption	Minimum	0.914 mW	1.38 mW
Total Compensation Capacitance	-	8pF	19 pF
CMR	-	1.61	1.60
Output Swing	-	1.65	1.61
Input referred offset	-	4.9mV	1.94mV

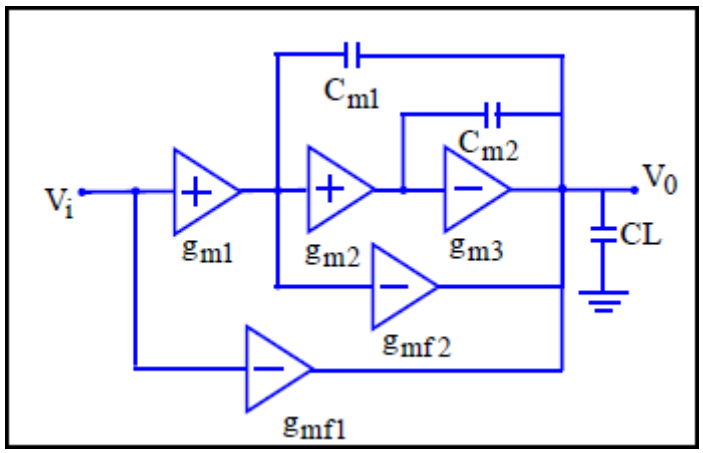
COMMENTS

It can be observed from the table the differences between the two schemes of compensation.with the three stage DFCFC we were able to achieve a gain of 101dB and about the same GBW and phase margin as the four NGCC which has a gain of 76dB. The two have comparable DC response but the input referred ioffset of the NGCC is better than that of the DFCFC. The DFCFC o n the other hand uses much less compensation caps than the NGCC and much less power (about 40% less in this case) as well. But the main issue with this scheme is the relatively bad rejection to common mode signals.

PROBLEM 3

Design of a three Stage NGCC based on the Settling Time Optimization techniques.

The closed loop transfer function of a three stage NGCC operational amplifier is given by :



Block Diagram of a three stage NGCC

$$H(s) = H_o \frac{1 + \frac{g_{mf2} - g_{m2}}{g_{m3}} \frac{C_{c2}}{g_{m2}} s + \frac{g_{mf1} - g_{m1}}{g_{m1}} \frac{C_{c1} C_{c2}}{g_{m3} g_{m2}} s^2}{1 + \left(\frac{C_{c1}}{f g_{m1}} + \frac{g_{mf2} - g_{m2}}{g_{m2}} \frac{C_{c2}}{g_{m3}} \right) s + \frac{g_{m3} + g_{mf2} - g_{m2} + f g_{m1}}{f g_{m1}} \frac{C_{c1} C_{c2}}{g_{m3} g_{m2}} s^2 + \frac{C_{c1} C_{c2} C_L}{f g_{m1} g_{m3} g_{m2}} s^3}$$

As per the compensation network design rules;

$$C_{c1} = \frac{g_{m1}}{g_{m3}} f \left(1 + \frac{2}{\rho}\right)(1 + 2\rho\zeta^2) C_L$$

$$and\ C_{c2} = \frac{g_{m2}}{g_{m3}} \zeta^2 \frac{(\rho + 2)^2}{1 + 2\rho\zeta^2} C_L$$

$$where\ \rho = \frac{p_1}{(\zeta \omega_n)}$$

Where $\rho\ and\ \zeta\ are\ parameters\ that\ will\ be\ optimized\ to\ optimize\ settling\ time.$

For the optimization of the settling time for a third order system,

$$G_{III}(s) = \frac{G_o\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+2\frac{\zeta}{\omega_n}s+\frac{s^2}{\omega_n^2}\right)}$$

To deal with the minimization problem systematically, it is instead convenient to consider the following normalized system.

$$G_{III}(s) = \frac{G_o\left(1+\frac{s}{X_1}\right)\left(1+\frac{s}{X_2}\right)}{\left(1+\frac{s}{\rho}\right)(1+2\zeta^2 s++\zeta^2 s^2)}$$

$$where\ \rho = \frac{p_1}{(\zeta\omega_n)}\ and\ X_1 = \frac{z_1}{(\zeta\omega_n)}\ and\ X_2 = \frac{z_2}{(\zeta\omega_n)}$$

represent the relative real pole and zero locations with respect to the real part of the complex poles $\zeta\omega_n$, which is the normalizing factor.

From the above, it can be shown that the minimization problem to find the minimum settling time for the third order system can be reduced to finding optimal values for ζ and ρ.

The absolute denormalized minimum settling time (MST) can be derived from the following:

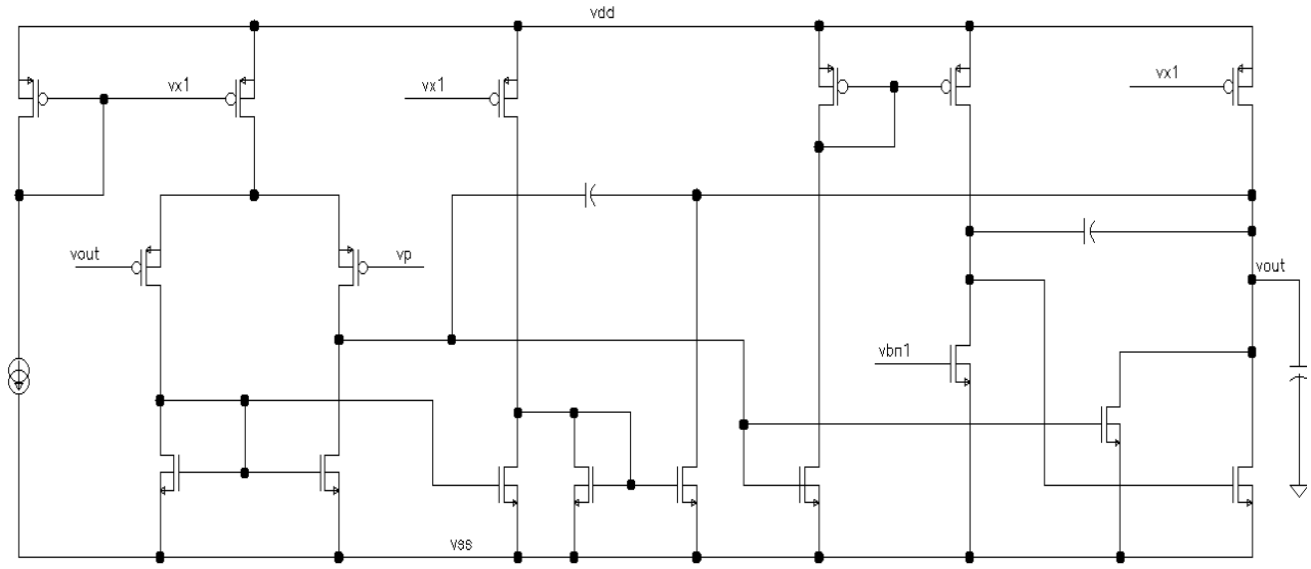
$$t_{SMIN} = \frac{Ts_{IIImin}}{\zeta_{IIIopt}\,\omega_n}$$

To obtain the parameters; $\rho_{opt}\ and\ \zeta_{IIIopt}\ and\ hence\ t_{SMIN}$ we need to do some sweep to obtain these values based on the level of accuracy we want.

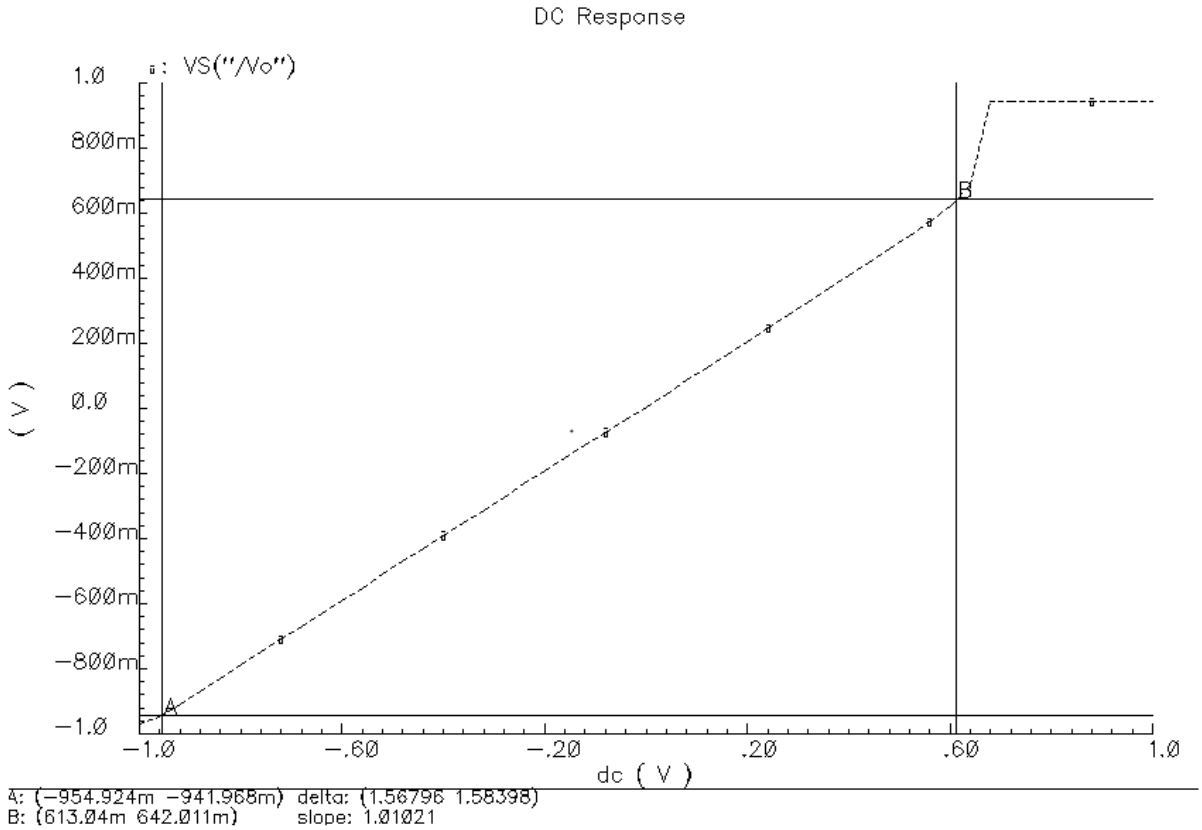
Based on these values we can obtain the required miller caps need to compensate the circuit to achieve minimum settling time as shown in the equations Cc1 and Cc2 above.. This was done and the results are shown below.

The miller caps obtained are used on the design of the three stage NGCC and the result shows a better settling time than the previous one designed.

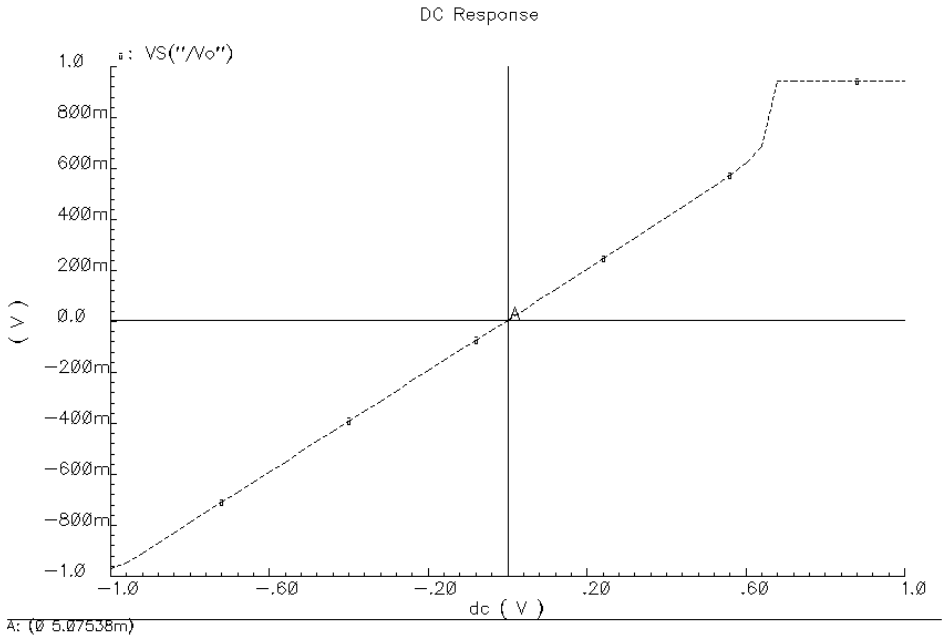
Schematic of the three stage NGCC



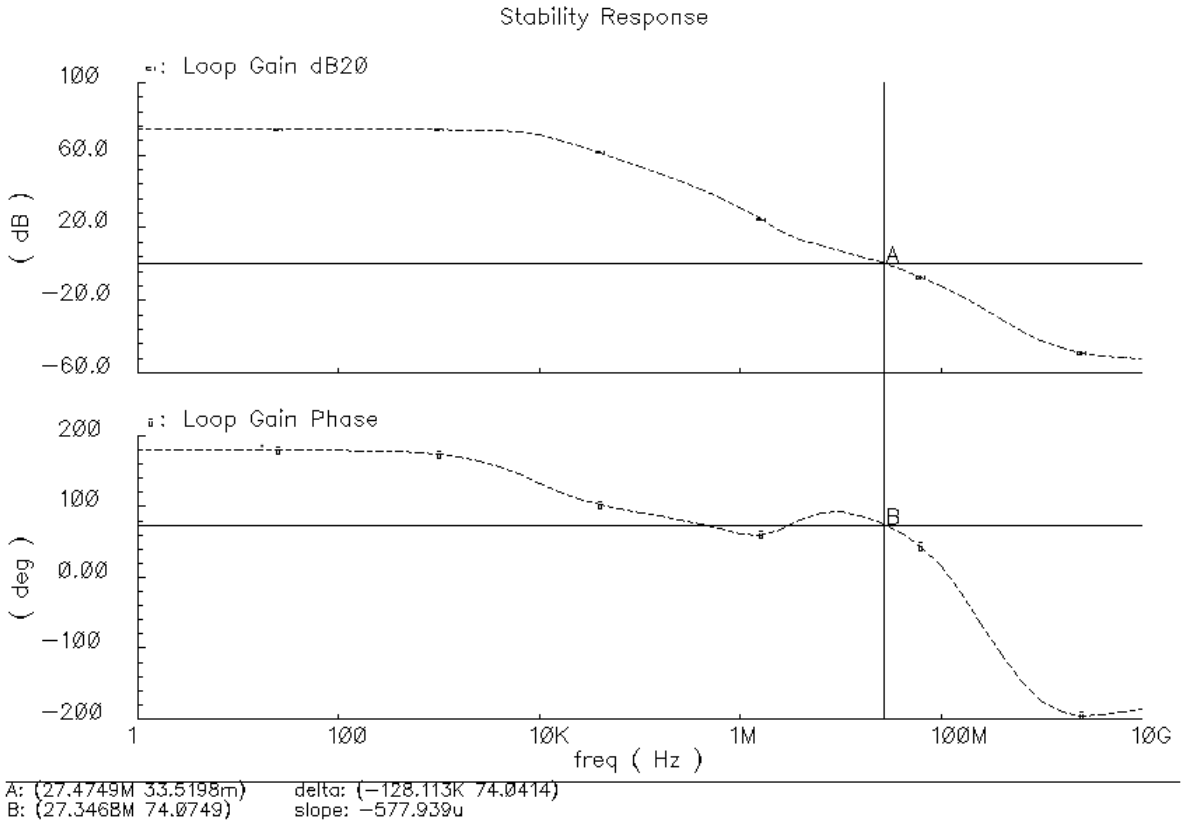
RESULTS



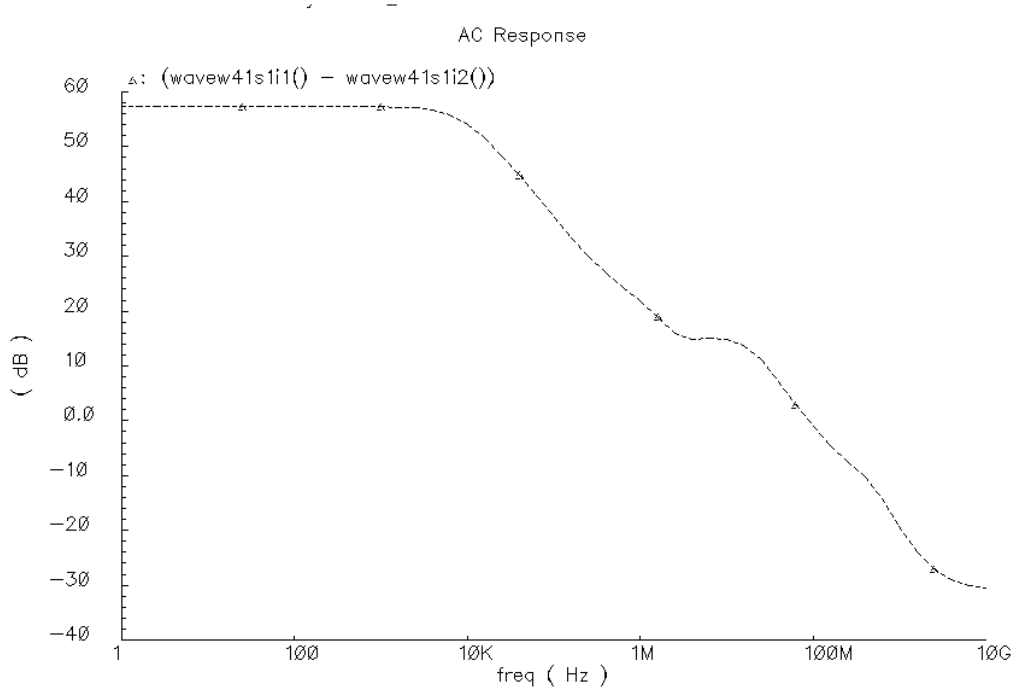
DC Response: Output swing = 1.58V, ICMR = 1.57V



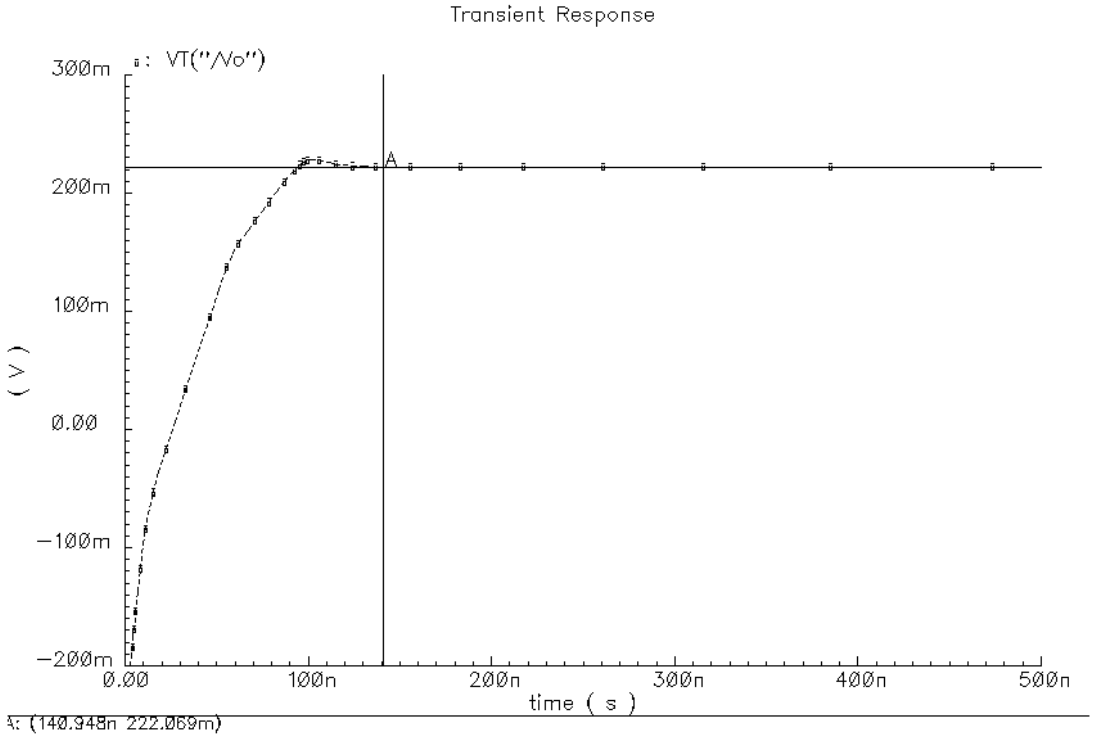
Dc Response: Input referred offset = 5.1mV



Magnitude and Phase Response, Gain = 72dB, GBW = 27.5M Hz, PM = 74deg



CMRR versus frequency; CMRR@dc = 57dB



Transient showing setlling time; Settling time = 140ns

Specification	Required	Conventional	With Settling Time Minimization Technique
Power Supply	**2V**	**2V**	**2V**
Load	**5pF**	**5pF**	**5pF**
GBW	**29MhZ**	**29MHz**	**27.5MHz**
DC Gain	**75dB**	**76dB**	**72dB**
Phase Margin	**70deg**	**69.6deg**	**74deg**
Settling time	**minimum**	**1.155us**	**140ns**
Power Consumption	**minimum**	**1.38mW**	**1.13mW**
Slew Rate	**10V/us**	**1.94V/us**	**4.9V/us**

COMMENTS

With the design using the settling time minimization techniques, it is very obvious the difference between the two settling times. While all other specs are comparable, the main difference between the two is that the settling time of the conventional is about 10 times that of the new technique and it consumes less power than the conventional. This certainly makes this a good choice in the design of such amplifiers.

PROBLEM 4 : DESIGN USING THE 65nm CMOS TECHNOLOGY`

General Design Procedure

A new variable which depends on the relative location of the poles of the system to each other will be used throughout the design. The general procedure for designing a 4^{th} order system is used here. The 3 stage is obtained by assuming f4 is at infinity. These are the 'f' variables. An N-stage NGCC has N 'f' variables, as such the following 4 are used henceforth, f1, f2, f3 and f4.

The transfer function for the 4 stage NGCC can be represented by the following equation

$$H(s) = \frac{A_o}{(1 + \frac{A_o}{f1})(1 + \frac{s}{f2} + \frac{s^2}{f2f3} + \frac{s^3}{f2f3f4})}$$

where A_o is the dc gain and $f1, f2, f3$ and $f4$ are the cut off frequencies of each stage

The stability criteria for this circuit can be fixed by using Routh-Hurwitz stability criterion on the unity-feedback transfer function which is given by the below equation

$$HCL(s) = \frac{1}{\frac{s}{f1} + \frac{s^2}{f1f2} + \frac{s^3}{f1f2f3} + \frac{s^4}{f1f2f3f4}}$$

We obtain the following conditions for stability

$$f4 > f2$$

$$f4 > \frac{f2}{1 - \frac{f1}{f3}}$$

Also phase margin can be approximated by the following equation if f3>f2 and f4>f2
$Ø_M = 90 – \arctan(GB/f2)$

- The cutoff of the first stage,f1 is set equal to the required GBW and f2 is obtained from the approximate expression of the phase margin.

$$\boldsymbol{f1 = GBW \cong 70MHz}$$

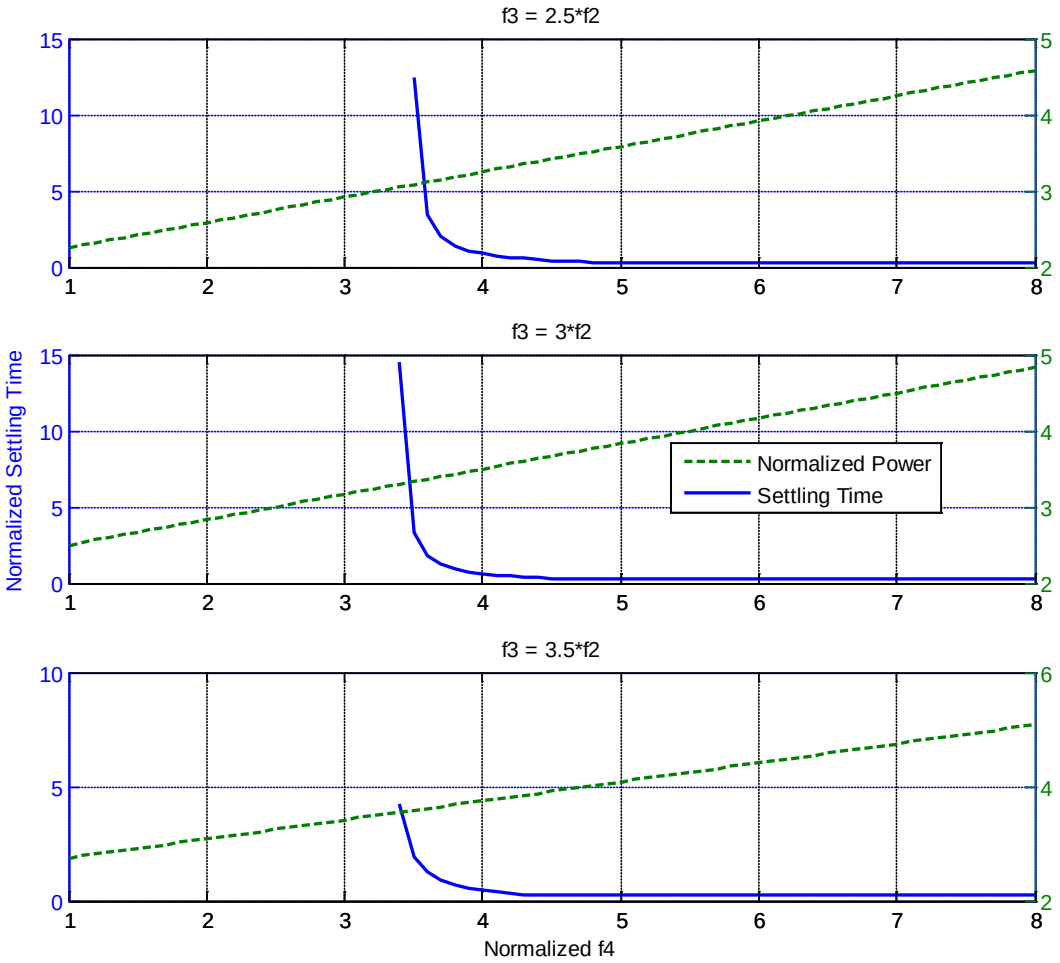
$$\emptyset m = 90^{\circ} - \tan^{-1}\left(\frac{GBW}{f2}\right) = 70^{\circ},\ \ GBW = 30MHz,$$

$$therefore, \qquad \boldsymbol{f2 \cong 3GBW = 210\ MHz}$$

- f3 and f4 are determined from the settling time and power requirement of the amplifier. A sweep of f3 and f4 can be done versus normalized power and settling power and the values of f3 and f4 that produces the minimum power and settling time and also meet the condition for phase margin >70deg is chosen. Using the full expression for the phase margin of the system, a numerical analysis can be performed to find optimum values of f3 and f4 such that settling time is minimized while the phase margin is not degraded. This can be performed using MATLAB. The code used is shown in Appendix A.
- To do that we need to choose values for the miller capacitors that we will use in the compensation. We require the ratios between the miller caps and the load cap to determine the normalized power for the MATLAB plots. For this design we use a miller caps of 2.5pF.
- The phase margin is computed from the expression below

$$\boldsymbol{\emptyset m = 90^{\circ} - \tan^{-1}\left[\frac{GBW}{f2}\left(\frac{1 - GBW^2/f3.f4}{1 - GBW^2/f3.f4}\right)\right]}$$

Settling time is obtained using the general transfer function of a 4th order NGCC, connecting it in unity feedback and taking the step response.



Matlab Plot of variation of settling time and power versus f3 and f4

From the plots, we again choose f3 = 2.5*f2 and f4 = 3.5f2 since this choice optimizes both settling time and power

Next we can determine the transconductance of each stage from the following equation:

$$fi = \frac{gm_i}{2\pi Cm_i} \qquad \ldots\ldots\ldots\ldots 1$$

$$\boldsymbol{f1 = 70MHz,\ \ f2 = 210MHz,\ \ \ f3 = 525MHz\ and\ f4 = 735MHz}$$

Substituting these values into eqn 1 *gives the following gms. and again assuming* $Cm1 = Cm2 = Cm3 = 1p$

$$\boldsymbol{gm1 = 439uS \;\; gm2 = 1.319\mu S \;\; gm3 = 3.3mS \; and \; gm4 = 4.6mS}$$

- The ACM model for the transistor is defined by the following equations.

1. $Id = gm * n * \emptyset_t \dfrac{1+\sqrt{1+id}}{2}$
2. $W/_L = \dfrac{gm}{\mu C_{OX} \emptyset_t}\left(\dfrac{1}{\sqrt{1+id}-1}\right)$
3. $f_T = \dfrac{\mu \emptyset_t}{2\pi L^2}\left(2\sqrt{1+id}-1\right)$

For this design, we choose an appropriate Vdsat for each stage and compute the corresponding inversion level, then we can compute the respective W/L for each transistor.

$$W/_L = \frac{gm}{\mu C_{OX} \emptyset_t}\left(\frac{1}{\sqrt{1+id}-1}\right)$$

The values for μC_{OX} for nmos and pmos for the 65nm technology is extracted from Cadence and the results found to be:

Kn = 540µ & Kp = 120µ

This is used in computing the aspect ratios for the various transistors in a similar manner as was done in Problem 1

4th Stage – nmos input

$$\boldsymbol{\left(W/_L\right)4n = 43}$$

Hence,

$$\boldsymbol{\left(W/_L\right)4p = \left(W/_L\right)4n * 3 = 129}$$

3rd Stage – nmos input

$$\left(\frac{W}{L}\right)3n = 35$$

Hence,

$$\left(\frac{W}{L}\right)3p = \left(\frac{W}{L}\right)3n * 3 = 105$$

2nd stage nmos input

$$\left(\frac{W}{L}\right)2n = 12$$

Hence,

$$\left(\frac{W}{L}\right)2p = \left(\frac{W}{L}\right)2n * 3 = 36$$

1st Stage – pmos input

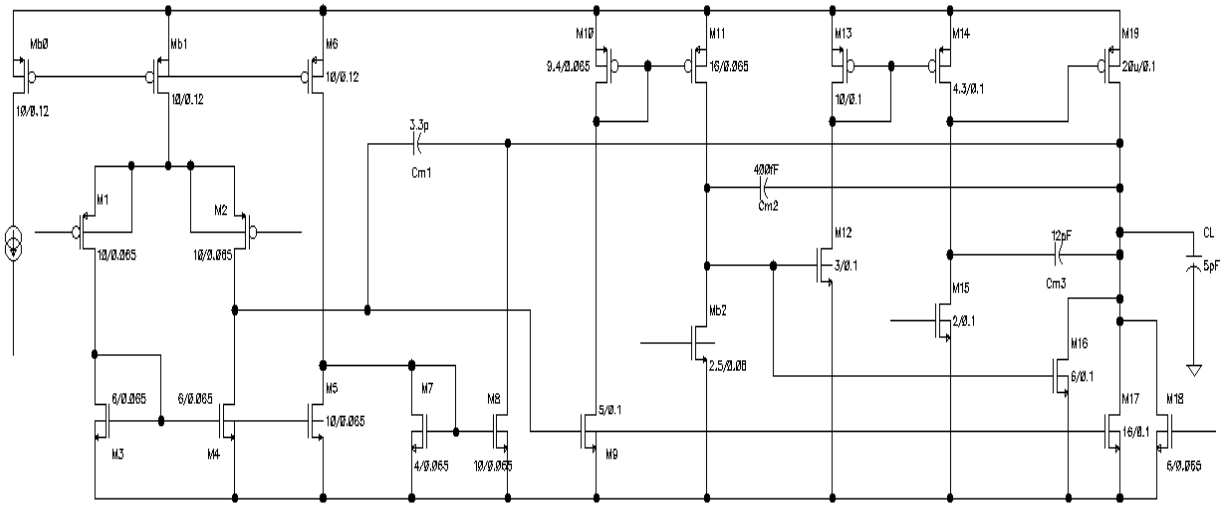
$$\left(\frac{W}{L}\right)1p = 102$$

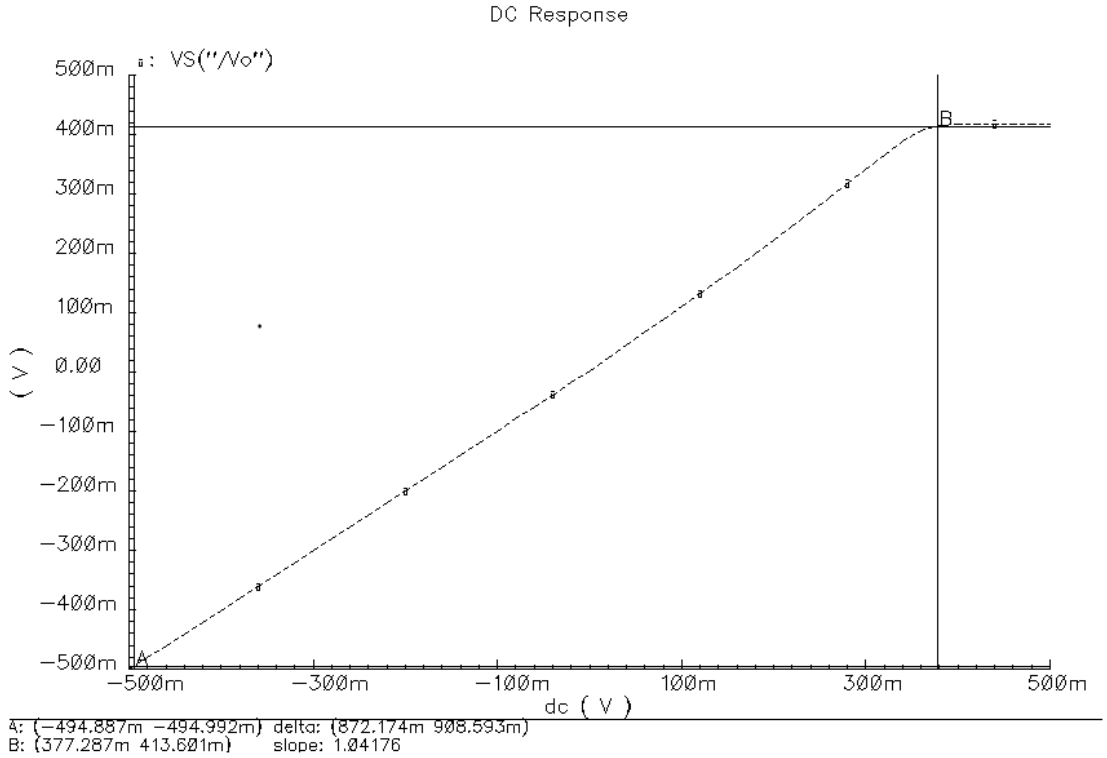
Hence,

$$\left(\frac{W}{L}\right)1n = \left(\frac{W}{L}\right)1p * 1/3 = 34$$

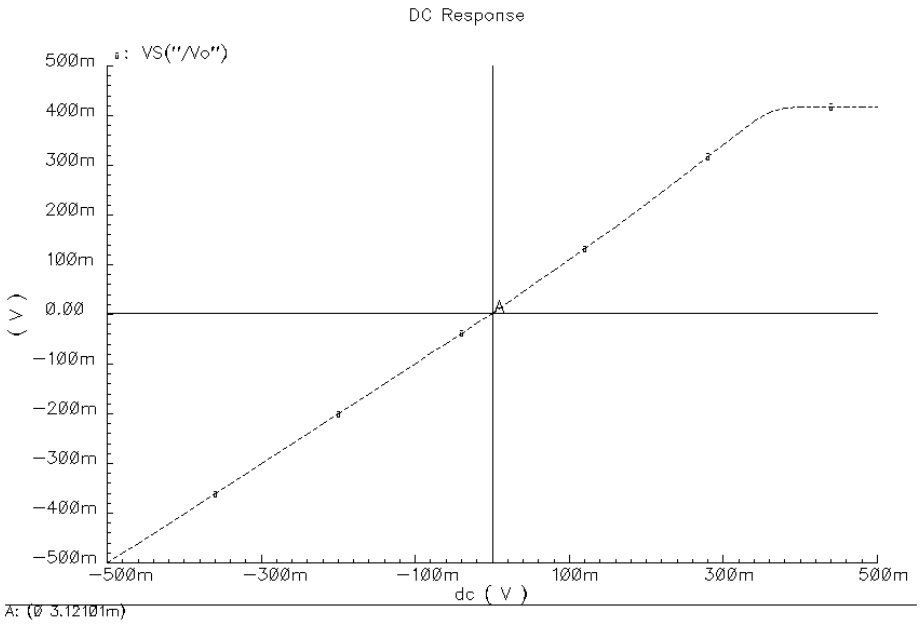
These computed values are used for the first set of simulations of the amplifier, and are adjusted as necessary to meet the required specifications.

The schematic of the opamp is shown below

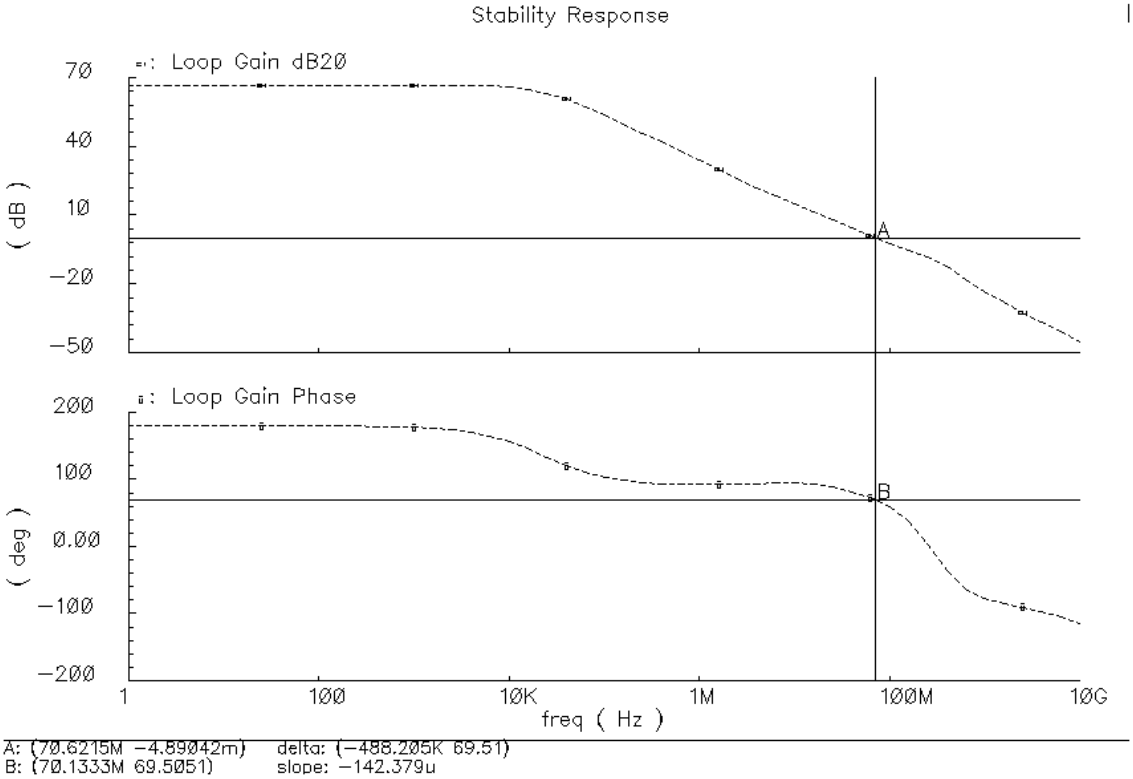




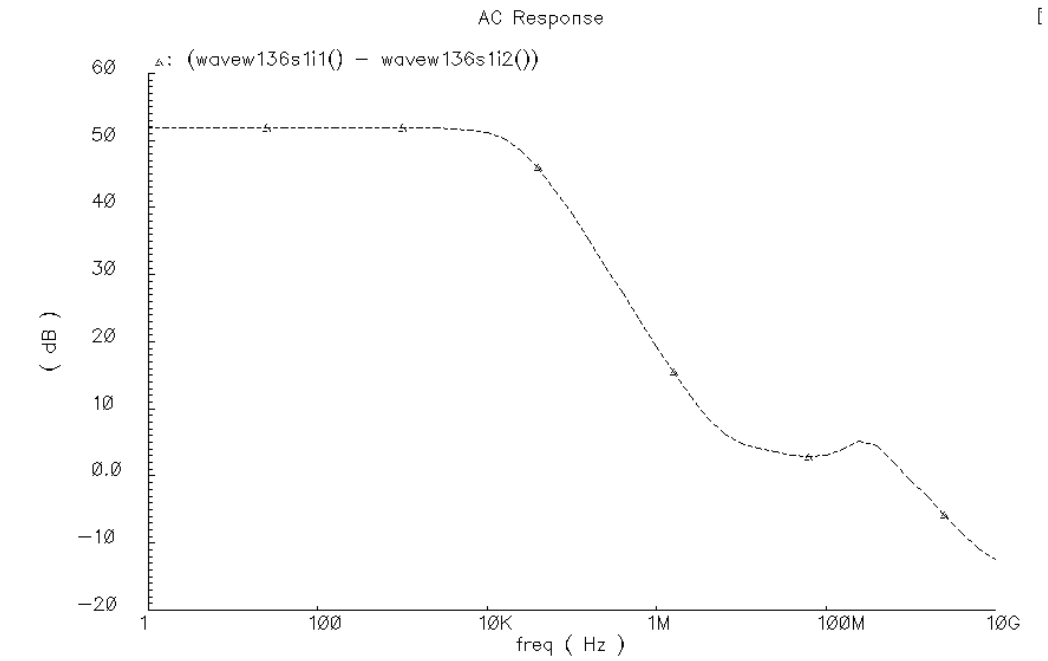
DC Response, Output Swing = 908mV and ICMR = 872mV



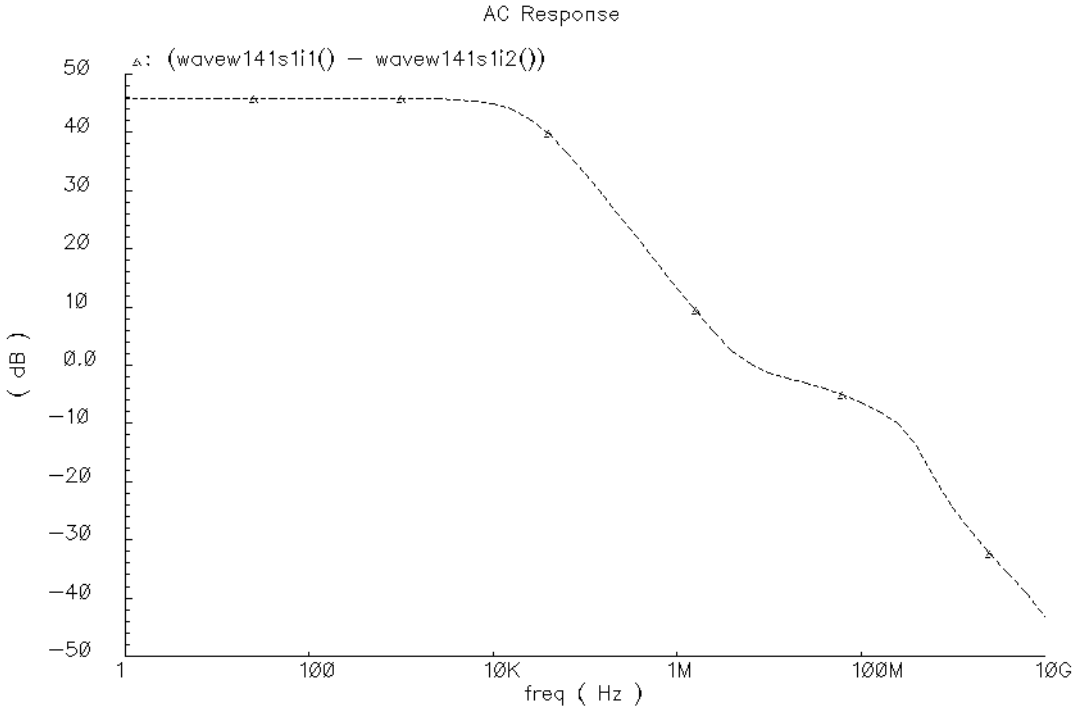
DC Response, Input referred offset = 3.12mV



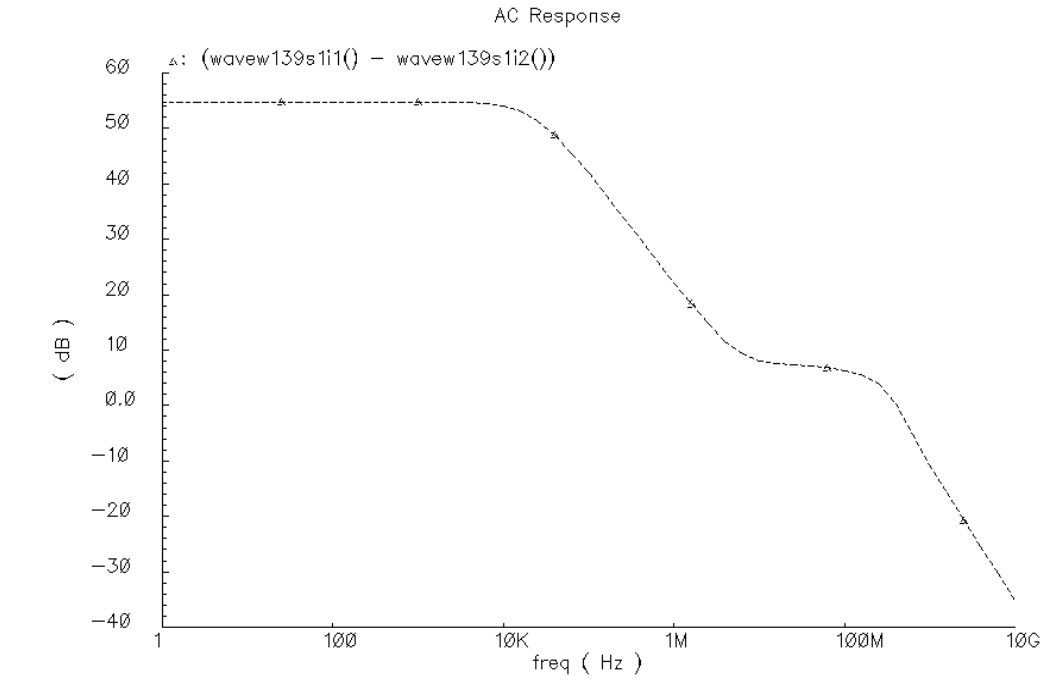
Magnitude ad Phase Response, Gain = 66dB GBW = 70.6MHz PM = 70 deg.



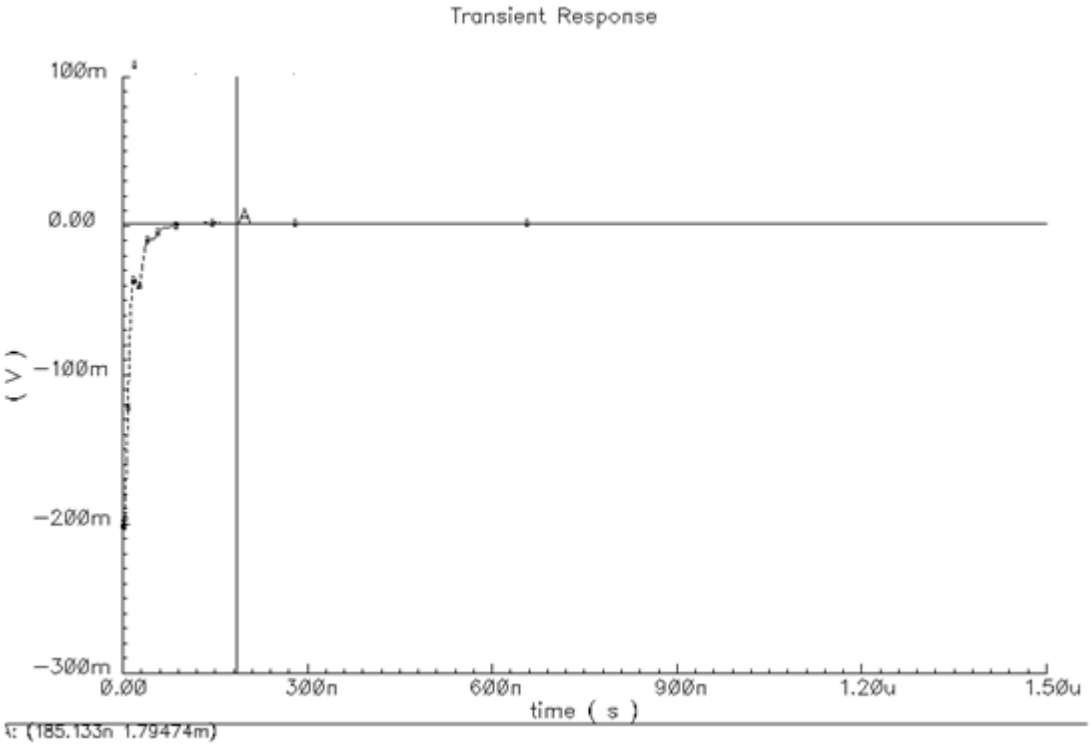
CMRR versus frequency, CMRR@dc = 53dB



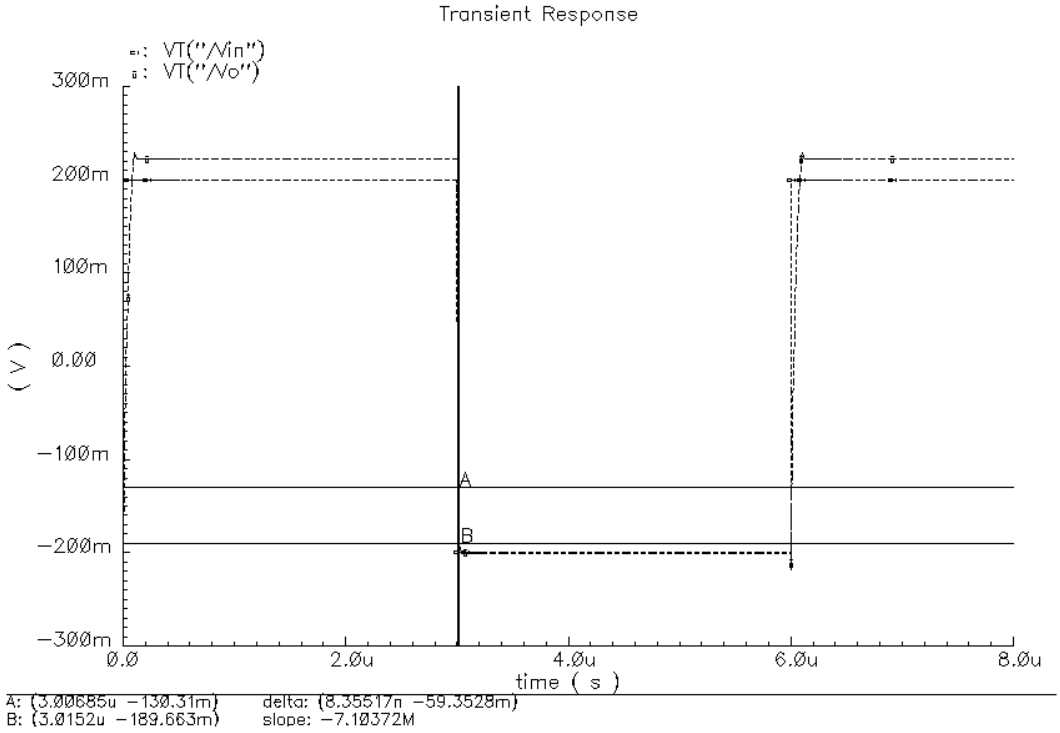
PSRR- versus frequency, PSRR- @dc = 46dB



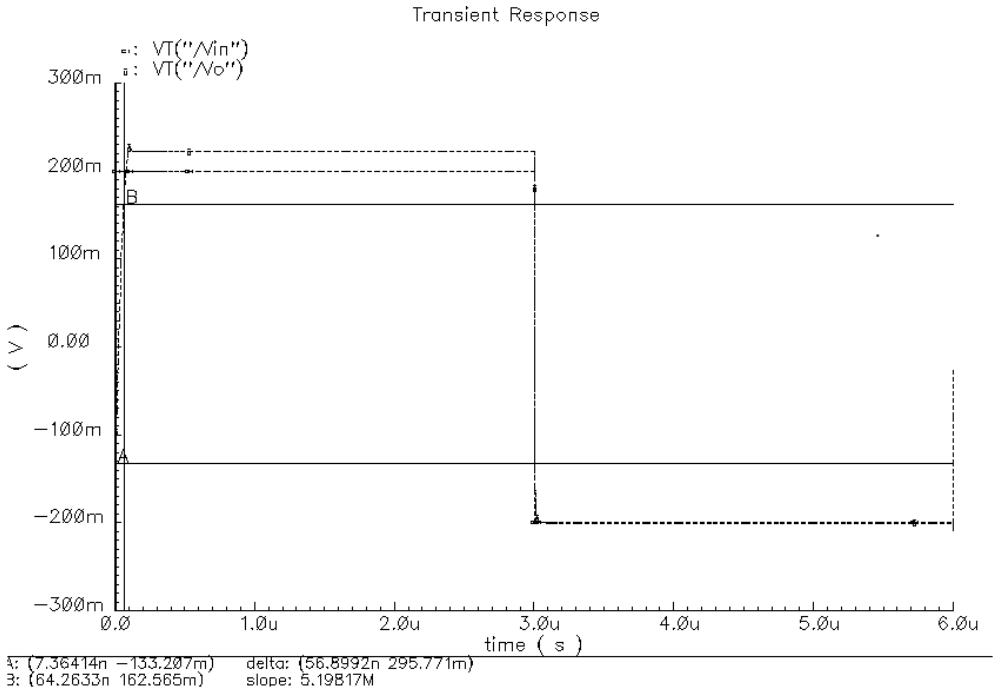
PSRR+ versus frequency, PSRR+ @dc = 54dB



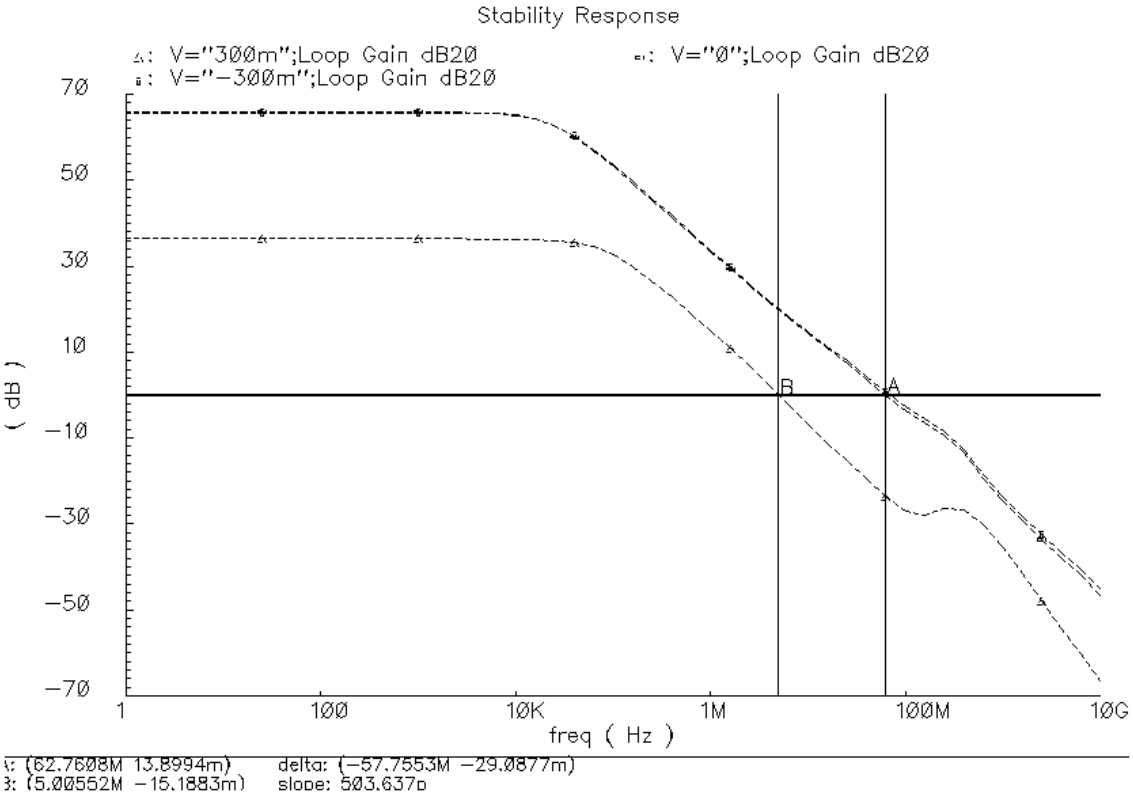
Transient Response showing settling behavior, settling time = 185ns



Transient Response, Negative Slew Rate = -7V/us

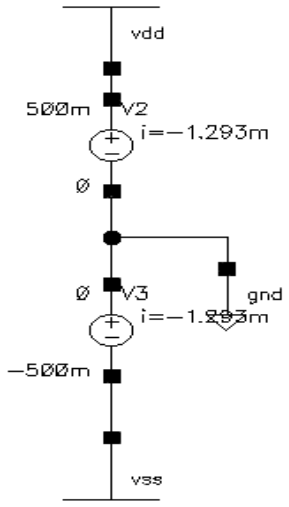


Transient Response, Negative Slew Rate = 5.2 V/us



Comparing Open Loop Response for a sinusoidal signal, with different DC levels.

For DC = -0.3V, 0 and 0.3 respectively from top to sown on the plot.



Current consumption

SUMMARY OF RESULTS

Specification	Required	Single output version
Power Supply	**1V**	**1V**
Load	**5pF**	**5pF**
GBW	**70MhZ**	**70.6MHz**
DC Gain	**55dB**	**66dB**
Phase Margin	**70deg**	**70deg**
Settling time	**minimum**	**185ns**
Power Consumption	**minimum**	**1.2mW**
Slew Rate (+/-)	**10V/us**	**5.2/-7 V/us**
CMRR @DC	**-**	**53dB**
PSRR(+/-)@DC	**-**	**54/46 dB**
CMR	**-**	**872mV**
Output Swing	**-**	**908mV**
Input referred offset	**-**	**3.12mV**

COMMENTS

We observe from the results here that almost all the specifications for the design were met except for the slew rate specification. This is due to the very small amount of current used in the tail. To increase the SR, more current should be pumped and that is also expensive. We realize that with this small sized technologies, it is much easier to achieve very frequencies than with the long channel technologies. But it comes at the cost of extra power.

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