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HW2

2/7/2017

ECEN 607

Problem 1

Part A

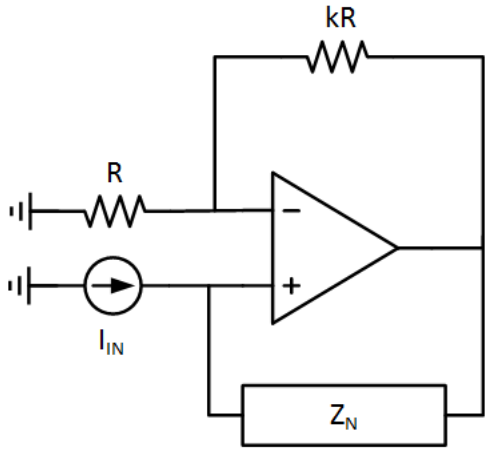


Figure 1: Negative Impedance Converter

To find the input impedance of the above NIC, we use the following equations:

$$\frac{V_+}{Z_N} - \frac{V_O}{Z_N} = I_{in}, -\frac{V_O}{kR} + \left(\frac{1}{R} + \frac{1}{kR}\right)V_- = 0, V_- = -\frac{V_O}{A} + V_+$$

Solving these equations simultaneously produces the following expression:

$$\frac{V_+}{I_{in}} = -Z_N \frac{1 + A + k}{k(A-1) - 1}$$

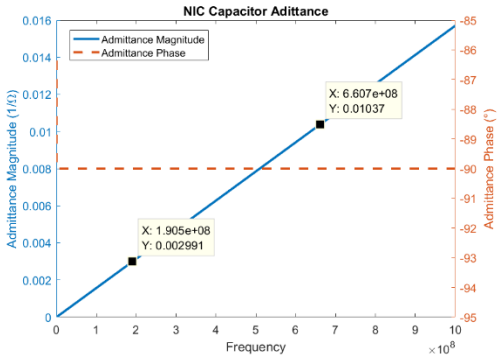
Therefore finite-gain op amp with a gain of A used as a negative impedance converter produces an input impedance of:

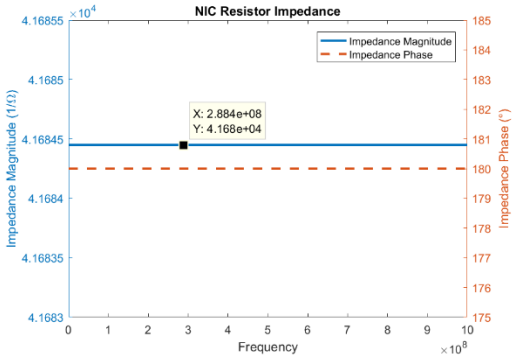
$$Z_{in} = -Z_N \frac{\left(1 + \frac{1+k}{A}\right)}{k - \frac{k+1}{A}}$$

For this part of the problem, an op amp with 80dB of gain is used. This means that the input impedance can be approximated as:

$$Z_{in} = -\frac{Z_N}{k}$$

A macromodel for the op amp was created from a simple voltage-controlled voltage source. Therefore, the output voltage of the op amp is simply the input voltage multiplied by the op amp gain. Two different impedances are used for Z_{in} in this problem: a resistor and a capacitor. The AC simulation showing the impedance magnitude and phase for both of these simulations can be found below. For these simulations, a k of 0.60 was used in the negative resistor while a k of 0.25 was used for the negative capacitor. While a resistance and capacitance of 25kΩ and 10pF are used.





As seen in the graphs above, the slope of the capacitor admittance is:

$$m = \frac{0.01037 - 0.002991}{6.607 * 10^8 - 1.905 * 10^8} = 1.57 * 10^{-12} = 2\pi C \rightarrow C = 2.5pF$$

Since the phase of the admittance is -90°, this capacitance is negative which is what is expected. The magnitude of the capacitance is equal to k times the capacitor used for Z_N which matches the 2.5pF measured. For the resistor, the impedance magnitude is simulated as 41.68kΩ which matches the expected value of $\frac{25k\Omega}{0.6}$. In addition to this, the phase of the impedance is 180° which matches the expectation for a negative resistor.

Part B

In the final expression, we can replace A with $\frac{GB}{s}$ to find the impedance expression with a finite gain bandwidth op-amp:

$$Z_{in} = -\frac{Z_N\left(1 + \frac{s(1+k)}{GB}\right)}{k - \frac{s(1+k)}{GB}} = -\frac{Z_N}{k}\frac{\left(1 + \frac{s(1+k)}{GB}\right)}{1 - \frac{s(1+k)}{kGB}}$$

This transfer function has a RHP pole and a LHP zero at :

$$\omega_z = -\frac{GB}{1+k}, \omega_p = \frac{GB}{\frac{1}{k}+1}$$

So, the final transfer function can be written as:

$$Z_{in} = -\frac{Z_N}{k} \cdot \left(\frac{1 + \frac{s}{\omega_Z}}{1 - \frac{s}{\omega_p}}\right)$$

Therefore, the gain-bandwidth of the op amp used in the NIC plays a large role in the frequency for which the negative impedance is valid. For the resistor, the input impedance will be:

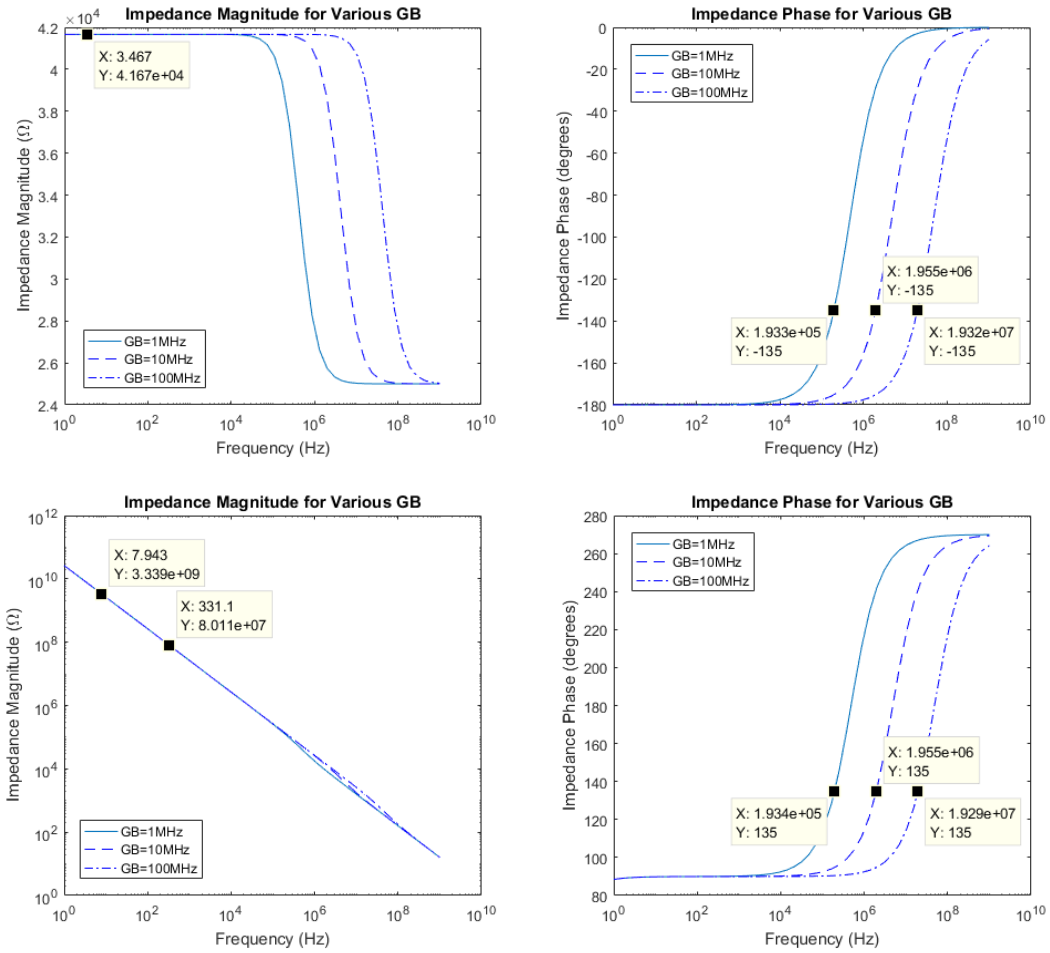
$$Z_{in} = -\frac{R}{k}\frac{\left(1 + \frac{s(1+k)}{GB}\right)}{1 - \frac{s(1+1/k)}{GB}} = -41.67k\Omega \cdot \frac{1 + \frac{s}{3.93Mrad/s}}{1 - \frac{s}{2.36Mrad/s}}$$

With a k-value of 0.6 and a GB of 1MHz, the input impedance expression will be

For the capacitor, the input impedance will be:

$$Z_{in} = -\frac{1}{sCk}\frac{\left(1+\frac{s(1+k)}{GB}\right)}{1-\frac{s\left(1+\frac{1}{k}\right)}{GB}} = -\frac{1}{s\cdot 6pF}\cdot\frac{1+\frac{s}{3.93Mrad/s}}{1-\frac{s}{2.36Mrad/s}}$$

Therefore, the negative resistor and capacitor will behave close to a certain frequency determined by the placement of the pole and zero. This is due to the fact that the phase shift and magnitude change due to the pole or zero will make the input impedance different than the desired form. As a result, the gain-bandwidth of the op amp used in the NIC plays a very large role in its performance at higher frequencies. This equation was tested using a simple op amp macromodel with $A(s) = \frac{GB}{s}$. The negative resistor and negative capacitor implementations were tested with a GB of 1MHz, 10MHz, and 100MHz. The maximum frequency of operation of the NIC was defined as the frequency at which the phase error from the ideal negative input impedance equals 45 degrees. The expressions above are confirmed using the simple op amp macromodel:



The negative capacitor input impedance can be calculated as:

$$\frac{1}{\frac{3.339G\Omega}{331.1Hz} - \frac{1}{80.11M\Omega}} * \frac{1}{2\pi} = 6pF$$

As seen in the graphs above, the maximum frequency of operation is a constant factor of the gain bandwidth of the operational amplifier used in the NIC. For a 45-degree phase error, the maximum frequency of operation is approximately half the pole frequency or:

$$\frac{1MHz}{1+\frac{1}{.6}}\cdot\frac{1}{2}=187.5kHz$$

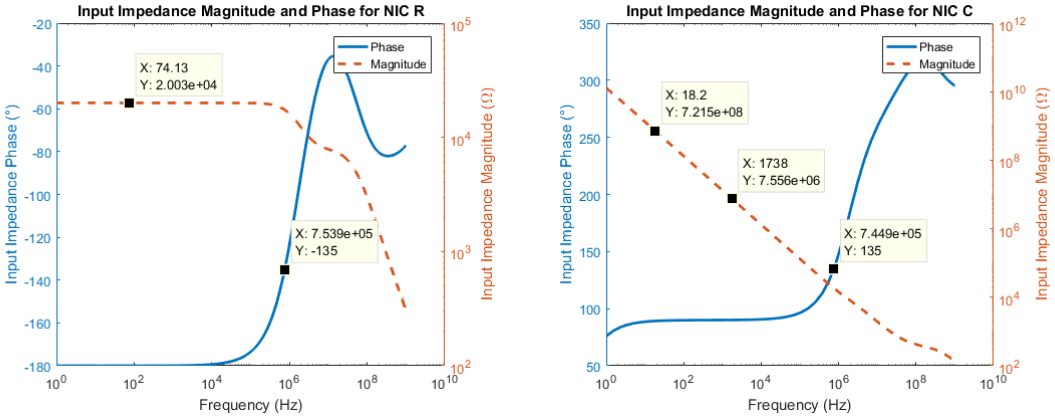
If the k value is greater than 1 and the zero frequency is lower than the pole frequency, the range of operation will be limited to half the zero frequency.

Part C

Finally, the ACM-designed op amp from the previous homework was used in the negative impedance converter. This op amp has a gain bandwidth product of approximately 4MHz. One NIC was designed with a resistance of 10kΩ while the other was designed with a capacitance of 6.28pF. In order to test the resistance/capacitance multiplying properties of the NIC, the k value for the resistor NIC was chosen to be 0.5 while for the capacitor NIC it was chosen to be 2. This will provide an effective input resistance of -20kΩ and an effective input capacitance of -12.56pF. In addition to this, we expect effective frequency of operation of the NIC to be at frequencies less than around 750kHz based off the results in the previous section:

$$\omega_{max}=\frac{4MHz}{1+\frac{1}{0.6}}\cdot\frac{1}{2}=750kHz$$

This estimate for the operating range is confirmed by the following AC simulations:

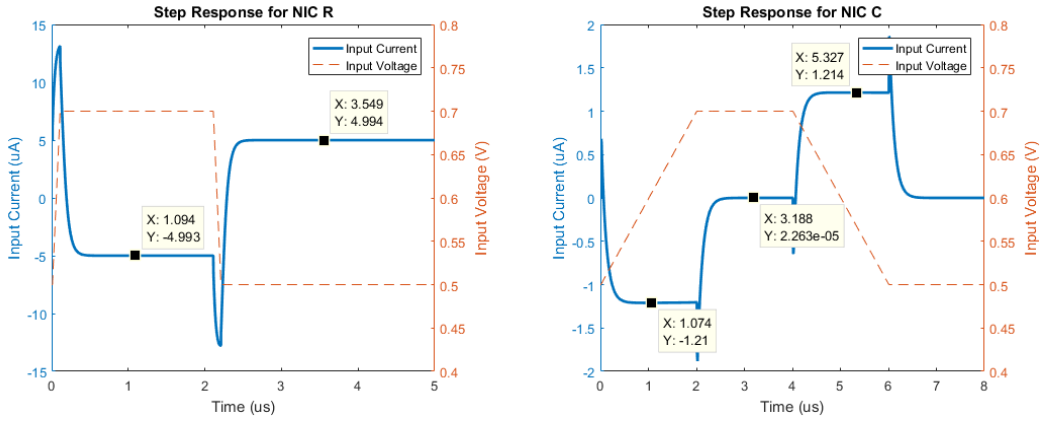


The NIC resistor indicates an impedance magnitude at low frequencies of 20.03kΩ and a maximum effective frequency of 754.3kHz. The capacitor indicates an impedance magnitude of:

$$\frac{\frac{1}{124.5M\Omega}-\frac{1}{5.661M\Omega}}{2320Hz-105.5Hz}*\frac{1}{2\pi}=12.11pF$$

Again, the negative capacitor is valid up until 744.1kHz. These impedance calculations and effective frequency ranges match very well with what we expect from the analysis in Part B. The magnitudes of the negative impedances also match very well with the expected values and any difference is most likely caused by the finite gain of the op amp.

Next, the step response of the two NICs were analyzed to ensure the input impedance is stable:



The NIC resistor shows a very stable step response with no ringing. In addition, we can see that as the input voltage increases, the input current decreases. This shows that the NIC resistor truly behaves as a negative resistor. We can also see this in the step response for the NIC capacitor. The step response once again shows no ringing and for a positive derivative of the input voltage produces a negative current. This shows that the NIC capacitor is truly behaving as a negative capacitor.

The most obvious improvement that could be made to the NIC is to design an op amp with a larger GBW. This would increase the effective range of the negative resistor or capacitor and would therefore improve performance in many situations. Additionally, the gain of the op amp could be increased. This would produce an input impedance value closer to the ideal impedance value. This would make the NIC more useful in situations where the input impedance must be very tightly controlled. Lastly,

Problem 2

Part A

This will utilize the same NIC used in the previous problem that is shown in Figure 1 above. To increase the gain of the op amp designed in the last homework, the output resistance of the op amp must be increased. A negative resistance can be used to do this since the output resistance magnitude of the op amp with the negative resistance included can be calculated as:

$$R_0 R_N / (R_0 - R_N)$$

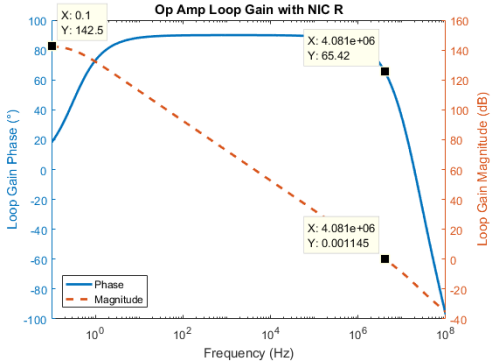
Therefore, if the negative resistance is close in magnitude to the output resistance of the op amp, the effective output resistance of the op amp will be greatly increased. This, in turn, will increase the gain of the second stage. From simulations, we can find that the output resistance of the op amp is approximately 80kΩ. Therefore, we will try to design the negative resistance to be as close to this value as possible. For this reason, the resistance used in the NIC is chosen to be 55kΩ while the value for k is chosen to be 0.7. Therefore, the feedback resistor is 7kΩ while the other resistor is 10kΩ. This provides a total output resistance magnitude of:

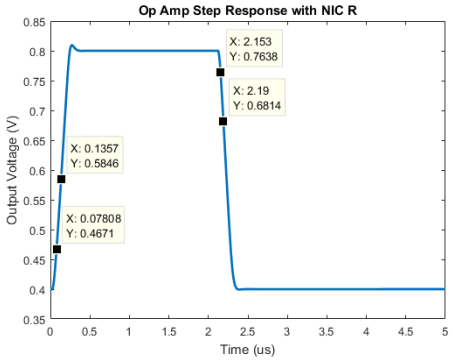
$$\frac{80k\Omega \cdot \frac{55}{0.7} k\Omega}{80k\Omega - \frac{55}{0.7} k\Omega} = 4.4M\Omega$$

This should therefore increase the gain of the op amp by:

$$20\log\left(\frac{4.4M\Omega}{80k\Omega}\right) = 34.81dB$$

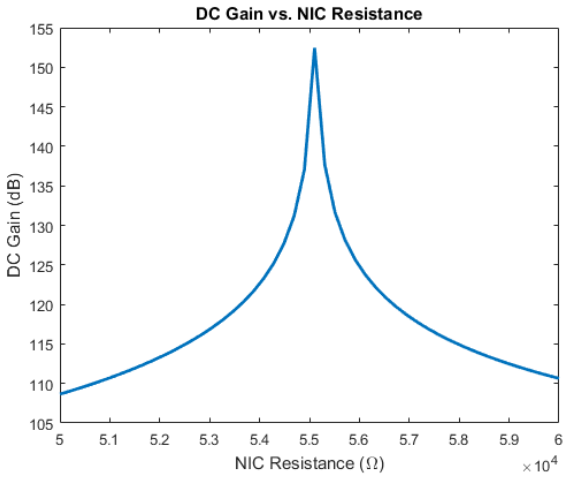
Therefore, this will achieve the required gain improvement. Since we are interested in increasing the DC gain, it is not imperative that this negative resistance be valid at high frequencies. Therefore, the op amp used in the NIC will be identical to the ACM amplifier designed in the previous homework but the bias current will be decreased to 3uA instead of 10uA. This will greatly decrease the power consumption as well as the gain-bandwidth of the amplifier. Therefore, the gain benefits of the NIC will be achieved with only at 10% increase in power. The results of the gain enhancement can be found below:





In the previous homework, the gain of the ACM designed amplifier was 89.25dB. As seen in the plot above, the new gain with the negative resistor added is 142.5dB. This represents a large increase in the DC gain of the op amp. In addition to this, the phase margin of the op amp remained much the same. In the previous homework, the phase margin was 65.61° while for this op amp the phase margin was 65.42°. The step response also shows a very stable response with no significant ringing. Since the ACM amplifier's slew rate is limited by its first stage, the slew rate did not change with the addition of the NIC resistor.

One important note regarding this gain-boosting strategy is the sensitivity of the gain to the resistor value used in the NIC. Since the k value is set by the ratio of resistors, it can be set very accurately. The NIC resistance value, however, depends on the absolute value of a resistor which, if implemented on an IC, may vary by a large amount. This, in turn, greatly decreases the achievable DC gain for the amplifier:

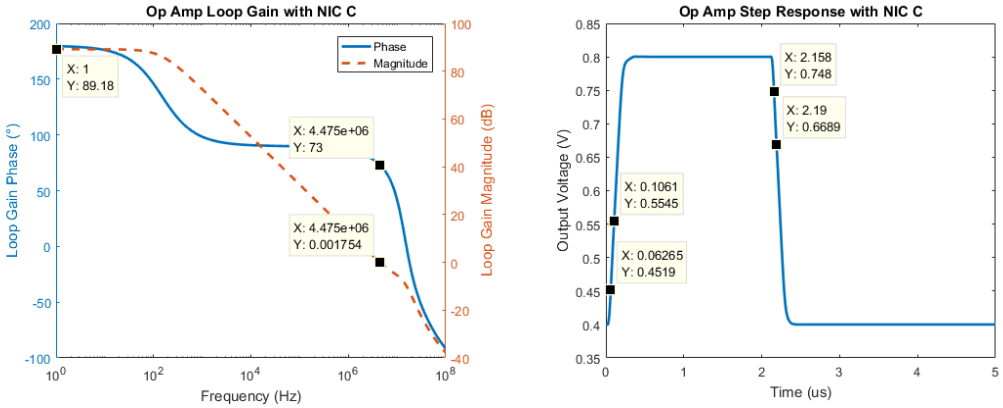


Part B

Next, the NIC was used to decrease the load capacitance of the amplifier from 25pF to 10pF. This requires a 15pF negative capacitor to be generated by the NIC capacitor. This is accomplished by using a capacitor of 10pF and a k value of 1.5. In order to improve the phase margin using this method, the negative capacitance must be effective bandwidth the gain-bandwidth of the op amp. Therefore, we will design the negative capacitor will need to be effective at approximately 8MHz. With a k value of 1.5, this means the gain bandwidth of the op amp used in the NIC must be:

$$GB = 2 \cdot (1 + 1.5) \cdot 8MHz = 40MHz$$

To ensure the effectiveness of the negative capacitance, an op amp was designed with a gain bandwidth of 50MHz. In order to achieve this, the Ahuja compensation method was used. The design of this op-amp can be found in Appendix A. The results of using this negative capacitor to decrease the overall load capacitance can be found below:



As seen in the figure above, the phase margin of the amplifier is now 73 degrees. This is an improvement from the phase margin in the last homework of 65.61 degrees. This phase margin improvement comes as a result of the decreased effective load capacitance at the UGB frequency. The slew rate also improved slightly:

$$SR_+ = \frac{0.5545V - 0.4519V}{0.1061\mu s - 0.06265\mu s} = 2.36V/\mu s$$
$$SR_- = \frac{0.748V - 0.6689V}{2.19\mu s - 2.158\mu s} = 2.47V/\mu s$$

This represents a marked improvement over the slew rate of the amplifier without the negative capacitance which was 2.07V/us for the positive slew rate and 2.11V/us for the negative slew rate. This is again caused by the decrease in the effective load capacitance.

Part C

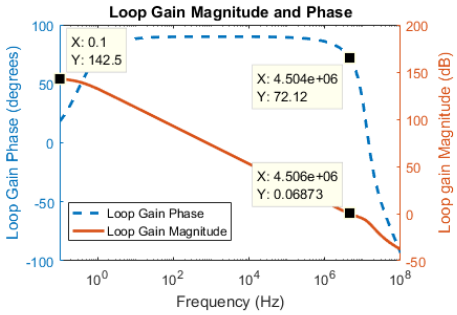
Finally, the two NICs used in the previous two sections were used simultaneously to both increase the gain as well as decrease the load capacitance of the amplifier. These results are shown in the figure below. The DC gain has been increased to 142.5dB which indicates a marked improvement over the original amplifier. In addition to this, the phase margin is increased to approximately 72.12 degrees from 65.61 degrees. The common-mode rejection ratio has improved to 98.73dB. This is approximately

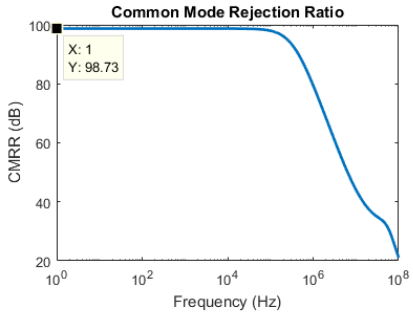
a 13dB improvement from the original case. The low frequency PSRR for the positive supply is 113.2dB while for the negative supply it is 80.27dB. These have both decreased from the original amplifier. The PSRR at 100kHz, on the other hand, remained much the same at 90.52dB for the positive supply and 32.48dB for the negative supply. The positive settling rate is 179.5ns while the negative settling rate is 181.9ns. These settling rates are much slower than in the original amplifier. The slew rate can be calculated as follows:

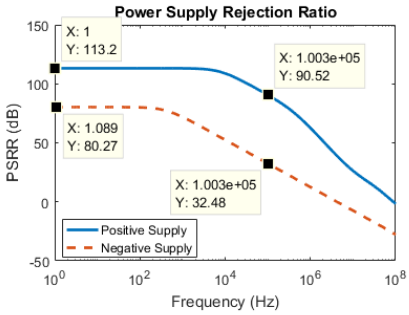
$$SR_+ = \frac{0.592V - 0.4423V}{0.1141\mu s - 0.04891\mu s} = 2.30V/\mu s$$

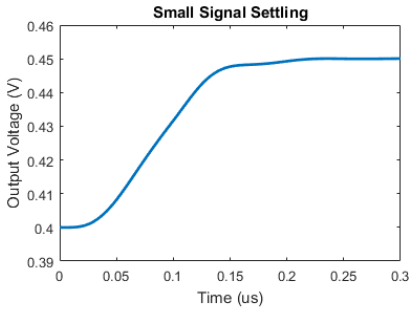
$$SR_- = \frac{0.7515V - 0.6233V}{2.701\mu s - 2.646\mu s} = 2.33V/\mu s$$

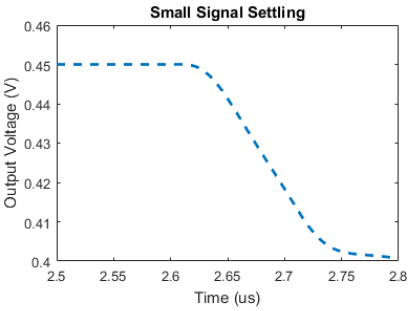
These slew rates indicate an improvement over the original amplifier. The THD of both amplifiers over a wide range of input peak-to-peak voltages was also measured. The amplifiers both indicated very similar THDs over the full range. Therefore, it seems that the NIC does not greatly impact the THD of the amplifier.

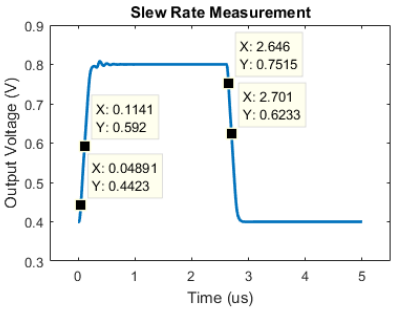


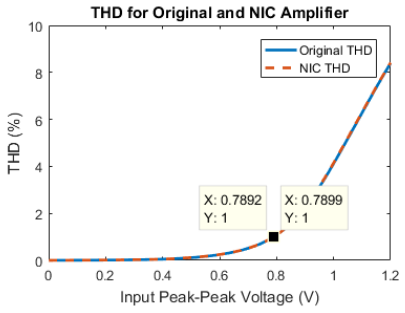




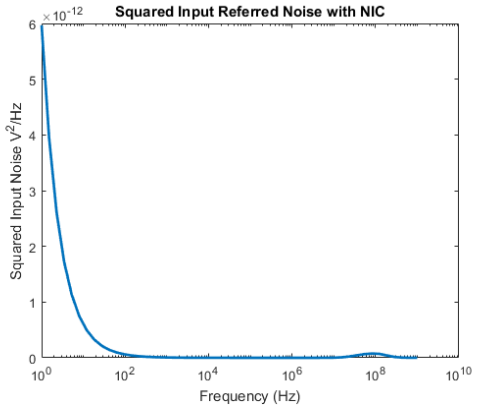


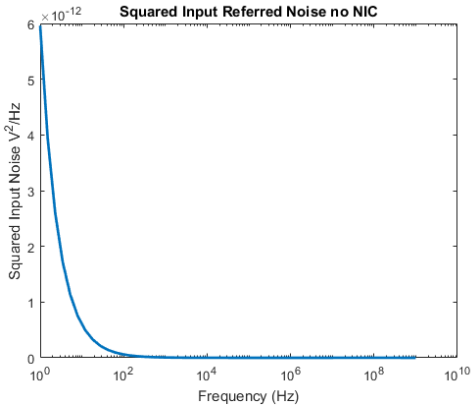






Lastly, the noise of both amplifiers was simulated in unity gain configuration:





For both cases, the noise was integrated from 1Hz to 1GHz. As seen in the input referred noise with the NIC added, there is some high frequency noise around 10MHz due to the negative-impedance capacitor. This adds significant noise when the integrated input-referred noise is calculated, although this noise could be filtered out in later stages. All of the results discussed as well as the results from the previous homework can be found in the table below:

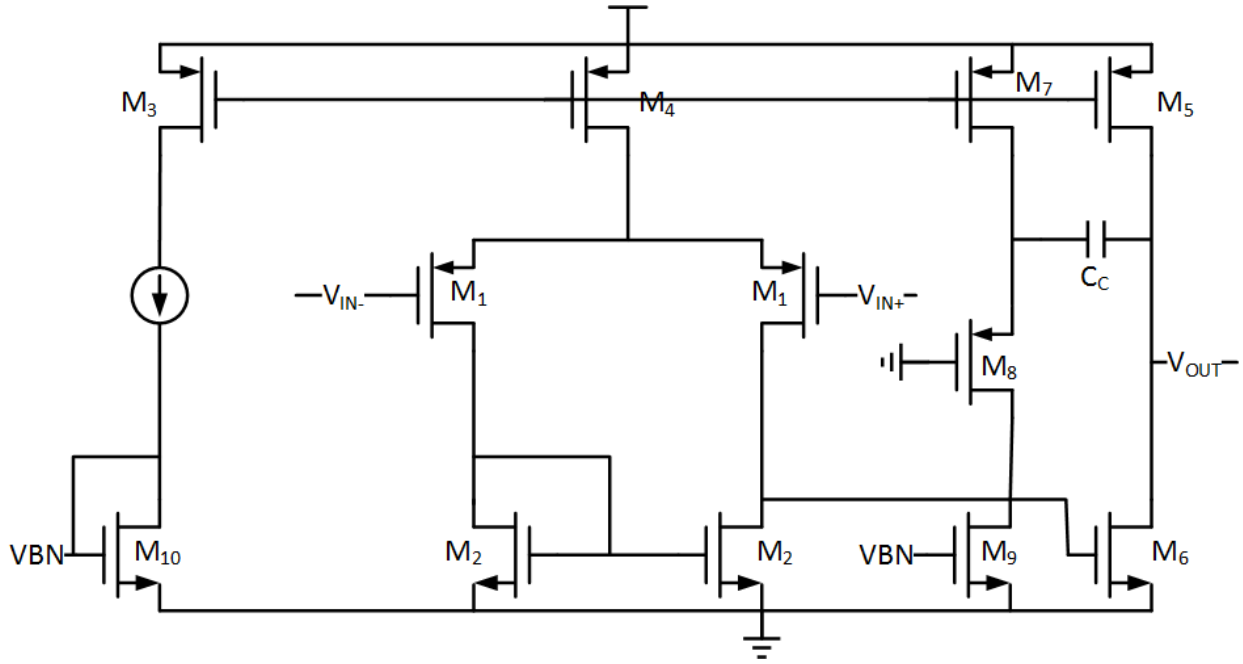
Parameter	HW1 Amplifier	HW1 Amplifier with Resistor and Capacitor NIC	HW1 Amplifier with only Resistor NIC
Gain	89.25 dB	142.5 dB	142.5 dB
DC CMRR	85.48 dB	98.73 dB	98.73 dB
GBW	4.095 MHz	4.506 MHz	4.091 MHz
PM (at C_L=25pF)	65.61°	72.12°	65.42°
Power	193.56 uW	934.44 uW	213.48 uW
$PSRR_+$ at DC	117.2 dB	113.2 dB	113.2 dB
$PSRR_-$ at DC	94.66 dB	80.27 dB	80.27 dB
$PSRR_+$ at 100 kHz	89.84 dB	90.52 dB	90.52 dB
$PSRR_-$ at 100 kHz	32.6 dB	32.48 dB	32.48 dB
1% Settling Time	150.2 ns	181.9 ns	157.1 ns
SR_+	2.07 V/us	2.30 V/us	2.04 V/us
SR_-	2.11 V/us	2.33 V/us	2.08 V/us
Input-Referred Noise	661.3 uV	3.992 mV	664.9 uV
Input Voltage at 1% THD	0.7899 V_{PP}	0.7892 V_{PP}	0.7892 V_{PP}
Active Area	556.8 um^2	1867.2 um^2	1113.6 um^2

As seen in the table above, the amplifier with the resistor and capacitor NIC had far greater DC gain and CMRR than the original amplifier. In addition to this, the negative capacitor increased the gain bandwidth, the phase margin, and the slew rate. Unfortunately, this comes at the cost of PSRR, settling time, and a much larger power consumption and input-referred noise. This tradeoff can be lessened somewhat by only using the resistor NIC. This improves the gain and CMRR while preserving the GBW, PM, settling time, and SR of the amplifier. Only including the resistor NIC also increases the power consumption by only 20 uW while the input referred noise is only increase by 3uV. The PSRR performance with only the resistor NIC, however, is still lower than in the original amplifier. In both cases, the harmonic distortion is much the same so it appears that the NIC does not add a lot of THD.

One major drawback of using the NIC resistor and capacitor is the large increase in the active area of the amplifier.

Appendix A: Capacitor NIC Op Amp Design

Since the capacitor NIC required an op amp with a large gain bandwidth (50MHz), another op amp was designed. This op amp used Ahuja compensation to achieve the large gain bandwidth with good stability and reasonable power consumption. The schematic is shown below:



The value of the compensation capacitor is set to 1pF and the load capacitance is assumed to be 10pF. In addition, the parasitic capacitance at the output of the first stage is assumed to be 500fF. We can then find the required values for g_{m1} and g_{m6} to provide the required GBW and a good phase margin:

$$g_{m1} = GBW \cdot 2\pi \cdot C_C = 50MHz \cdot 2\pi \cdot 1pF = \frac{320\mu A}{V}$$

$$g_{m6} = \frac{C_P(C_C + C_L)}{C_C} \cdot 3GBW = \frac{500fF(10pF + 1pF)}{1pF} \cdot 3 \cdot 2\pi \cdot 50MHz = 5.2mA/V$$

The current in the first stage is chosen to be 40uA while the current in the second stage is chosen to be 500uA to achieve the required g_m. The current through the Ahuja compensation network is chosen to be 50uA to ensure it does not limit the slew rate of the amplifier. This produces the following transistor sizes and currents:

Transistor	Calculated Size	Bias Current
M_1	$\frac{38\mu m}{520nm}$	$20\mu A$
M_2	$\frac{2\mu m}{520nm}$	$20\mu A$
M_3	$\frac{40\mu m}{1\mu m}$	$10\mu A$

M_4	$\frac{10\mu m}{1\mu m}$	$40\mu A$
M_5	$\frac{500\mu m}{1\mu m}$	$500\mu A$
M_6	$\frac{100\mu m}{520nm}$	$500\mu A$
M_7	$\frac{50\mu m}{1\mu m}$	$50\mu A$
M_8	$\frac{90\mu m}{520nm}$	$50\mu A$
M_9	$\frac{50\mu m}{1\mu m}$	$50\mu A$
M_{10}	$\frac{10\mu m}{1\mu m}$	$10\mu A$

The amplifier produces the following parameters:

Parameter	Value
GBW	50.8 MHz
PM	75.13 °
Power Consumption	726.8 uW
SR_+	25.15 V/us
SR_-	38.56 V/us
DC Gain	81.07 dB

It was found that these specifications were sufficient to decrease the load capacitance of a 4MHz GBW amplifier by 15pF.