HW 1

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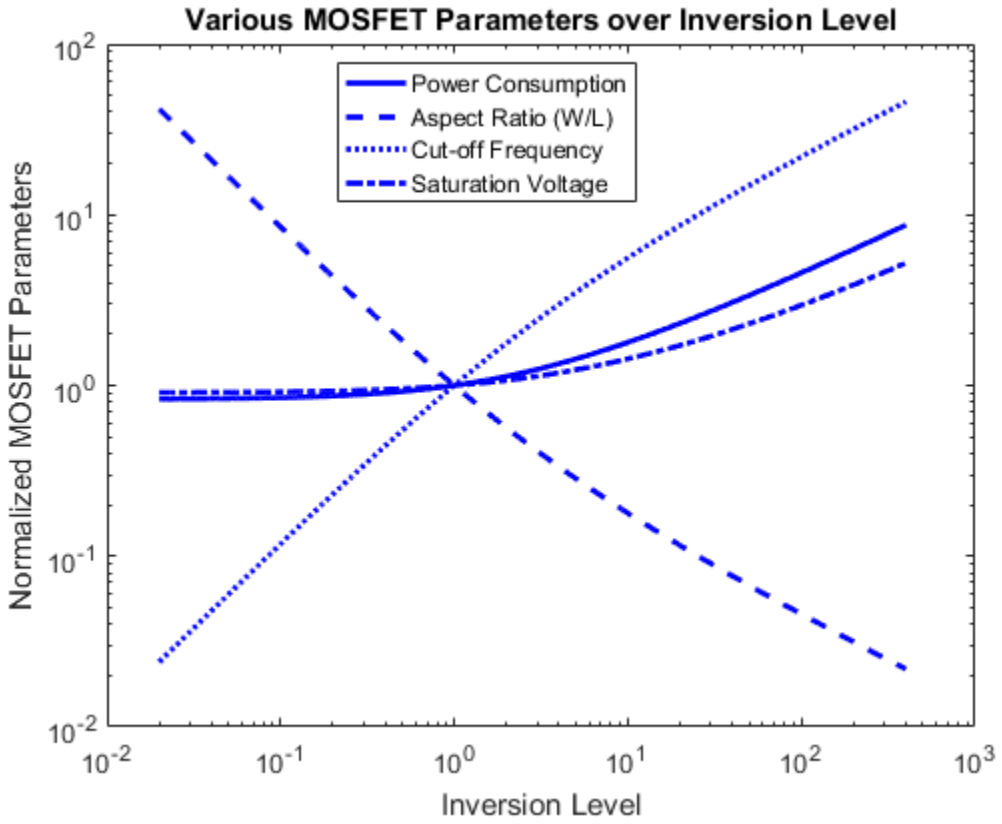
Problem 1

This problem involves graphing various MOSFET parameters, namely the power consumption, the transit frequency (f_t), the aspect ratio (W/L), and the saturation voltage (V_{DSAT}) across a wide range of inversion levels. For this graph, the ACM parameters from the predictive 130nm process from ASU were used to generate the graph, although the normalization makes the tradeoffs shown in the graph applicable for design in any process. The graph is shown in the figure below:



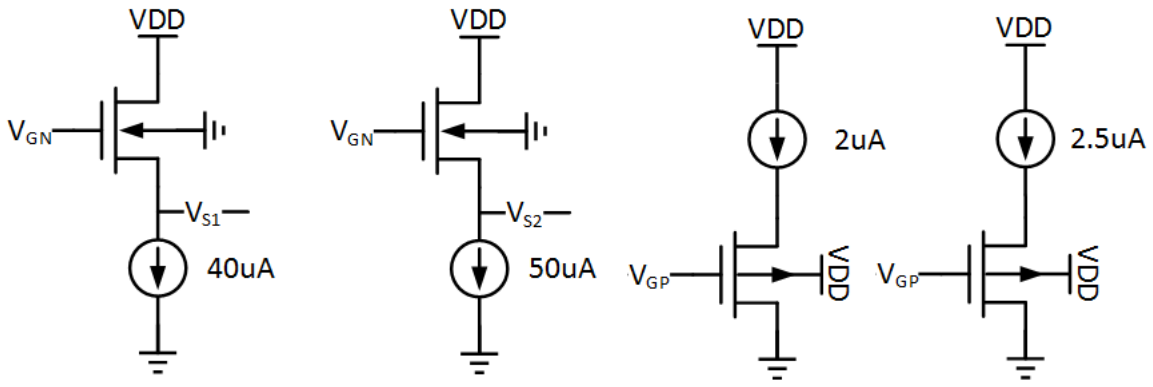
This graph indicates several important tradeoffs that must be considered when choosing the inversion level for a particular transistor. As the inversion level increases, the power consumption and saturation voltage increase but the aspect ratio (and therefore active area of the transistor) decreases and the cut-off frequency increases. Therefore, for designs where area or frequency response are the primary concerns, a large inversion level should be chosen. For moderate or weak inversion levels, the power consumption is decreased and the saturation voltage also decreases. This means that parameters like the output swing or input common mode range can be improved at lower inversion levels. In addition to this, designers are required to push the power consumption of designs lower than ever before. Designing in moderate inversion provides an attractive option for lowering the power consumption as long as high frequency operation is not required and area is not a major limitation. Again, these tradeoffs can be easily seen in the graph above.

Problem 2

This problem involved the measurement of several parameters in the 130nm and 65nm predictive processes from ASU required for the ACM equations.

Normalization Current:

The first parameters that is measured is the normalization current. This parameter is measured with the schematic below:



According to the ACM model, the normalization current can be found for this particular transistor size as follows:

$$I_S = I\left(\frac{\frac{\Delta I}{I}}{\frac{2\Delta V_s}{\phi_t}}\right)^2$$

The normalization current for any transistor size can be found by dividing the above expression by the tested transistor size and then multiplying by the actual transistor size used in design. For the NMOS parameter extraction, $I = 40\mu A, \Delta I = 10\mu A$:

$$I_{S,NMOS} = 50\mu A * \left(\frac{\frac{10\mu A}{50\mu A}}{\frac{2(9.568mV - 3.525mV)}{.026V}}\right)^2 = 2.465\mu A$$

For the PMOS parameter extraction, $I = 2\mu A, \Delta I = 0.5\mu A$

$$I_{S,PMOS} = 2\mu A * \left(\frac{\frac{.5\mu A}{2\mu A}}{\frac{2(1.129V - 1.121V)}{.026V}}\right)^2 = 208.24nA$$

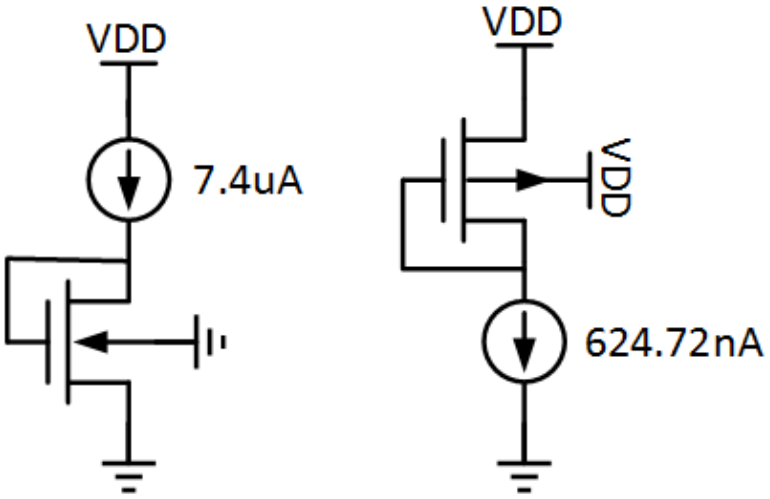
These can both be divided by the aspect ratio of the transistor used (8) to find the process-dependent part of I_S:

$$I_{SN} = \frac{2.465\mu A}{8} = 308.1nA$$

$$I_{SP} = \frac{208.24nA}{8} = 26.03nA$$

Threshold Voltage:

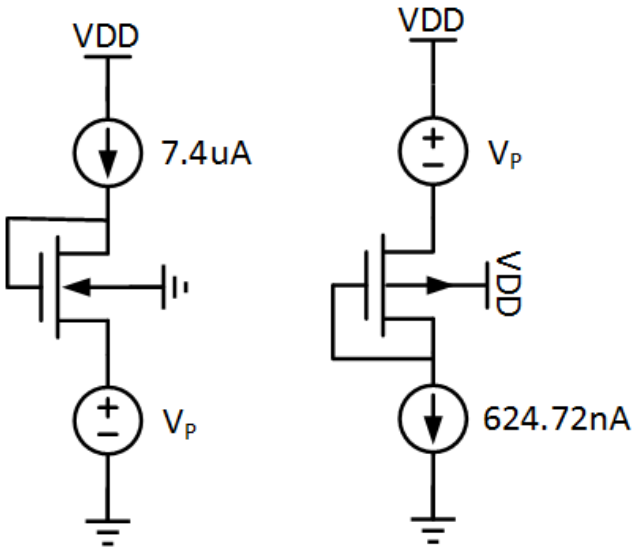
Next, the ACM model specifies that if V_{SB}=0, then V_{GS} when I_D=3I_S is the same as V_{T0}. Therefore, we use the following circuit and measure V_{GS} to determine the threshold voltage:



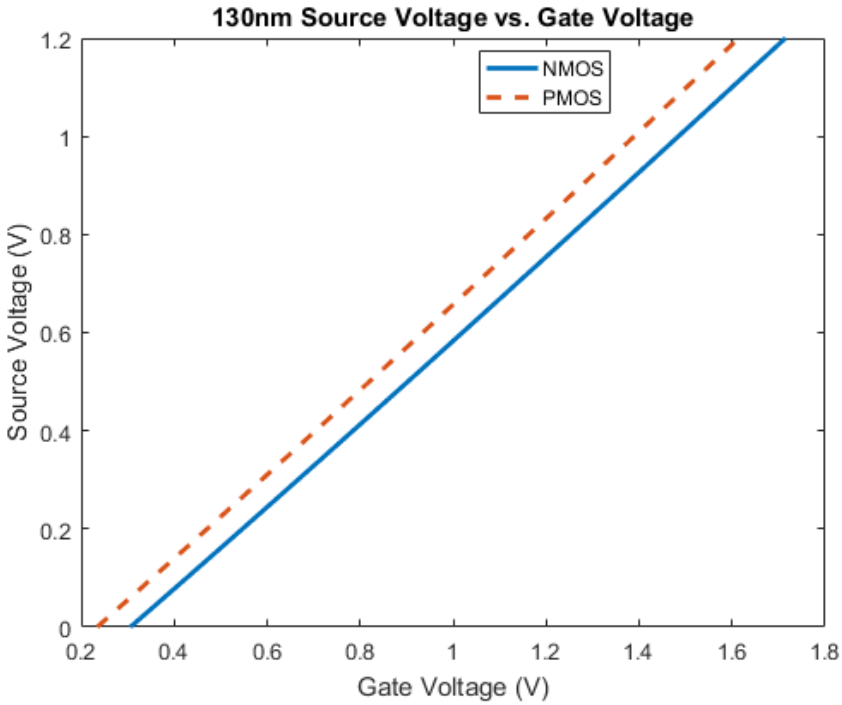
The threshold voltage for the 130nm is found to be 305.8mV for NMOS transistors while the threshold voltage for PMOS transistors is found to be -234.5mV.

Slope Factor:

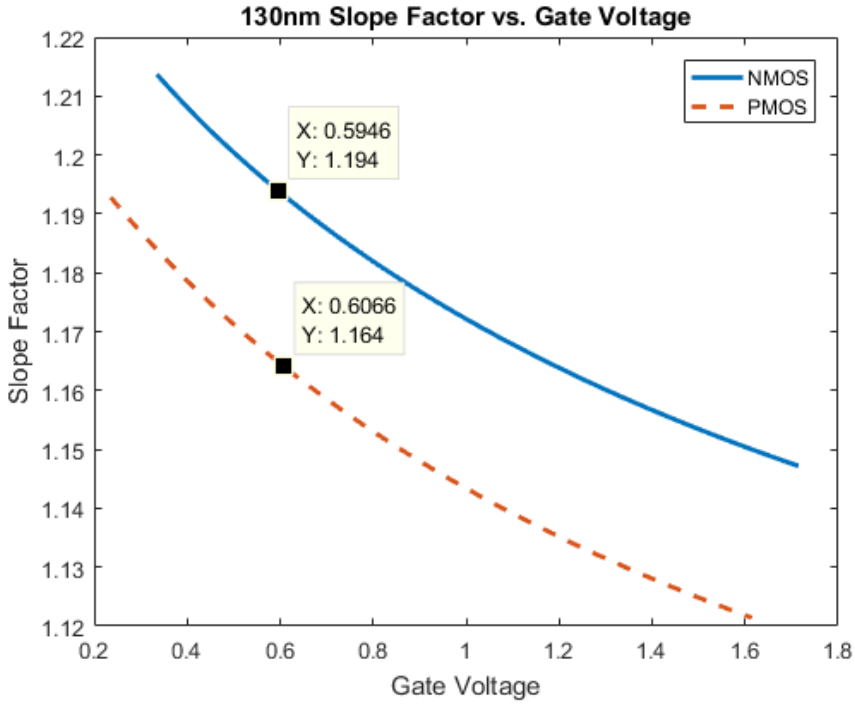
Next, the slope factor required in the ACM equations, as well as the value of the parameter γ, can be found using a circuit similar to the one above, but the source voltage of the transistor is swept while the bulk voltage is kept constant. This produces a varying gate voltage since the effective threshold voltage of the transistor is being changed as the source-bulk voltage changes. This schematic can be found in the figure below:



The result of this sweep is found in the graph below:



As expected, when the source voltage increases the gate voltage increases since an increase in the source voltage leads to an increase in the effective threshold voltage for the transistor. The slope factor can be found by taking the derivative of the gate voltage with respect to the source voltage. This is found in the figure below:



The nominal slope factor is taken at a gate voltage of 600mV. This means the slope factor is 1.194 for the NMOS transistors and 1.164 for the PMOS transistors. The slope factor can then be used to find the value of γ for this process according to the ACM model:

$$\gamma = (n-1)2\sqrt{2\phi_F + V_P}$$

$$\gamma_N = (1.194-1)2\sqrt{2 * .026V + .24V} = 0.210\, V^{\frac{1}{2}}$$

$$\gamma_P = (1.164-1)2\sqrt{2 * .026V + .316V} = 0.200\, V^{\frac{1}{2}}$$

Mobility:

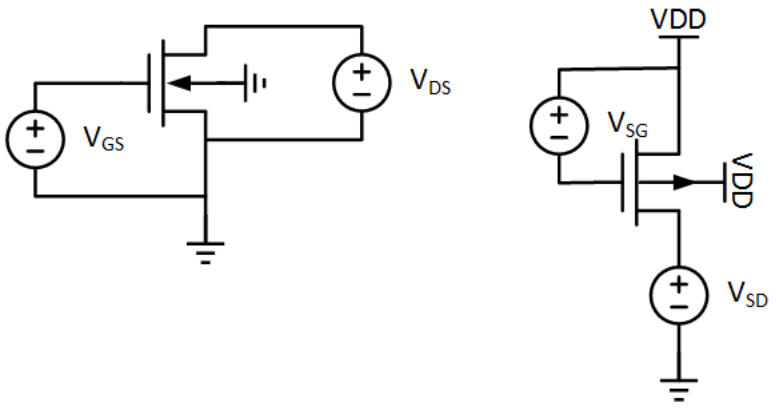
Lastly, the electron and hole mobility must be extracted for the ACM model. According to the ACM model, in the strong inversion, linear region:

$$\frac{1}{\frac{\mu C_{ox} W}{L}} = \frac{(V_G - V_{T0})(V_{DS})}{I_D}$$

And:

$$\mu = \frac{\mu_0}{1 + \theta(V_G - V_{T0})}$$

Therefore, if we plot $\frac{(V_G - V_{T0})(V_{DS})}{I_D}$ versus $(V_G - V_{T0})$, then the y-intercept allows us to determine μ_0 while the slope allows us to determine θ. Therefore, we sweep V_{GS} with a set V_D and measure I_D using the following schematic where V_{DS}=150mV and V_{SD}=950mV:



The results of the gate voltage sweep can be found in the figures below. The results for both the NMOS and PMOS transistors are fitted with a linear approximation and the slope and y-intercept of this linear approximation are used to find the θ and μ_0 values respectively. It should be noted that only large gate-source voltages are used to ensure the transistor is in the linear region when the curve fitting is done. The y-intercept for the NMOS transistor is $140.887\, V^2/A$ while for the PMOS it is $975.89\, V^2/A$. We can find μ_0 using the value for C_{OX} found from the model card for this process:

$$\mu_0 = \frac{1}{\left(\frac{W}{L}\right) C_{OX} B}$$

$$\mu_N = \frac{1}{8 * \frac{1.534 * 10^{-6}F}{cm^2} * \frac{140.887V^2}{A}} = \frac{578.38cm^2}{Vs}$$

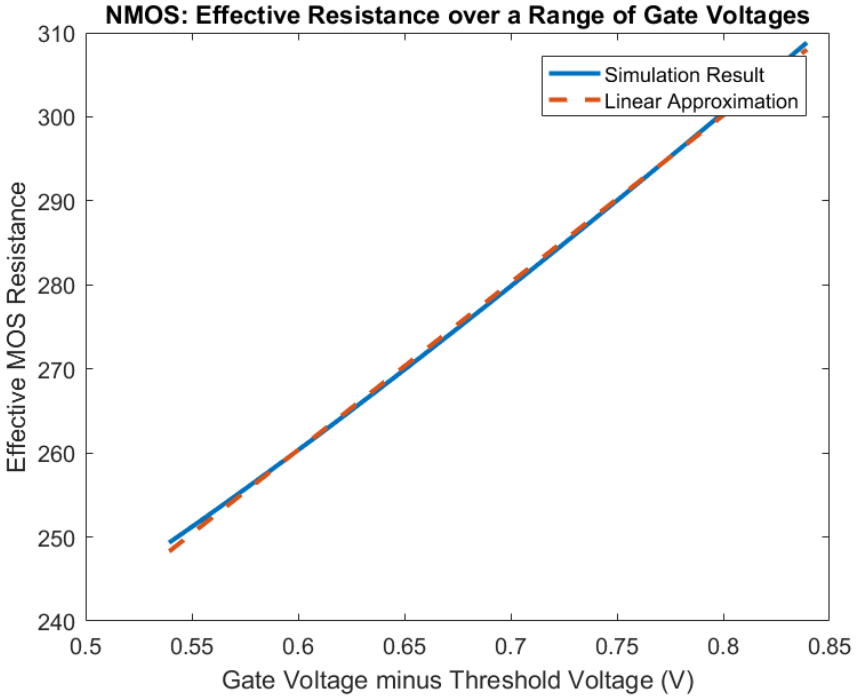
$$\mu_P = \frac{1}{8 * \frac{1.4687 * 10^{-6}F}{cm^2} * \frac{975.89V^2}{A}} = \frac{87.21cm^2}{Vs}$$

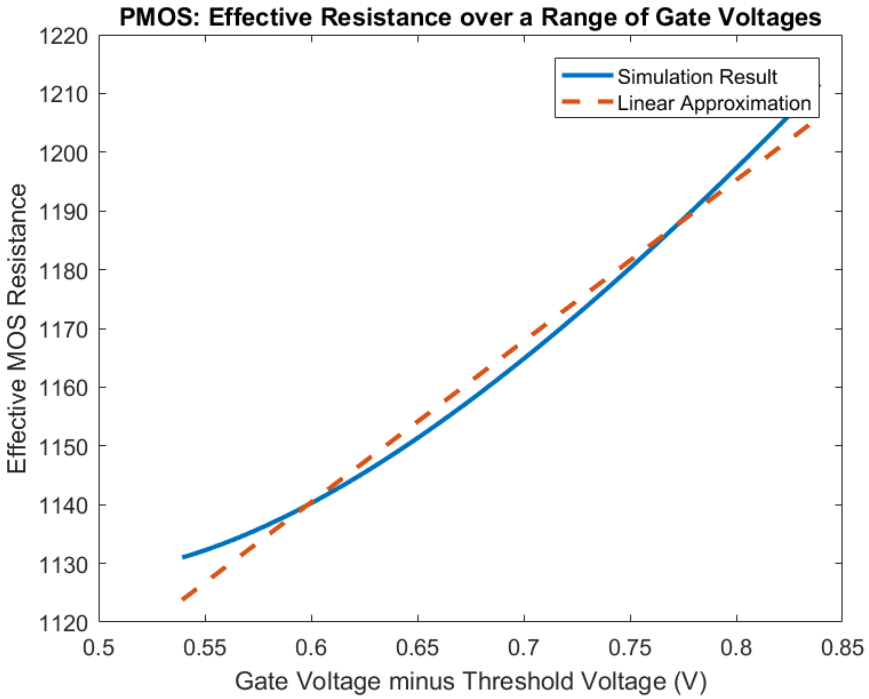
Next, the value for θ can be found from the slopes of $199.1237V/A$ and $274.2086V/A$ for the NMOS and PMOS transistors, respectively:

$$\theta = \mu_0 C_{Ox} \left(\frac{W}{L}\right)$$

$$\theta_N = \frac{578.38cm^2}{Vs} * 1.534 * \frac{10^{-6}F}{cm^2} * \frac{199.1237V}{A} = 0.177V^{-1}$$

$$\theta_P = \frac{87.32cm^2}{Vs} * 1.4687 * \frac{10^{-6}F}{cm^2} * \frac{274.2086V}{A} = 0.0351V^{-1}$$





This procedure was repeated for the 65nm predictive technology from ASU. Any graphs and equations needed for the 65nm parameters are found below.

Normalization Current:

For the following equations: (W/L)=15.385. For the NMOS, $I = 40\mu A, \Delta I = 10\mu A$ and for the PMOS, $I = 2\mu A, \Delta I = 0.5\mu A$.

$$I_{S,NMOS} = 40\mu A\left(\frac{\frac{10\mu A}{40\mu A}}{\frac{2(54.21mV - 42.84mV)}{.026V}}\right)^2 = 3.268\mu A$$

$$I_{S,PMOS} = 2\mu A\left(\frac{\frac{.5\mu A}{2\mu A}}{\frac{2(829.9mV - 821.9mV)}{.026V}}\right)^2 = 330.078nA$$

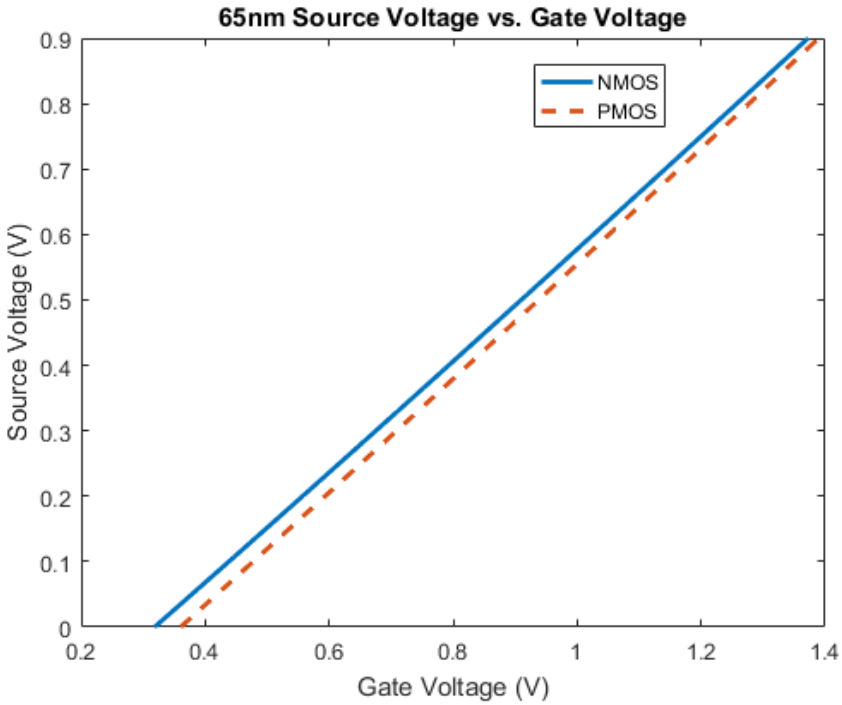
$$I_{SN} = \frac{3.268\mu A}{15.385} = 212.4nA$$

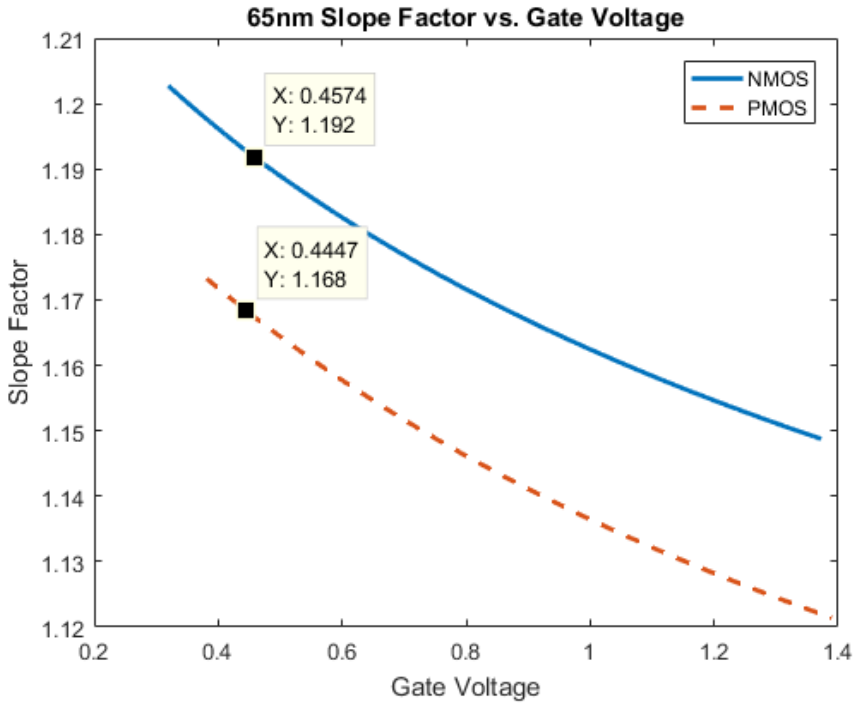
$$I_{SP} = \frac{330.078nA}{15.385} = 21.455nA$$

Threshold Voltage:

$$V_{TH0N} = 318.5mV$$
$$V_{TH0P} = -260.9mV$$

Slope Factor:

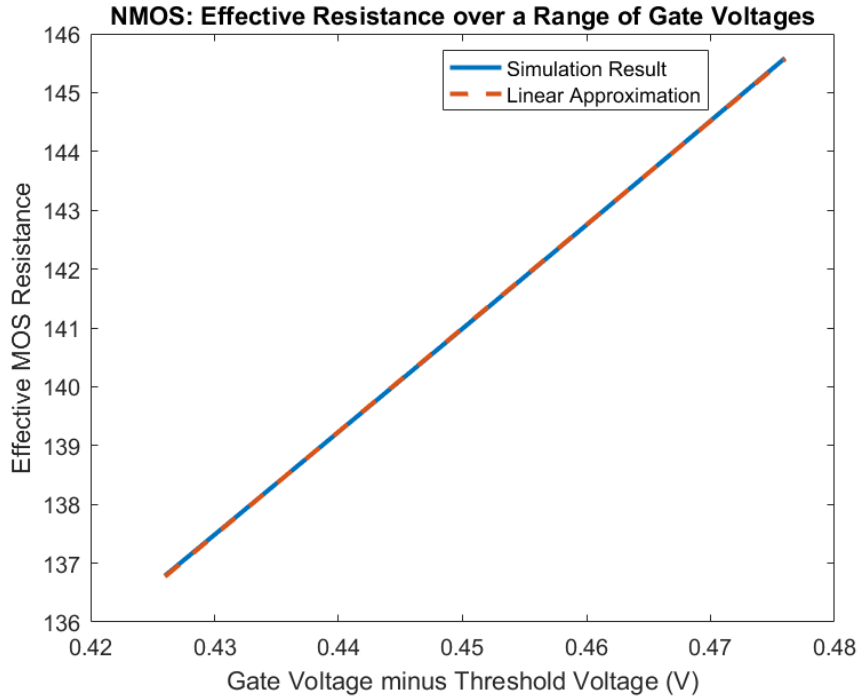


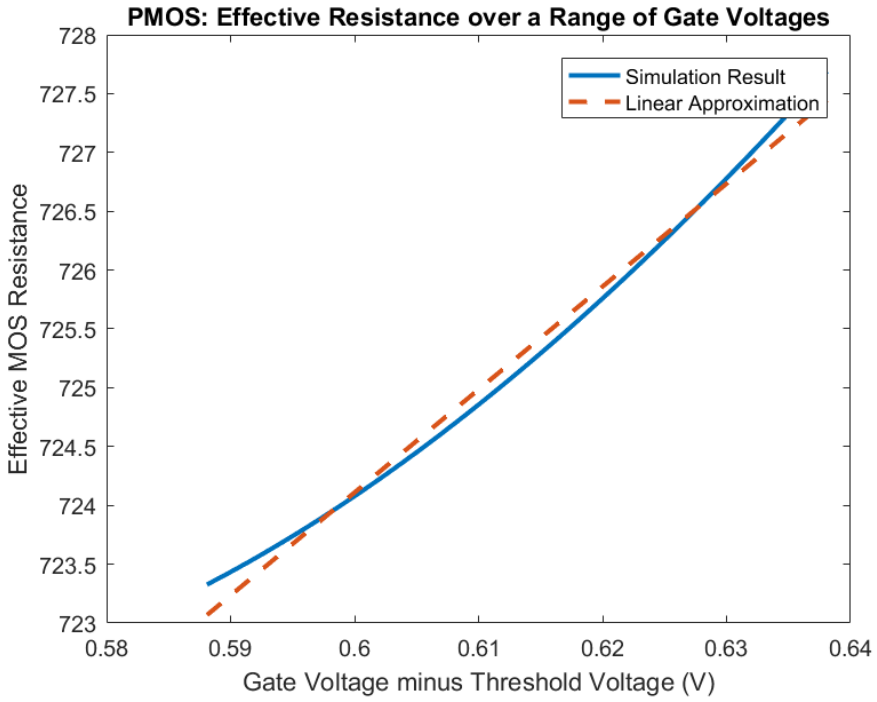


$$\gamma_N = (1.192 - 1)2\sqrt{2 * .026V + 0.112V} = 0.156\, V^{\frac{1}{2}}$$

$$\gamma_P = (1.168 - 1)2\sqrt{2 * .026V + 0.072V} = 0.118\, V^{\frac{1}{2}}$$

Mobility:





From the linear regression, we can find the following parameters:

$$m_N = 176.0029V/A$$

$$m_P = 87.5165V/A$$

$$b_N = 61.7948V^2/A$$

$$b_P = 671.5997V^2/A$$

$$\mu_{0N} = \frac{1}{15.835 * \frac{1.866\mu F}{cm^2} * \frac{61.7948V^2}{A}} = \frac{547.76cm^2}{Vs}$$

$$\mu_{0P} = \frac{1}{15.835 * \frac{1.77\mu F}{cm^2} * \frac{671.5997V^2}{A}} = \frac{53.125cm^2}{Vs}$$

$$\theta_N = \frac{547.76cm^2}{Vs} * \frac{1.866\mu F}{cm^2} * \frac{176.0029V}{A} = 0.180V^{-1}$$

$$\theta_P = \frac{53.125cm^2}{Vs} * \frac{1.77\mu F}{cm^2} * \frac{87.5165V}{A} = 0.0823V^{-1}$$

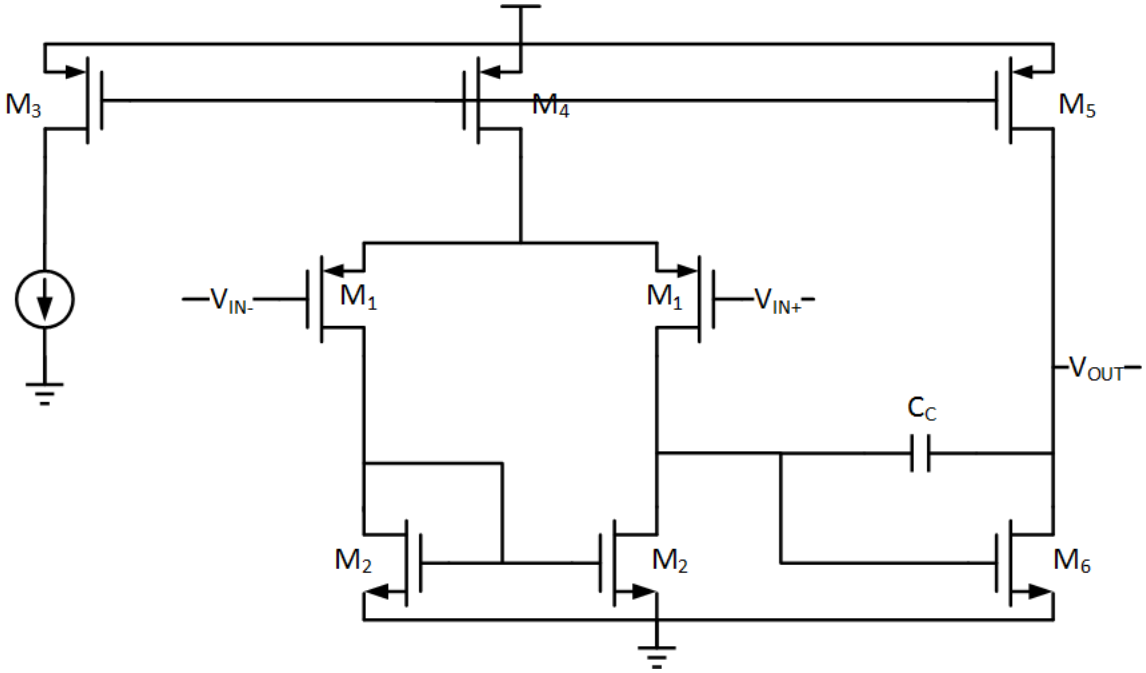
The results from both processes are found in the following table. There are several interesting features to note. Firstly, the normalization current for the PMOS transistors for both processes is about 10 times lower than for the NMOS. This is due to the greatly decreased mobility of holes in silicon when compared with electrons. Another interesting note is that the threshold voltage remained much the same when moving from 130nm technology to 65nm technology, however the supply voltage decreased from 1.2V to 0.9V. This illustrates the headroom problem with advanced CMOS technologies. The slope factor remained relatively constant across both processes but was slightly smaller for the PMOS transistors. The gamma value decreased somewhat when moving from the 130nm process to the 65nm process, which indicates that the body effect does not impact circuit performance as much. The values for mobility remained much the same across the processes but were very clearly larger for the NMOS transistors. Lastly, the mobility degradation constant, θ, remained mostly the same across the two processes, but was much smaller for the PMOS transistors. This indicates that mobility degradation plays a much larger role in the performance of NMOS transistors.

Parameter	130nm NMOS	130nm PMOS	65nm NMOS	65nm PMOS
I_S	308.1nA	26.03nA	212.4nA	21.455nA
V_{THO}	305.8mV	-234.5mV	318.5mV	-260.9mV
n	1.194	1.164	1.192	1.168
γ	$0.21V^{\frac{1}{2}}$	$0.2V^{\frac{1}{2}}$	$0.156V^{\frac{1}{2}}$	$0.118V^{\frac{1}{2}}$
μ_0	$578.38\frac{cm^2}{Vs}$	$87.21\frac{cm^2}{Vs}$	$547.76\frac{cm^2}{Vs}$	$53.125\frac{cm^2}{Vs}$
θ	$0.177V^{-1}$	$0.0351V^{-1}$	$0.18V^{-1}$	$0.0823V^{-1}$

Problem 3

Design:

For this problem, we will use the simple 2-stage operational amplifier that is found in the schematic below:



Firstly, we set C_C to half the load capacitance which is 12.5pF. Next, we determine the necessary ratio between g_{m1} and g_{m6} for a phase margin of 65 degrees:

$$PM = 90° - \tan^{-1}\left(\frac{C_L}{C_C} * \frac{g_{m1}}{g_{m6}}\right) - \tan^{-1}\left(\frac{g_{m1}}{g_{m6}}\right) \rightarrow 65° = 90° - \tan^{-1}\left(\frac{2g_{m1}}{g_{m6}}\right) - \tan^{-1}\left(\frac{g_{m1}}{g_{m6}}\right)$$

$$\frac{g_{m1}}{g_{m6}} < \frac{1}{6.73} \rightarrow \frac{g_{m1}}{g_{m6}} = 8$$

Next, we find the required value for g_{M1} to provide the required gain bandwidth:

$$GBW = \frac{g_{m1}}{C_C} \rightarrow g_{m1} > 5MHz * 2 * \pi * 12.5pF = \frac{392.7\mu A}{V} \rightarrow g_{m1} = 400\mu A/V$$

This, in turn provides the required value for g_{m6}:

$$g_{m6} = 8g_{m1} = 3.2mA/V$$

To remain within the power specification, the total bias current must be:

$$1.2V * I < 500\mu W \rightarrow I < 416.67\mu A$$

Therefore, we choose a bias current of $20\mu A$ through M_3, a current of $70\mu A$ through M_4, and a current of $320\mu A$ through M_5. For all biasing transistors, we choose a length of $1\mu m$ to provide good common-mode rejection ratio. For M_3 we choose a width of $10\mu m$ to provide a reasonable V_{DSAT}, which will allow a good ICMR and output swing. Therefore:

$$\left(\frac{W}{L}\right)_3 = \frac{10\mu m}{1\mu m}, \left(\frac{W}{L}\right)_4 = \frac{35\mu m}{1\mu m}, \left(\frac{W}{L}\right)_5 = \frac{160\mu m}{1\mu m}$$

For M_1 we use the traditional square law equation to find the required aspect ratio. In addition, we set the length of all other transistors to 520nm to achieve the gain specification.

$$\frac{W}{L} = \frac{g_m^2}{2\mu_n C_{ox} I_D} = \frac{\left(\frac{400\mu A}{V}\right)^2}{2 * \frac{85\mu A}{V^2} * 35\mu A} = 26.9 \rightarrow \left(\frac{W}{L}\right)_1 = \frac{14\mu m}{520nm}$$

Next, we find the required size for M_6:

$$\frac{W}{L} = \frac{\left(\frac{3.2mA}{V}\right)^2}{2 * \frac{710\mu A}{V^2} * 320\mu A} = 22.535 \rightarrow \left(\frac{W}{L}\right)_6 = \frac{12\mu m}{520nm}$$

Lastly, we size M_2 to ensure the systematic offset is as low as possible:

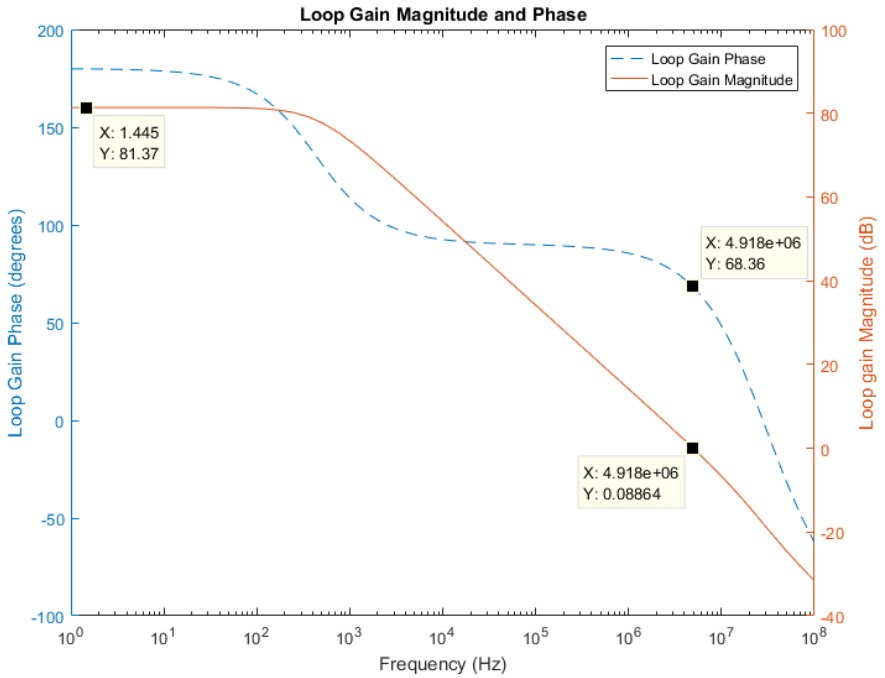
$$\frac{W}{L}_2 = \frac{W}{L_6}\left(\frac{35\mu A}{320\mu A}\right) = 22.535\left(\frac{35\mu A}{320\mu A}\right) = 2.465 \rightarrow \left(\frac{W}{L}\right)_2 = \frac{1.3\mu m}{520nm}$$

Since the square law equation is quite inaccurate, especially as the transistor region of operation approaches moderate inversion, the transistor sizes had to be adjusted slightly to achieve the desired transconductances. A table with the calculated and final transistor sizes can be found below:

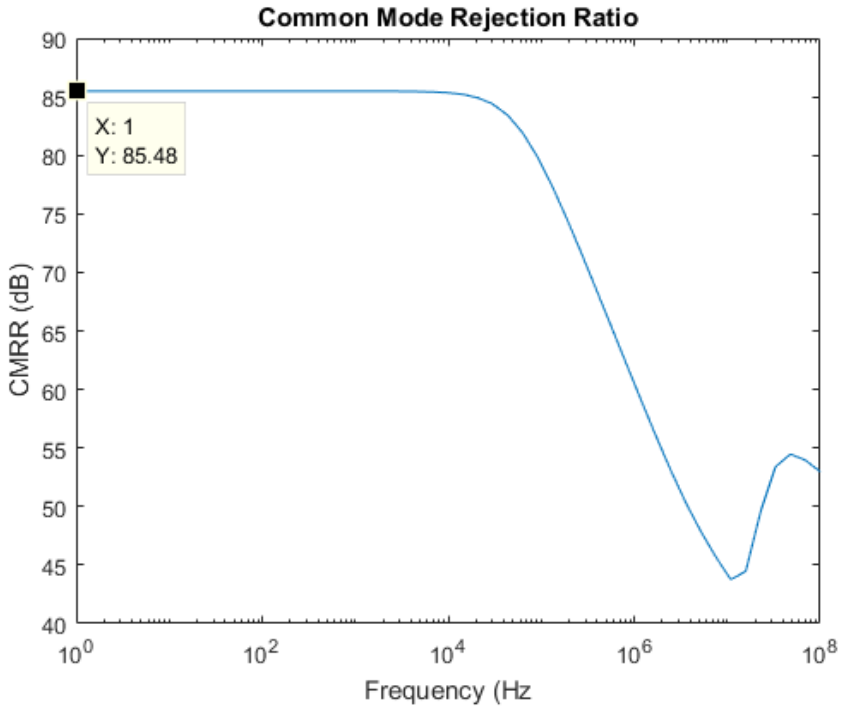
Transistor	Calculated Size	Final Size
M_1	$\frac{14\mu m}{520nm}$	$\frac{20\mu m}{520nm}$
M_2	$\frac{1.3\mu m}{520nm}$	$\frac{1.75\mu m}{520nm}$
M_3	$\frac{10\mu m}{1\mu m}$	$\frac{10\mu m}{1\mu m}$
M_4	$\frac{35\mu m}{1\mu m}$	$\frac{35\mu m}{1\mu m}$
M_5	$\frac{160\mu m}{1\mu m}$	$\frac{160\mu m}{1\mu m}$
M_6	$\frac{12\mu m}{520nm}$	$\frac{16\mu m}{520nm}$

Simulation Results

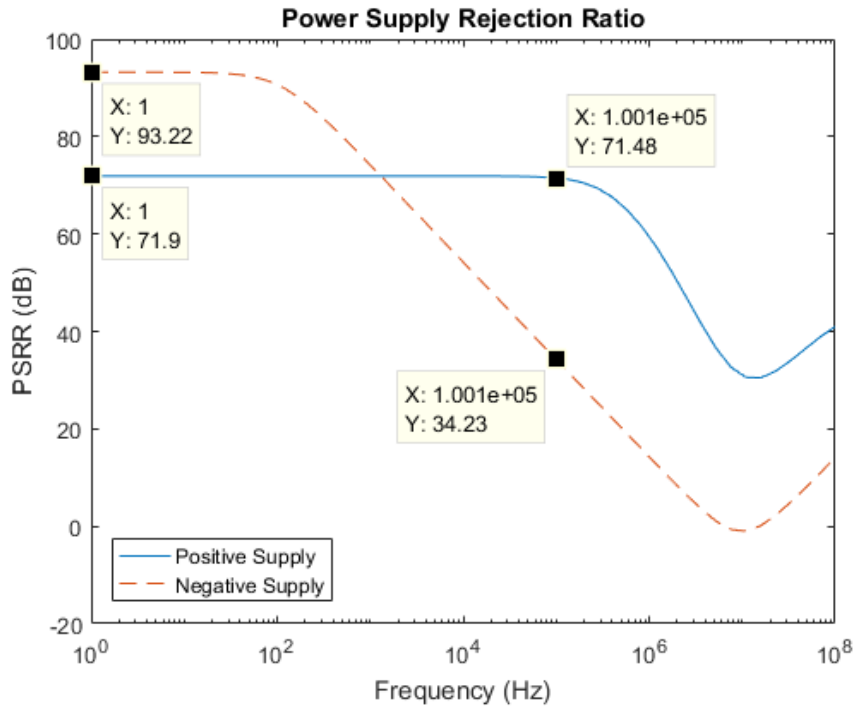
The figure below shows the loop gain of the op amp in unity-gain configuration with al oad capacitance of 25pF. The low-frequency gain is 81.37dB, which is far greater than the 50dB required in the specification. In addition to this, the UGB frequency is 4.918MHz, which is above the given specification of 4MHz. Lastly, the simulated phase margin is 68.36 degrees which should provide good stability at a load capacitance of 25pF.



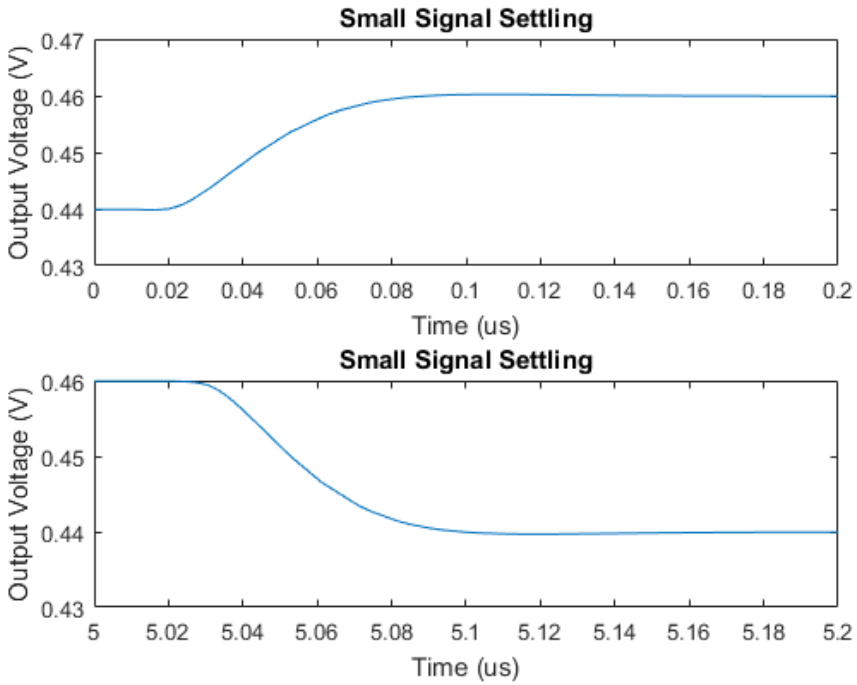
The next graph shows the common-mode rejection ratio of the amplifier. The DC CMRR is 85.48dB which is well above the required specification of 55dB.



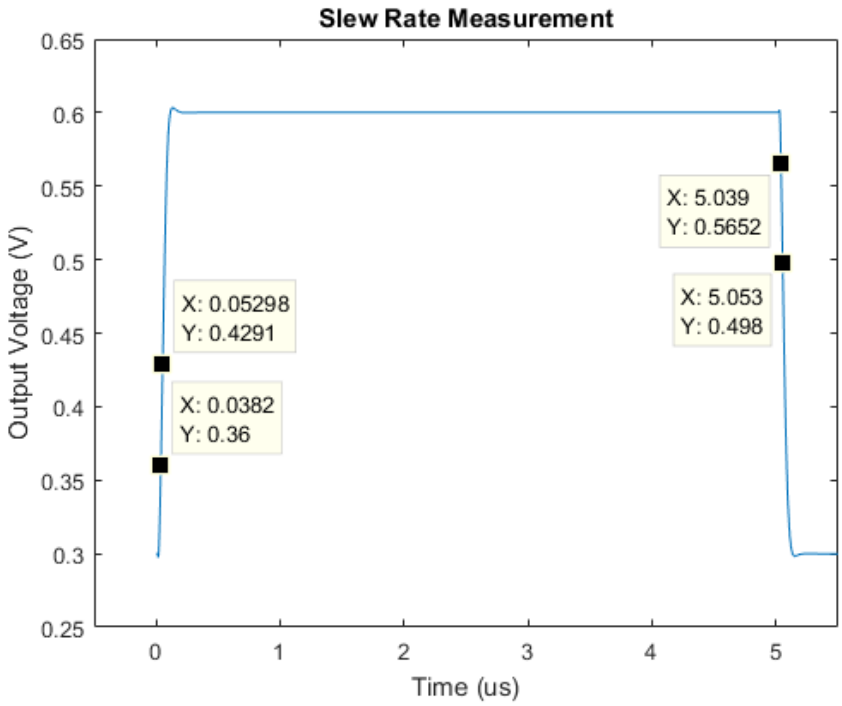
The next graph shows the power supply rejection ratio. This graph marks two points along both PSRR curves: the DC PSRR and the PSRR at 100Hz. For the positive supply, the PSRR at both DC and 100Hz is -71.9dB. For the negative supply, the PSRR at DC is -93.22dB while the PSRR at 100Hz is -90.61dB.



The next graph shows the output of the amplifier for a small positive and negative step. This is used to measure the small signal 1% settling time. The rising settling time is measured to be 116.9ns while the falling time is measured to be 114.2ns.



The final graph shows the output of the amplifier for large positive and negative step that drives the amplifier into slew rate limiting. This graph is used to measure the positive and negative slew rates of the amplifier.



The slew rates can be computed as follows:

$$SR_+ = \frac{0.4291V - 0.36V}{0.05298\mu s - 0.0382\mu s} = 4.675V/\mu s$$

$$SR_- = \frac{0.5652V - 0.498V}{5.053\mu s - 5.039\mu s} = 4.8V/\mu s$$

ACM Design:

To reduce the power consumption of the op-amp, the ACM model was utilized to place many of the transistors in the moderate inversion region. This is accomplished by using the ACM equations with i_f=1. This places the transistors in moderate inversion where a smaller current can be used to achieve the same transconductance. Of course, as found in problem 1, this will decrease the f_t of these transistors as well as increase the active area. We can find the f_T of the transistors with a length of 520nm:

$$f_{TN} = \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1 + i_f} - 1\right) = \frac{\frac{578.38cm^2}{Vs} * .026V}{2\pi * 520nm^2} * 2 * \left(\sqrt{1+1} - 1\right) = 733.25MHz$$

$$f_{TP} = \frac{\frac{87.21cm^2}{Vs} * .026}{2\pi 520nm^2} * 2 * \left(\sqrt{1+1} - 1\right) = 72.53MHz$$

We find that for a GBW of 5MHz, the f_T of the transistors is much higher, so the small inversion level should not greatly affect the frequency response of the amplifier. We will use the same compensation capacitor C_C and the same transconductance for g_{m1} and g_{m6}, but we will adjust the bias current sources and transistor sizes to provide the desired inversion level.

For g_{m1}:

$$I_1 = \frac{1+\sqrt{1+i_f}}{2}(\phi_t g_m n) = \frac{1+\sqrt{1+1}}{2}\left(.026V * \frac{400\mu A}{V} * 1.164\right) = 15\mu A$$

$$\frac{W}{L_1} = \frac{g_m}{\mu C_{ox}\phi_t} * \frac{1}{\sqrt{1+i_f}-1} = \frac{\frac{400\mu A}{V}}{\frac{85\mu A}{V^2} * .026V} * \frac{1}{\sqrt{1+1}-1} = 436.96 \rightarrow \left(\frac{W}{L}\right)_1 = \frac{230\mu m}{520nm}$$

For g_{m6}:

$$I_6 = \frac{1+\sqrt{1+1}}{2}\left(.026V * \frac{3.2mA}{V} * 1.194\right) = 120\mu A$$

$$\frac{W}{L_6} = \frac{\frac{3.2mA}{V}}{\frac{710\mu A}{V^2} * .026V} * \frac{1}{\sqrt{1+1}-1} = 418.5 \rightarrow \left(\frac{W}{L}\right)_1 = \frac{220\mu m}{520nm}$$

For M_2:

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1 * \frac{15\mu A}{120\mu A} = \frac{27.5\mu m}{520nm}$$

We reduce the bias current to 10uA, so:

$$\left(\frac{W}{L}\right)_4 = 3 * \left(\frac{W}{L}\right)_3 = \frac{30\mu m}{1\mu m}$$

$$\left(\frac{W}{L}\right)_5 = 12 * \left(\frac{W}{L}\right)_3 = \frac{120\mu m}{1\mu m}$$

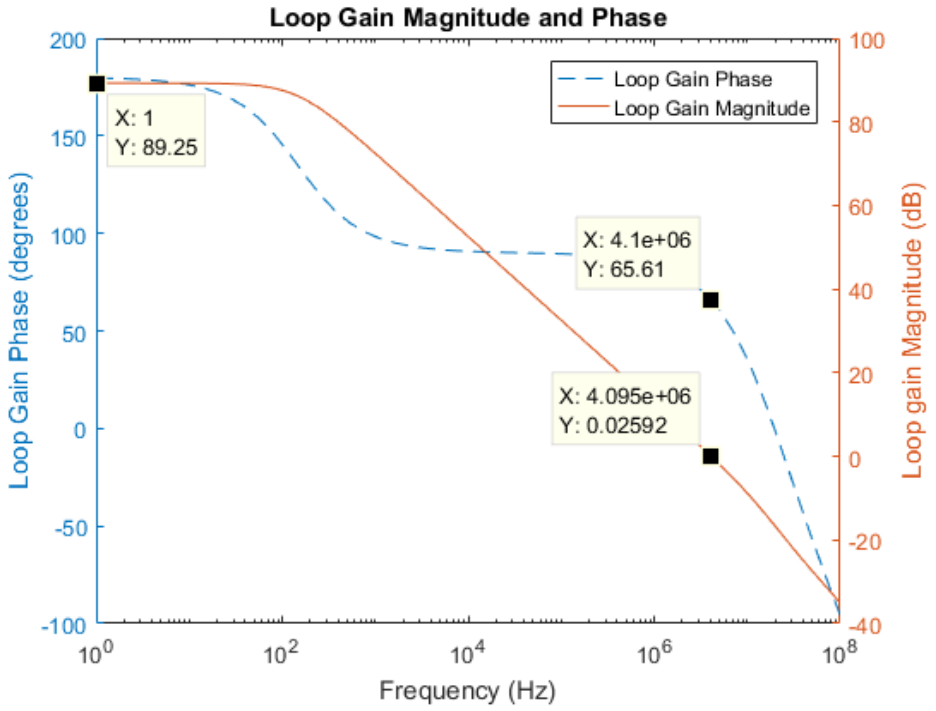
The calculated transistor sizes (which were also the transistor sizes used in simulation) can be found in the table below along with the inversion level for each transistor:

Transistor	Calculated Size	Inversion Level (i_f)
M_1	$\frac{230\mu m}{520nm}$	1
M_2	$\frac{27.5\mu m}{520nm}$	1
M_3	$\frac{10\mu m}{1\mu m}$	35
M_4	$\frac{30\mu m}{1\mu m}$	35
M_5	$\frac{120\mu m}{1\mu m}$	35
M_6	$\frac{220\mu m}{520nm}$	1

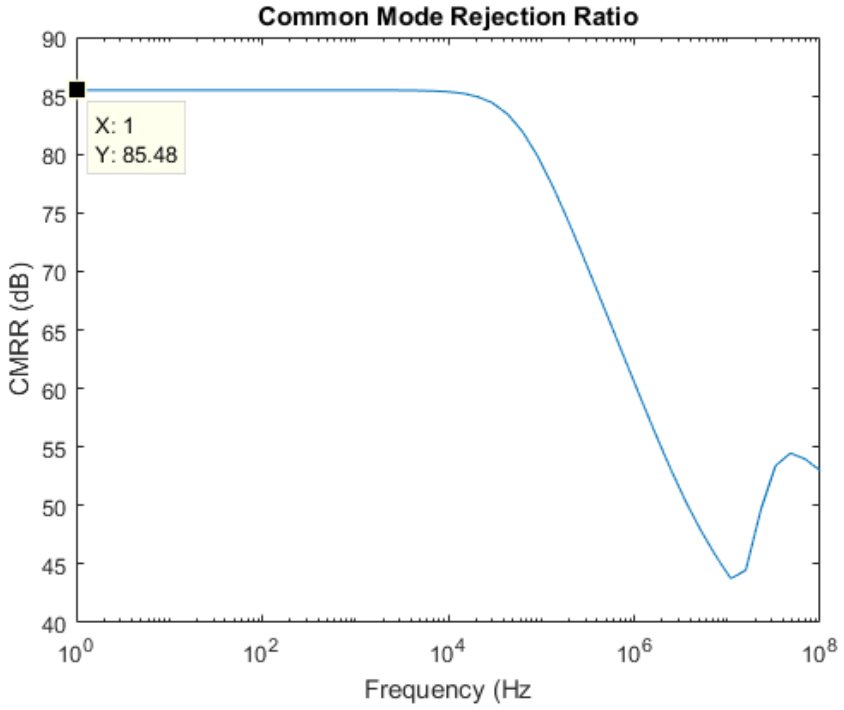
Simulation Results:

The graph below shows the loop gain of the amplifier in unity-gain configuration with a load capacitance of 25pF. The UGB of the amplifier is about 4.1MHz while the phase margin at this frequency is 65.61 degrees. The UGB of the amplifier decreased somewhat because the g_{m1} provided by the above calculations was slightly lower than in the original simulations. This UGB, however, still

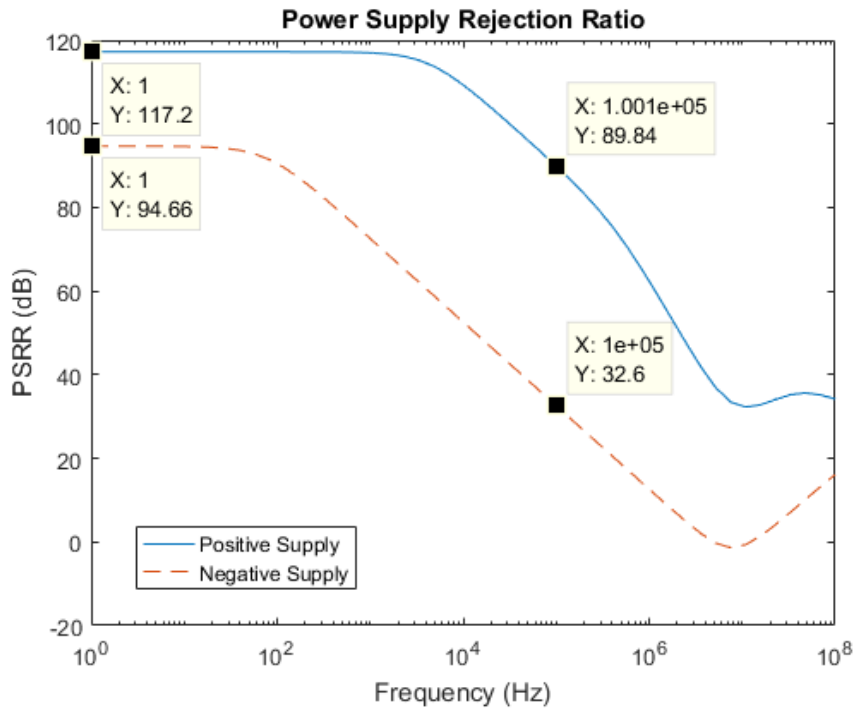
meets the specification. It is also interesting to note that the DC gain of the amplifier has increased by approximately 6dB. This is due to the decreased current flowing through the transistors which in turn increases their output resistance.



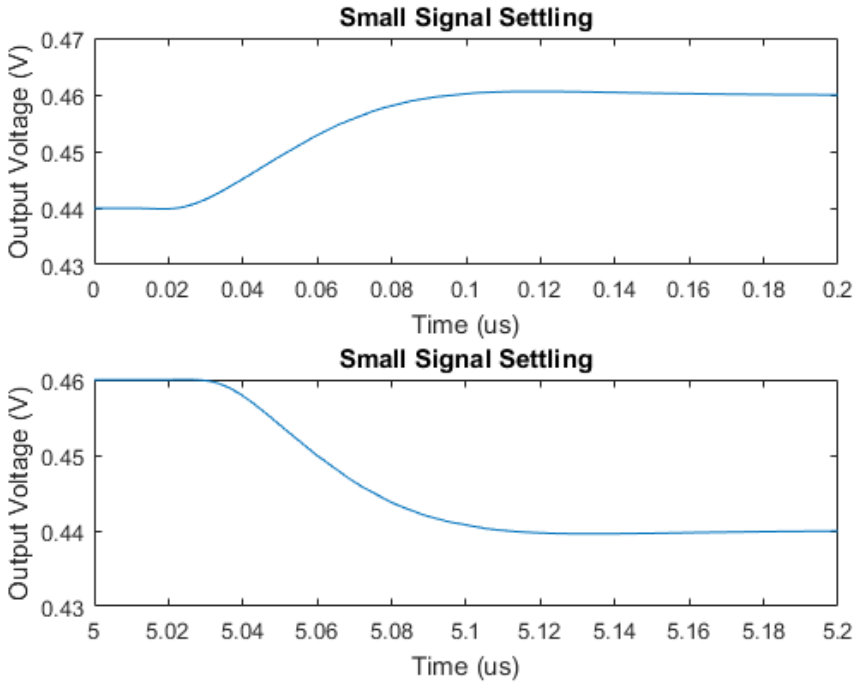
The following graph shows the CMRR of the amplifier. The DC CMRR of 85.48dB matches with the DC CMRR of the square-law op amp and meets the required specification.



The following graph shows the PSRR of the amplifier. The PSRR is greatly improved in this design when compared against the square law design.



The graph below shows the small signal settling of this amplifier. Compared to the square law amplifier, this amplifier has larger rising and falling settling times of 150.2ns and 143.8ns respectively. This is due to the decreased GBW.

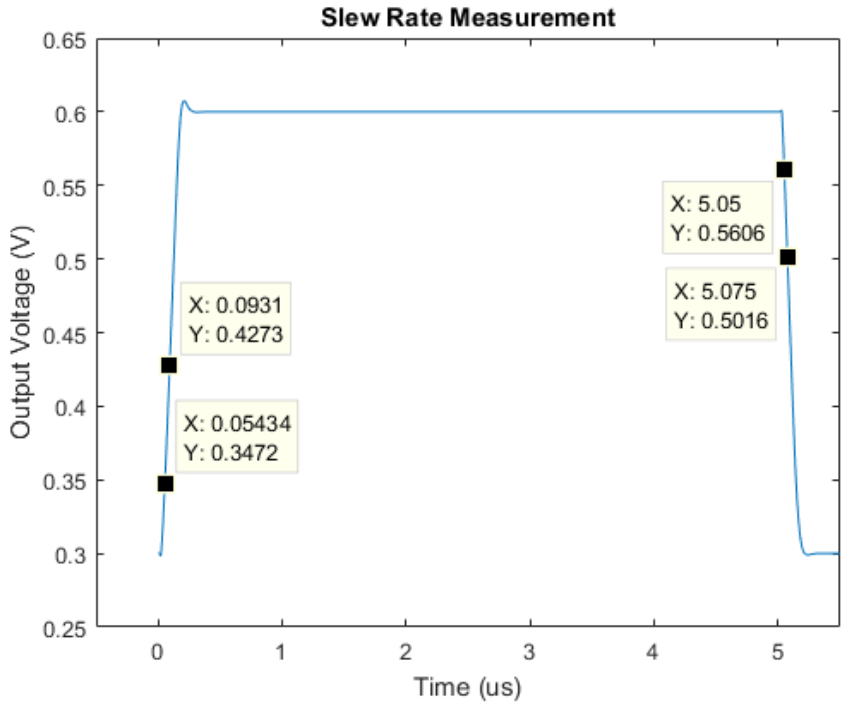


Lastly, the large signal step response of the amplifier was tested to find the slew rate. The slew rate can be calculated as follows:

$$SR_+ = \frac{0.3472V - 0.4273V}{.05434\mu s - .0931\mu s} = 2.07V/\mu s$$

$$SR_- = \frac{0.5606V - 0.5016V}{5.075\mu s - 5.047\mu s} = 2.11V/\mu s$$

These slew rates are much smaller than the slew rates for the square-law amplifier due to the fact that the current in the input stage is much smaller.



The results from both amplifiers in this problem are summarized in the table below:

Parameter	**Square Law Amplifier**	**ACM Amplifier**
Gain	81.37 dB	89.25 dB
DC CMRR	85.48 dB	85.48 dB
GBW	4.918 MHz	4.095 MHz
PM	68.36	65.61
Power	493.08 uW	193.56 uW
$PSRR_+$ at DC	71.9 dB	117.2 dB
$PSRR_-$ at DC	93.22 dB	94.66 dB
$PSRR_+$ at 100 kHz	71.48 dB	89.84 dB
$PSRR_-$ at 100 kHz	34.23 dB	32.6 dB
1% Settling Time	116.9 ns	150.2 ns
SR_+	4.675 V/us	2.07 V/us

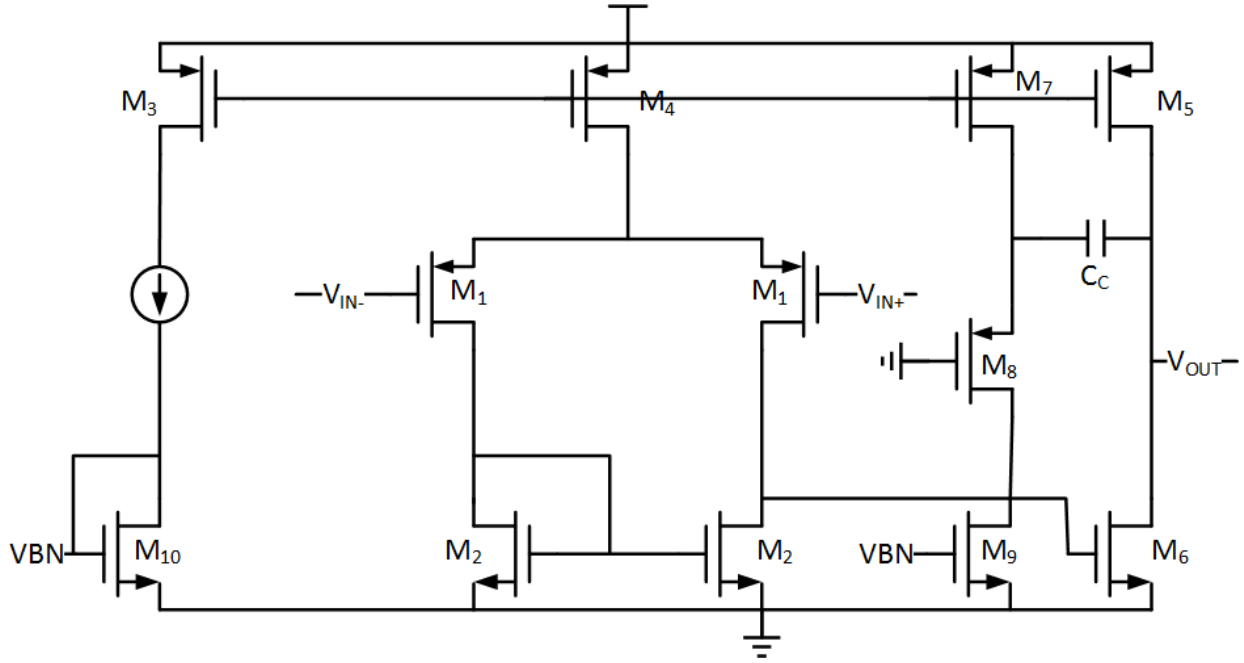
Problem 4

Design:

We will use the schematic below for the design with Ahuja compensation. The compensation capacitor C_C is once again chosen to be 12.5pF. As a result, the transconductance of the first stage will remain the same to provide the required gain bandwidth product. The transconductance of the second stage can be determined as follows if we assume the parasitic capacitance at the output of the first stage is approximately 0.5pF:

$$70° = 90° - \tan^{-1}(5MHz * 2 * \pi * \left(\frac{0.5pF(12.5pF + 250pF)}{g_{m6} * 12.5pF}\right))$$

$$g_{m6} = 950\mu A/V$$



Once again, we will use i_f=1 for the design of this stage:

$$I_6 = \frac{1+\sqrt{1+1}}{2}\left(.026V * \frac{950\mu A}{V} * 1.194\right) = 36\mu A$$

$$\frac{W}{L_6} = \frac{950\mu A/V}{\frac{710\mu A}{V^2} * .026V} * \frac{1}{\sqrt{1+1}-1} = 124.24 \rightarrow \left(\frac{W}{L}\right)_1 = \frac{65\mu m}{520nm}$$

For the size of M_2:

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1 * \frac{15\mu A}{36\mu A} = \frac{27\mu m}{520nm}$$

The current through M_7 is chosen to be 40uA to ensure this branch does not limit the slew rate of the amplifier. Therefore:

$$\left(\frac{W}{L}\right)_7 = 4\left(\frac{W}{L}\right)_3 = \frac{40\mu m}{1\mu m}$$

The size for the NMOS bias transistor M_{10} is chosen to be:

$$\left(\frac{W}{L}\right)_{10} = 10\mu m/1\mu m$$

Therefore, to reduce the input-referred offset of the amplifier:

$$\left(\frac{W}{L}\right)_9 = \frac{40\mu m}{1\mu m}$$

The dimensions of M_8 are chosen to ensure a high enough g_m that the node is a "pseudo" virtual ground and the LHP zero introduced by this transistor does not greatly affect the circuit:

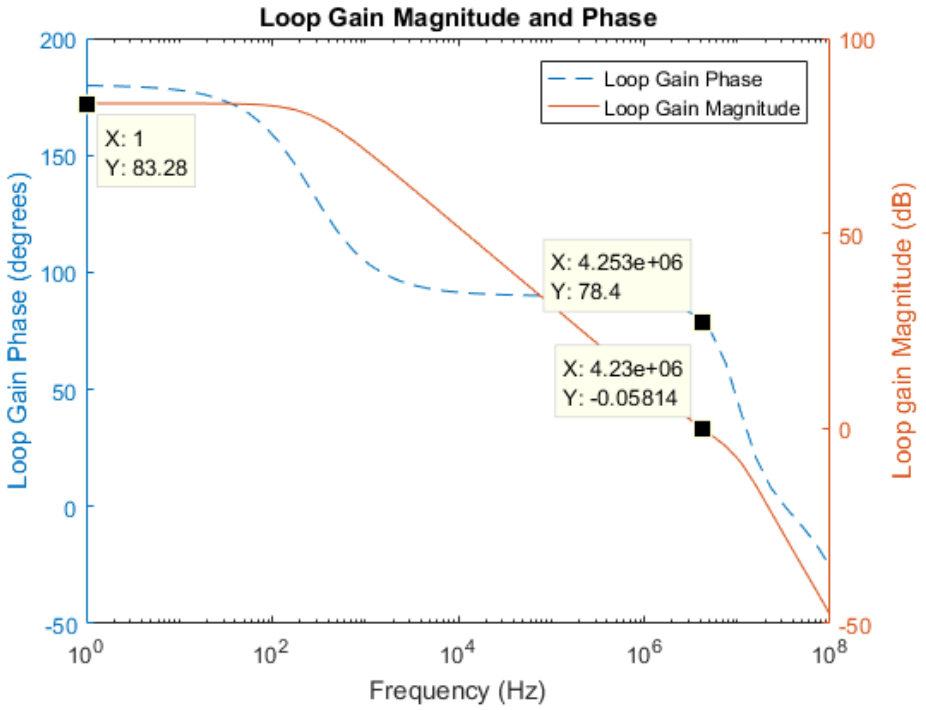
$$\frac{W}{L_8} = \frac{\frac{700\mu A}{V}}{2 * \frac{85\mu A}{V^2} * .026V * \left(\frac{40\mu A}{.026V * 1.164 * \frac{700\mu A}{V}} - 1\right)} = 178.3 \rightarrow \left(\frac{W}{L}\right)_8 = \frac{90\mu m}{520nm}$$

Transistor	Calculated Size	Inversion Level (i_f)
M_1	$\frac{230\mu m}{520nm}$	1
M_2	$\frac{27\mu m}{520nm}$	1
M_3	$\frac{10\mu m}{1\mu m}$	35
M_4	$\frac{30\mu m}{1\mu m}$	35
M_5	$\frac{120\mu m}{1\mu m}$	35
M_6	$\frac{65\mu m}{520nm}$	1
M_7	$\frac{40\mu m}{1\mu m}$	35
M_8	$\frac{90\mu m}{520nm}$	9
M_9	$\frac{40\mu m}{1\mu m}$	3.25
M_{10}	$\frac{10\mu m}{1\mu m}$	3.25

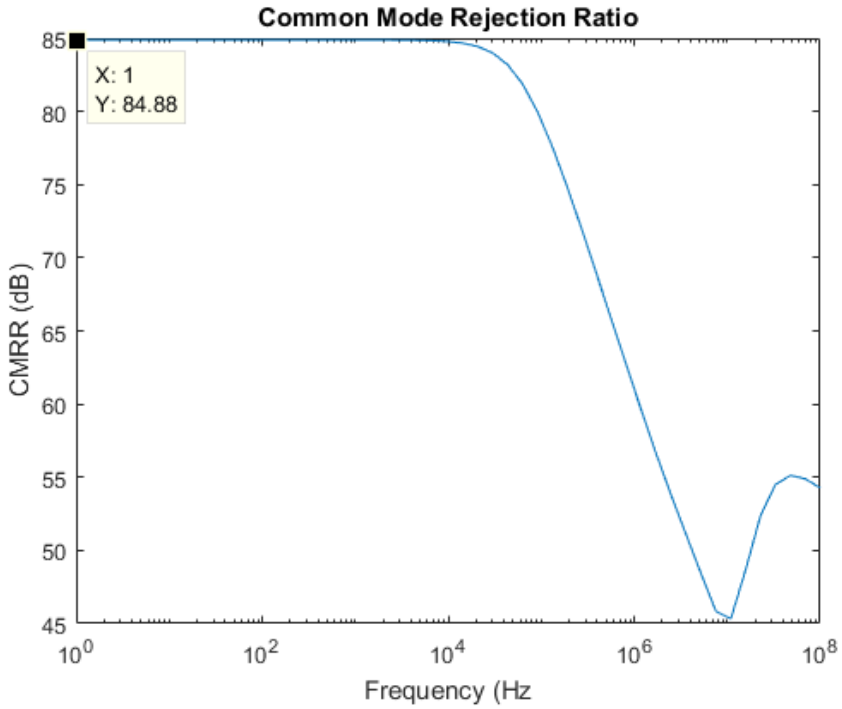
Simulation Results:

The graph below shows the loop gain phase and magnitude of the amplifier with a load capacitance of 250pF. The low-frequency gain is 83.28dB which is well above the specification of 50dB. In addition to this, the GBW of the op amp is 4.23MHz which is also well above the requirement. Lastly,

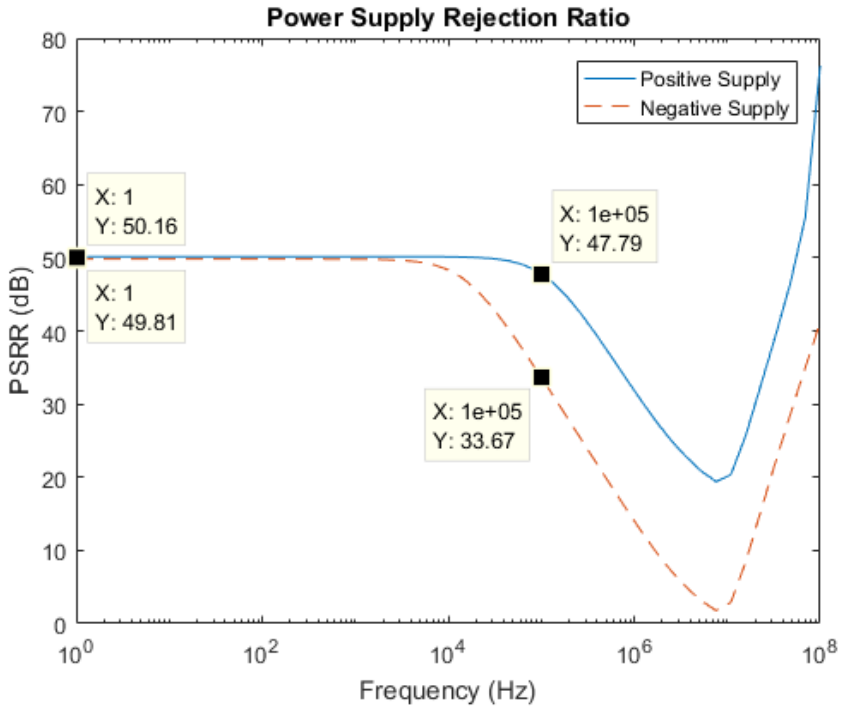
the phase margin of the amplifier is 78.4 degrees which provides great stability at a very large capacitive load. In addition to this, the power of the op amp was decreased dramatically since the transconductance of the second stage is not required to be as high. Indeed, the power dissipation is about 72.2% lower than the amplifier designed using a simple compensation capacitor and the square law equations in ECEN 474.



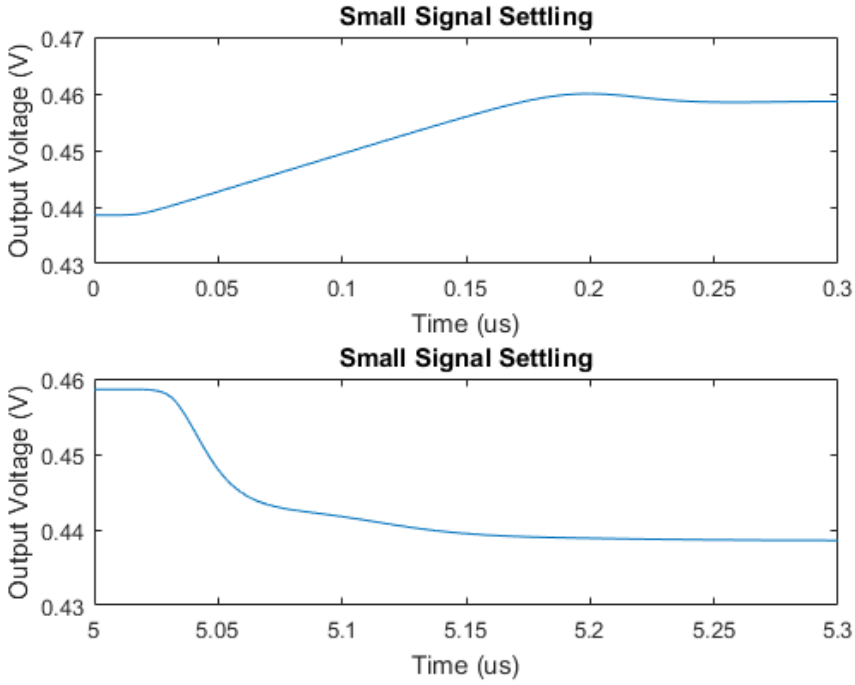
The next plot shows the CMRR of the amplifier. The DC CMRR is 84.88dB which is far greater than the 55dB required by the specification.



The next plot shows the PSRR of the amplifier. Unfortunately, the low-frequency PSRR of the amplifier is much worse for the Ahuja compensated amplifier than it is for the normally compensated amplifier. At very high frequencies, the Ahuja compensated amplifier has better PSRR performance.



The next plot shows the small signal step response of the amplifier. The rising settling time is 225.4ns while the falling settling time is 200.7ns. These measurements indicate a much greater settling time for the Ahuja compensated amplifier.

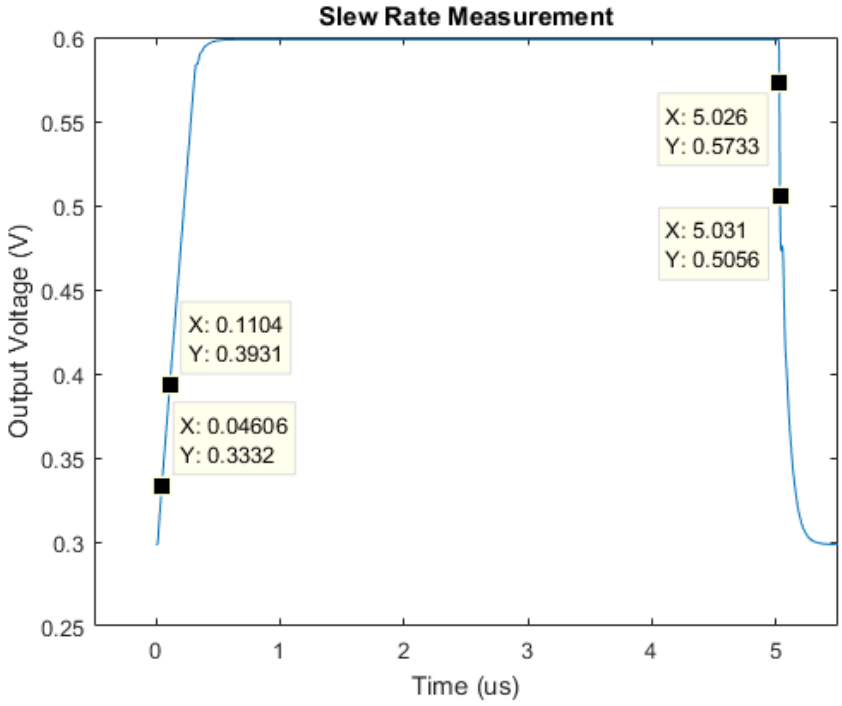


The next plot shows the large signal step response of the amplifier with a 25pF load capacitance. The SR can be calculated as follows:

$$SR_+ = \frac{0.3931V - 0.3332V}{0.1104\mu s - 0.04606\mu s} = 0.93V/\mu s$$

$$SR_- = \frac{0.5733V - 0.5056V}{5.031\mu s - 5.026\mu s} = 13.54V/\mu s$$

It is interesting to note that the rising slew rate is far smaller than the falling slew rate.

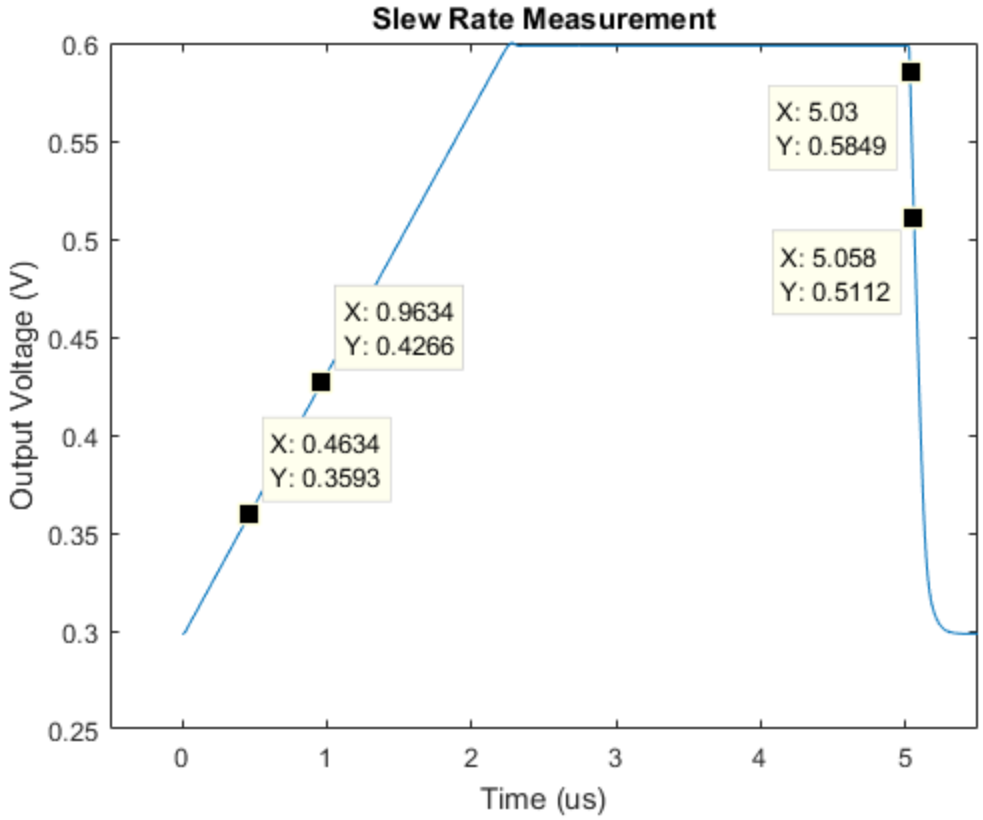


The figure below shows the large signal step response with a load capacitance of 250pF. The SR can be calculated as follows:

$$SR_+ = \frac{0.4266V - 0.3593V}{0.9634\mu s - 0.4634\mu s} = 0.135V/\mu s$$

$$SR_- = \frac{0.5849V - 0.5112V}{5.058\mu s - 5.03\mu s} = 2.63V/\mu s$$

Once again, the rising slew rate is far smaller than the falling slew rate. In addition to this, the slew rates are both much smaller than the slew rates for a load capacitance of 25pF. This is clearly one drawback of the Ahuja compensated amplifier: the rising slew rate is much lower than that of the traditionally compensated amplifier.



The results for all three amplifiers are shown in the table below:

Parameter	**Square Law Amplifier**	**ACM Amplifier**	**Ahuja Amplifier**
Gain	81.37 dB	89.25 dB	83.28 dB
DC CMRR	85.48 dB	85.48 dB	84.88 dB
GBW	4.918 MHz	4.095 MHz	4.23 MHz
PM	68.36° (at C_L=25pF)	65.61° (at C_L=25pF)	78.4° (at C_L=250pF)
Power	493.08 uW	193.56 uW	138.84 uW
$PSRR_+$ at DC	71.9 dB	117.2 dB	50.16 dB
$PSRR_-$ at DC	93.22 dB	94.66 dB	49.81 dB
$PSRR_+$ at 100 kHz	71.48 dB	89.84 dB	47.79 dB
$PSRR_-$ at 100 kHz	34.23 dB	32.6 dB	33.67 dB
1% Settling Time	116.9 ns	150.2 ns	225.4 ns
SR_+	4.675 V/us	2.07 V/us	0.93 V/us (at C_L=250pF)
SR_-	4.8 V/us	2.11 V/us	13.54 V/us

There are several tradeoffs between the square law design and ACM design that are easily visible in the table above. Firstly, the power dissipation was greatly decreased while the gain and DC PSRR were increased by using transistors in moderate inversion. However, the phase margin and GBW as well as the high frequency PSRR for the negative supply suffered. In addition to this, reduction of the power consumption also led to a decrease in both the positive and negative slew rates due to the decreased current in the input stage.

Again, there are several visible tradeoffs when comparing the Ahuja compensated amplifier with the traditionally compensated amplifier. Clearly, the Ahuja amplifier can handle a much larger load capacitance since it has a higher phase margin at 10X the load capacitance of the other amplifiers. In addition to this, since the required transconductance of the second stage is much lower with the Ahuja amplifier, the power dissipation was decreased even further. This increase in capacitive load handling comes with several drawbacks, however. Firstly, the low-frequency PSRR is greatly reduced for both the positive and negative supplies. In addition to this, the high frequency PSRR for the positive supply is significantly worse than in the traditionally-compensated case. The negative PSRR performance, however, remains close to the traditionally compensated case. The settling time for the Ahuja amplifier was much larger than the settling times for the traditionally compensated amplifiers as well. Lastly, while the negative slew rate seems to improve greatly with the Ahuja compensation, the positive slew rate suffers greatly. Therefore, while the Ahuja compensation technique improves capacitive load handling and power dissipation, it sacrifices performance in PSRR, settling time, and slew rate.