Using Floating Gate and Quasi-Floating Gate Techniques for Rail-to-Rail Tunable CMOS Transconductor Design

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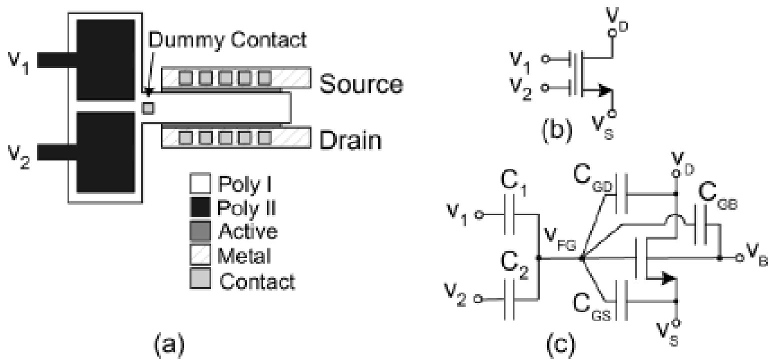

Fig. 1. Two-input FGMOS transistor. (a) Layout. (b) Symbol. (c) Equival- circuit.

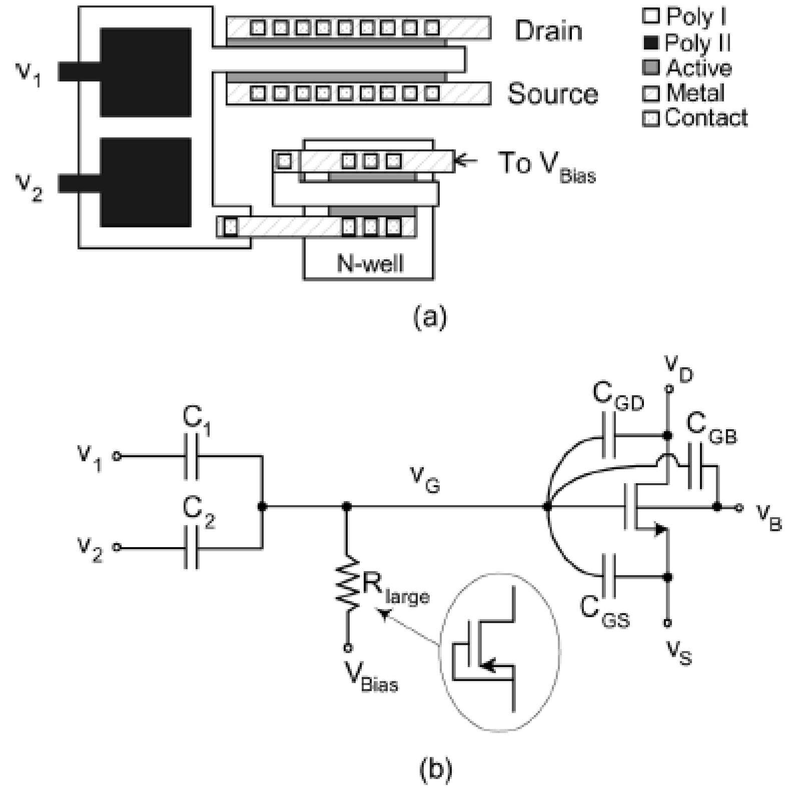

Fig. 2. Two-input QFGMOS transistor. (a) Layout. (b) Equivalent circuit.

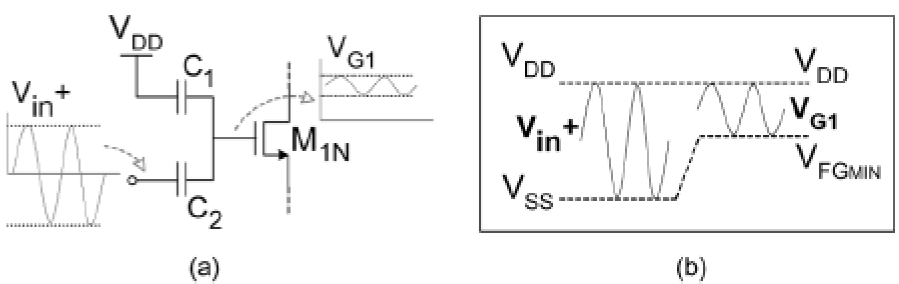

Fig. 3. Input FGMOS transistor. (a) Schematic. (b) Rail-to-rail operation.

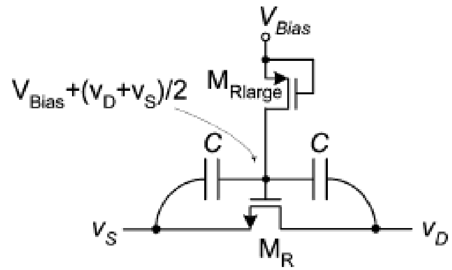

Fig. 5. Triode transistor with enhanced linearity using QFG technique.

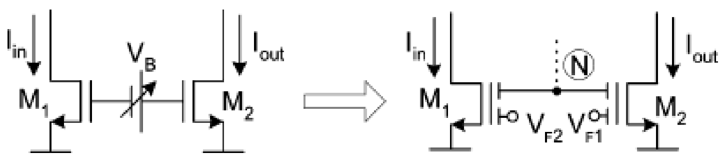

Fig. 6.

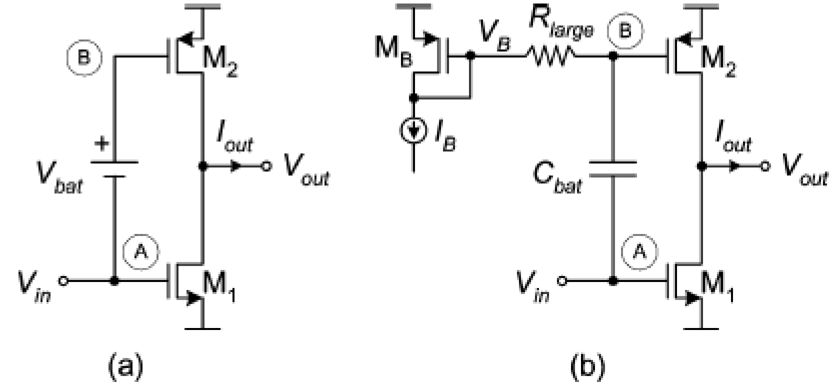

Fig. 7. (a) Class AB output stage. (b) QFG implementation.

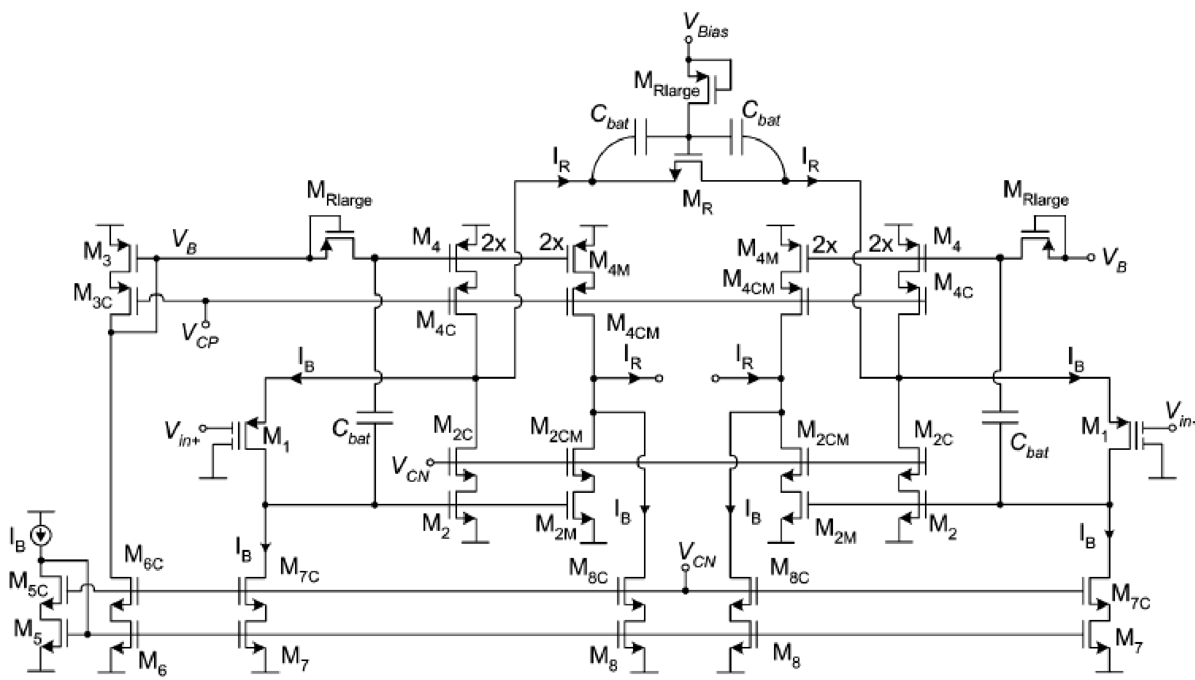

Fig. 8. Class AB rail-to-rail tunable transconductor.

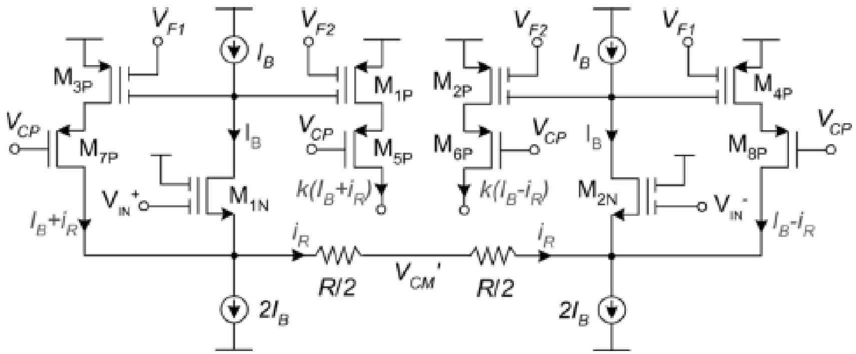

Fig. 13. Class A rail-to-rail tunable transconductor.

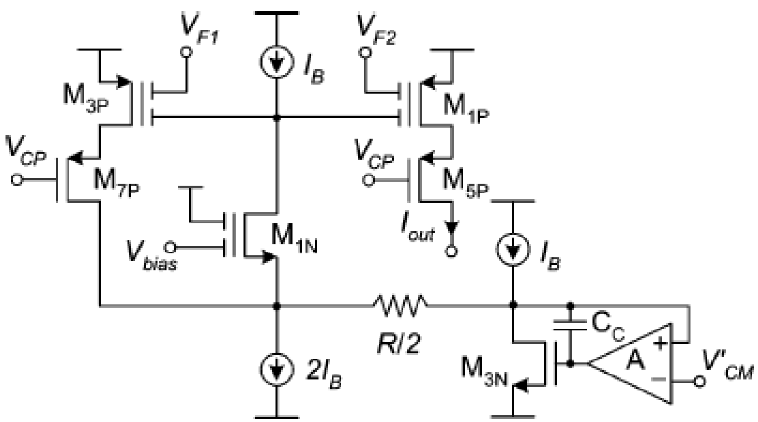

Fig. 14. Transconductance control circuit ($Gm1/2$ block).

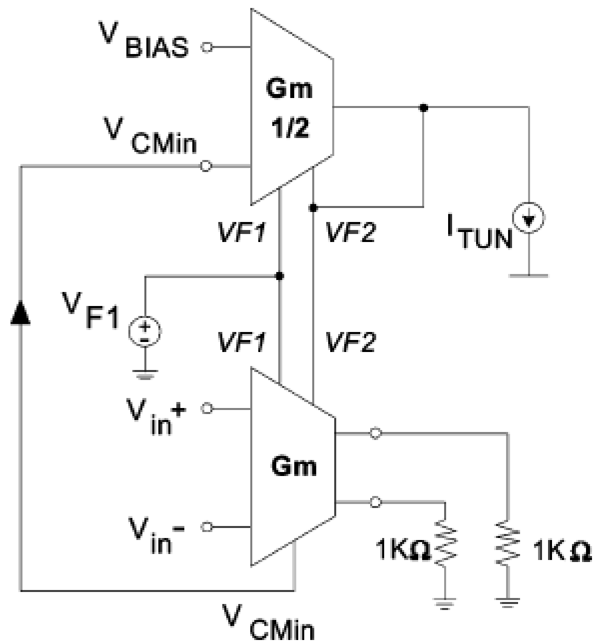

Fig. 15. Transconductance control system.

TABLE III
MEASUREMENT RESULTS OF TRANSCONDUCTORS

Parameter	This work, Fig. 8	This work, Fig. 13	[27] 2006	[28] 2006	[29] 2006	[16] 2008	[14] 2009	[30] 2010
Technology	0.5µm CMOS	0.5µm CMOS	0.5µm CMOS	0.35µm CMOS	0.35µm CMOS	0.18µm CMOS	0.5µm CMOS	0.13µm CMOS
Supply voltage	5 V	3.3 V	3.3 V	3.3 V	3.3 V	1.5V	5V	1.2V
IM3 @freq @Vin**	-52 dB @1MHz 2Vpp	-55 dB @1MHz 2Vpp	< -70dB @20MHz 0.5Vpp	<-70dB @26MHz 0.7Vpp	< -70dB @70MHz 0.65Vpp	-60dB @40MHz 0.9Vpp	-79.5dB @10MHz 1Vpp	-74.2dB @350MHz 0.1Vpp
IIP3	19.5 dBVp	22 dBVp	23 dBVp*	26 dBVp*	25 dBVp*	23 dBVp*	33.7 dBVp*	10.6 dBVp
IIP2	72 dBVp	54 dBVp	--	--	--	--	--	23.7 dBVp
Input noise @freq	98 nV/√Hz @1MHz	22 nV/√Hz @1MHz	--	--	7 nV/√Hz	23 nV/√Hz @40MHz	64 nV/√Hz @1MHz	22 nV/√Hz
CMRR @ freq	56 dB @ 100kHz	58 dB @ 100kHz	>50dB @ 100kHz	--	40dB @ 70MHz	--	61 dB @1MHz	--
Power	2.2 mW	1 mW	4 mW	6.6mW	9.5mW	9.5mW	30mW	5.2mW
Silicon area	0.07 mm^2	0.085 mm^2	0.06 mm^2	0.027 mm^2	0.025 mm^2	0.015 mm^2	0.18mm^2	--

(*) Estimated from IM3
(**) Peak-to-peak amplitude of each input tone, total input is twice this value