Design of a two stage amplifier using ACM model

ECEN 607(ESS)

Courtesy of

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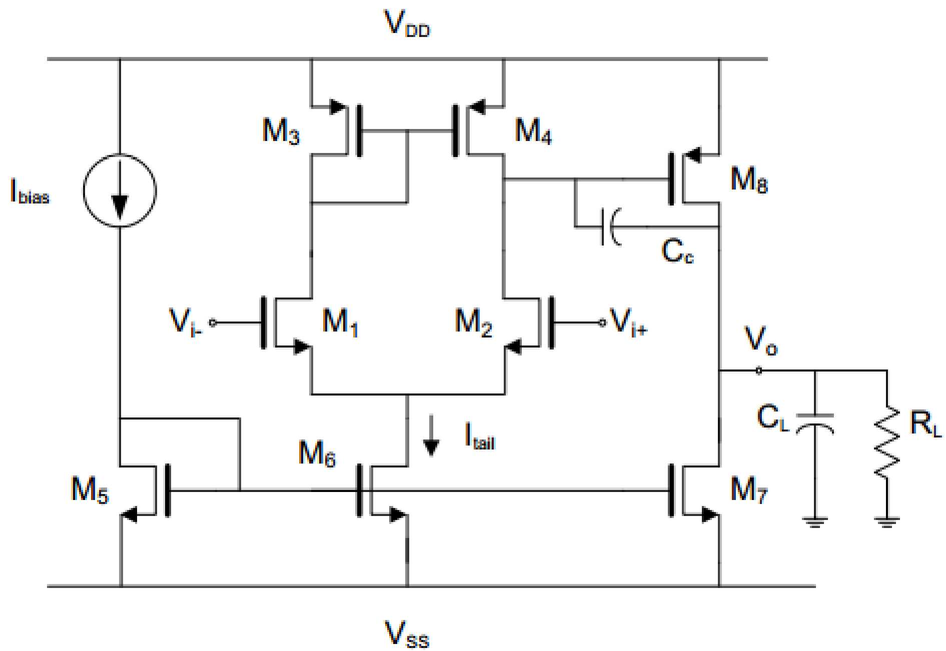
Why ACM model?

- Powerful tool for the simulation of MOS transistors
- Simple, precise equations to extract physical parameters
- Parameters describe effects particular to newer small channel technologies
- Valid for the efficient design of analog circuits
- Better match between simulations and actual circuit performance

Amplifier Specifications



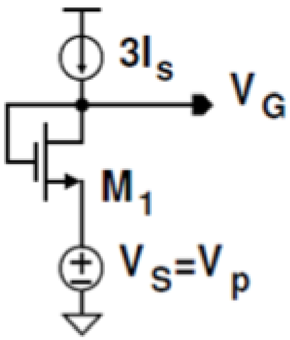
Specifications	Value
A_{vo} (DC gain)	> 50 dB
GBW	> 20 MHz
PM (Phase Margin)	> 50^{o}
SR (Slew Rate)	> 1.7 V/us
C_L	50pF
C_{in}	<0.8 pF
In band noise (DC-10MHz)	<10μV
Supply	1V

Amplifier Specifications

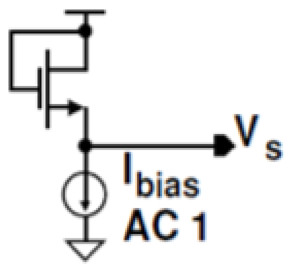
- Boundary conditions

- $\frac{gm_1}{Cc} = GBW > 20\ MHz$..........(1)
- $\frac{I_{tail}}{Cc} = Slew\ Rate > \frac{1.7V}{\mu s}$..........(2)
- ${V_{eq}}_{in}^{2} \cong \frac{16KT}{3gm_1}\left[1 + \frac{gm_8}{gm_1}\right]$..........(3)
- $PM = 180 - tan^{-1}\left[\frac{GBW}{w_{p1}}\right] - tan^{-1}\left[\frac{GBW}{w_{p2}}\right] -$ ~~$tan^{-1}\left[\frac{GBW}{w_{z1}}\right]$~~ ....(4)
- Cancel zero by using $R_z = \frac{1}{g_{m8}}$
- Assume phase contribution of w_{p1} is about $\frac{\pi}{2}$ and $f_{p2} > 80MHz$(from (4) and amplifier specifications for phase margin > 60°)
- $\left[\frac{g_{m8}}{C_L}\right] = f_{p2} \Rightarrow g_{m8} > 1mS$
- From (1) $gm_1 > 240\mu S$
- From (3), $I_{tail} > 8.5\mu A$

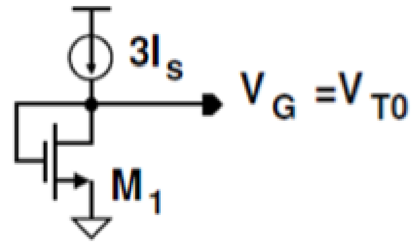
Parameter extraction for design(65nm)



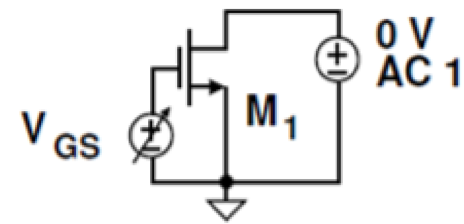
extraction of γ



Is extraction



Vto extraction



extraction of μo

- Using [1], the following parameters can be extracted

Parameter	NMOS(65nm)	PMOS(65nm)
Is/nA	333.8	46.8
Vth0/V	0.4238	-0.349
Gamma/$V^{1/2}$	0.207	0.293
Sigma/m^2	21.12f	5.679p
PCLM	0.0409	0.159
μo /cm2/Vs	267.3	70.4
θ/ V^{-1}	0.32	0.1995

[1] A.I.A. Cunha, Schneider, M.C.; Galup-Montoro C.; "An MOS transistor model for analog circuit design". IEEE J.of Solid-State Circuits, Vol. 33, Issue 10, pp. 1510-1518, Oct. 1998.

Amplifier dimensions calculations

- Choose $i_f = 0.5$, assume $g_{m1,8} = 1.5mS$
- Check intrinsic cutoff frequency of transistor at $i_f = 0.5$
- $f_T = \frac{\mu \phi_t}{2\pi L^2}\left(2\sqrt{1+if} - 1\right) = 51.5GHz \gg 20MHz$—(5)
- $Id = gm * n * \phi_t \frac{1+\sqrt{1+if}}{2} \cong 50\mu A$—(6)
- $\frac{W}{L} = \frac{gm}{\mu C_{ox} \Phi_t (-1+\sqrt{1+i_f})}$—(7)
- $\frac{W}{L}_N\ (65nm) = 336\ \frac{W}{L}_P\ (65nm) = 1276$
- $\frac{V_{DSAT}}{\phi_t} \cong \left(\sqrt{1+if} - 1\right) + 4 \Rightarrow V_{DSAT} \cong 0.1V$

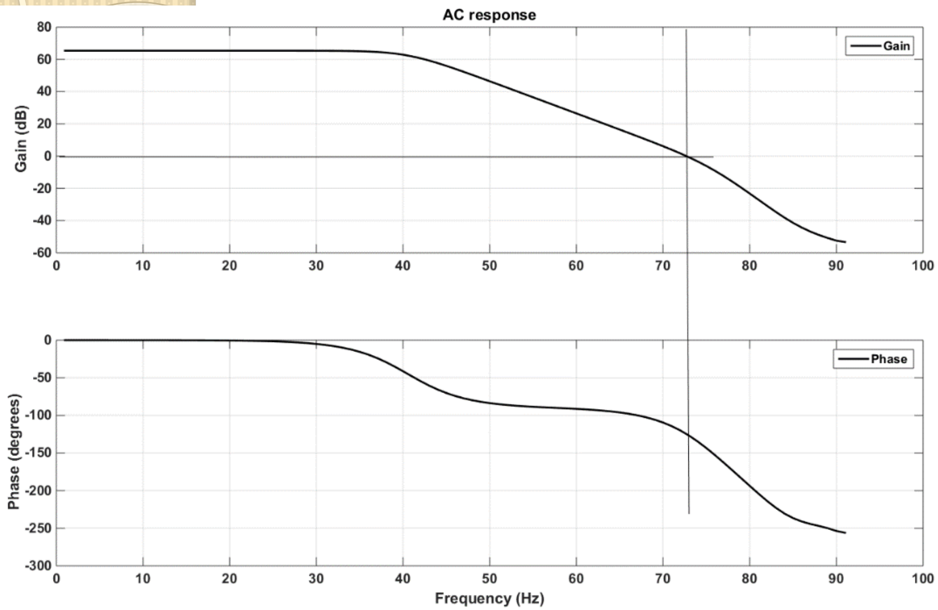
Amplifier design (i_f=8)

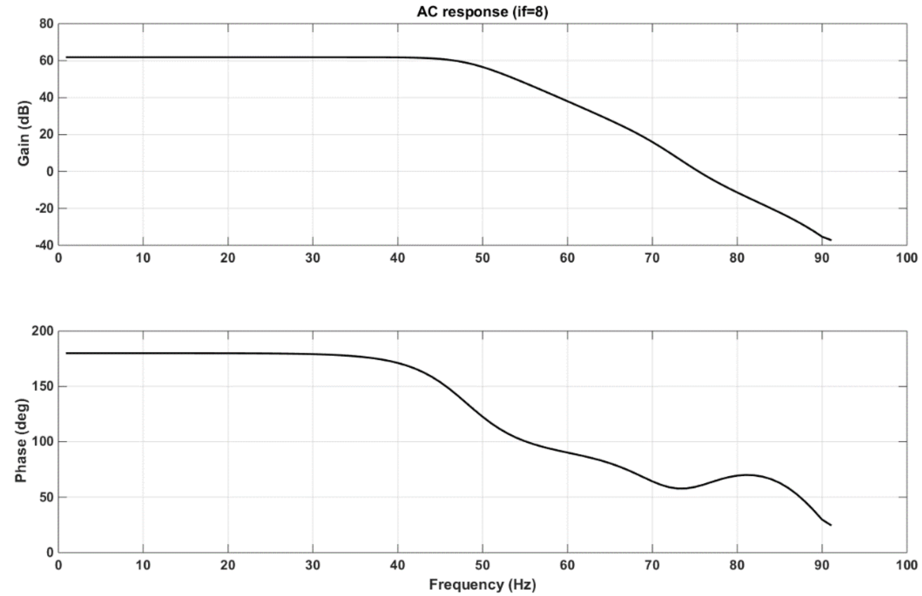
- Choose i_f = 8,choose $g_{m1,8} = 1.5mS$
- Check intrinsic cutoff frequency of transistor at i_f = 8 using (5)
- f_T =130GHz ≫ 20MHz
- $Id \cong 93\mu A$
- $\frac{W}{L}_N\ (65nm) = 4;\ \frac{W}{L}_P\ (65nm) = 16$
- $V_{DSAT}\ \cong 0.208V$

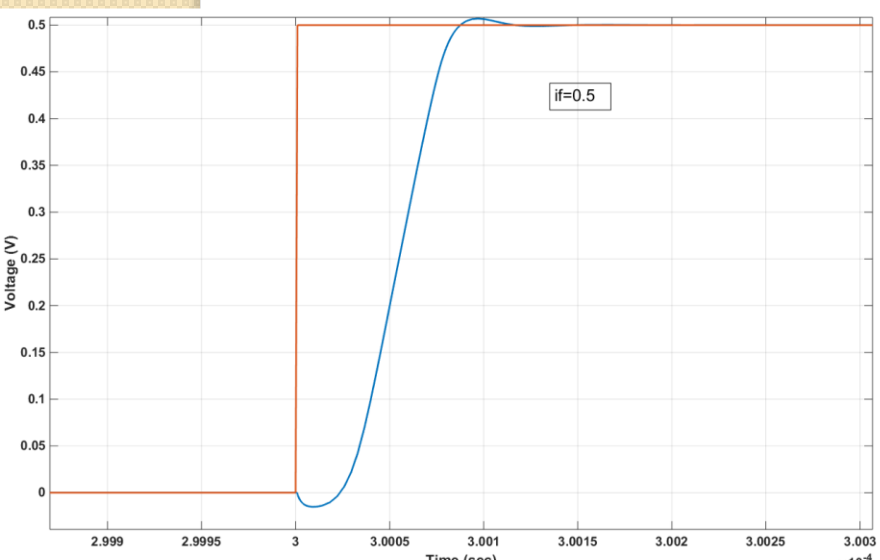
Amplifier design recap

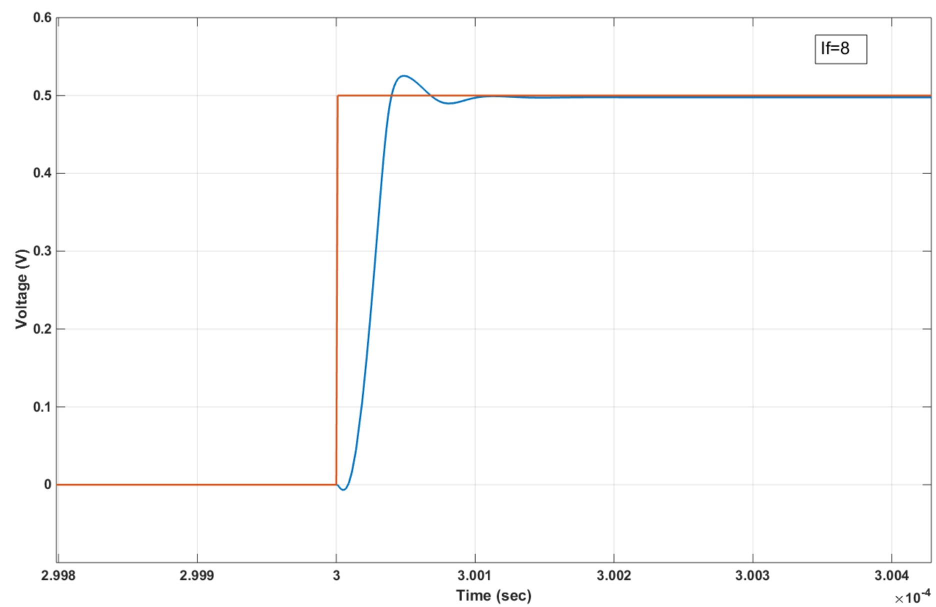
- First extract transistor parameters using ACM model and test benches
- First check if selected inversion level is adequate for your design, this is done by calculating the f_t of transistor, f_t >>3xGBW (5)
- Use extracted parameters to calculate required transconductances, saturation voltage, dimensions based on specifications given as a first trial point
- Bias your circuit properly and perform your simulations
- Calculated values of M1, M2, M8 kept the same producing relative same gm at selected currents when ACM model is used (1)-(6).
- Reevaluate operational points to obtain required specifications

Example of results









Results

Parameter	I_f=0.5	I_f=8
Gain (dB)	65	61
Phase margin (deg)	50	60
Power dissipation (μW)	409	558
Settling time (nsec)	180	130
PSRR (dB)	66.3	62.4
Slew rate (V/μsec)	8.4	17.3
Area estimation ($\mu^2 m^2$)	2400	100

- Smaller inversion level, larger area, slower response, lower power consumption
- Moderated inversion level, smaller area, larger power consumption, faster response

Conclusions

- ACM model effective in calculation of design parameters
- Very good first approximation
- Not region of operation specific