Low Voltage Analog Circuit Design Techniques

by S. S. Rajput and S. S. Jamuar

Abstract—*Analog signal processing is fast and can address real world problems. The applications of battery powered analog and mixed mode electronic devices require designing analog circuits to operate at low voltage levels. In this paper, some of the issues facing analog designers in implementing low voltage circuits are discussed, and possible low voltage design techniques are examined. We do not intend to present a review of state-of-the-art technology, but we do describe briefly almost all low voltage design techniques suitable for analog circuit structures along with their merits and demerits.*

Introduction

The desire for portability of electronic equipment generated a need for low power systems in battery-operated products like hearing aids, implantable cardiac pacemakers, cellphones, and hand held multimedia terminals. Low power dissipation is attractive, and perhaps even essential in these applications to have reasonable battery life and weight. The ultimate goal in design is close to having battery-less systems, because the battery contributes greatly to volume and weight. Solar power, fuel cells, RF power, and so forth, are the most viable alternatives [1]. The biggest issue that must be considered with these power sources is their low voltage levels. The voltage of a single solar cell is about 0.5V (even lower for other sources), which is well below the nominal voltage of dry cells or even their end-of-discharge values (0.9V). The design of integrated circuits (ICs) capable of working with solar cells offers a wide range of possibilities in portable signal processing instruments. But integrated circuits require much

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higher voltages for their operation. A possible solution to get higher dc voltage on-chip is voltage multiplication. This technique is noisy and not compatible with sensitive analog circuits. Furthermore, analog designers would have the additional burden of taking care of Power Supply Rejection (PSR) in these circuits, an issue usually disregarded in battery-powered equipment. Increasing demands of such products obviously encourage research and development efforts in designing and perfecting low voltage circuits with low power consumption.

Circuit operation at reduced voltages is a common practice adopted to reduce power consumption. However, the circuit performance degrades and one gets low circuit bandwidth and voltage swings at low voltages. Scaling down the threshold voltage of MOSFETs compensates for this performance loss to some degree, but this results in increased static power dissipation. Analog circuits benefit marginally from scaling, as the minimum size transistors cannot be used in analog circuits because of noise and offset voltage constraints. However, scaling results in better performance in digital circuits [2].

Furthermore, heat removal and internal power distribution pose major problems in the growth of CMOS circuits. The cost of heat removal (i.e. cooling) has resulted in significant interest in power reduction even in non-portable applications [2]. But, low voltage operation complicates the design, and the circuit performance may degrade. Simple circuits, which have fewer MOSFETs, will have minimum stray and device capacitances and are expected to perform better. It is desirable to have efficient and simple circuit structures for low voltage operations [2].

Low voltage analog circuit design techniques differ considerably from those of high voltage analog circuit design. This generates a need for adaptation of alternative design techniques to suit the low voltage environments. The current mode approach proves a better alternative for low voltage high performance analog circuit design in which the circuit designer is more concerned with current levels for the operation of the circuits. The voltage levels present at various nodes are immaterial.

This paper is aimed at providing a comprehensive treatment of all possible low voltage design techniques prevalent today for analog circuits. The selection criteria along with their merits and demerits have been presented.

Analog Signal Processing

Analog signal processing (ASP) has gone through a dramatic change in the last decade and is an essential ele-

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ment in real time signal processing applications because all physical phenomena are analog in nature. Advances in technology, increased market demands, and sophisticated and innovative information processing applications have motivated renewed interest in analog system design. The interdisciplinary view of VLSI is particularly important for analog design because VLSI technology and CAD tools have been developed primarily for digital VLSI design. If we have analog cells as in digital system design then the analog systems can also be designed like digital systems. This will make the design process simpler. Field programmable analog arrays (FPAA) [3], configurable and modular analog circuits [4, 5], fall in this category. Analog VLSI has tremendous potential for addressing real world problems [6].

The behavior of electrical circuits is always the result of interplay between voltage and current. All conventional analog circuits like operational amplifiers (op amps) are voltage mode circuits (VMCs). They suffer from the drawback that the output voltage does not change instantly, due to stray and circuit capacitances, when there is a sudden change in the input voltage. The bandwidth of VMCs is usually low. The slew rate (SR) is also not very high. VMCs are not suitable for use in high frequency applications and do not have high voltage swings. For better signal to noise ratio (SNR), higher supply voltages are required [7].

If the input and output signals are currents, some of the above demerits could be eliminated. In current mode circuits (CMCs), the currents determine the complete circuit response. The voltage signals are irrelevant in determining the circuit performance. The sensitive nodes inside CMCs are low impedance nodes, where the resultant voltage swings are also small. This results in low time constant circuits with high bandwidth. The slew rate for CMCs is also high. CMCs have simple architectures and are suitable for integration in CMOS technology.

Analog circuits should have rail-to-rail input and output voltage swing capability. Many conventional circuit topologies have been replaced by new innovative design. Simple CMC structures, especially those circuits that are capable of operating at low voltages [2], have been invented. A most important and common CMC structure is the current conveyor (CC) introduced in 1968 [8].

Critical Issues

The speed and bandwidth of analog circuits depend strongly on circuit capacitances, which arise partly because of MOSFET intrinsic capacitances and partly because of intercon-

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nect parasitic capacitances. In deep sub-micron technologies, interconnect capacitance dominates; and simple reduction of the transistor sizes will not have a proportional impact in bandwidth improvement. This is due to higher aggressiveness of device scaling in comparison with interconnect scaling. As die sizes are also getting larger, correspondingly longer wiring lengths worsen the distributed RC delays and susceptibility for substrate noise coupling, cross talk and other phenomena.

Voltage reductions guarantee the reliability of devices as the lower electrical fields inside oxide layers of a MOSFET produce less risk to the thinner oxides, which result from device scaling. Thus one of the solutions of all the problems lies in the adoption of low voltage techniques in analog circuit designs so that these MOSFETs can operate at low voltage levels.

Today's design strategies are directed toward achieving higher speed and large dynamic range. One of the factors which affects these parameters is power dissipation in the circuit. So it is essential to identify the agents of power consumption and minimize them. There are three main components of power dissipation in any circuit, namely, dynamic power caused by charging and discharging of (usually parasitic) capacitance, static power due to non-zero current of MOSFETs in the OFF state in digital circuits or biasing current in analog circuits, and the short-circuit power due to current flowing during the lapse of time when both PMOS and NMOS transistors are in the on state.

The total power (P_{TOTAL}) consumption of a circuit can be approximated as the sum of $NC_{eq}V^2_{DD}$ and $I_{off}V_{DD}$.Thus the main interest is to minimize P_{TOTAL} and the obvious way to reduce it would be to operate the circuits at low supply voltages (V_{DD}).

Low Voltage Design

Applications do exist where it is crucial that current levels are extremely small and supply voltage be also low. These applications include low voltage circuits in biomedical engineering and mobile communication, by way of example.

At low voltage, the main constraints faced are the device noise level and the threshold voltage (V_T). Reduction in V_T is dependent on the device technology. Higher V_T gives better noise immunity and the lower V_T reduces the noise margin to result in poor SNR. Hence, for present day CMOS technology, reduction in V_T is limited to the noise floor level, below which further reduction will introduce an amount of noise sufficient to result in very complex circuits. The restriction

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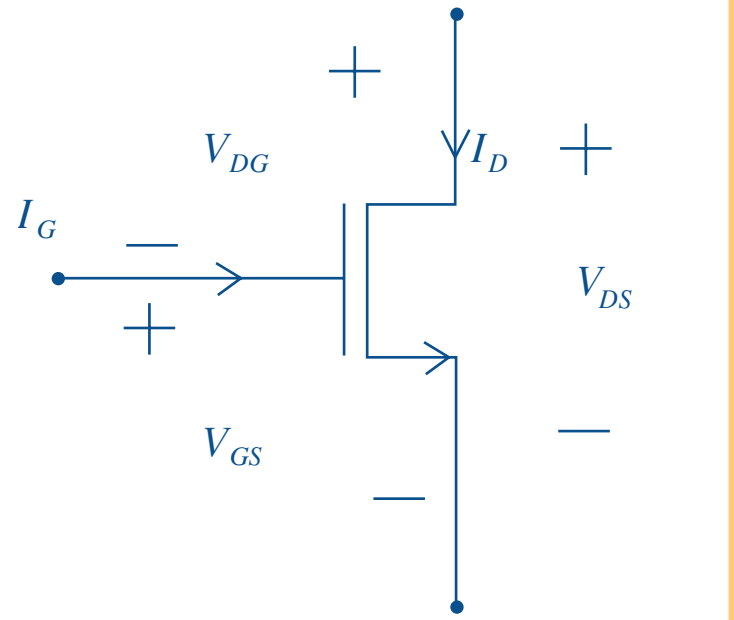


Figure 1. A MOSFET model.

on further reduction in V_T paves the way to have simpler, smarter and efficient circuits [2]. Many new design techniques for low voltage analog circuits are available, for instance, MOSFETs operating in the sub-threshold region [6, 9–14], bulk driven transistors [9, 10, 12–15], self-cascode structures [9, 12, 13], floating gate approach [6, 9, 16–21] and the level shifter techniques [9, 12, 22–27]. Use of low voltage high performing building blocks in low voltage analog circuits is another promising approach and yields a modular design concept in analog circuits as well [9, 13]. We will briefly look into these techniques.

Sub-Threshold Circuits

Circuits operating in the sub-threshold region have gained importance in recent years because of the need for low voltage and low power battery powered circuits in human implantable biomedical instruments.

When the applied drain source voltage in a MOSFET (Fig. 1) exceeds the threshold voltage, the drain current

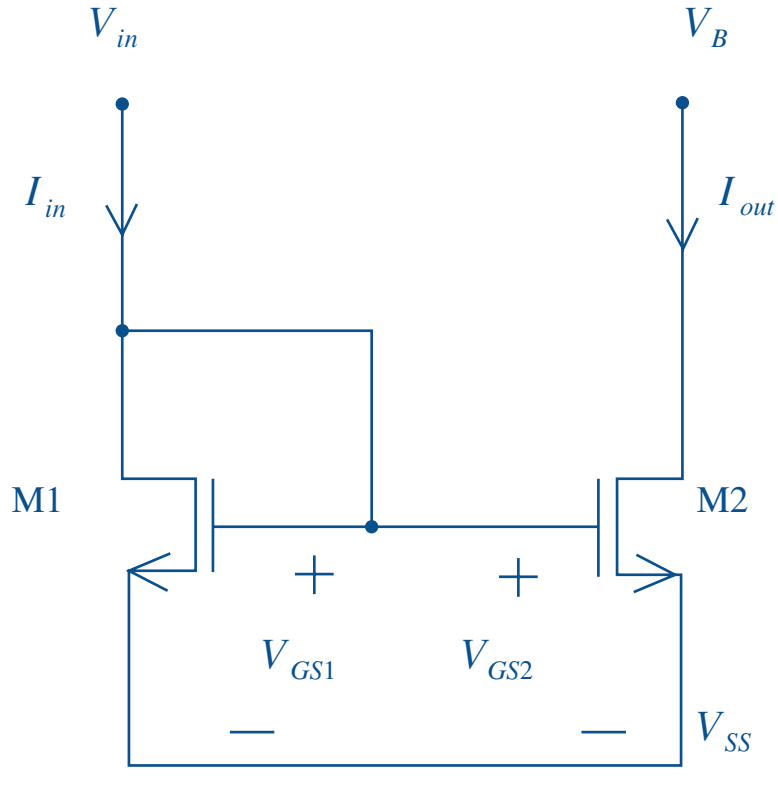


Figure 2. Current mirror (CM) based on sub-threshold MOSFETs.

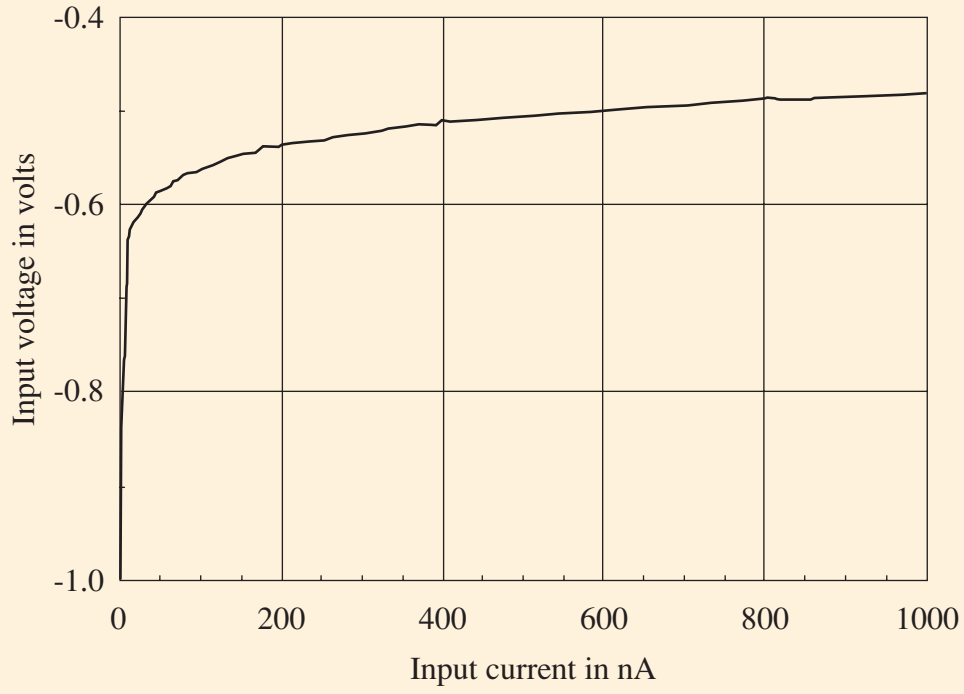


Figure 3. Input voltage characteristics of the CM.

in the sub-threshold region [26] is given by

$$I_{DS} = \frac{K' W}{L}\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right]V_{DS} \quad (1)$$

and the drain current is zero when $V_{DS} < V_T$.

This model was derived for small values (both positive and negative) of V_{DS}, which correspond to the ohmic region of operation. In the above equation W, L, and K' (μC_{ox}) represent the channel width, channel length and trans-conductance parameter respectively. The drain current (I_{DS}) is assumed to be zero for $V_{GS} < V_T$ and non-zero for $V_{GS} > V_T$. In a physical device, such an abrupt change does not occur. I_{DS} is, however, much smaller for $V_{GS} < V_T$ than for $V_{GS} > V_T$ and is attributed to diffusion in the region ($V_{GS} < V_T$, known as the sub-threshold region). In the sub-threshold region I_{DS} is given by [6, 11, 13, 26, 27]

$$\frac{2K' W}{L}\left(\frac{nkT}{qe}\right)^2 \exp\left(\frac{q(V_{GS} - V_{TN})}{nkT}\right) \quad (2)$$

where n is the sub-threshold slope factor and lies between 1.2 and 2. Parameters q, k, V_{TN}, and T represent the electronic charge, Boltzman constant, threshold voltage of NMOSFET and temperature respectively.

In sub-threshold region, MOSFETs have low saturation voltages (≈ 100mV). This gives larger voltage swings at low-supply voltage even in cascaded MOSFET structures. Similar to a bipolar transistor, the trans-conductance (g_m) equals ($q\ I_{DS} / nkT$) and is expected to be large. However, it may be noted that the current I_{DS} itself is low in sub-threshold region, and g_m cannot be high as in the case of bipolar transistors.

As an example the circuit diagram of a CM based on sub-threshold MOSFETs is shown in Fig. 2, which is similar to any conventional CM. The simulated output current characteristics of the CM are shown in Fig. 3. Though these characteristics are similar to any conventional CM, the re-

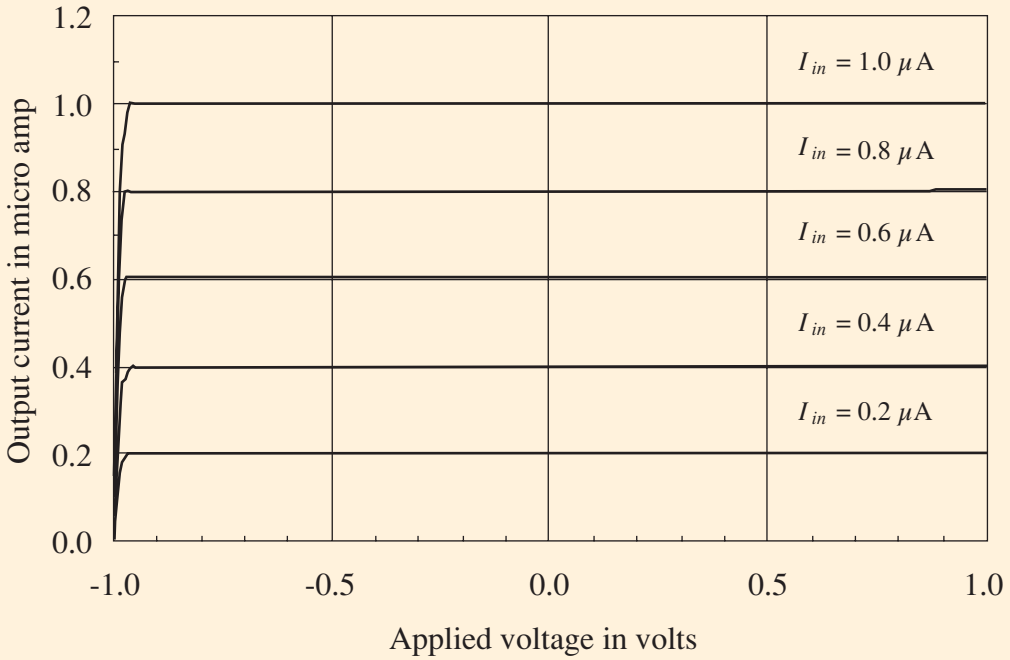


Figure 4. Output current voltage characteristics of the CM.

quired input compliance voltage is only a few hundred millivolts (≈ 500mV for a current of 1μA). This compliance voltage can further be decreased if we use the level shifter technique discussed later. The current voltage characteristics are shown in Fig. 4, which is quite similar to any conventional CM.

There are several limitations of devices operating in sub-threshold region. First, the frequency response of devices is poor. Second the drain and source substrate currents associated with the reverse biased moat-substrate junction are not necessarily negligible compared to sub-threshold drain current. Third, the linearity is quite poor for $V_{DS} < 3V_{ther}$ ($V_{ther} = kT/q$). This makes the low voltage circuit design quite complicated. Further, these circuits are meant for very low currents and are not suitable for medium power instruments.

Bulk-Driven MOSFETs

Blalock *et al*. have adopted the bulk driven MOSFETs technique [9, 10, 12–15] for low voltage analog circuits. For a MOSFET to perform any signal-processing task, there should be some biasing current through its drain. This biasing current in a conventional gate driven MOSFET comes when the applied gate bias overcomes the threshold voltage. However, in the bulk driven technique shown in Fig. 5, a MOSFET is biased in saturation mode so as to have a continuous drain cur-

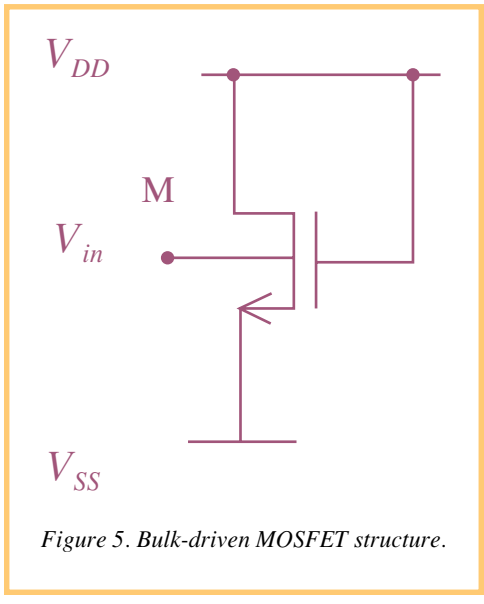


Figure 5. Bulk-driven MOSFET structure.

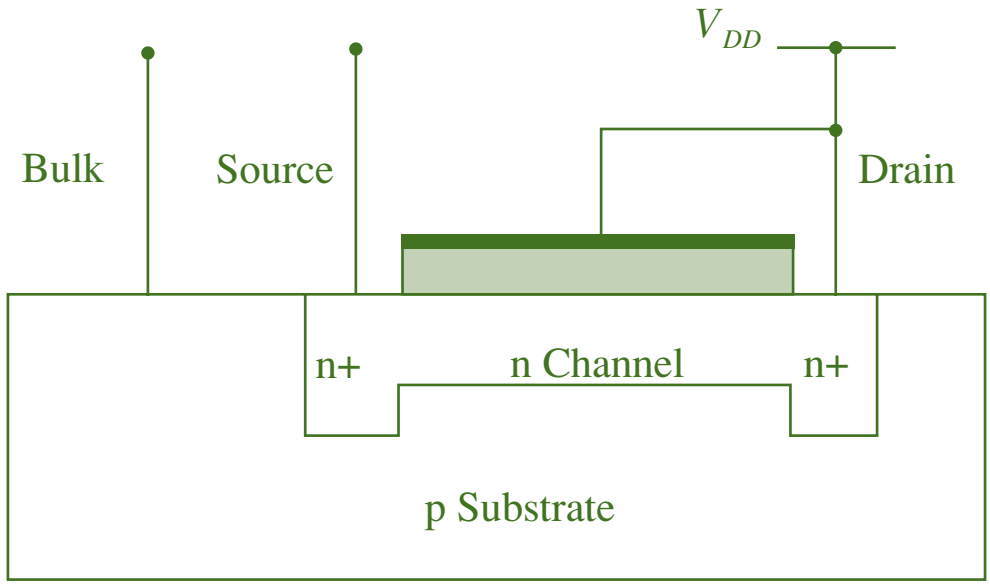


Figure 6. JFET equivalent of bulk-driven MOSFET.

rent; and the input signal is applied at the bulk contact. A close look at bulk driven MOSFETs suggests that the bulk driven MOSFET structure acts similarly to a JFET. The resultant JFET is shown in Fig. 6. Because of the applied gate voltage, a channel exists between the source and drain of the MOSFET. The channel width is constant as long as gate bias does not change as the case is for bulk-driven MOSFETs. The bulk contact serves the function of the gate of the virtual JFET and modulates the channel width according to the applied voltage. Thus the bulk driven MOSFET operates as a depletion type device; and it can work with negative, zero or slightly positive bias voltages also. The other major advantages offered by bulk driven MOSFETs are their large voltage ON/OFF ratio, which can be used for modulation.

We take the example of a simple current mirror shown in Fig. 7 to explain the functionality of the bulk driven devices. This circuit utilizes bulk driven n-type MOSFETs. The structure of the current mirror resembles a conventional mirror, where M1 and M2 are used in the conventional way except that the gate of both

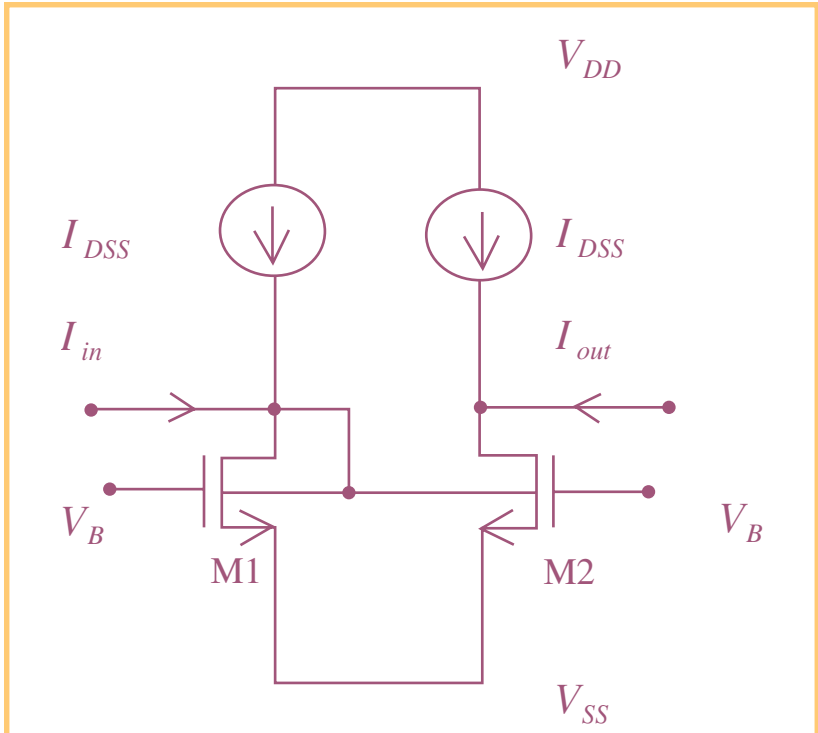


Figure 7. CM based on bulk-driven MOSFETs.

Low Voltage Analog Circuit Design Techniques

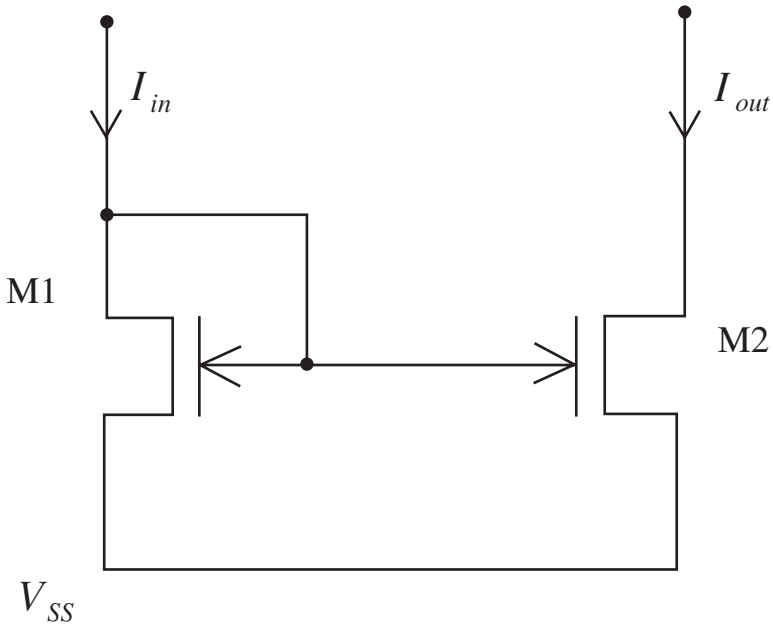


Figure 8. JFET equivalent circuit of CM based on bulk-driven MOSFETs.

M1 and M2 are tied to positive supply in this configuration. The currents through the MOSFETs M1 and M2 are equal to drain saturation current, and are supplied by two current sources as shown in the figure. The input current is injected into the input port formed at the drain of M1. This current can only flow through the drain of M1 when the width of the MOSFET (M1) channel changes. The channel width can either change by changing the gate bias (which is now fixed and tied to positive supply voltage) or by modulation of channel through the bulk. It may be noted that the MOSFETs act as simple depletion type n-JFETs, where the bulk of the device serves as the gate for the JFET. The equivalent circuit of the bulk-driven MOSFET based current mirror is shown in Fig. 8, which is similar to any conventional CM with similar input output characteristics. The required input compliance voltage is sufficiently low in this case and is about V_T.

Another example of bulk-driven MOSFET based circuit structure is a differential pair, as shown in Fig. 9 [9, 10, 12–15]. The circuit operation can easily be understood if we again consider bulk driven MOSFETs as JFETs (Fig. 10).

The bulk driven technique removes the threshold voltage requirements, and these devices can work even at 0.9V (for $V_T \approx 0.8$V). However the foremost disadvantage of the bulk driven technique requires all the MOSFETs to have isolated bulk terminals. Other disadvantages of the bulk driven technique for low voltage circuit applications are as follows.

I. g_m of a bulk driven MOSFET is substantially smaller than a gate driven MOSFET, and the two bandwidths are related as [9, 10, 12–15]:

$$f_{T,\,bulk-driven} \approx \frac{\eta}{3.8} f_{T,\,gate-driven} \quad (3)$$

where η is the ratio of g_{mb} to g_m and typically has a value in the range of 0.2 to 0.4.

II. The polarity of the bulk-driven

MOSFETs is process related. For *P*-well process, only *N*-channel bulk driven MOSFETs are available, and for *N*-well process, only *P*-channel MOSFETs are available. Thus, bulk-driven MOSFETs cannot be used in CMOS structures where both *N* and *P* type MOSFETs are required.

III. Bulk driven MOSFETs are fabricated in differential wells to have isolated bulk terminals and the matching between bulk-driven MOSFETs in differential wells suffers. Thus analog circuits with tight matching between MOSFETs are difficult to fabricate.

IV. There is a likelihood to have latch up problems because of potential turning ON of the parasitic BJT.

Self-Cascode Approach

As device sizes are shrinking, the output impedance of the MOSFET is also becoming smaller because of channel length modulation. For high gain, one needs high output impedance of the devices, and short channel MOSFETs cannot provide high gain structures. To obtain high output impedance, one uses cascode structure as shown in Fig. 11, where two MOSFETs are placed one above the other [9, 12–14]. The use of cascode structure increases the gain but it decreases the output signal swing at the same time. The output signal swing reduces at least by one V_T if used in the

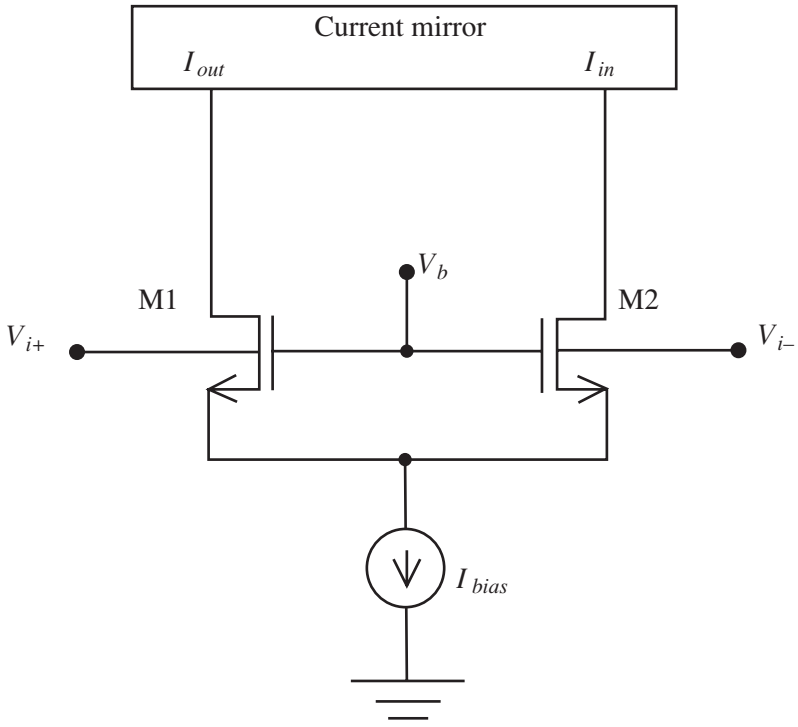


Figure 9. Differential pair based on bulk-driven MOSFETs.

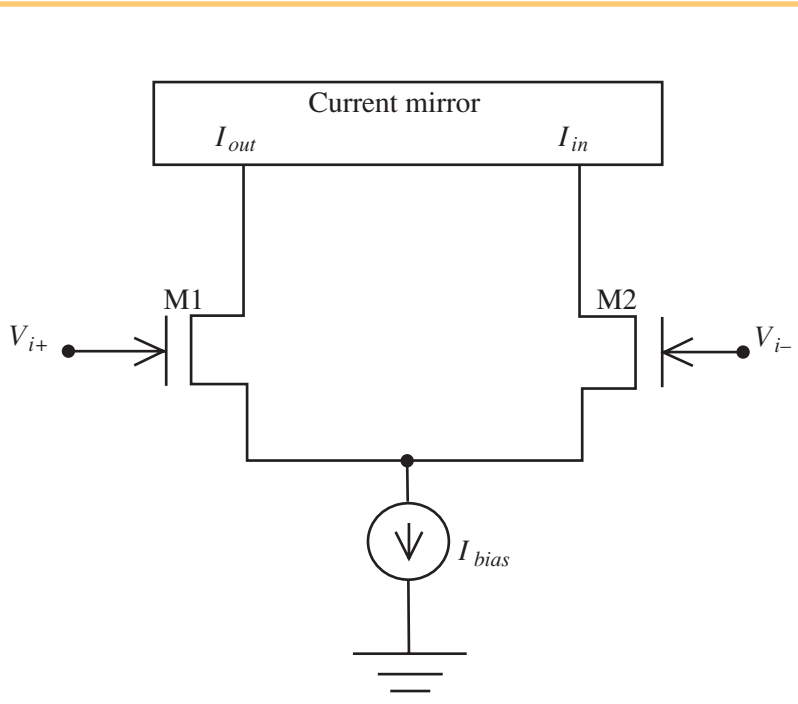


Figure 10. JFET equivalent circuit of the circuit shown in Fig. 9.

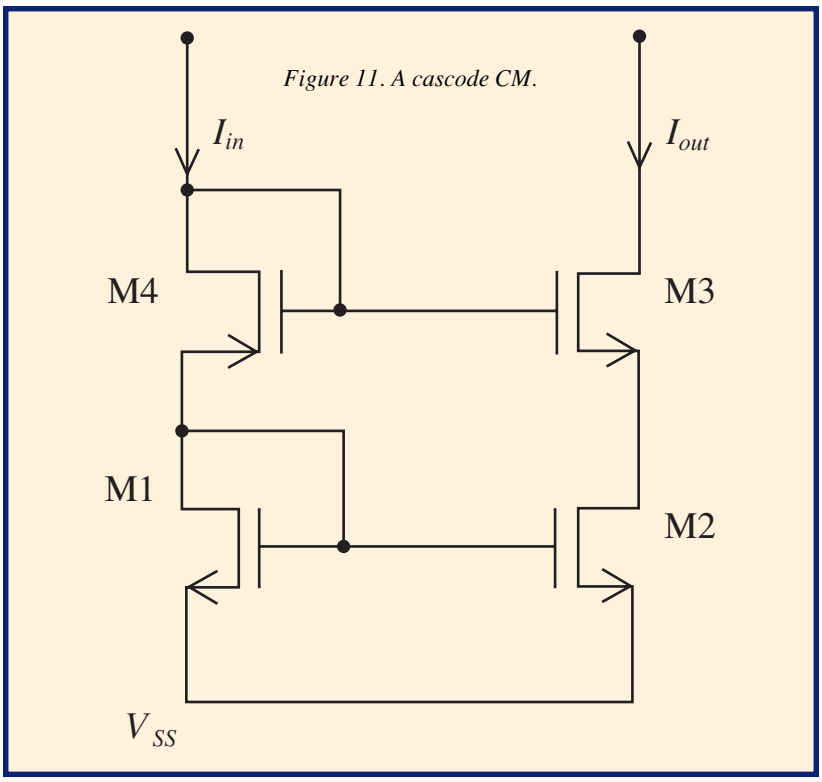


Figure 11. A cascode CM.

design of current mirrors. This decrease in the output voltage is due to the structure followed in the design of cascode biasing. Because V_T is of the order of 0.75V, cascode structures cannot be used in low voltage systems [9, 12–14].

If this circuit is modified in such a way that the biasing of the transistor M2 does not affect the output voltage swing, the output impedance of the structure can be increased to have high gain structures at low voltage levels. This is achieved by having an independent biasing for M2 as shown in Fig. 12 [12]. Although high gain is provided by the structure shown in Fig. 12 it uses a large number of transistors increasing the silicon area. Thus there is interest in alternative schemes. Another possibility is to use the same gate bias for both M1 and M2. Because the gate biasing is the same, it is called a self-cascode structure. A self-cascode does not require high compliance voltages at output nodes and provides high

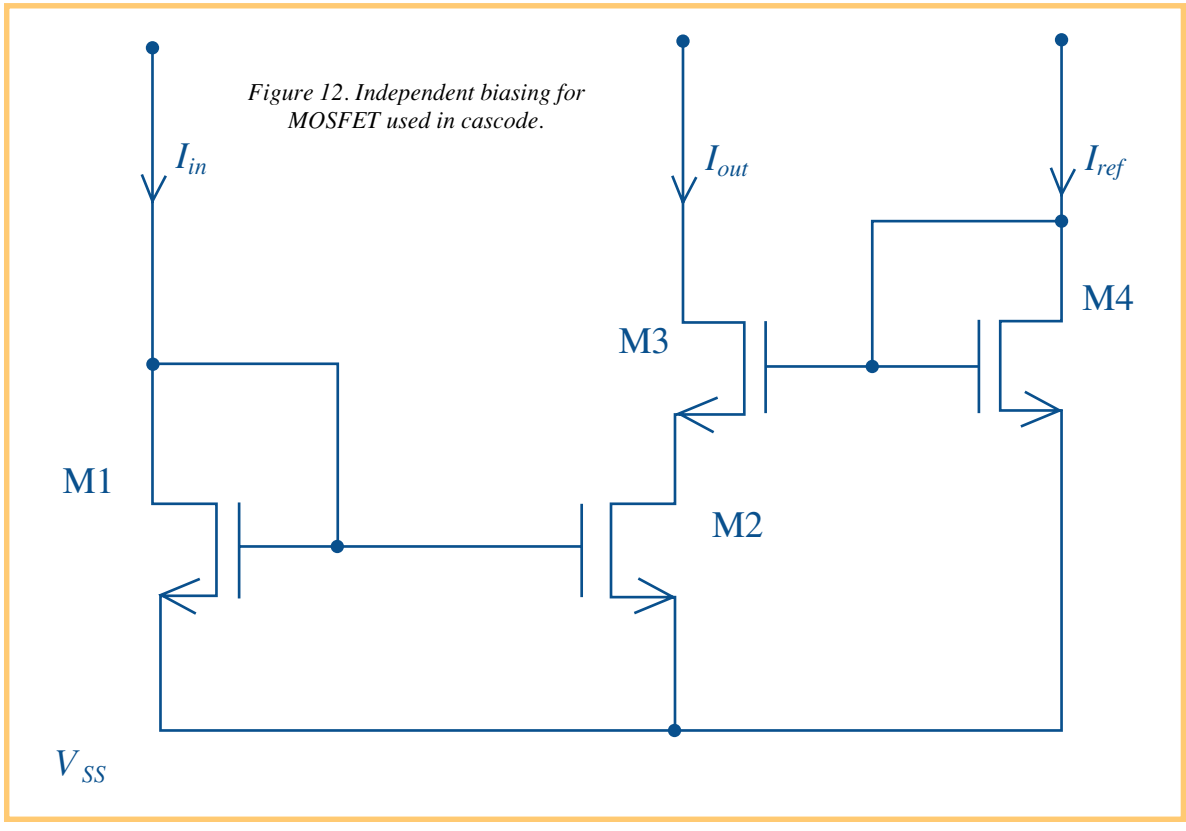


Figure 12. Independent biasing for MOSFET used in cascode.

output impedance to give high output gains. This approach has potential applications in low voltage design.

A self-cascode is a 2-transistor structure as shown in Fig. 13 (a). This structure can be treated as a single composite transistor as shown in Fig. 13 (b). The composite structure has much larger effective channel length and the effective output conductance is much lower. The lower transistor M1 is equivalent to a resistor whose value is input dependent. For optimal operation, the *W/L* ratio of M2 is kept larger than that of M1, that is, $m > 1$. For the composite transistor, the effective transconductance ($g_m(effective)$) will be g_{m2} / m, which is equivalent to the transconductance of M1 (g_{m1}). Now the drain current (I_D) through M1 and M2 will be $\beta_{effective} (V_{in} - V_T)^2 / 2$, where $\beta_{effective}$ equals $\beta_1\beta_2 / (\beta_1 + \beta_2)$, which can be approximated by β_1 when m is large [9].

The voltage between source and drain of M1 is small, and there is no appreciable difference between the V_{DSAT} of composite and simple transistors; and a self-cascode can be used in low voltage operation. For a self-cascode $V_{DSAT} = V_{DSATM2} + V_{DSATM1}$.

The operating voltage of a regular cascode is much higher than that of a self-cascode. The advantage offered by self-cascode structure is that it offers high output impedance similar to that of a cascode structure while output voltage requirements are similar to those of a single transistor.

A current mirror developed using self-cascode structure is shown in Fig. 14. The output current transfer

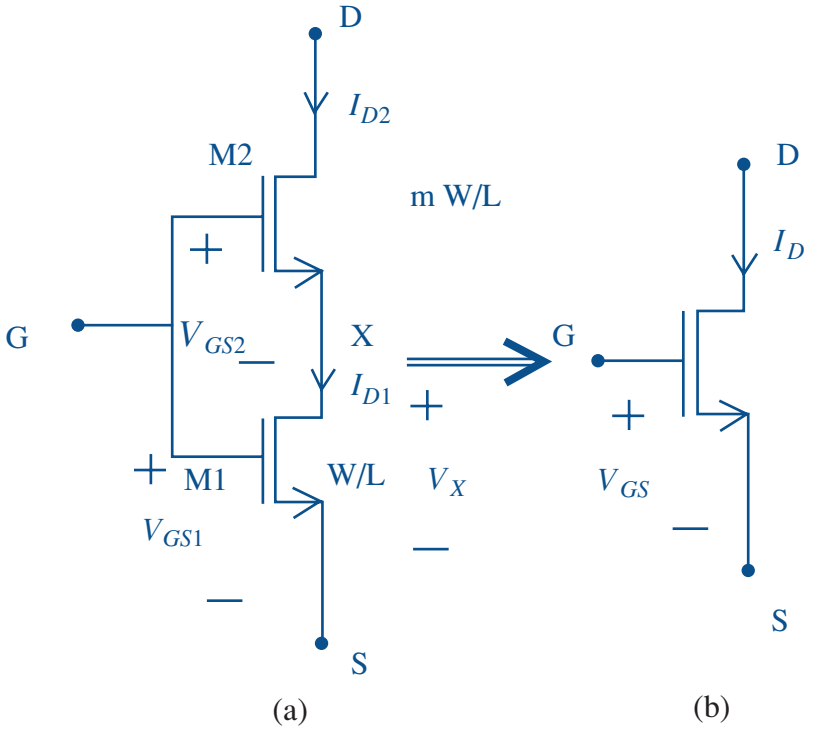
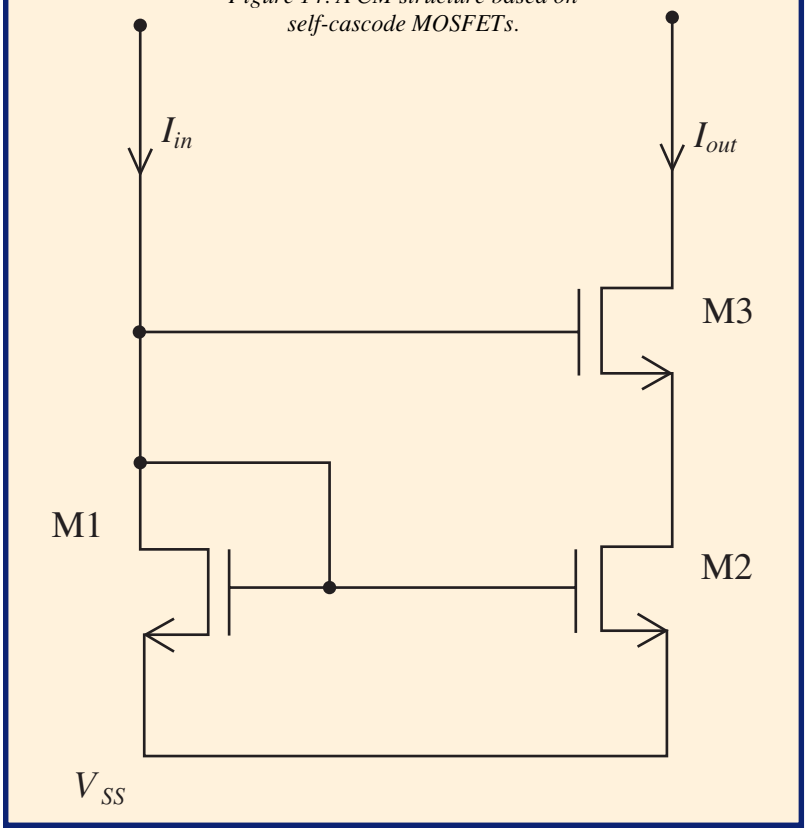


Figure 13. (a) Self-cascode structure (b) Equivalent composite transistor.

Figure 14. A CM structure based on self-cascode MOSFETs.



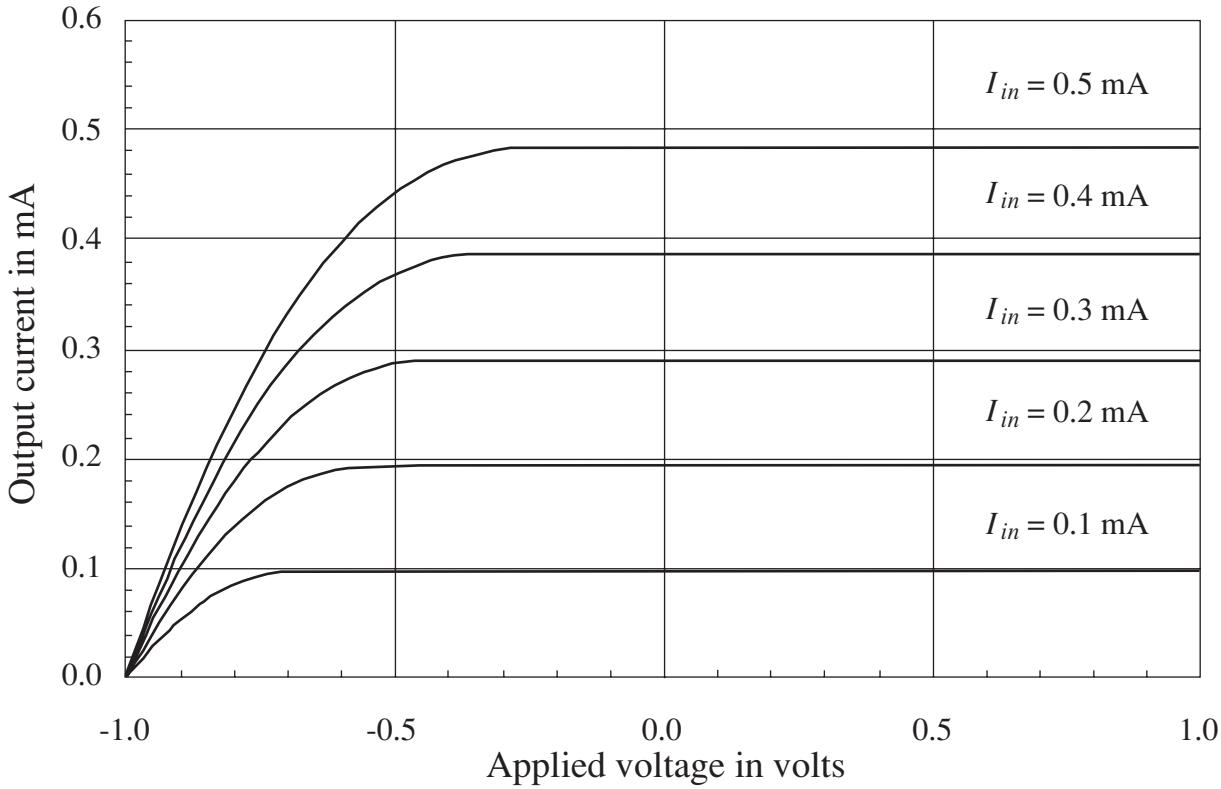


Figure 15. Output current characteristics.

characteristics of the CM are shown in Fig. 15. The output impedance of the CM is large. Input current versus input voltage characteristics are shown in Fig. 16. It may be noted that this technique does not provide any benefit in input compliance voltage at input front.

Floating Gate MOSFETs

Floating gate (FG) MOSFETs are being utilized in a number of new and exciting analog applications. These devices are available in standard CMOS technology because they are being widely used in digital circuits. Thus floating gate devices are now finding wider applications by analog researchers. As a result the floating gate devices are not only used for memories but are also being used as circuit elements. FG MOSFETs are used as analog memory elements, as part of capacitive biased circuits, and as adaptive circuit elements.

In this article, we emphasize the use of FGMOSFET devices for low voltage design. Low voltage analog design is possible through the use of FGMOSFET devices because threshold voltage tuning is possible, which reduces the headroom to a minimum. Now one can use these devices in analog circuits for designing the circuit structures, which can operate at ultra-low voltage supplies. Several such structures have been presented in the literature [12, 15–21]. Now we will discuss this aspect of floating gate MOSFETs in detail.

The gate of an FG MOSFET is normally floating, with an electrical charge residing. This charge discharges very slowly because of very good insulation properties of SiO_2. When the floating gate transistor is bathed in UV light for some time, the charge on the floating gate disappears.

For low voltage analog circuits, an

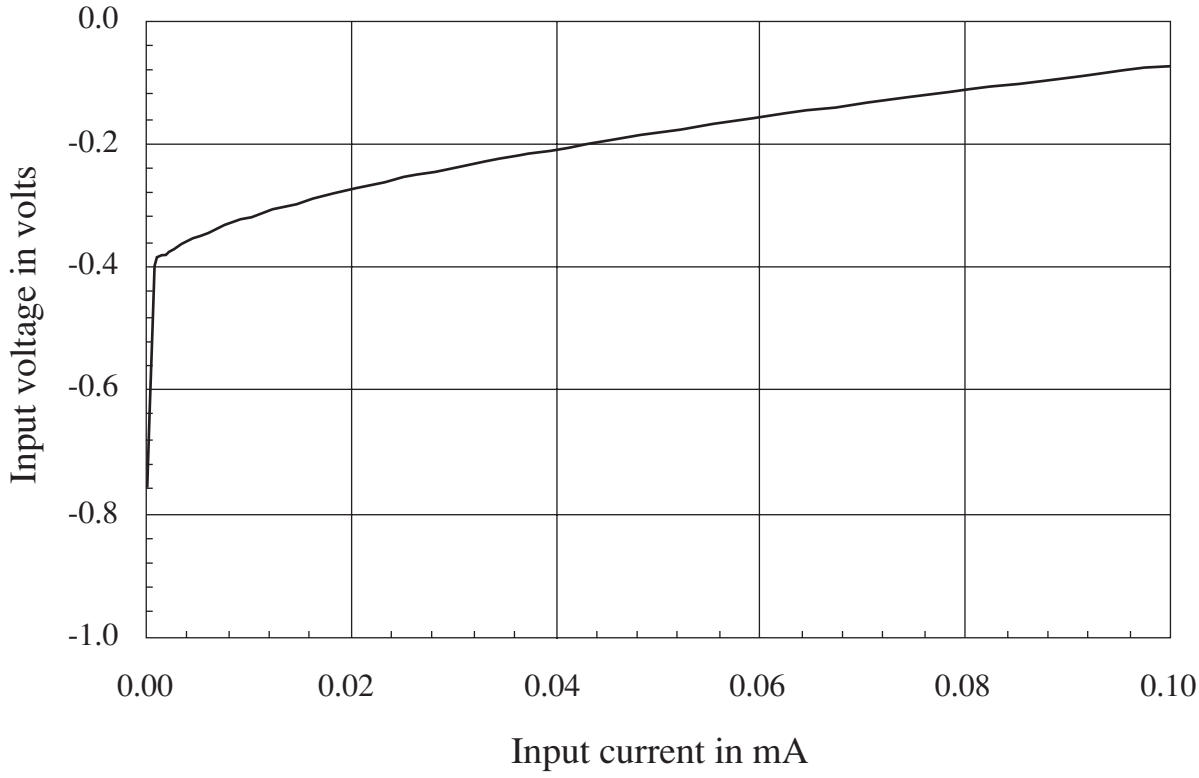


Figure 16. Input voltage characteristics.

FG is assumed to have no charge accumulation. A multi-input floating gate (MIFG) MOSFET, like the one shown in Fig. 17, is used for analog circuit design. For a 2-input MIFG MOSFET, a higher dc voltage (V_b) is applied at one gate (bias gate) and the signal is applied at a second gate (signal gate). The V_T for the MOSFET adjusts itself to a new value V_T (*equivalent*) which is $(V_T - V_b k_1) / k_2$ [16] where k_1 equals C_{G1} / C_{TOTAL} and k_2 equals C_{G2} / C_{TOTAL}. C_{G1} and C_{G2} are the capacitances between floating gates and control gates. C_{TOTAL} is the sum of the capacitances between control gates and floating gates, capacitance between floating gate and drain, capacitance between floating gate and source, and capacitance between floating gate and bulk [9, 13, 14].

We find that the V_T (*equivalent*) will be less than V_T if we select V_b, k_1 and k_2 properly. Thus we have been able to get a MOSFET where V_T (*equivalent*) is lower than the normal V_T. If $g_{m(FG)}$ is the trans-conductance seen from the floating gate, the g_m of the combined structure equals $g_{m(effective)} = k_2 g_{m(FG)}$ [9, 13, 14].

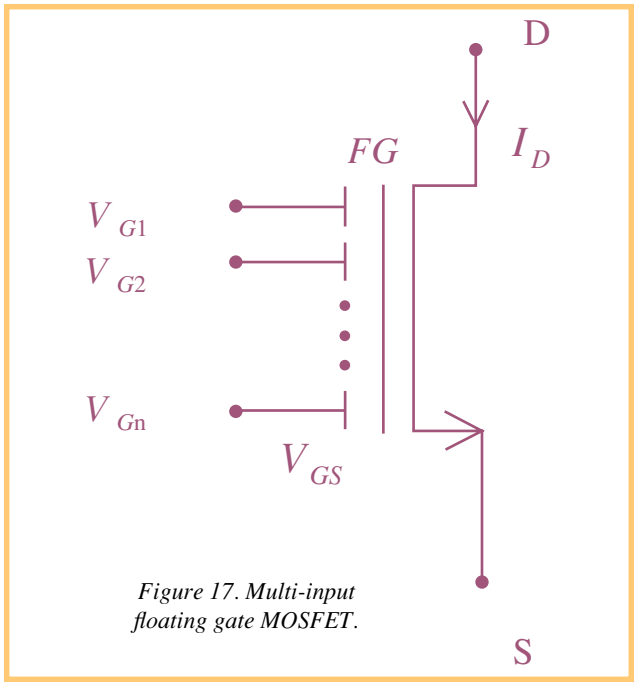


Figure 17. Multi-input floating gate MOSFET.

Here, $g_{m(effective)}$ is less than $g_{m(FG)}$ by a factor of k_2. Because there is DC and AC feedback from drain to floating gate through C_{gd}, the output impedance is less than that of a MOSFET working in the same biasing condition. When C_{gd} and g_o are the gate-to-drain capacitance and output conductance of a MOSFET, the effective output conductance $g_{o(effective)}$ of the floating gate MOSFET equals $(g_o + (C_{gd} g_m / C_{TOTAL}))$.

Thus the floating gate technology can be used in low voltage analog design. A differential pair using the floating gate technique is shown in Fig. 18. The output impedance of a floating gate transistor is lower, and only low gain structures can be realized. Further, this technique requires fabrication of the floating gates. Hence the conventional technology cannot be used, and this results in increased cost. The technique is now undergoing experimental study in low voltage analog circuit design. Researchers have used floating gate MOSFETs for the design of an ultra-low-voltage transconductor [18, 19], CMOS op amp [20], auto zeroing amplifiers, and so forth [21].

The circuit diagram of a current mirror based on FGMOS technology is shown in Fig. 19. The voltage V_b is used to adjust the threshold voltage of the input MOSFET. The functioning of the circuit is similar to that of any CM.

Level Shifter Approach

In this technique, MOSFETs are either operating in saturation or in the sub-threshold region [6, 22–25]. To understand the technique, we take the example of a simple current mirror, shown in Fig. 2, in which the input current (I_{D1}) flowing through M1 is

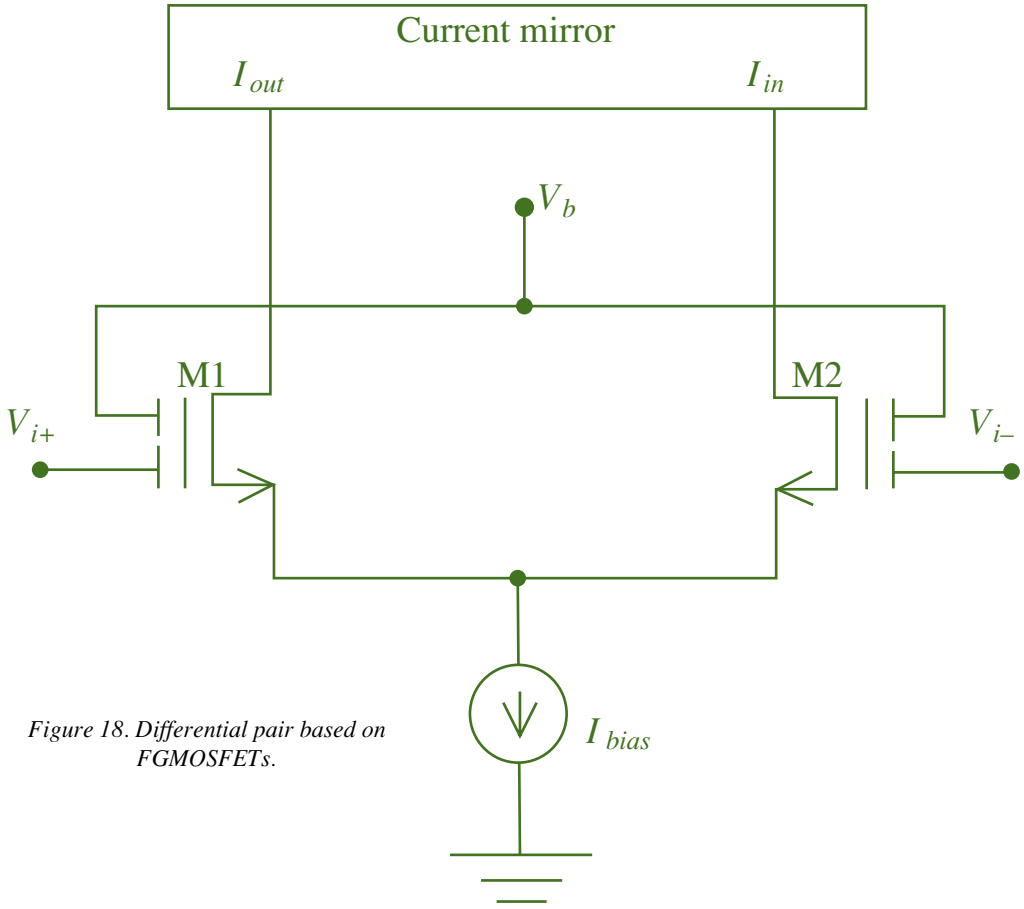


Figure 18. Differential pair based on FGMOSFETs.

$K'W(V_{GS1} - V_T)^2 / 2L$ for W, L, K', V_{GS1} and V_T having their usual meanings. Thus the minimum voltage required at the input has to be more than V_T for the operation of this circuit. So it is not possible to use these mirrors for input voltage levels less than V_T.

If this circuit is modified as shown in Fig. 20, the input voltage requirements of one V_T can be removed. The required input voltage (V_{in}) equals $V_{GS1} - V_{GS3}$. We find that the input and output resistances are the same as two MOSFET structures; but the input voltage requirements are smaller.

A drawback in this circuit is the offset current (I_{offset}) flowing into the output transistor for zero input current. One finds that V_{GS2} depends on V_{DS1} and I_{bias}. For low input current ($I_{in} \leq 1\mu A$), V_{DS2} is nearly equal to zero volts and I_{bias} alone decides V_{GS2}. I_{bias} drives V_{GS2} to be near V_{T1} even for zero I_{in}. V_{in} will also be zero. But V_{DS2} increases independently with V_B. Under this condition, a current flows through M2 (even though I_{in} is zero), because I_{bias} decides the gate bias for M2 and V_{DS2} increases independently with V_B. This condition drives M2 into the sub-threshold region and a small current, known as the offset current (I_{offset}), flows through M2. This effect is more troubling when the input current is of the order of the offset current. I_{offset} decides the range of operation for such circuits.

Interestingly, I_{bias} decides the operational regime. If I_{bias} is low enough, M3 operates in the sub-threshold region. However when I_{bias} is high, M3 operates in saturation mode. We can calculate I_{offset} accordingly.

I_{offset} is defined as the current flowing through the transistor M2 when the input current is zero. This condition establishes that M1 and M2 operate also in sub-threshold region. So, the output current through M2 is decided

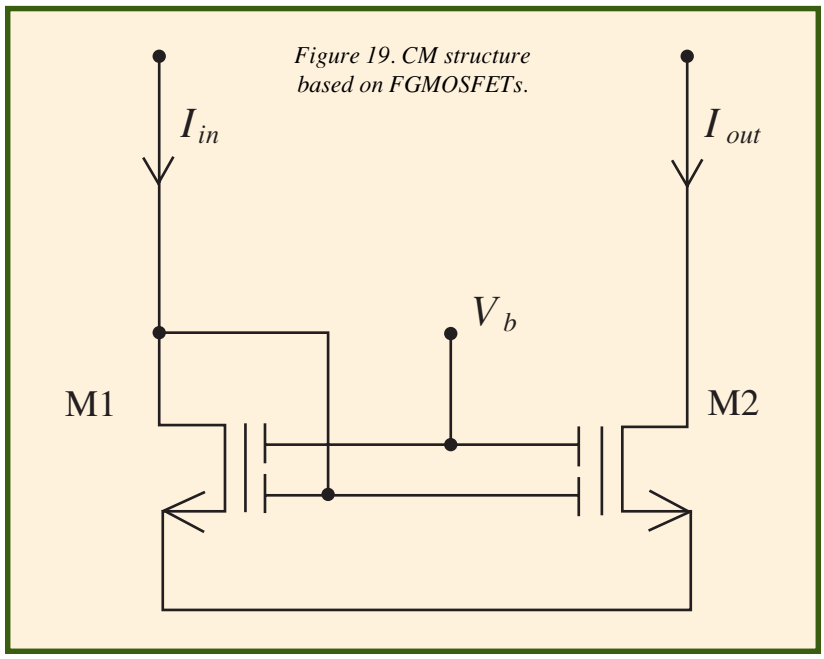


Figure 19. CM structure based on FGMOSFETs.

through this bias voltage (V_{DS2} is quite high due to applied bias voltage) [18]. Thus the offset current will be given by

$$I_{offset} \approx \frac{W_2}{L_2}\frac{L_3}{W_3}\frac{I_{DO2}}{I_{DO3}} I_{bias} \exp\left(\frac{\Delta V_T}{\eta V_{ther}}\right) \quad (4)$$

where ΔV_T is the mismatch between the threshold voltages of NMOS and

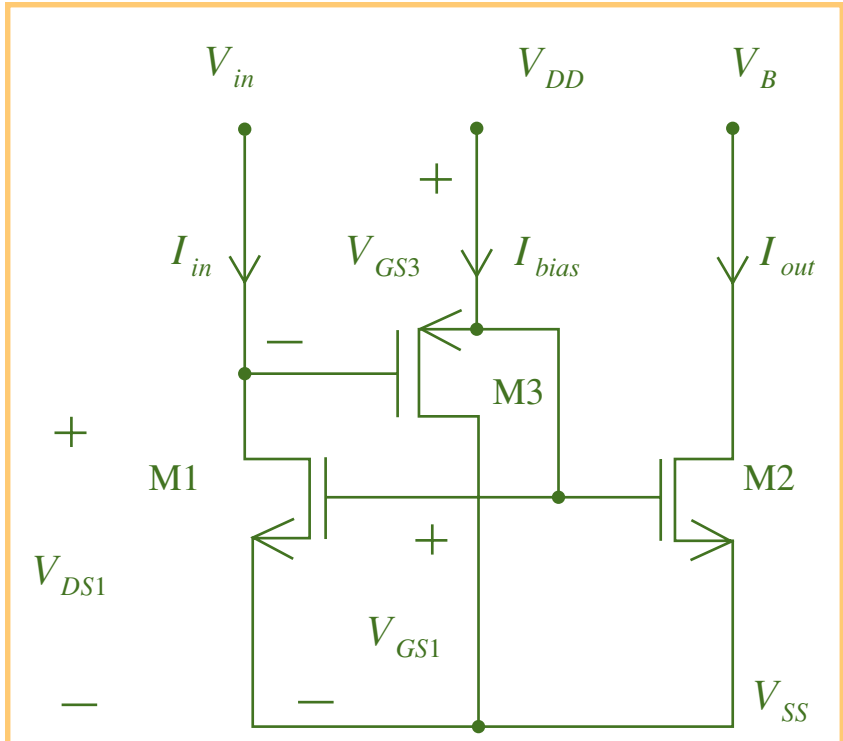


Figure 20. Modified CM based on level shifter technique.

. . . we have presented techniques which promise low voltage design. The comparative analysis of these techniques is given in Table 1. Depending upon the nature of the application, one can choose an appropriate technique or a combination of these techniques for the intended analog circuit design.

PMOS and V_{ther} equals 26mV at room temperature. When the threshold voltages of the PMOS and NMOS are perfectly matched and $I_{DO2} = I_{DO3}$, the minimum I_{offset} equals $W_2L_3I_{bias} / L_2W_3$. This can further be tailored according to the designer's specifications by choosing appropriate values for transistor aspect ratios.

When I_{bias} is sufficiently high, it drives M3 into the saturation region; but M1 will be in linear mode due to low input current. However, M2 will operate in the saturation region because the external bias voltages will decide its drain voltage. In this situation the offset current is given by

$$I_{offset} = \frac{\beta_2}{2}\left(\sqrt{\frac{2I_{bias}}{\beta_3}} + V_{TP3} - V_{TN2}\right)^2 . \quad (5)$$

For the condition where threshold voltages of PMOS and NMOS are matched, the minimum offset current is $K'_2W_2L_3I_{bias} / K'_3L_2W_3$.

Thus, I_{offset} is sufficiently high in the case when M3 is operated in the saturation region. This follows because I_{bias} is higher and K_2' / K_3' equals 3. Here K_2' and K_3' are the trans-conductance parameters ($= \mu C_{OX}$) for M2 and M3 respectively.

In this configuration, the number of MOSFETs increases, which is likely to increase the power dissipation. The most desirable characteristics include higher bandwidth at low voltage. The input resistance is also low, which is desirable for current mode circuits. These circuits have the capability for rail-to-rail operation, both at input and output ends.

Use of Low Voltage Analog Cells

Inasmuch as all analog circuits can be built using MOSFETs, and the properties of the MOSFETs determine the circuit properties, similarly all analog circuits can be decomposed into several sub-circuits, which may be regarded as analog cells. The properties of these analog cells decide the characteristics of the resultant circuit structure. If these analog cells can be designed to operate at low voltages, then the circuits in which they are used can be expected to operate at low voltages as well. This technique is now gaining more attention and has been used by the authors in the design of various low voltage analog circuits [9, 28, 29]. As an example of the technique we have used a low voltage CM [9, 13] in the design of low voltage analog circuit structures.

The circuit given in [30] has been modified to include low voltage CMs [22]. The resultant structure is now capable of operating at much lower voltages. This structure is then suitably modified to act as different types of CCs. These resultant structures are found to be high performing and modular in nature [29].

Conclusions

In this paper, we have presented techniques which promise low voltage design. The comparative analysis of these techniques is given in Table 1. Depending upon the nature of the ap-

plication, one can choose an appropriate technique or a combination of these techniques for the intended analog circuit design. Further, all analog circuits can be decomposed into several subcircuits, which may be termed analog cells. If these analog cells can be designed to operate at low voltages, using any of the techniques meant for low voltage design, then the circuits in which they are used can be expected to operate at low voltages. In this way one can design a low voltage analog circuit. Such techniques are now gaining more attention and have been used by the authors in the design of various low voltage analog circuits. The resultant structures are high performing and modular in nature.

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Table 1. Characteristics of Various Techniques for CMOS Design

Technique	Available BW	Supply Voltage Requirements	Power Consumption	Technology Requirements
Sub-threshold MOSFETs	Low	$\approx 2V_T$	Low	Standard
Bulk-driven MOSFETs	Low	$\approx 2V_T$	High	Special
Self-Cascode MOSFETs	Medium	$> 2V_T$	High	Standard
Floating gate MOSFETs	Medium	$< 2V_T$	Medium	Special
Level shifter MOSFETs	High	$< 2V_T$	Medium	Standard
Use of low voltage cells	High	$< 2V_T$	Medium	Standard

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