
# Texas A&M University
# Department of Electrical and Computer Engineering

**ECEN 607, Spring 2017**

**Homework #1**

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## Problem 1

Use any size technology and generate the equivalent plot (see around page 21 Lect. #1) of various parameters versus the inversion level. i.e. $f_T$ vs $i_f$, power consumption, (W/L) vs $i_f$. Also add a trace for Vdsat vs $i_f$ in the same plot.

$$Id = \frac{n*gm*\emptyset_t*(1+\sqrt{1+i_f})}{2} \quad (1)$$

$$f_T = \frac{\mu*\emptyset_t*(\sqrt{1+i_f}-1)}{\pi L^2} \quad (2)$$

$$\frac{W}{L} = \frac{gm}{\mu*C_{ox}*\emptyset_t*(\sqrt{1+i_f}-1)} \quad (3)$$

$$V_{dsat} \approx \emptyset_t * \left(\sqrt{1+i_f}+3\right) \quad (4)$$

Id is the drain current of transistor, gm is the trans-conductance in saturation region. n is the slope factor, $\emptyset_t$ is thermal voltage, approximately 25.85 mV ≈ 26 mV at room temperature 300K. $i_f$ represents the inversion level as $i_f = Id/I_s$, where $I_s = \frac{1}{2}\mu * C_{ox} * n * \left(\frac{W}{L}\right) * \emptyset_t{}^2$, $i_f < 1$ means the transistor is in weak inversion, $i_f >> 1$ means in strong inversion. For any size technology, the normalization equation versus the inversion level is determined by the order of equations. All the parameters could be normalized by setting the value as 1 when $i_f = 1$.

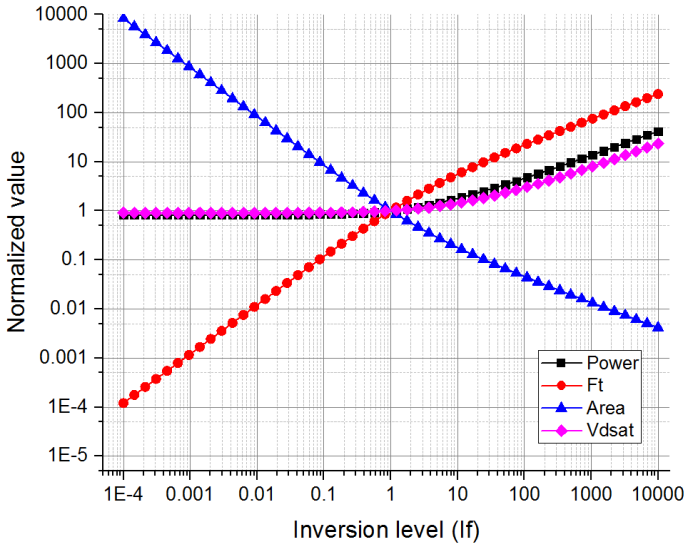


Figure 1. Normalized power, ft, area and Vdsat plot vs. if.

We can conclude that a moderate range of $i_f$ is set to compromising performance between power, speed($f_T$) area and signal swing ($V_{dsat}$), particularly in low power and low voltage designs.

## Problem 2

Extract the parameters of transistors PMOS and NMOS for the ACM model, that is one equation all regions. See Ref. 6 on Lect. #1. Consider the 65nm and 130 nm CMOS technology and if = 9. Discuss how the parameters are extracted. Provide a table summarizing results of the extracted parameters. Discuss the results.

A. Extraction of $I_S$

$I_S$ is the normalization current when over-drive voltage is equal to thermal voltage, therefore $I_S$ is defined by:

$$Is = \mu * C_{ox} * n * \frac{\emptyset_t{}^2}{2} * \frac{W}{L} \tag{5}$$

Simulation circuit is shown in figure 2. When transistor is in strong inversion, $i_f = \frac{Id}{I_s} \gg 1$, $I_S$ can be determined from following equation. [1]

$$Is = Id * (\frac{\Delta I/I}{2*\Delta V_S/\emptyset_t})^2 \text{ for } \Delta I \ll I \tag{6}$$

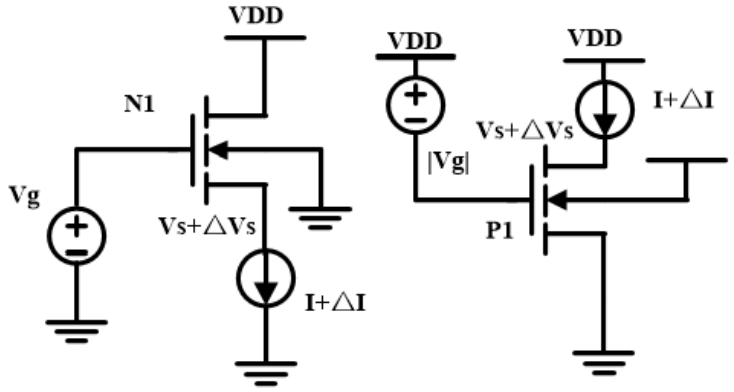


Figure 2. Extraction of $I_S$ circuit simulation schematic ($i_f > 50, \frac{W}{L} = 5$)

Table 1. Extraction of $I_S$ and comparison

| PTM CMOS | NMOS | PMOS |
|---|---|---|
| **65 nm** | 0.936 μA | 0.237μA |
| **130 nm** | 1.227μA | 0.307μA |

B. Extraction of Vth0

Vth0 is the threshold voltage under zero-bias. A drain current equivalent to 3*$I_S$ is provided to a saturated MOSFET under diode connected configuration. As shown in figure 3, measured Vg is representing the Vth0.

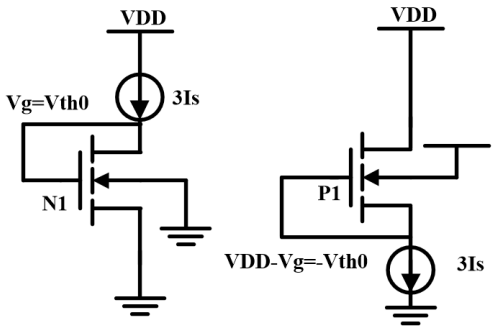


Figure 2. Extraction of Vth0 circuit simulation schematic (Id=3*$I_S$)

Table 2. Extraction of Vth0 and comparison

| PTM CMOS | NMOS | | PMOS | |
|---|---|---|---|---|
| **Model** | **ACM** | **BSIM4** | **ACM** | **BSIM4** |
| **65 nm** | 313.7 mV | 423 mV | -294.4 mV | -365 mV |
| **130 nm** | 295.4 mV | 378.2 mV | -270.8 mV | -321 mV |

C. Extraction of GAMMA(γ)

$$\gamma = (n-1) * 2 * \sqrt{2 * \emptyset_F + V_p},\ 2 * \emptyset_F = 0.7 \qquad (7)$$

Where $V_P$ is the pinch-off voltage and n=($dV_G$ / $dV_P$), therefore these two parameter should be extracted before γ.

i. Extraction of $V_P$ and n

Setting drain current equal to 3*$I_S$ as figure 3. then $V_P = V_S$ by sweeping $V_S$. a relation between $V_G$ and $V_P$ is plotted, and its derivative equation will determine n.

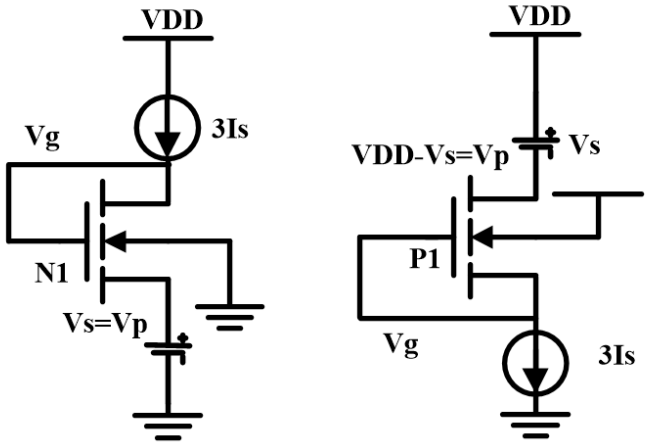


Figure 3. Extraction of $V_P$ and n circuit simulation schematic (Id=3*$I_S$)

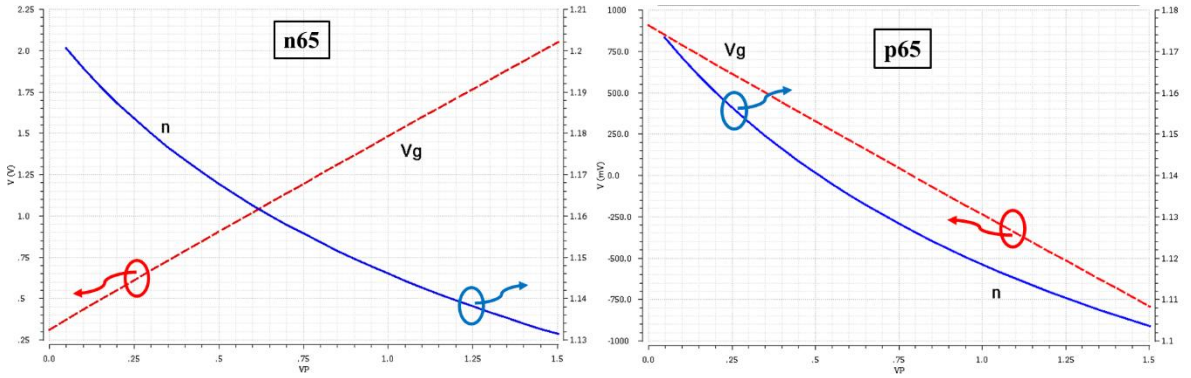


Figure 4. Extraction of n and Vg vs. Vp of 65nm technology.

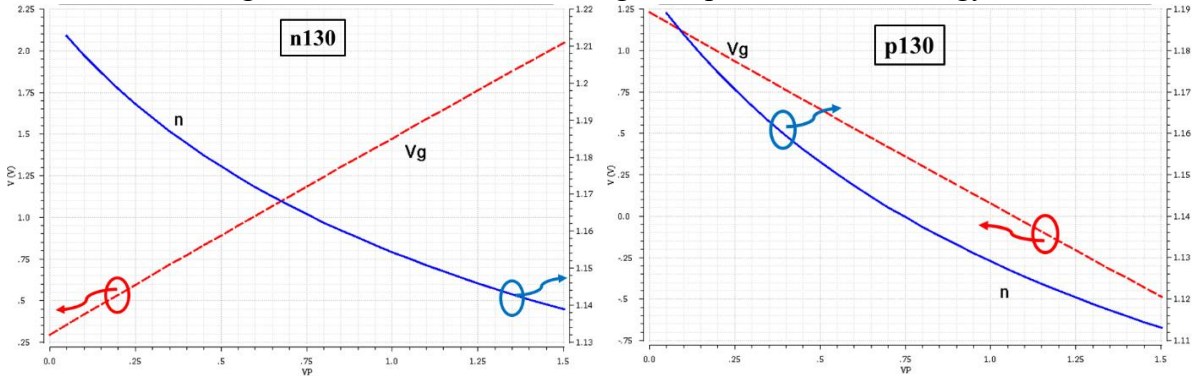


Figure 4. Extraction of n and Vg vs. Vp of 130nm technology.

ii. Calculation of γ by Vp and n.(For Vp=Vs=0.75 V)

By setting Vp=0.75 for simplicity in calculation and moderate Vg values.
For 65nm: n of NMOS is 1.1557 and n of PMOS is 1.12833.

$$\gamma\_nmos = (1.1557 - 1) * 2 * \sqrt{0.7 + 0.75} = 0.375 \ V^{1/2}$$

$$\gamma\_pmos = (1.12833 - 1) * 2 * \sqrt{0.7 + 0.75} = 0.309 \ V^{1/2}$$

For 130nm: n of NMOS is 1.1647 and n of PMOS is 1.13975.

$$\gamma\_nmos = (1.1647 - 1) * 2 * \sqrt{0.7 + 0.75} = 0.397 \ V^{1/2}$$

$$\gamma\_pmos = (1.13975 - 1) * 2 * \sqrt{0.7 + 0.75} = 0.337 \ V^{1/2}$$

Table 3. Extraction of γ and comparison

| Technology | NMOS | PMOS |
|---|---|---|
| **65 nm** | 0.375 $V^{0.5}$ | 0.309 $V^{0.5}$ |
| **130 nm** | 0.397 $V^{0.5}$ | 0.337 $V^{0.5}$ |

D. Extraction of $\mu_0$ and θ (THETA)

μ0 is the carrier mobility for low values of the electric field. θ is the ACM fitting parameter which accounts for the mobility variation.

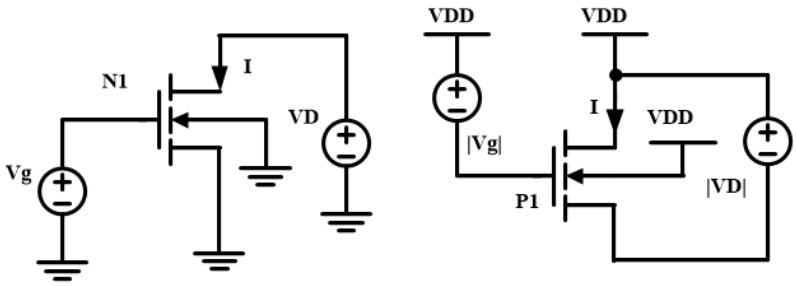


Figure 5. Extraction of $\mu_0$ and $\theta$ circuit schematic (W/L=5).

In the DC simulation, $I_D$ is obtained as a function of $V_{GS}$ with the transistor biased from the linear region (Vds = 100mV) to strong inversion. Therefore, $V_{GS}$ is swept from 2*Vth0 to VDD.

$$\mu = \frac{\mu_0}{1+\theta(V_G - V_{tho})} \tag{8}$$

By sweeping Vgs and plot the $\frac{1}{\mu Cox\left(\frac{W}{L}\right)} \cong (V_{GS} - Vth0) * \frac{V_{DS}}{I_D}$, with first order estimation, a function Y=A*X+B could be employed to fit the plotted curve. With:

$$\mu_0 = \frac{1}{Cox\left(\frac{W}{L}\right) * B} \tag{9}$$

$$\theta = \mu_0 * Cox * \left(\frac{W}{L}\right) * A \tag{10}$$

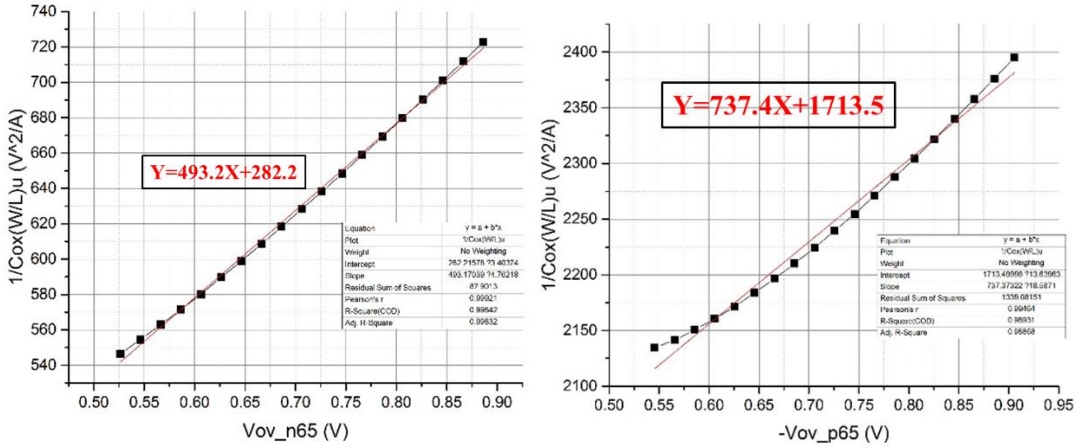


Figure 6. Extraction of $\frac{1}{\mu Cox\left(\frac{W}{L}\right)}$ of 65nm with first order curve-fitting

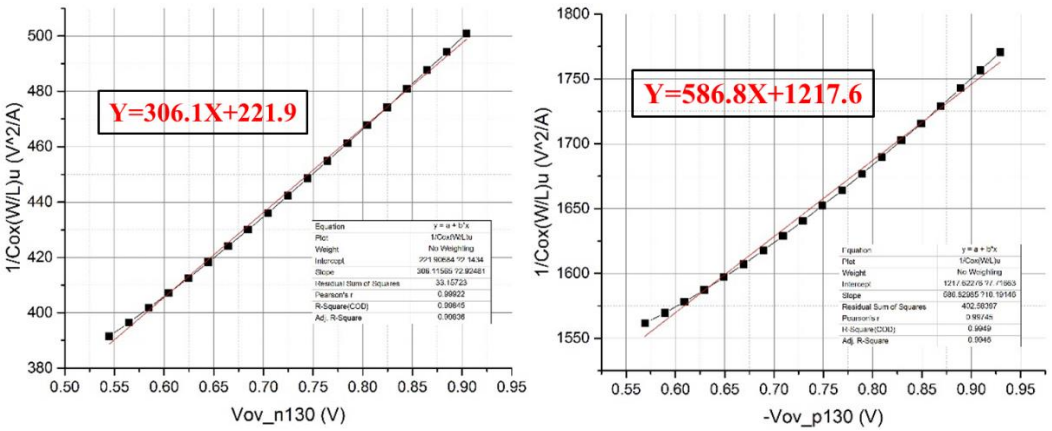

Figure 7. Extraction of $\frac{1}{\mu Cox\left(\frac{W}{L}\right)}$ of 130nm with first order curve-fitting

Table 4. Extraction of Y=A*X+B

| Technology | NMOS | | PMOS | |
|---|---|---|---|---|
| | A | B | A | B |
| 65 nm | 493.17 | 282.216 | 737.37 | 1713.5 |
| 130 nm | 306.116 | 221.907 | 586.83 | 1217.622 |

With the table 4 above and equation (9) and (10), $\mu_0$ and $\theta$ (THETA) are provided in table 5. All the transistor size ratio W/L=5 and Cox is calculated by $\frac{\varepsilon_{ox}}{tox}$, and tox value is provided in BSIM model.

$$\varepsilon_{ox} = \varepsilon * \varepsilon_{sio2} \approx 8.854 * 10^{-12} * 3.97 = 3.51504\text{E-}11\ \text{F/m}$$

Table 5. Extraction of Cox (F/m$^2$)

| Technology | NMOS | PMOS |
|---|---|---|
| 65 nm | 1.90E-02 | 1.80E-02 |
| 130 nm | 1.56E-02 | 1.50E-02 |

Table 6. Extraction of $\mu_0$ and $\theta$

| Technology | NMOS | | PMOS | |
|---|---|---|---|---|
| Parameters | $\mu_0$ (m^2/V*s) | $\theta$ | $\mu_0$ (m^2/V*s) | $\theta$ |
| 65 nm | 3.73E-02 | 1.75E+00 | 6.48E-03 | 4.30E-01 |
| 130 nm | 5.77E-02 | 1.38E+00 | 1.10E-02 | 4.82E-01 |

E. Extraction of SIGMA

SIGMA is a parameter to evaluate the DIBL (Drain-Induced-Barrier-lowering). The inversion layer is affected by the voltage of drain and source. This effect is more severe in weak inversion and SIGMA is defined as:

$$SIGMA = \sigma * (Leff)^2 \quad (11)$$

$$Vth = Vth0 - \sigma * (V_D + V_S)/2 \quad (12)$$

Simulation schematic is presented as figure 8 with Ib = 0.1*Is for weak inversion and varying $V_D$ from 200 mV to 400 mV.

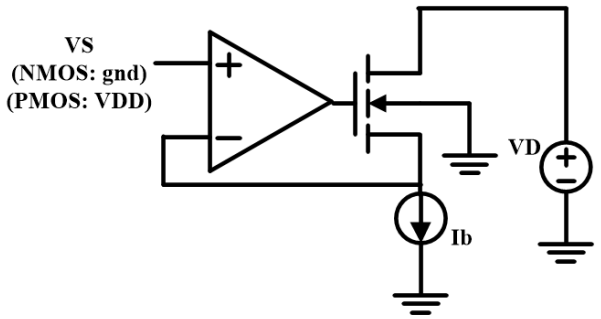


Figure 8. Extraction of SIGMA simulation principle schematic (NMOS)

$$\sigma = -\Delta V_G/\Delta V_D \quad (13)$$

$$Leff = L_{draw} + xl, xl\ \ is\ \ from\ \ BSIM \quad (14)$$

Simulation results are showing the SIGMA value for different transistors in figure 9.

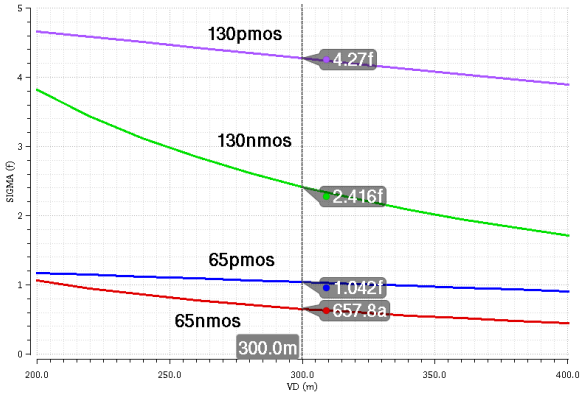


Figure 9. Extraction of SIGMA vs. $V_D$ for different transistors.

Table 7 summarize the value of SIGMA and provides a comparison.

Table 7. Extraction of SIGMA ($m^2$) when $V_D$=300 mV

| Technology | NMOS | PMOS |
|---|---|---|
| 65 nm | 658E-15 | 1042E-15 |
| 130 nm | 2416E-15 | 4270E-15 |

F. Extraction of PCLM (=LAMBDA)

PCLM is a parameter to represent the reduction of effective length of channel due to the increase of drain voltage $V_D$. The PCLM parameter can be extracted by plotting the Early voltage ($V_A$) as function of $V_{DS}$-$V_{DSSAT}$. And $V_A$=$I_D$*$dV_D$/$dI_D$. Figure 10 shows the simulation schematic for NMOS, and the $i_f$=200, the length is all set to be 10 times the minimum transistor length and keep ratio W/L =5 for better comparison. In 65nm, W/L=3.25 um/650 nm and in 130nm, W/L= 6.50 um/1.30 um.

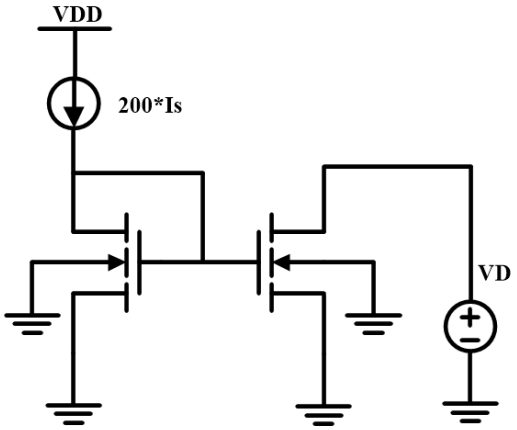


Figure 10. Extraction of PCLM simulation schematic principal (NMOS)

$$\Delta L = P_{CLM} * L_C * \ln\left(1 + \frac{V_{DS}-V_{DSAT}}{L_C * U_{CRIT}}\right) \quad (15)$$

$$U_{CRIT} = \frac{V_{MAX}}{U_0}, V_{MAX} \ is \ vsat \ from \ BSIM \quad (16)$$

$$\varepsilon \approx \frac{\emptyset_t}{L_{eff} * U_{CRIT}} \ and \ L_C = \sqrt{\varepsilon_{si} * \frac{Xj}{Cox}}, \text{ Xj is from BSIM} \quad (17)$$

$$P_{CLM} = \frac{L_{eff}}{\left(\frac{dV_A}{dV_{DS}}\right) * L_C} * \left(\frac{\emptyset_t}{L_{eff} * U_{CRIT}}\right) \quad (18)$$

$$V_{DSAT} = \emptyset_t * [\ln\left(1 + \frac{\sqrt{1+i_f}-1}{0.5*\varepsilon*i_f}\right) + \sqrt{1+i_f} - 1] \quad (19)$$

With $V_A$=$I_D$*$dV_D$/$dI_D$, a function of $V_A$ versus $V_{DS}$-$V_{DSAT}$ is plotted in figure 11 and 12. Then $\frac{dV_A}{dV_{DS}}$ is extracted with first order curve fitting as the slope.

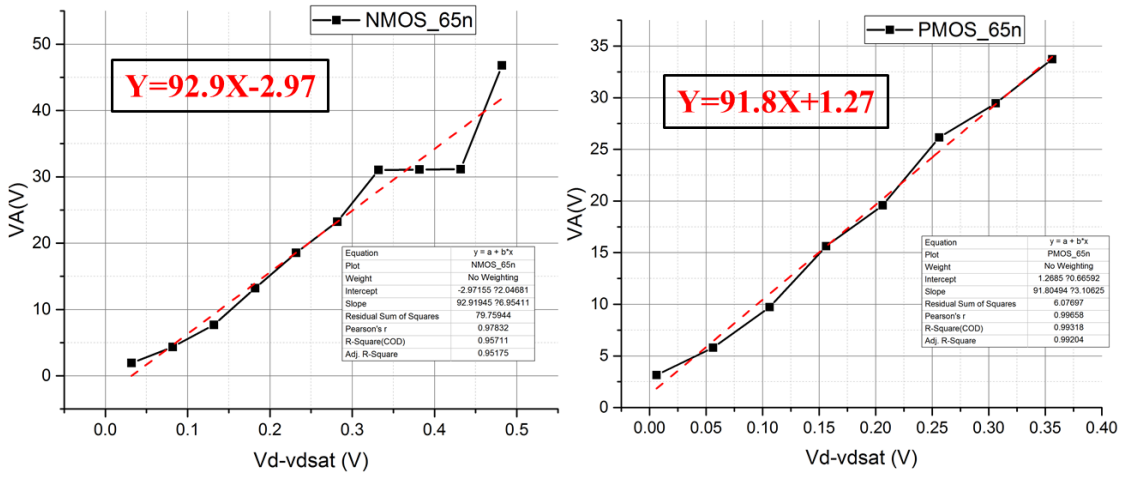


Figure 11. Extraction of $\frac{dV_A}{dV_{DS}}$ function vs. $V_{DS}$-$V_{DSAT}$ (65nm)

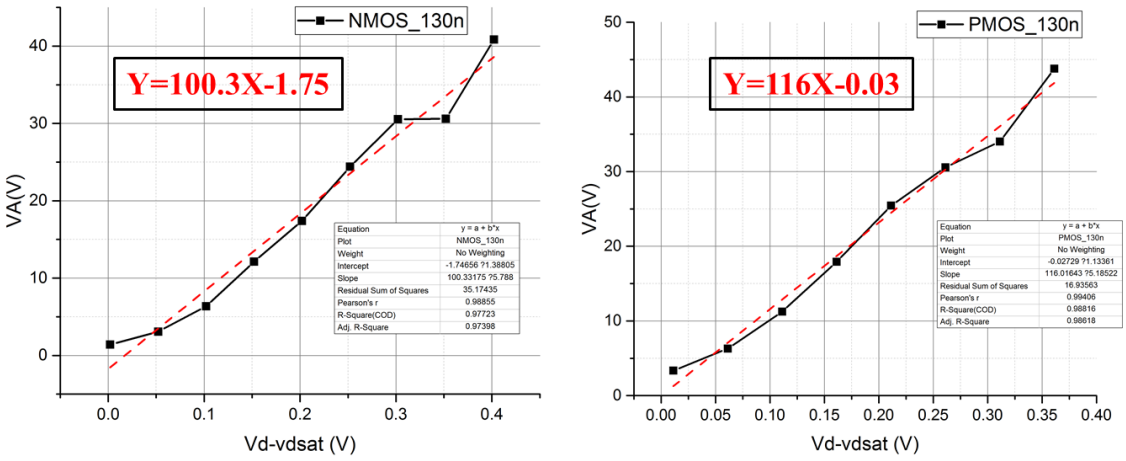


Figure 11. Extraction of $\frac{dV_A}{dV_{DS}}$ function vs. $V_{DS}$-$V_{DSAT}$ (130nm)

Despite of some nonlinearity in the function, which may be introduced by simulation step accuracy, the $\frac{dV_A}{dV_{DS}}$ is extracted. One major observation is for relative large value of $V_{DS}$-$V_{DSAT}$, the slope will vary from predicted curve, which means in strong inversion this extracted value is less accurate as in weak inversion. And with all the equation from 15 to 19. PCLM is calculated and list in table 8.

Table 8. Extraction of PCLM ($V^{-1}$)

| Technology | NMOS | PMOS |
|---|---|---|
| 65 nm | 0.26 | 0.12 |
| 130 nm | 0.30 | 0.12 |

| | 65nm NMOS | 65nm PMOS | 130nm NMOS | 130nm PMOS |
|---|---|---|---|---|
| Cox (F/m$^2$) @ BSIM | 0.019 | 0.018 | 0.016 | 0.015 |
| Is (μA) | 0.936 | 0.237 | 1.227 | 0.307 |
| Vth0 (mV) | 313.7 | -294.4 | 295.4 | -270.8 |
| n | 1.156 | 1.128 | 1.165 | 1.140 |
| $\gamma$ (V$^{1/2}$) | 0.375 | 0.309 | 0.397 | 0.337 |
| $\mu_0$ (m$^2$/V*s) | 0.037 | 0.006 | 0.058 | 0.011 |
| $\theta$ (V$^{-1}$) | 1.75 | 0.43 | 1.38 | 0.48 |
| SIGMA (f) | 0.658 | 1.042 | 2.416 | 4.270 |
| PCLM=λ (V$^{-1}$) | 0.26 | 0.12 | 0.30 | 0.12 |

## Problem 3.

(a) Design, using conventional quadratic saturation transistor equation, a simple two stage trans-conductance amplifier for the following specs and using 0.13um technology

VDD = 1.2 V

VSS = 0 V

Gain > 50 dB

CMRR > 55 dB

GBW greater or equal to 4 MHz

PM > 60º

CL = 25 pF

Power < 500 μW

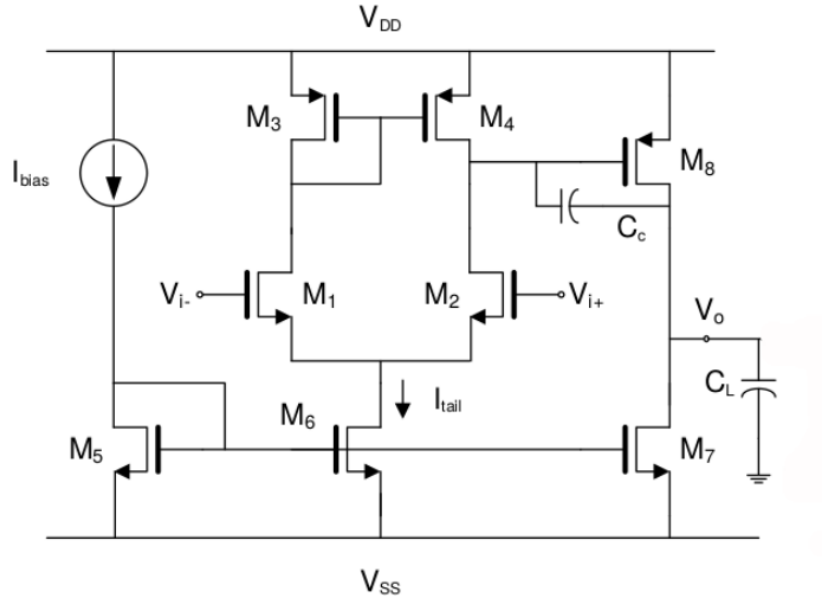


Figure 12. Conventional two-stage amplifier with miller compensation.

From problem 2 solution, parameter extraction of 130 nm:

NMOS: Vth= 295 mV, Kn=$\mu_0 * Cox$ =0.058*0.016=928uA/V$^2$, $\lambda = 0.30$ V$^{-1}$

PMOS: Vth=-271 mV, Kn=$\mu_0 * Cox$ =0.011*0.015=165uA /V$^2$, $\lambda = 0.12$ V$^{-1}$

Design procedure with conventional hand calculation model:

For design margin, GBW is designed to be 5.10 MHz = 32M rad/sec

For 60° phase margin, p2 > tan (60°) *GBW=1.73*32M = 55.5M ≈ 56M rad/sec
With miller compensation OTA system equation:

$$Av=Av_1*Av_2=[gm_{1,2}*(ro_4//ro_2)]*[gm_8*(ro_8//ro_7)] \quad (3.1)$$

$$p1=1/[(ro_4//ro_2)*gm_8*(ro_8//ro_7)*Cc] \text{ (LHP)} \quad (3.2)$$

$$p2=gm_8/C_L \text{ (LHP)} \quad (3.3)$$

$$z1=gm_8/Cc \text{ (RHZ)} \quad (3.4)$$

$$GBW=Av*p1=gm_{1,2}/Cc \quad (3.5)$$

$$CMRR=Av/[1/(2*ro_6*gm_{3,4})*Av2]=2*ro_6*gm_{3,4}*Av_1$$
$$=2*ro_6*gm_3*gm_{1,2}*(ro_4//ro_2) \quad (3.6)$$

p2= gm8/$C_L$=56M rad/sec, $C_L$=56*$10^{-12}$ F: $gm_8$=56*$10^6$*25*$10^{-12}$=1.4*$10^{-3}$ S
Assuming Vov=0.1 V, $I_{D8}$=$gm_8$*Vov/2=1.4*$10^{-3}$*0.1/2=70 uA
With system stability consideration, RHZ should be much larger than second pole. Therefore Cc<< $C_L$ is needed to guarantee target phase margin, choosing Cc= 0.04*$C_L$= 1 pF
For GBW= $gm_{1,2}$/Cc = 32M rad/sec, Cc=1*$10^{-12}$ F, $gm_{1,2}$=32*$10^6$*1*$10^{-12}$=32*$10^{-6}$ S
Assuming Vov=0.1 V, $I_{D1,2}$=$gm_{1,2}$*Vov/2=32*$10^{-6}$*0.1/2=1.6 uA
Therefore:
$ro_6$=1/λn ∗$I_{D6}$=1/(0.3*3.2u) =1.04Mohm, gm6=2* $I_{D6}$/Vov=32*$10^{-6}$ S (Vov=0.2 for current mirror)
$ro_4//ro_2$= (1/λp ∗$I_{D4}$ // 1/λn ∗$I_{D2}$) =(0.12*1.6u)$^{-1}$//(0.30*1.6u)$^{-1}$=5.21Mohm//2.08Mohm=1.5Mohm
$ro_8//ro_7$= (1/λp ∗$I_{D8}$ // 1/λn ∗$I_{D7}$) =(0.12*70u)$^{-1}$//(0.30*70u)$^{-1}$=120 Kohm//48 Kohm=34 Kohm
AV=[$gm_{1,2}$*($ro_4//ro_2$)] *[$gm_8$*($ro_8//ro_7$)] = 32*$10^{-6}$*1.5*$10^6$*1.4*$10^{-3}$*34*$10^3$=48*47.6=67 dB
CMRR=2*ro6*gm3*gm1,2*(ro4//ro2)=2*1.04M*32u*32u*1.5M=70 dB
Power=1.2*(2*3.2uA+70uA) =1.2*73.2u=96.3 uW
Transistor sizing:

$$(W/L)_{1,2}=\frac{2Id}{u*cox*Vov^2}=2*\frac{1.6u}{928u*0.01}\approx 0.35=\frac{210nm}{600nm}$$

$$(W/L)_{3,4}=\frac{2Id}{u*cox*Vov^2}=2*\frac{1.6u}{165u*0.01}\approx 2=\frac{1.20um}{600nm}$$

$$(W/L)_{5,6}=\frac{2Id}{u*cox*Vov^2}=2*\frac{3.2u}{928u*0.04}\approx 0.17=\frac{210nm}{1.20um}$$

$$(W/L)_7=(W/L)_{5,6}*70u/3.2u=21.875*(W/L)_{5,6}=\frac{4.60um}{1.20um}$$

$$(W/L)_8=\frac{2Id}{u*cox*Vov^2}=2*\frac{70u}{165u*0.01}\approx 85=\frac{51um}{600nm}$$

Table 9. Spec summary with conventional design method

| Parameter | Calculation | Simulation |
|---|---|---|
| Gain | 67 dB | 58.88 dB |
| GBW | 5.1 MHz | 4.35 MHz |
| PM | 60° | 60° |
| CMRR | 70 dB | 64 dB |
| Power | 96 uW | 213 uW |
| SR | 3.2 V/us | SR+:6.1 V/us SR-:5.1 V/us |
| PSR (Av(dm)/Av(vdd)) | NA | @DC: 88.2 dB<br>@100 kHz: 35.3 dB |
| 1% Settling time | NA | ST+:130ns ST-:241ns |

(b) Design procedure with ACM model:

Recall the equation above:

$$Av=Av_1*Av_2=[gm_{1,2}*(ro_4//ro_2)]*[gm_8*(ro_8//ro_7)] \quad (3.1)$$

$$p1=1/[(ro_4//ro_2)*gm_8*(ro_8//ro_7)*Cc] \text{ (LHP)} \quad (3.2)$$

$$p2=gm_8/C_L \text{ (LHP)} \quad (3.3)$$

$$z1=gm_8/Cc \text{ (RHZ)} \quad (3.4)$$

$$GBW=Av*p1=gm_{1,2}/Cc \quad (3.5)$$

$$CMRR=Av/[1/(2*ro_6*gm_{3,4})*Av2]=2*ro_6*gm_{3,4}*Av_1$$
$$=2*ro_6*gm_3*gm_{1,2}*(ro_4//ro_2) \quad (3.6)$$

p2= gm8/$C_L$=56M rad/sec, $C_L$=56*$10^{-12}$ F: $gm_8$=56*$10^6$*25*$10^{-12}$=1.4*$10^{-3}$ S

With system stability consideration, RHZ should be much larger than second pole. Therefore Cc<< $C_L$ is needed to guarantee target phase margin, choosing Cc= 0.04*$C_L$= 1 pF

For GBW= $gm_{1,2}$/Cc = 32M rad/sec, Cc=1*$10^{-12}$ F, $gm_{1,2}$=32*$10^6$*1*$10^{-12}$=32*$10^{-6}$ S

These parameters are based on small signal transfer function; Therefore, it remains unchanged value with any model to identify transistor's DC bias condition. Recall

$$Id=\frac{n*gm*\emptyset_t*(1+\sqrt{1+i_f})}{2} \quad (1)$$

$$f_T=\frac{\mu*\emptyset_t*(\sqrt{1+i_f}-1)}{\pi L^2} \quad (2)$$

$$\frac{W}{L}=\frac{gm}{\mu*C_{ox}*\emptyset_t*(\sqrt{1+i_f}-1)} \quad (3)$$

$$V_{dsat}\approx\emptyset_t*\left(\sqrt{1+i_f}+3\right) \quad (4)$$

Step 1: Choosing $i_f$, for input pair transistor M1,2 and M8, smaller $i_f$ provides better gm over id efficiency. A moderate value of $i_f$=2 is chosen and L=600nm is chosen for higher output resistance and better comparison with the design based on conventional method. For current mirror, a larger $i_f$ value = 5 is chosen to guarantee the mirror accuracy.

For $I_{d1,2}$=$\frac{n*gm*\emptyset_t*(1+\sqrt{1+i_f})}{2}=1.165*32u*26m*\frac{1+\sqrt{1+2}}{2}=1.32\ uA$

For $I_{d7,8}$=$\frac{n*gm*\emptyset_t*(1+\sqrt{1+i_f})}{2}=1.14*1.4m*26m*\frac{1+\sqrt{1+2}}{2}=56.68\ uA$

Check with $f_T$: $f_T=\frac{\mu*\emptyset_t*(\sqrt{1+i_f}-1)}{\pi L^2}=0.011*26\text{m}*\frac{\sqrt{1+2}-1}{3.14159*300n^2}=740MHz\gg 10MHz$

PMOS transistor for second pole is the critical condition for high frequency performance, therefore the channel length meets the requirement for both NMOS and PMOS.

Step 2: Check with output resistance, Av and CMRR:

Similarly:

$ro_6$=1/λn ∗$I_{D6}$=1/(0.3*2.64u) =1.26 Mohm

$ro_4//ro_2$= (1/λp ∗$I_{D4}$ // 1/λn ∗$I_{D2}$) =(0.12*1.32u)$^{-1}$//(0.30*1.32u)$^{-1}$=6.31Mohm//2.53Mohm=1.81Mohm

$ro_8//ro_7$= (1/λp ∗$I_{D8}$ // 1/λn ∗$I_{D7}$) =(0.12*57u)$^{-1}$//(0.30*57u)$^{-1}$=147 Kohm//59 Kohm=42 Kohm

$A_V$=[$gm_{1,2}$*($ro_4//ro_2$)] *[$gm_8$*($ro_8//ro_7$)] = 32*$10^{-6}$*1.8*$10^6$*1.4*$10^{-3}$*42*$10^3$

=57.6*58.8= 70.6 dB

CMRR=2*$ro_6$*$gm_3$*$gm_{1,2}$*($ro_4//ro_2$) = 2*1.26M*32u*32u*1.8M=73.3 dB

Power=1.2*(2*1.32 uA+57 uA) =1.2*59.64u=71.57 uW and all the specs are meeting requirement

Step 3: Determine the W/L size of transistors.

Assuming $gm_{5,6}=gm_{1,2}=gm_{3,4}$

$$(W/L)_{1,2}=\frac{gm}{\mu*C_{ox}*\emptyset_t*(\sqrt{1+i_f}-1)}=\frac{32u}{928u*26m(\sqrt{1+2}-1)}=1.81\approx\frac{1040n}{600n}$$

$$(W/L)_{3,4}=\frac{gm}{\mu*C_{ox}*\emptyset_t*(\sqrt{1+i_f}-1)}=\frac{32u}{165u*26m(\sqrt{1+2}-1)}=10.19=\frac{6.1u}{600n}$$

$$(W/L)_{5,6}=\frac{gm}{\mu*C_{ox}*\emptyset_t*(\sqrt{1+i_f}-1)}=\frac{32u}{928u*26m(\sqrt{1+5}-1)}=0.91=\frac{550n}{600n}$$

$$(W/L)_7=(W/L)_{5,6}*57u/2.64u=21.6*(W/L)_{5,6}=\frac{11.9u}{600n}$$

$$(W/L)_8=\frac{gm}{\mu*C_{ox}*\emptyset_t*(\sqrt{1+i_f}-1)}=\frac{1.4m}{165u*26m(\sqrt{1+2}-1)}=445.8=\frac{133.74u}{300n}$$

Table 10. Inversion level and size of second stage amplifier design

| | Parameters | M1,2 | M3,4 | M5,6 | M7 | M8 |
|---|---|---|---|---|---|---|
| Calculation | W/L | $\frac{1040n}{600n}$ | $\frac{6.1u}{600n}$ | $\frac{550n}{600n}$ | $\frac{11.9u}{600n}$ | $\frac{133.74u}{300n}$ |
| | $i_f$ | 2 | 2 | 5 | 5 | 2 |
| Simulation | W/L | $\frac{1040n}{600n}$ | $\frac{6.1u}{600n}$ | $\frac{550n}{600n}$ | $\frac{18.75u}{600n}$ | $\frac{165u}{300n}$ |
| | $i_f$ | 3.16 | 3.09 | 11.94 | 3.0 | 1.0 |

Table 11. Spec summary and comparison with two different method

| | Conventional model | | ACM model | |
|---|---|---|---|---|
| Parameter | Cal. | Sim. | Cal. | Sim. |
| Gain | 67 dB | 58.88 dB | 70.6 dB | **83.5 dB** |
| GBW | 5.1 MHz | 4.35 MHz | 5.1 MHz | **5.93 MHz** |
| PM | 60° | 60° | 60° | 60° |
| CMRR | 70 dB | 64 dB | 73.3 dB | **94.9 dB** |
| Power | 96 uW | 213 uW | 71.57 uW | **177 uW** |
| SR | 3.2 V/us | SR+:6.1 V/us SR-:5.1 V/us | 2.6 V/us | SR+:4.5 V/us SR-:4.3 V/us |
| PSR (Av(dm)/Av(vdd)) | NA | @DC: 88.2 dB @100 kHz: 35.3 dB | NA | @DC: 88.1 dB @100 kHz: 36.63 dB |
| 1% Settling time | NA | ST+:130ns ST-:241ns | NA | ST+:136ns ST-:210ns |

Conclusion: From table 11 we find out in simulation results based on ACM model, a higher gain and CMRR with better GBW and PM performance is achieved with less power consumption. Design iteration is much less than conventional design method and moderate accuracy compared with calculation is achieved except of gain, where nonlinearity is appearing as previous extraction results. If of M8 is tuned to be close to 1 to minimize the power consumption. ACM is more efficient for transistors working in weak inversion level, however the transistors in weak inversion are very sensitive to any dc bias variation and process

vibration. It is the main drawback for weak inversion design despite of its gm-id power efficiency. An improvement could be focused on increasing the $i_f$ of second stage.

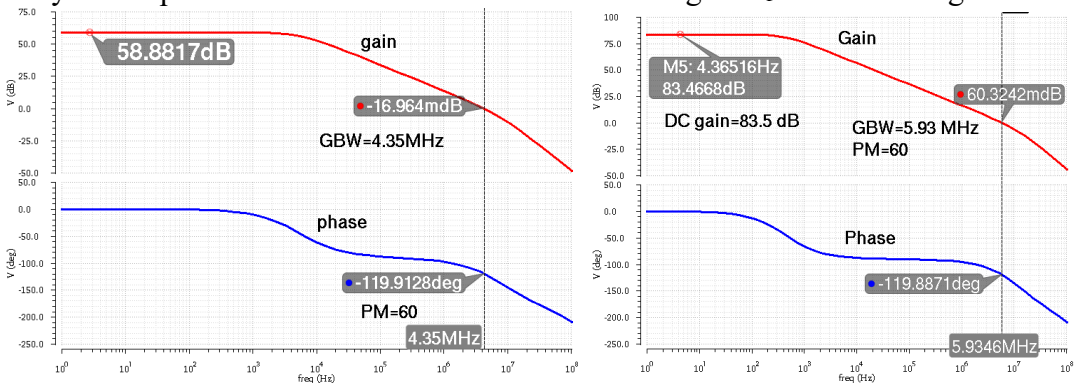


Figure 13. Simulation of AC performance for (a) convention method (b) ACM based method

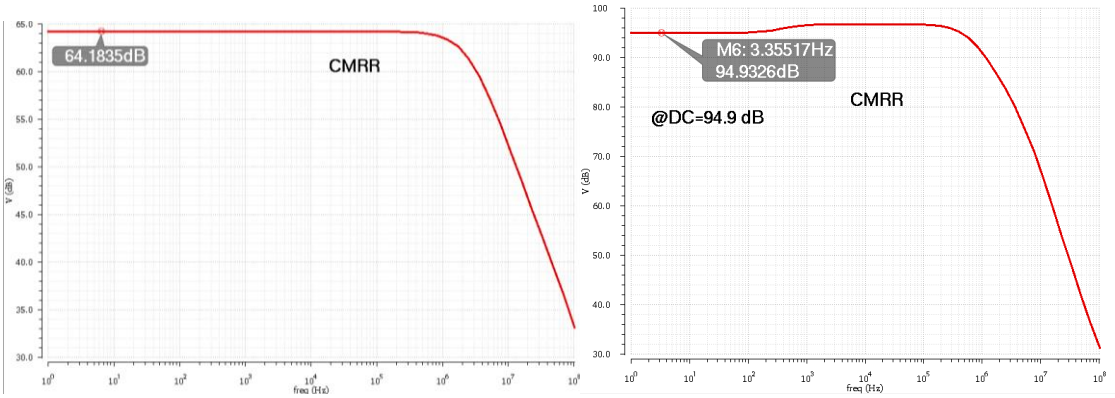


Figure 14. Simulation of CMRR for (a) convention method (b) ACM based method

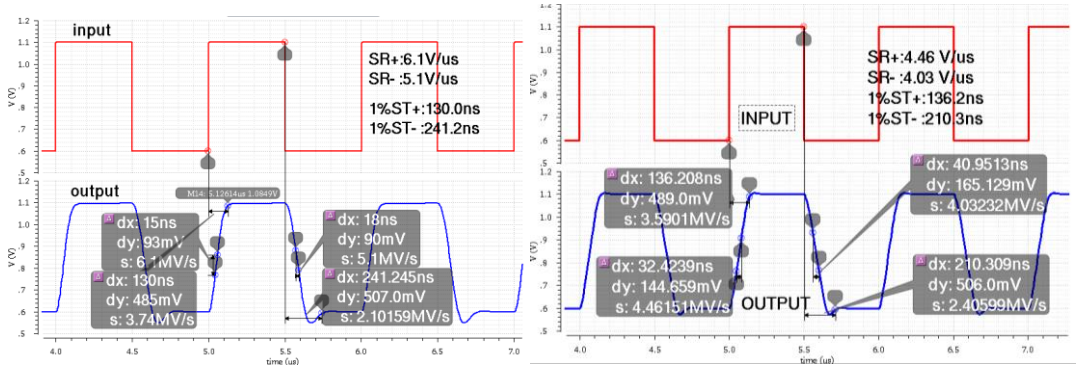


Figure 15. Simulation of transient response (a) convention method (b) ACM based method

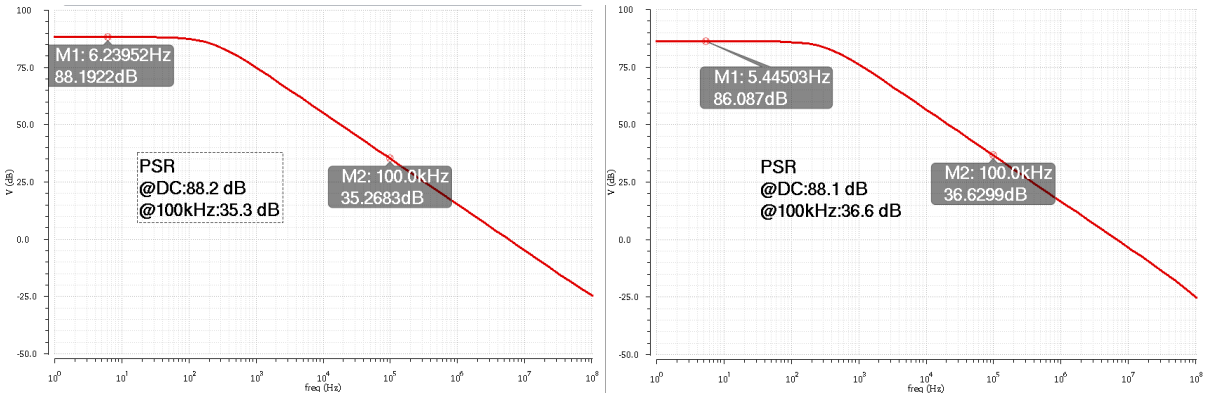


Figure 16. Simulation of PSR (a) convention method (b) ACM based method

## Problem 4.

Design using one equation all region equation, an Ahuja current buffer amplifier that meets the specs in Prob. 3, except the SR but consumes at least 50% less than the one designed in 704 and can handle a 10X larger load capacitance.

Provide a table summarizing the results of Probs. 2 and 3, include in the comparison also active area, PSR at DC and 100 KHz, 1% settling time, CMRR (0), SR-, and SR+. Comment these results and trade-offs.

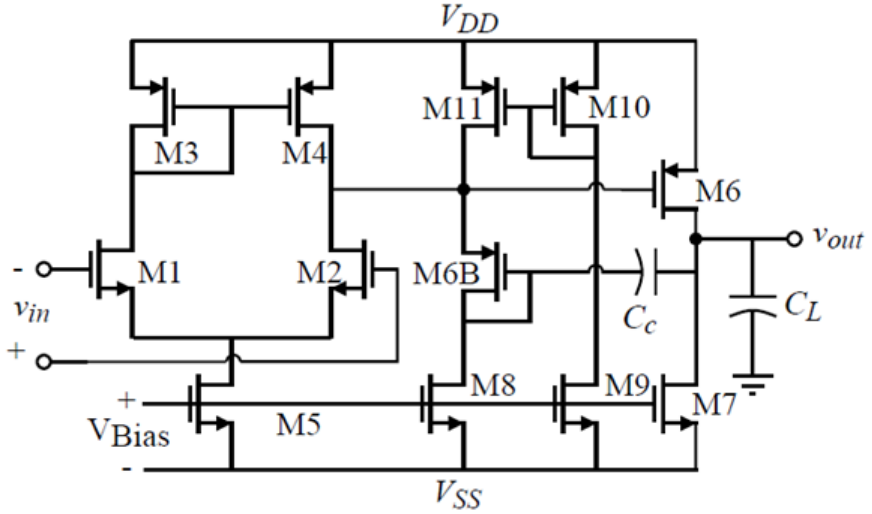


Figure 17. Ahuja compensation to generate nulling resistance.

For Av=Av1*Av2 and GBW=gm1/Cc remain unchanged. However, the second pole is located as gm6*Cc/(Cp*(Cc+$C_L$))≈gm6*Cc/(Cp*$C_L$). For same loading capacitor, the gm requirement is decreased by Cc/Cp, where Cp is the parasitic capacitor of first stage output. Therefore, large value of Cc with constant gm2 will increase the maximum loading capacitor for same GBW and PM requirement but large Cc will increase the gm requirement of first stage, which increases the power consumption in first stage. Overall, the second stage gm requirement is alleviated and large driving ability is achieved with similar power consumption.

Similarly, for first stage and GBW:

Choosing Cc= 0.04*$C_L$= 4 pF,

for GBW= $gm_{1,2}$/Cc = 32M rad/sec, Cc=4*$10^{-12}$ F, $gm_{1,2}$=32*$10^{6}$*4*$10^{-12}$=128*$10^{-6}$ S

for second pole: gm6*Cc/(Cp*(Cc+$C_L$))≈gm6*Cc/(Cp*$C_L$)= 56M rad/sec. The worst case is in driving 10X larger capacitor than problem 2 and 3, setting $C_L$=250 pF. Estimating $C_P$=100 fF

Therefore gm6=56M*254*$10^{-12}$*(0.1/4) ≈356*$10^{-6}$ S

gm6B will generate a LHZ z1 to improve PM, setting z1=p1:

gm6B=gm6*(Cc)/ (Cc+$C_L$) = 356*$10^{-6}$ S*4/254= 5.6*$10^{-6}$ S

For $I_{d1,2}$=$\frac{n*gm*\emptyset_t*(1+\sqrt{1+i_f})}{2} = 1.165 * 128u * 26m * \frac{1+\sqrt{1+3}}{2} = 5.82\ uA$

For $I_{d6B,8,11}$=$\frac{n*gm*\emptyset_t*(1+\sqrt{1+i_f})}{2} = 1.14 * 5.6u * 26m * \frac{1+\sqrt{1+24}}{2} < 500$ nA

For $I_{d6}$=$\frac{n*gm*\emptyset_t*(1+\sqrt{1+i_f})}{2} = 1.14 * 356u * 26m * \frac{1+\sqrt{1+3}}{2} = 15.83$ uA

Sizing transistor with ACM model, setting if =3 for amplifying transistors, = 8 for bias transistors.

Assuming $gm_5 = gm_{1,2} = gm_{3,4}$

$$(W/L)_{1,2} = \frac{gm}{\mu * C_{ox} * \emptyset_t * (\sqrt{1+i_f}-1)} = \frac{128u}{928u * 26m(\sqrt{1+3}-1)} = 5.3 \approx \frac{3.2u}{600n}$$

$$(W/L)_{3,4} = \frac{gm}{\mu * C_{ox} * \emptyset_t * (\sqrt{1+i_f}-1)} = \frac{128u}{165u * 26m(\sqrt{1+3}-1)} = 29.83 = \frac{17.9u}{600n}$$

$$(W/L)_5 = \frac{gm}{\mu * C_{ox} * \emptyset_t * (\sqrt{1+i_f}-1)} = \frac{128u}{928u * 26m(\sqrt{1+8}-1)} = 2.65 = \frac{1.6u}{600n}$$

$$(W/L)_6 = \frac{gm}{\mu * C_{ox} * \emptyset_t * (\sqrt{1+i_f}-1)} = \frac{356u}{165u * 26m(\sqrt{1+3}-1)} = 82.98 = \frac{24.9u}{300n}$$

$$(W/L)_{6B} = \frac{gm}{\mu * C_{ox} * \emptyset_t * (\sqrt{1+i_f}-1)} = \frac{5.6u}{165u * 26m(\sqrt{1+8}-1)} = 0.65 = \frac{650n}{1u}$$

$$(W/L)_7 = (W/L)_5 * (15.83/5.82*2) = 1.36*2.65 = \frac{2.2u}{600n}$$

$$(W/L)_{8,9} = (W/L)_5 * (0.5/2*5.82) \approx \frac{300n}{7u}$$

$$(W/L)_{10,11} = (W/L)_{8,9} * (kn/kp) \approx \frac{1.7u}{7u}$$

Table 12. Inversion level and size of second stage amplifier design

| | Par. | M1,2 | M3,4 | M5 | M6 | M6B | M7 | M8,9 | M10,11 |
|---|---|---|---|---|---|---|---|---|---|
| Cal. | W/L | $\frac{3.2u}{600n}$ | $\frac{17.9u}{600n}$ | $\frac{1.6u}{600n}$ | $\frac{24.9u}{300n}$ | $\frac{650n}{1u}$ | $\frac{2.2u}{600n}$ | $\frac{300n}{7u}$ | $\frac{1.7u}{7u}$ |
| | $i_f$ | 3 | 3 | 8 | 3 | 2 | 8 | 8 | 8 |
| Sim. | W/L | $\frac{3.2u}{600n}$ | $\frac{17.9u}{600n}$ | $\frac{1.6u}{600n}$ | $\frac{113u}{300n}$ | $\frac{1.6u}{1u}$ | $\frac{10u}{600n}$ | $\frac{900n}{2u}$ | $\frac{1.7u}{520n}$ |
| | $i_f$ | 2.96 | 2.96 | 11.8 | 3.1 | 17.5 | 12.2 | 10.9 | 8.7 |

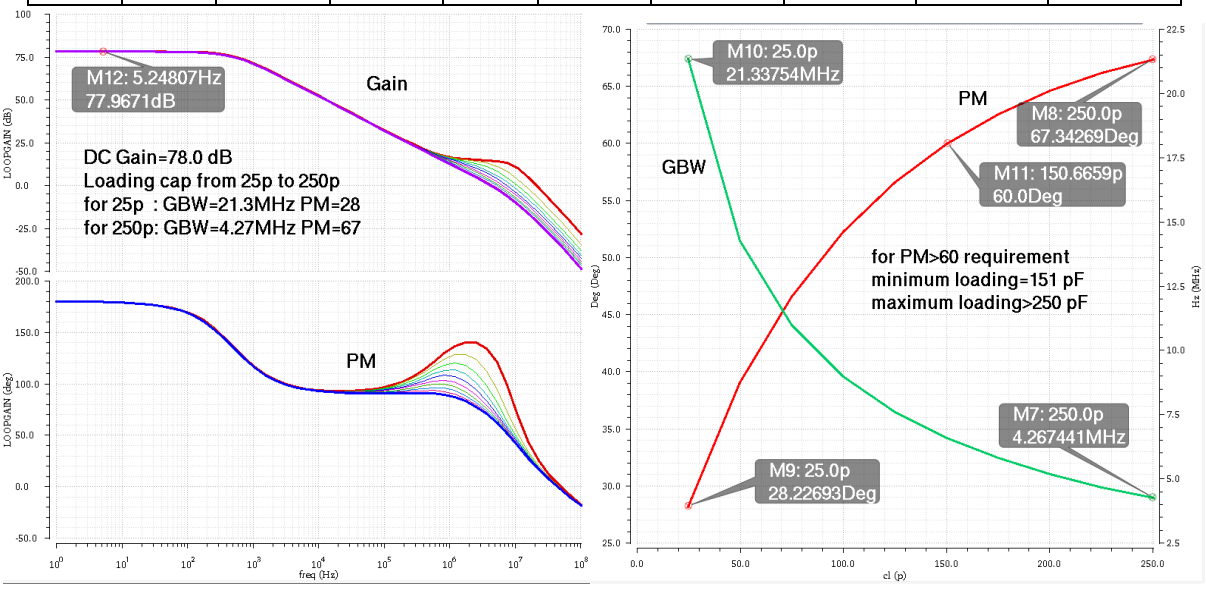


Figure 18. AC Simulation results for DC gain, GBW and PM with different loading

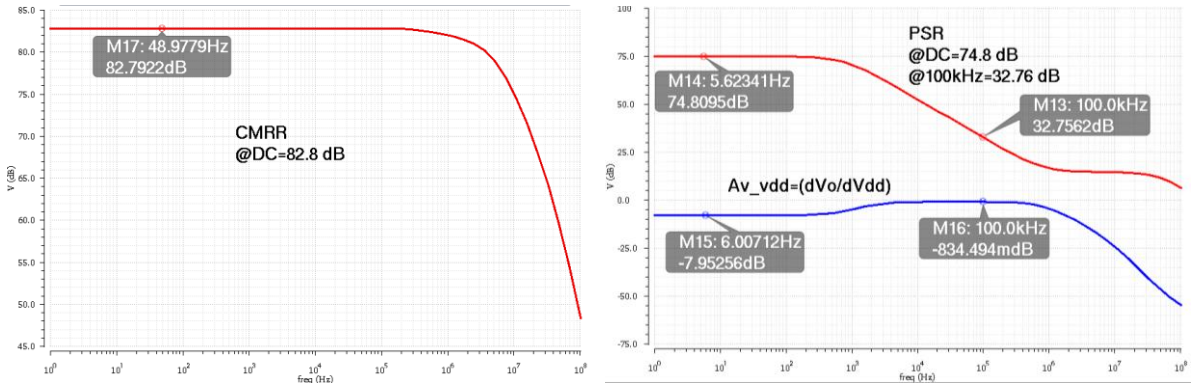


Figure 19. CMRR and PSR simulation results.

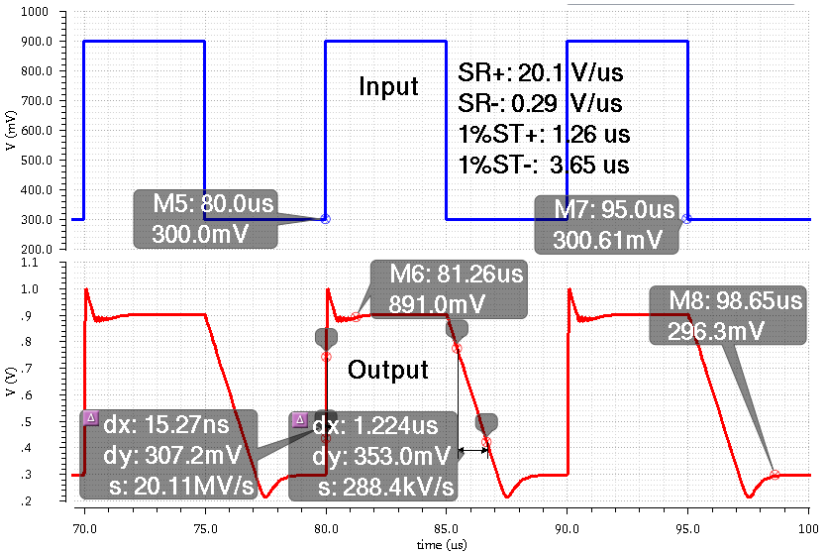


Figure 20. SR and settling time transient simulation results.

Table 13. Spec comparison with two miller compensation designs and Ahuja's compensation

| Design | Conventional method | ACM method | Ahuja compensation |
|---|---|---|---|
| Gain | 58.88 dB | **83.5 dB** | 78 dB |
| GBW | 4.35 MHz | 5.93 MHz | **4.27 MHz for 250pF** |
| PM | 60° | 60° | **67.3°** |
| CMRR | 64 dB | **94.9 dB** | 82.8 dB |
| Power | 213 uW | 177 uW | **116 uW** |
| SR | SR+:6.1 V/us<br>SR-:5.1 V/us | **SR+:4.5 V/us**<br>**SR-:4.3 V/us** | SR+: 20.1 V/us<br>SR-:0.29 V/us |
| PSR<br>$Av_{dm}/Av_{vdd}$ | @DC: 88.2 dB<br>@100 kHz: 35.3 dB | **@DC: 88.1 dB**<br>**@100 kHz: 36.63 dB** | @DC: 74.8 dB<br>@100 kHz: 32.76 dB |
| 1% Settling time | ST+:130 ns<br>ST-:241 ns | **ST+:136 ns**<br>**ST-:210 ns** | ST+:1.26 us<br>ST-: 3.65 us |
| Loading range | <25 pF | <25 pF | **151<$C_L$<250 pF** |
| Active area<br>(MIMcap=2 fF/um$^2$) | 47.44+450=497 um$^2$<br>(Cc=0.9 pF) | **69.978+400=470 um$^2$**<br>**(Cc=0.8 pF)** | 71.35+2000=2071 um$^2$<br>(Cc=4 pF) |
| Area/loading | 19.9 um$^2$/pF | 18.8 um$^2$/pF | **8.28 um$^2$/pF** |

## Comparison and conclusion:

For comparison, Ahuja miller compensation provides large capacitor driving ability in specified GBW and PM without increasing power consumptions. Without increasing tail current and the current for second stage is comparable with the first stage, therefore, the slew rate performance shows non-symmetrical in positive and negative edge. Its negative slew rate is every small because it is dominated by output stage with large loading capacitor. For required phase margin and GBW, parameter sweeping shows the loading capacitor can range from 151 pF to 250 pF, which means such topology is power efficient in large loading capacitor applications with relax requirement of slew rate and settling time. Ahuja's compensation is not as good as conventional compensation in CMRR and PSR performance because it is introducing more bias circuit to affect the signal. As for the active area, two designs are similar excluding the compensation capacitor, however, if considering normalization by loading capacitor, Ahuja's compensation is more than 2X improvement compared to the conventional method. In conclusion, Ahuja's compensation achieves power and area efficiency for large loading capacitor maximum to 250 pF. However, in compromise, its performance is worse in CMRR and PSR, particularly in SR and settling time. One observation is that Ahuja's compensation will introduce delay in feedback despite of eliminate the RHP, or the feed-forward effects. Additional bias path will introduce power consumption and decrease PSR performance, one tentative improvement could be current-reuse technique, such as nested miller compensation used in cascode amplifier for first stage.

In this homework, ACM model extraction and implementation in circuit design are introduced, simulation results show its moderate accuracy in transistor biasing and sizing with physical parameters. Compared to conventional hand calculation, ACM based calculation could avoid too much iteration and achieve power efficient performance in the same time. Then two different compensation methods used in two stage amplifiers are introduced and comparisons are given and are illustrated by simulation results. Ahuja's topology provides an approach to increase amplifier's ability to drive large capacitor without increasing power consumption. This topology also introduces an intuitive approach to eliminate the RHP by using indirect feedback.

## Reference:

[1] Coitinho, R.M.; Spiller, L.H.; Schneider, M.C.; Galup-Montoro, C., "A simplified methodology for the extraction of the ACM MOST model parameters," in Symposium on Integrated Circuits and Systems Design, 2001, 14th, vol., no., pp.136-141, 2001

[2] Dr. Sanchez's lecture note on ECEN 607

[3] BSIM4 Manuel, UC Berkley.