CEG-453/653 Laboratory Project 2
Motorola 68008-based Microcomputer System

The objective of this project is to build a microcomputer system using the MC68008P8 microprocessor (Figures 1 and 2). The system (Figure 3) will be similar to (but simpler than) the SBC68K, and will run the same TUTOR monitor firmware. A modified version of the hardware and software of Project 1 will be used to demonstrate the functionality of the system.

MODULE 1: FREE-RUN TEST (one week)

1. **Construct a minimum system** (Figure 4) consisting of a MC68008P8, the necessary reset logic, and an LED on address line A19. Use a 4 MHz clock for the system. Make sure that
    a. the processor correctly resets itself on power up, and in response to the activation of a reset switch (or grounding a reset wire) and
    b. the microprocessor can successfully run an idle loop through the entire address space. Record the frequency of the LED flashing in the lab notebook.

MODULE 2: GLUE-LOGIC (one week)

2. **Add the Address-decoder/DTACK*-generator/VMA-VPA-generator (ADDV) chip** provided by the instructor to the circuit. Connect a pull-up resistor to the AS* pin of the MC68008P8. With the MC68008P8 DTACK* input pin still grounded, check the operation of the decoder chip during execution of the idle loop (read the manual "Using the Logic Analyzer To Test the Altera Decoder Chip".) With a logic analyzer, record suitable information to show that the circuit generates correct
    a. chip-select signals for both RAM chips, both ROM chips, and the two synchronous interface chips. Make sure ROM is selected for the first eight bytes right after reset,
    b. DTACK* signals for zero wait state RAM access and can be set to provide zero- and one-wait-states for ROM access, (two-wait-states can not be tested at this stage) and
    c. VPA* signal for peripherals' accesses.

    NOTE: no DTACK or VPA* will be generated for addresses which do not correspond to any configured device.)*

3. **Add the Single-Step/Watchdog Timer/Interrupt Logic (SWIM) chip** provided by the instructor. Connect the DTACK* and VPA* outputs of the ADDV to the MC68008.
    a. Before connecting BERR*, use the idle loop, i.e., the data bus is still grounded, to verify proper operation of the single-step and watchdog timer functions. Show that
        1. single-step operation of the circuit is possible and
        2. when used in run mode, attempts to read addresses in ranges which do not result in the generation of DTACK* or VPA* result in the assertion of BERR*.
    b. After connecting BERR*, show that a double-bus fault (textbook, p. 492) occurs.

MODULE 3: MEMORY (one week)

4. **Add to the circuit** the following memory components
    a. **16K Bytes of RAM** (two 6264 chips) at address 0.
    b. **16K Bytes of ROM** (two 2764 chips containing the TUTOR code) at address $8000.
        - These devices can be programmed using an EPROM burner available in the lab (read the manual ‘‘Instructions for Programming TUTOR EPROMs”).
        - Use a logic analyzer to verify bootstrap action (refer to the manual ‘‘Using the Logic Analyzer To Verify Bootstrap Action”.)

MODULE 4: ACIA (one week)

5. **Add to the circuit** the following components and test the circuit using the TUTOR.
    a. **One ACIA** (Motorola 6850) at address $10040 (even bytes only).
    b. **One bit-rate generator** (Motorola 14411) to generate transmit and receive clocks (4800 baud). Note that the TUTOR is set up so that the ACIA divides the clock rate by 16 and uses the slower clock for communication.
    c. **MAX232 Line Drivers/Receivers** for the ACIA.
    d. **An ABORT switch**, which causes a level 7 auto-vectored interrupt.

    Make sure that TUTOR can be run, including successful use of the MD, BT, and MM commands.

MODULE 5: PIA (two weeks)

6. **Add to the circuit one PIA (Motorola 6821)** at address $10081 (odd bytes only). The PIA must be capable of operation under auto-vectored interrupt control. The IRQA interrupt output of the PIA should cause a level-2 interrupt.
    a. Connect the 7-segment switch and keypad from Project 1 to the circuit through the PIA. Since your system does not have a timer, use one of the outputs from the 14411 chip, which you use for baud rate generation, to provide timing for the generation of the sample timing level-2 interrupt through one of the PIA handshake inputs. Select an output of the 14411, which allows a suitable sampling timing interval. To achieve the desired interval, some unnecessary interrupts need to be skipped with software.
    b. Modify the software of Project 1 to use the PIA instead of the PI/T.

    Make sure that the modified program can duplicate the results of Project 1.

7. **Modify the software** so that the output of characters to the PC monitor via the ACIA can be done without using any TRAP #14 instruction.

Checkout

For lab groups of two or more students, each group member must be present for the checkout of each feature and questioned separately by the TA with respect to the operation of the group's hardware and software. The group should bring to the checkout a complete set of applicable circuit diagrams and software listings, so that the TA can refer to them during the checkout process. Students using the chip set provided by the instructor must be able to explain the chips' operation from an external viewpoint; that is, how the output signals from the chips are logically related to the input signals. The internal details of the chips have not been discussed, but students may be asked to speculate as to the probable internal functioning of some of the chips' circuits. Studying the .ADF files may help in this area. You must understand how all of your hardware and software work (even if your lab partner did the actual work).

Final Report

A report describing the course projects should be turned in with the lab notebook to the professor no later than the final exam time. Each student must submit a report.

The level of the report should be such that a reader who is familiar with the Motorola 68000 family and with the ECB but not with the particular requirements of this course should have no trouble understanding the report. Circuit diagrams, software listings, etc. may be shared (Xeroxed) between team members, but the main body of each report must be the independent work of the individual student.

Each report should include a Table of Contents, an introductory section, which describes the organization of the report, one or more sections describing the Project 2 hardware, one or more sections describing the Project 1 software and its adaptation for Project 2, and a section summarizing the project. The last section should also include any constructive suggestions, which the instructor might find useful in improving the effectiveness of similar projects in the future. Software listings and a complete set of hardware diagrams should be included as appendices.

The reports will be graded on organization, clarity, style, grammar, and spelling as well as on technical completeness and accuracy. Reports must be typed or neatly printed in ink.

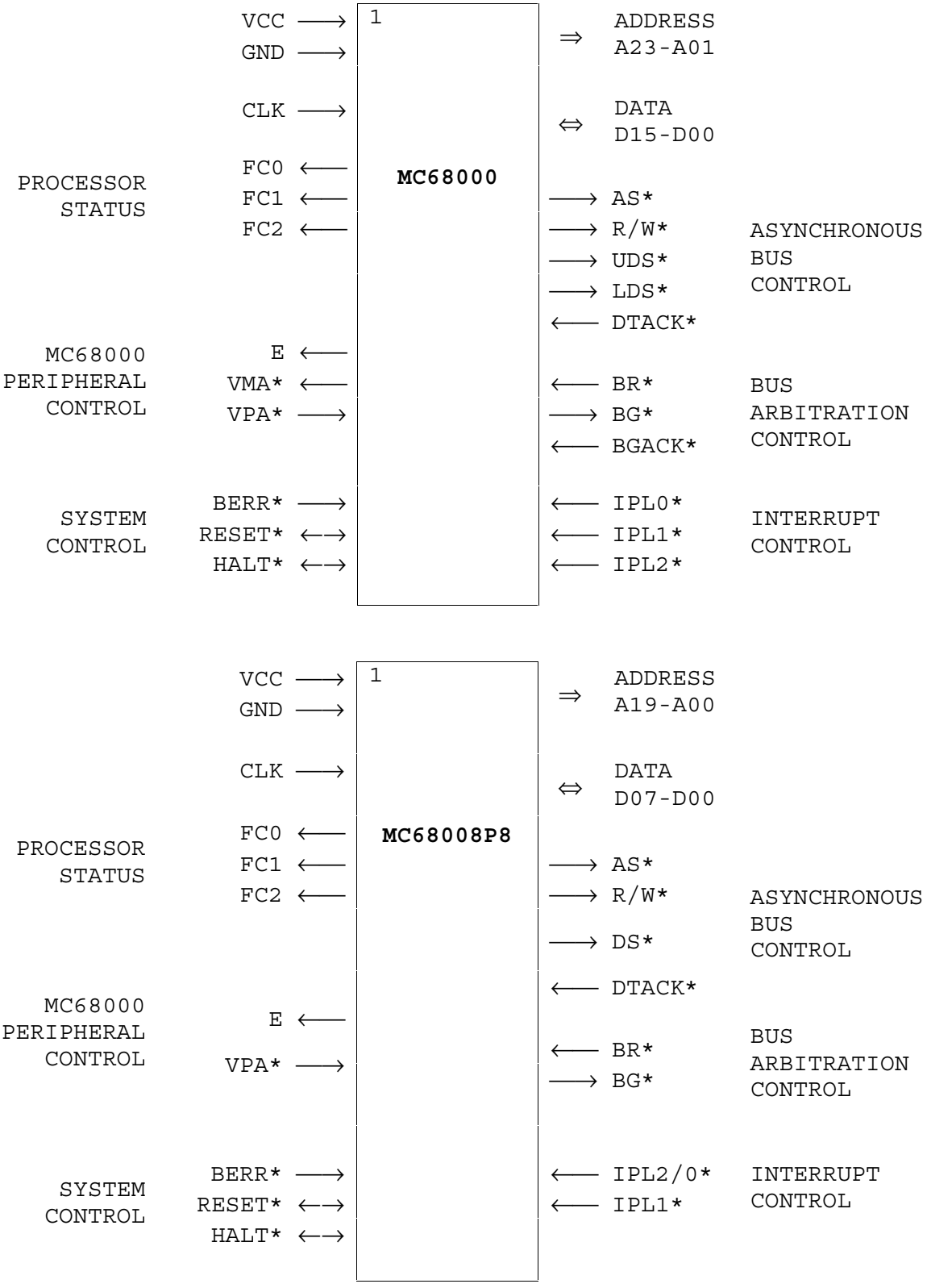

Figure 1. Comparison of 68000 and 68008 external interface

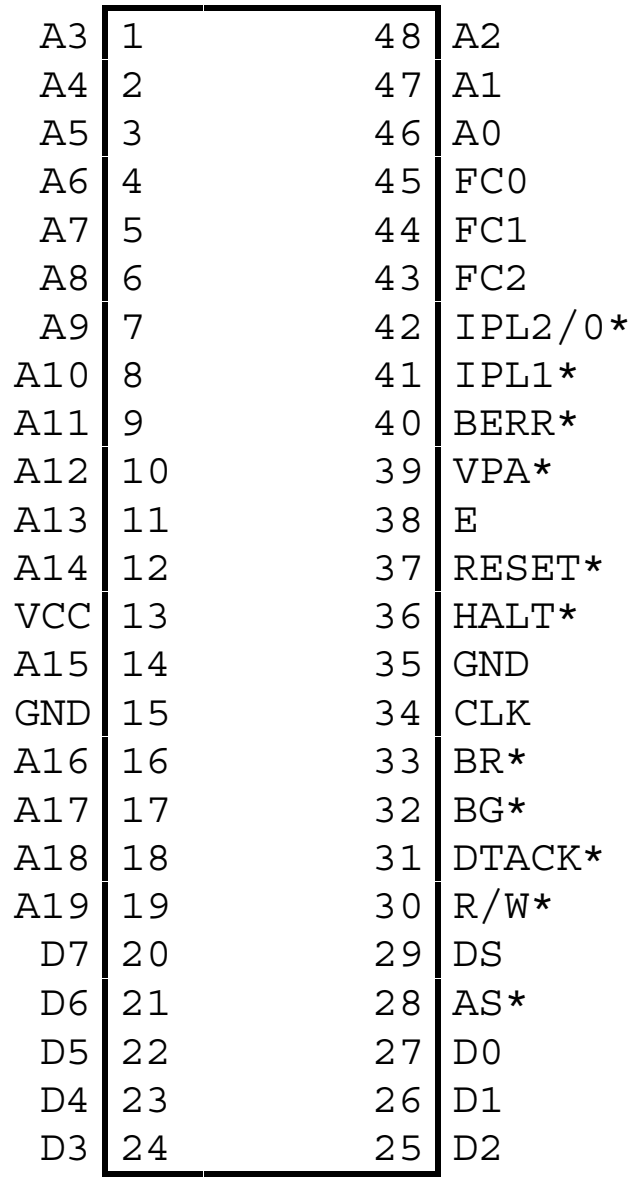

Figure 2. 68008P8 (plastic DIP) pinout

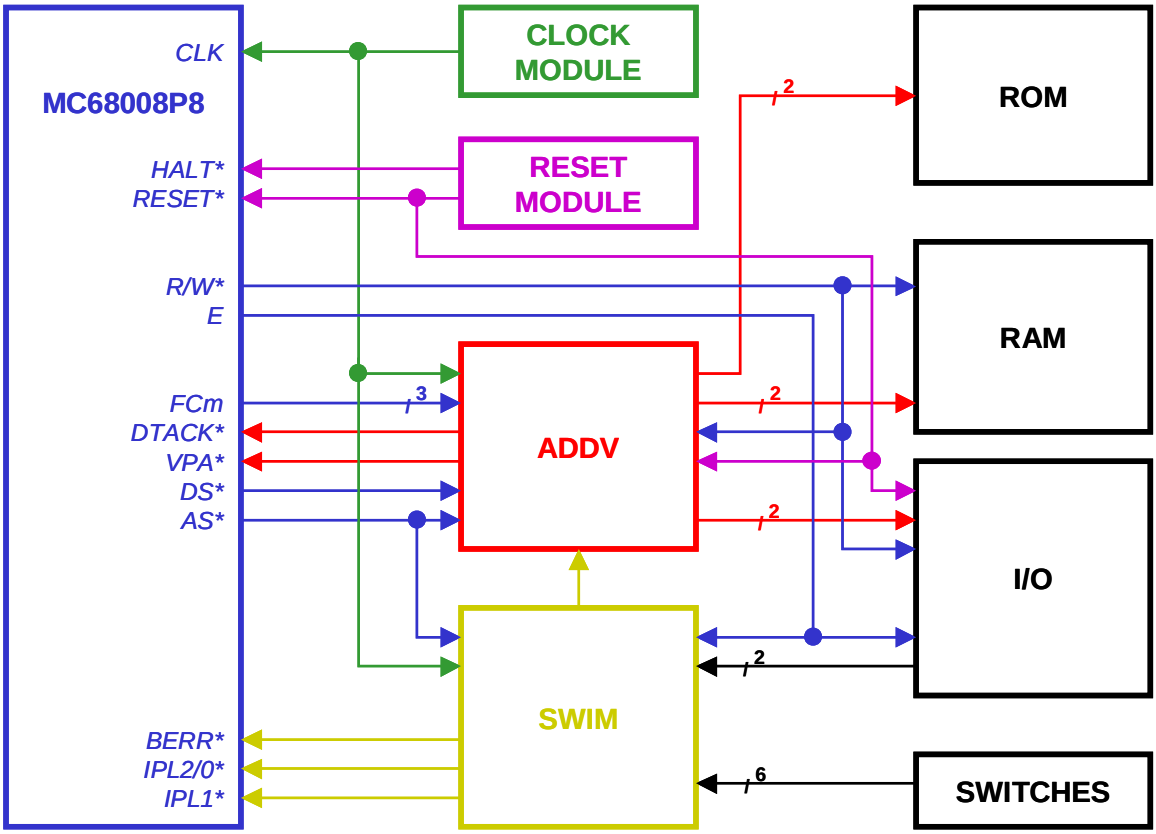

Figure 3. BLOCK DIAGRAM (Address and data lines NOT shown)

This diagram is NOT for the board layout.
A good floor-planning may save you a lot of time later

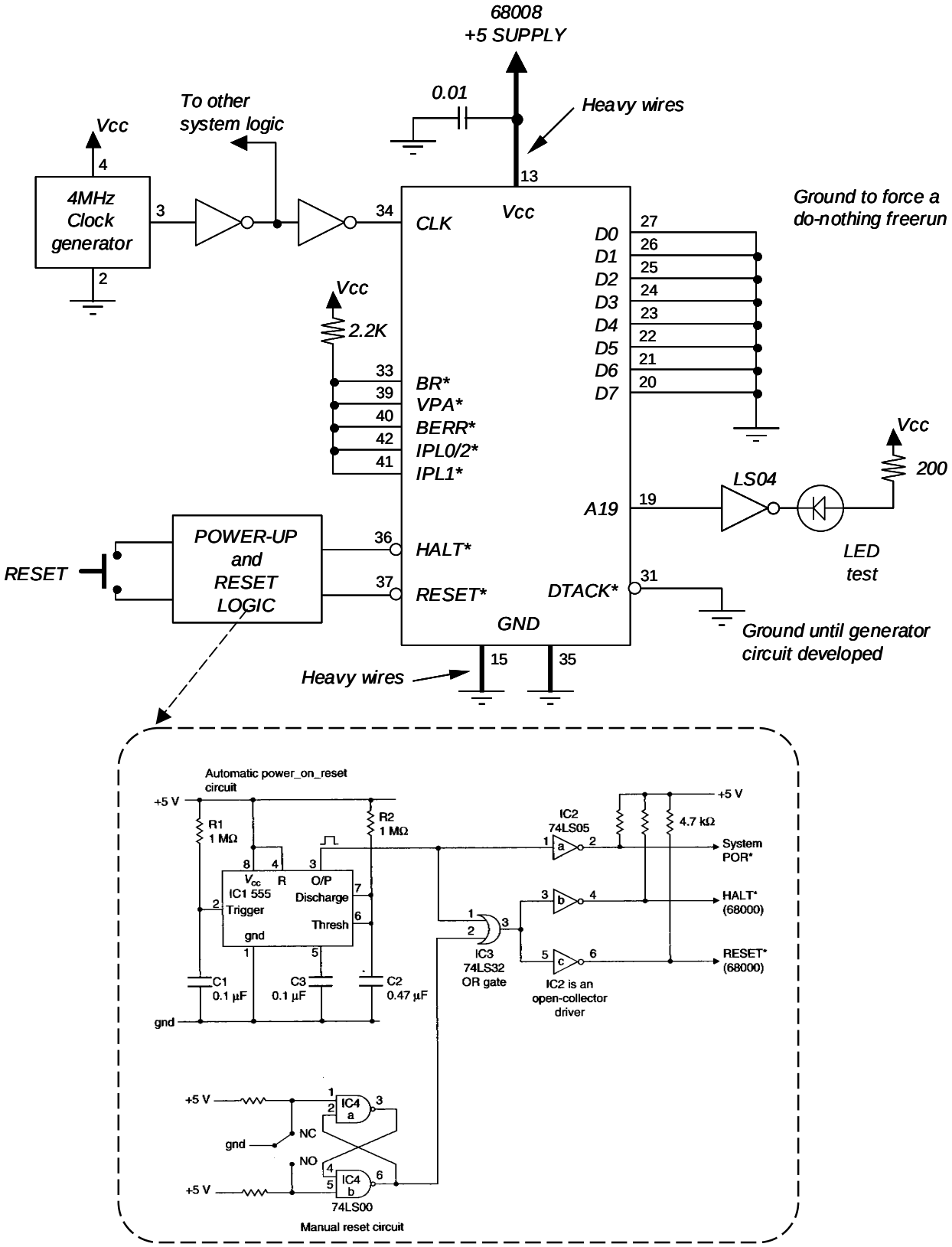

Figure 4. Circuit diagram for the minimum 68000 system (free-run test)