Course Projects

Preliminary report (1 per team): Due on April 19, 2013. **It must be submitted electronically**
Final report: April 27 2014. **It must be submitted electronically by Email to Prof. Hoyos**
8 minutes Power Point presentation: During last day of classes on May 4.

Policies:
The projects can be developed by a team of no more than 3 students.
The project report must consist of the following sections:
· Specifications and background.
· Search of existing solutions; use IEEExplore.
· Justify and define your architecture; provide simulations results for your architecture.
· Design and simulate your building blocks using Matlab and/or Cadence .
· Comparison of results (hand calculations and Matlab and/or Cadence).
· Show the final results that proof your theory.
· Conclusions. (10%)

Pay attention to all sections!

After 10 pages usually the quality of the results is inversely proportional to the number of pages. Cover all the aforementioned issues, but please do not expend time discussing trivial or irrelevant stuff. In no more than 6 pages of theory (you may have more pages due to the simulation results) you should be able to explain your concepts, and convince the instructor about the suitability of your approach. Please be clear and concrete.

SMART PEOPLE DISCUSS IDEAS, CONCEPTS, INNOVATIONS!

Here you have a list of potential projects, but feel free to suggest other projects.

Project #1. Pipeline data converter with calibration
Design a 10 bits SQNR 100MHz ADC. Add a significant non-linearity to the residue amplifier such that SDR is no more than 7bits.

a) Design a calibration scheme for improving the ADC linearity up to 10 bits
b) Show the results with and without calibration to support your claims.
c) Estimate the area and power consumption of the proposed solution
d) Design the ADC at transistor level, but the calibration can be at macromodel level. Show Cadence results

Names:

Project #2 10MHz 12-bits Continuous-Time Sigma-Delta Modulator.

Design a 10Mhz bandwidth 12-bit continuous-time sigma-delta modulator. Minimize the power consumption as much as you can.

a) Make a model for the 5psecs jittered clock and simulate the modulator with and without jitter. Consider the case where the clock is very noisy; e.g. jitter >5psecs-rms.
b) Add non-linearities to the DAC assuming that the mismatch between DAC components mismatch can be 0.1, 0.5 and 1%. Make a plot of SDR versus mismatch. Suggest a calibration scheme to minimize DAC non-linearities.
c) Quantify the SQNR versus excess phase errors. Add excess loop delay on purpose

Names:

Project #3 10MHz 12-bits Continuous-Time Sigma-Delta Modulator.

Design a 10Mhz bandwidth 12-bit continuous-time sigma-delta modulator. Minimize the power consumption as much as you can. **Please use TDC based quantizer.**

a) Make a model for the jittered clock and simulate the modulator with and without jitter. Consider the case where the clock is very noisy; e.g. jitter >5psecs-rms.
b) Add non-linearities to the DAC assuming that the mismatch between DAC components mismatch can be 0.1, 0.5 and 1%. Make a plot of SDR versus mismatch
c) Quantify the SQNR versus excess phase errors. Add excess loop delay on purpose

Names:

Project #4 100MHz 10-bits Continuous-Time Sigma-Delta Modulator..

Design a 100MHz low-pass sigma-delta modulator that achieves 10 effective number of bits. Consider:

a) Find the architecture and specifications for the building blocks
b) Show macromodel simulations
c) Quantify maximum jitter, and excess loop delay the architecture can tolerate
d) Design the amplifier required for this modulator
e) Show Cadence results

Names

Your project suggestions are more than welcome!