Spring 2015
MW 4:10-5:25 PM
THOM 107A

ECEN 610: MIXED-SIGNAL INTERFACES

"An aggie does not lie, cheat, steal, or tolerate those who do"

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Prerequisites: ELEN 474 or approval of instructor

Textbooks:

R. Van der Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters" Kluwer Academic Publishers, new edition.

R. Scheier and G. Temes, "Understand Delta-Sigma-Modulators", IEEE and CRC Publishers, last edition.

Mikael Gustavsson, J. Jacob Wikner and Nianxiong Nick Tan, "CMOS Data Converters for Communications", Kluwer Academic Publishers, 2000.

Technical reports on ADCs from a number of companies such as TI, MAXIM, National Semiconductors and ADI

Class notes and technical papers (JSSC, ISSCC, CICC and TCAS)

References:

[1] D.A. Johns and K. Martin, "Analog Integrated Circuits and Systems McGraw-Hill, NY 1994

[2] Behzad Razavi, "Principles of Data Conversion System Design", IEEE Press, 1995.

[3] B. Murmann, "ADC Performance Survey 1997-2010, http://www.stanford.edu/~murmann/adcsurvey.html..

[4] [3] Paul Gray and Robert Meyer and Paul Hurst, "Analysis and Design of Analog Integrated Circuits," John Wiley and Sons, fourth edition.

Objectives: To discuss circuit architectures and design related issues for relevant analog-to-digital converters. Firstly, ADC parameters will be discussed, then S/H, Nyquist architectures and oversampled topologies will be covered. Relevant building blocks issues will be highlighted as well as effects on ADC performance of clock jitter, finite gain and frequency response of the active devices, component mismatch of relevant blocks and supply noise.

Calibration techniques for both pipeline and sigma-delta architectures will be discussed as well. Most of the simulations will be done on CADENCE, Matlab, System view, and other dedicated software packages.

Grading policy:

Exams	55 %	
Assignments (HWs and LABs)	35%	
Final Project	10 %	Power Point presentation.

3 midterms; no final. Closed book exams and NO cheating pages.
No late homeworks!

A ➔ Grade ≥ 90
B ➔ 90 > Grade ≥ 80
C ➔ 80 > Grade ≥ 68
D ➔ 68 > Grade ≥ 55
F ➔ 55 > Grade

Absences

Documented absence from exams will governed by applicable University Regulations If you are absent from an exam, you must **immediately** get in touch with me by email so we can deal with the missing grade.

Disabilities Act

The Americans with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact the Department of Student Life, Services for Students with Disabilities, in Room 126 of the Koldus Building or call 845-1637.

Academic Integrity

Academic Integrity Statement

Outline

- Data Conversion Fundamentals and Performance
- Sampling of Analog Signals, Quantization Error, Quantization Noise.
- Offset, DNL and INL, Dynamic Performances, SNR and SFDR
- Sample and Hold Circuits
  - Design issues
  - Practical limitations
  - Accuracy and speed issues
  - Aperture error
- Low Speed Nyquist-rate A/D Converters
  - Fundamentals and data Converter Performances
  - Integrating Data Conversion
  - Successive Approximation Converters
  - Algorithmic A/D Converters
- High Speed Nyquist-rate A/D Converters: Part I
  - Flash Converters
  - Two-Step Converters
  - Folding Converters

➢ First midterm

- Nyquist ADCs Part II and Oversampled Architectures
- Pipeline Converters
  - Basic concepts
  - Architectural issues
  - Building blocks
  - ADC limitations
  - Calibration
  - Time Interleaved Converters
- Oversampling A/D Converters
  - Basic concepts: Noise shaping
  - Switched-Capacitor architectures
  - Building blocks
  - Mash architectures

➢ Second midterm

- Continuous-Time architectures
  - Building blocks
  - ADC limitations: Excess loop delay, clock jitter, Linearity
  - Calibration
- DAC related issues
  - Basic considerations Switched-Capacitor MDAC

- Resistive-based Architectures
- Current Steering D/A Converters

- Oversampling Bandpass A/D Converters
  - Continuous-Time architectures
  - Building blocks
  - ADC limitations: Excess loop delay, clock jitter, Linearity
  - Digital Calibration

- **Third midterm**

Notes

1 No final exam will be given. Partial exams are closed book. Exams can be scheduled to be out of class.

2 There will be no make-up exams for individual cases, unless it is properly justified, e.g. medical or family emergencies.

3 Homework is due at the beginning of the class on the due date. Late homeworks will not be accepted unless there is a valid excuse.